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Soft Error Simulation of Near-Threshold SRAM Design for Nanosatellite Applications

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Abstract: This paper presents the benefit of the near-threshold design of random-access memory (SRAM) design to reduce software errors during very low-power operations in nanosatellites. The near-threshold design is based on an optimization of the use of the Schmitt trigger structure for a 45 nm technology. The results of the soft error susceptibility of the optimized design are compared to a standard 6T SRAM cell. These two designs are modeled and validated by comparing the results with experimental measurements of both static noise margin (SNM) and single event upset (SEU). The optimized circuit reduces the multiple upsets occurrence from 95% down to 14%. Based on the use of simulation tools, the paper demonstrates that the near-threshold design of SRAM is an excellent candidate for the radiation point of view for agile nanosatellites. The results computed for the near-threshold SRAM device demonstrate an improvement of a factor of up to 25 of the soft error rate (SER) in a GEO orbit.

Keywords: single event upset; near-threshold region; Schmitt trigger; static noise margin; upset threshold voltage; very low power; nanosatellite; soft error rate; LEO orbit; MEO orbit; GEO orbit

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1. Introduction

The reliability of CMOS (Complementary Metal Oxide Semiconductor) microelectronic devices is a major concern, especially for very highly integrated circuit technologies [1]. Soft errors are transient faults induced by radiation particles such as protons, electrons or cosmic rays [1]. If the transient fault occurs in a memory, it can be captured to induce an upset of the bit. This phenomenon is named Single Event Upset (SEU). In some cases, radiation particles can induce Multiple Bit Upset (MBU). This phenomenon is critical for the system because it is harder to correct than SEU. Moreover, soft errors are becoming one of the main reliability issues for very large-scale integration (VLSI) circuits. With the need to design integrated circuits (ICs) that use as little voltage as possible to save energy, particularly for embedded applications, such as nanosatellites, ICs are at voltage regimes close to or below their operating system threshold. Actually, at a very low core voltage, the stability of the cross-coupled inverter pair is of concern. Specific circuits are designed in order to improve their reliability at low power, such as the Schmitt trigger (ST) circuit [2–4]. However, no work has demonstrated their operational use for nanosatellites.

As reported by previous works, both voltage and technological scaling lead to an increase in the importance of soft error [5,6]. Actually, the widths of Single Event Transient (SET) pulse increase with decreasing bias voltage [6]. An issue that results in a higher SER for low-power circuits compared to nominal-power circuits. Based on this context, for circuits at a voltage near to and below their operating threshold, it is important for microelectronic manufacturers and designers to assess the susceptibility to soft errors induced by radiation particles, especially for nanosatellites, which have an extremely limited power budget.

The purpose of this work is to demonstrate that SRAM cells based on near-threshold designs are promising for nanosatellite application.

This work presents the analysis of the impact of voltage scaling on the soft error susceptibility of conventional and low-power SRAM cells for the 45 nm technology node. The Schmitt trigger structure is known to improve the reliability of logic cells [4].

This work highlights the interest in the use of circuits based on the Schmitt trigger circuit initially designed for ultra-low consumption but which has become a hardening technique for SRAM cells. In this work, several modeling tools are used to reach these objectives. First, the simulation tool MUSCA SEP3 (Multi-Scale Single Event Phenomena Prediction Platform) coupled with the injection tool TERRIFIC is used to calculate the SEU cross sections as a function of the design of SRAM bits. Second, the SER is computed using SEE-U for a nanosatellite platform. In the last section of the paper, the Radiation Hardness Assurance (RHA) considerations are discussed as a function of operational orbits.

2. Device/Layout Description of the SRAM Memories

In this work, two designs of SRAM cells built in 45 nm bulk technology are studied: a conventional 6T SRAM [6] and an optimized ST SRAM [3] shrunk to 45 nm.

The standard Schmitt trigger design requires six transistors instead of two transistors to form an inverter as depicted in Figure 1a. An SRAM would then need 14 transistors in total for each bit, which would lead to a large area penalty. Since p-MOS transistors are used as weak pull-ups to hold the "1" state, a feedback mechanism in the p-MOS pull-up branch of the circuit is not used. The feedback mechanism is only used in the pull-down path. The modified circuit is shown in Figure 1b. In this work, the difference in terms of soft error sensitivity between the standard ST inverter and modified ST inverter is not addressed. In this work, only the difference in terms of soft error sensitivity at SRAM level is investigated.

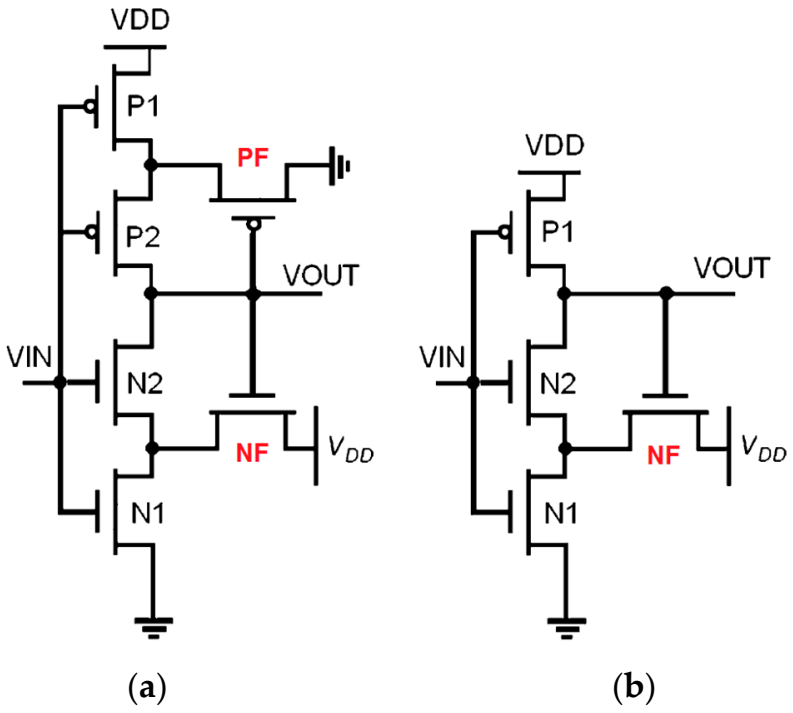
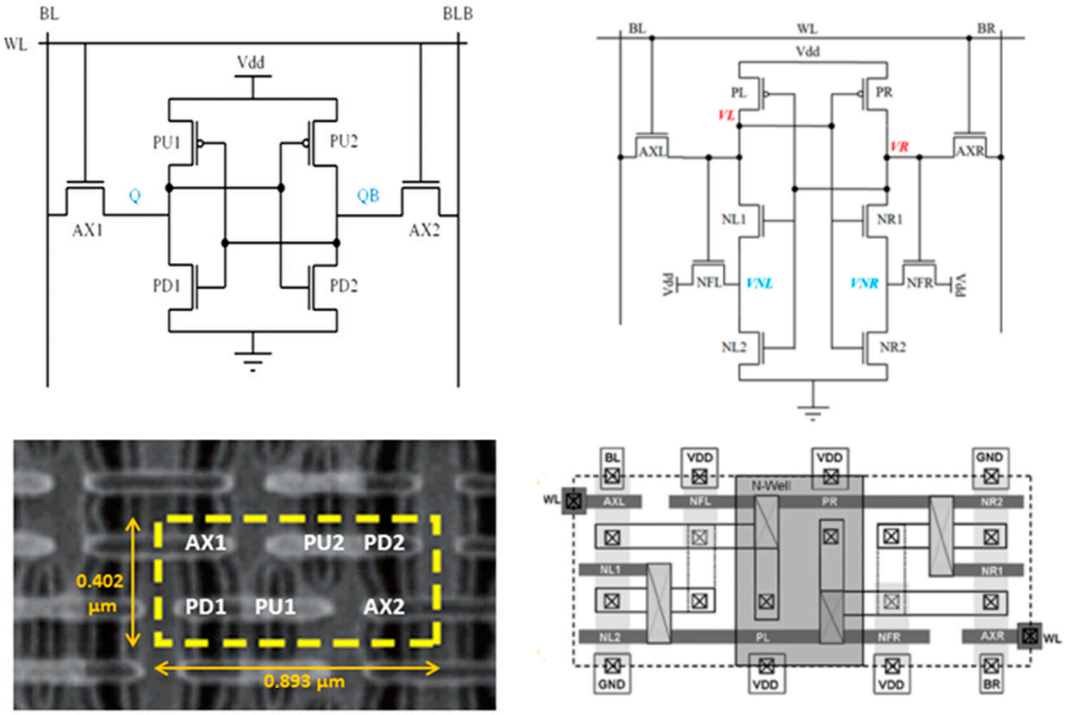


Figure 1. Schematic of (**a**) basic Schmitt trigger inverter and (**b**) optimized Schmitt trigger inverter dedicated for 10T ST SRAM cell [3].

Figure 2a shows the circuit and layout of the standard 6T SRAM cell for the 45 nm technologies, while Figure 1b shows the circuit of the optimized SRAM cell built with an optimized Schmitt trigger (ST) inverter. Transistors PL/NL1/NL2/NFL form the first ST inverter (left), while PR-NR1-NR2-NFR form another ST inverter (right). AXL and AXR are the access transistors for the two inverters, left and right, respectively.



(**a**) (**b**)

Figure 2. Circuits and top views of layouts of SRAM cell: (**a**) the conventional 6T SRAM cell for 45 nm technologies [6], (**b**) the 10T optimized Schmitt trigger SRAM [3] shrunk to the 45 nm technology.

The positive feedback from NFL/NFR changes the switching threshold of the inverter depending on the direction of the input transition. During a read operation (VL = 0, VR = VDD), the node voltage rises because of the action of the voltage divider between the access transistor and the pull-down transistor. If this voltage is higher than the switching threshold (trigger point) of the other inverter, the contents of the cell can be flipped, resulting in a read failure event. The feedback mechanism should increase the switching threshold of the inverter PR/NR1/NR2 with the aim of avoiding a read failure. The n-MOS transistors NFR and NR2 raise the voltage at the node and increase the switching threshold of the inverter storing the logic state "1".

As mentioned, the Schmitt trigger works well at ultra-low voltages. This is because the ST structure keeps a suitable on/off current ratio at lower voltages than a standard inverter (used in standard SRAM cells) at an equivalent core voltage [7]. Thus, the Schmitt trigger action is used to preserve the logic "1" state of the memory cell. The proposed ST SRAM cell is based on differential operations, providing better noise immunity [8]. It requires no architectural change compared to the conventional one. Thus, the optimized ST SRAM investigated in this work is designed with two p-MOS transistors and eight n-MOS transistors. The pull-up transistors, PL and PR, share the same N-well implant. It is interesting to note that the number of p-MOS transistors is the same as that of a standard 6T cell, and the N-well area consumed by ST SRAM cell could be the same as the standard 6T cell. The horizontal dimension is increased by 40% compared to the 6T cell. Since the read path has three n-MOS transistors in series, it results in a 50% increase in the vertical dimension. Thus, the proposed ST SRAM cell consumes 2.1 times more area compared to a standard 6T SRAM cell. This area penalty should be considered in the trade-off as a function of the improvement of the SEU robustness of the ST SRAM cell.

3. Circuit Modeling

3.1. Validation of Electrical Transistors Behavior on Standard 6T SRAM Cell

Figure 3a shows the butterfly curves obtained by static electrical simulations of the modeled 45 nm 6T SRAM cells as a function of the core voltage. The modeled cards are calibrated with the aim of fitting the static transfer characteristics of the 6T SRAM cell. This calibration is performed by optimization of several static electrical and process parameters such as the threshold voltage, drain and source junction depth, GIDL (Gate Induce Drain Leakage) coefficient, or the equivalent oxide thickness. These butterfly curves are shown in Figure 4. It allows for calculating the corresponding SNMs of the cell. The SNM is a usual metric for SRAM cell reliability and is the minimum parasitic static voltage required to destabilize the nominal behavior of the cell. It corresponds graphically to the larger square included in the butterfly curve.

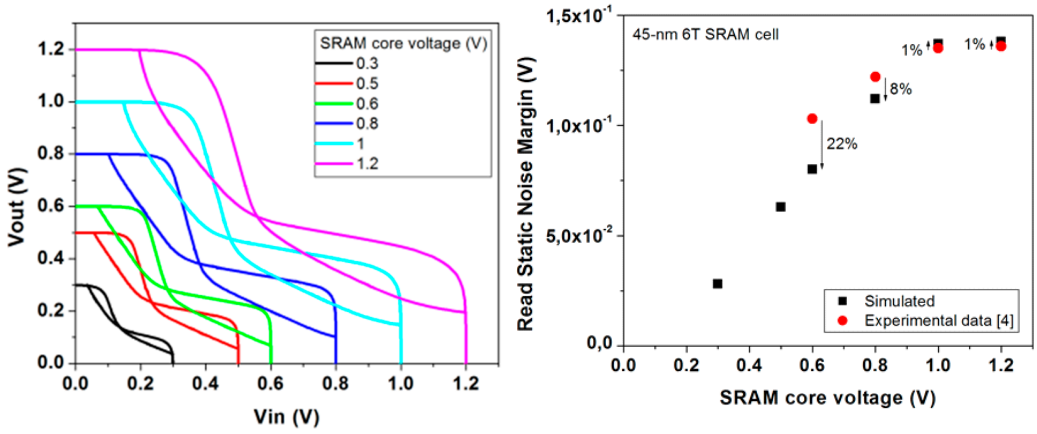


Figure 3. (**a**) Simulated butterfly curves of the 45 nm SRAM in read mode and (**b**) the simulated SNM (black) and measured SNM (red) [6] of 6T SRAM cell as a function of core voltage in read mode.

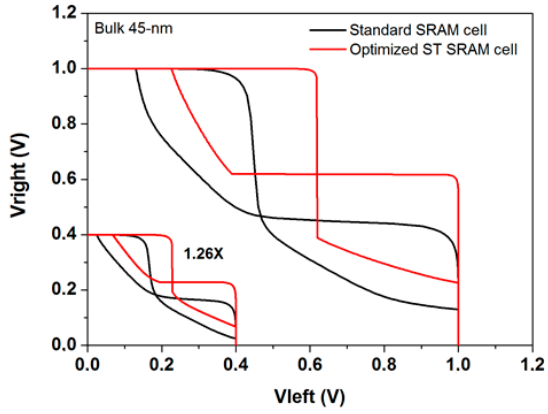


Figure 4. SRAM cell characteristics modeled for the standard 6T SRAM (black lines) and optimized ST SRAM (red lines) which operate at 1.0 V and 0.3 V.

Figure 4 presents the SRAM cell characteristics modeled for the standard 6T SRAM (black lines) and optimized ST SRAM (red lines) which operate at 1.0 V and 0.4 V. As reported in [3], the enhancement of the read SNM due to the use of optimized ST SRAM is about 1.24×. In this work, the ratio presented in Figure 4 is about 1.26×. It confirms the relevant modeling of the optimized ST SRAM cell with an error lower than 2%.

3.2. SNM Performance: Standard Versus Optimized Schmitt Trigger SRAM Cell

In this sub-section, the SNM, during the read and hold operations is analyzed. The SNM is compared for the standard 6T SRAM cell, whose electrical behavior has been validated in the previous sub-section, and the optimized ST SRAM cell.

Figure 5 presents the increase in the read SNM induced by the design of optimized ST SRAM. The increase in the SNM is about 1.3× and up to 1.45× for a 1.2 V core voltage. Figure 6 presents the evolution of the hold SNM for the two SRAM designs as a function of voltage. It is interesting to note that the better stability of the optimized ST SRAM is emphasized in the sub-threshold voltage range, i.e., 0.3–0.5 V. On the other hand, in the voltage range 0.6–1.2 V, the SNM is better for the standard 6T SRAM.

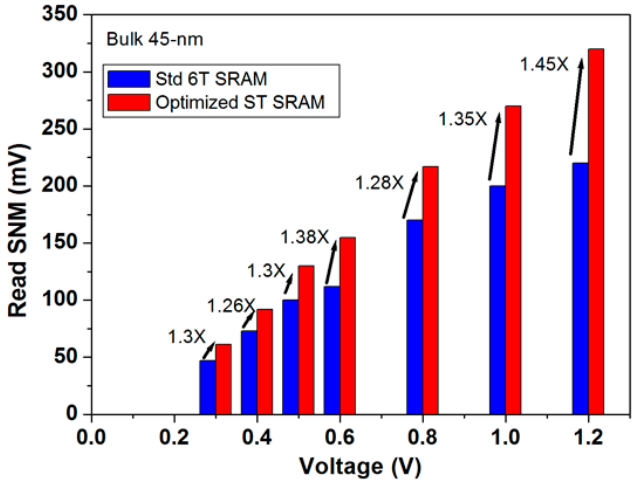


Figure 5. Read SNM obtained by simulation for standard 6T SRAM (blue) and the optimized ST SRAM (red) as a function of voltage.

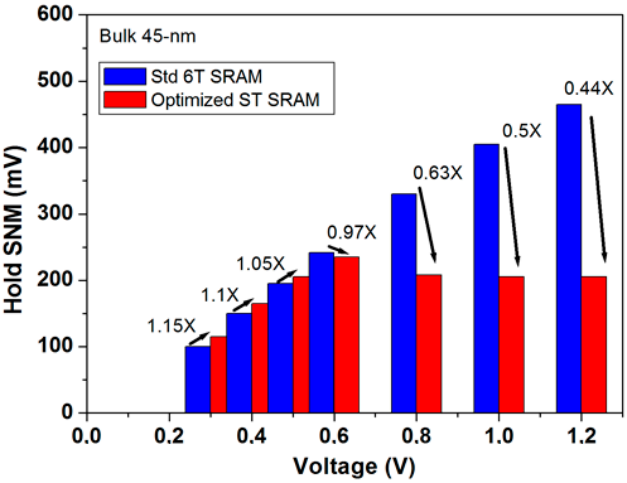


Figure 6. Hold SNM obtained by simulation for standard 6T SRAM (blue) and the optimized ST SRAM (red) as a function of voltage.

The other interesting electrical parameter that can be useful with the aim of investigating the soft error sensitivity of a digital circuit is its upset voltage threshold. It corresponds to the voltage needed to induce the upset of the memory cell. It can be defined when *Vrigh* or *Vleft* reaches *VDD*/2. Figure 7 presents the differences in the evolution of this metric modeled for standard the 6T SRAM (black squares) and the optimized ST SRAM (red dots) as a function of the bias voltage. It is interesting to note that, unlike the SNM, the upset voltage threshold is kept higher for the optimized ST SRAM for each SRAM bias.

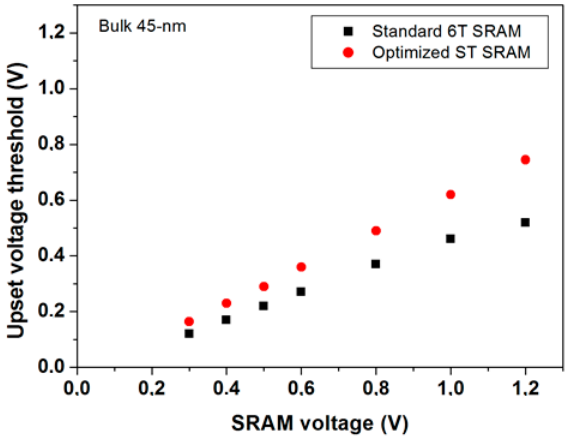


Figure 7. Evolution of the upset voltage threshold simulated for standard 6T SRAM (black squares) and optimized ST SRAM (red dots) as a function of bias voltage.

The competition of the two metrics, i.e., the SNM during the hold operation (Figure 7) and the upset voltage threshold, should impact the SEU susceptibility of the SRAM cell as a function of bias. This point will be presented and discussed for two voltage ranges in the final section of this work.

4. Single Event Effect Modeling

This work uses several modeling tools. First, MUSCA SEP3 (Multi-Scale Single Event Phenomena Prediction Platform) coupled with TERRIFIC is used to calculate the SEU cross sections as a function of the design of SRAM bits [9–11]. MUSCA SEP3 is a soft error prediction tool based on a Monte-Carlo approach which allows a complete simulation from the interactions of radiation particles with the matter to the occurrence of single event effects (SET, SEU) in the IC as shown in Figure 8 below.

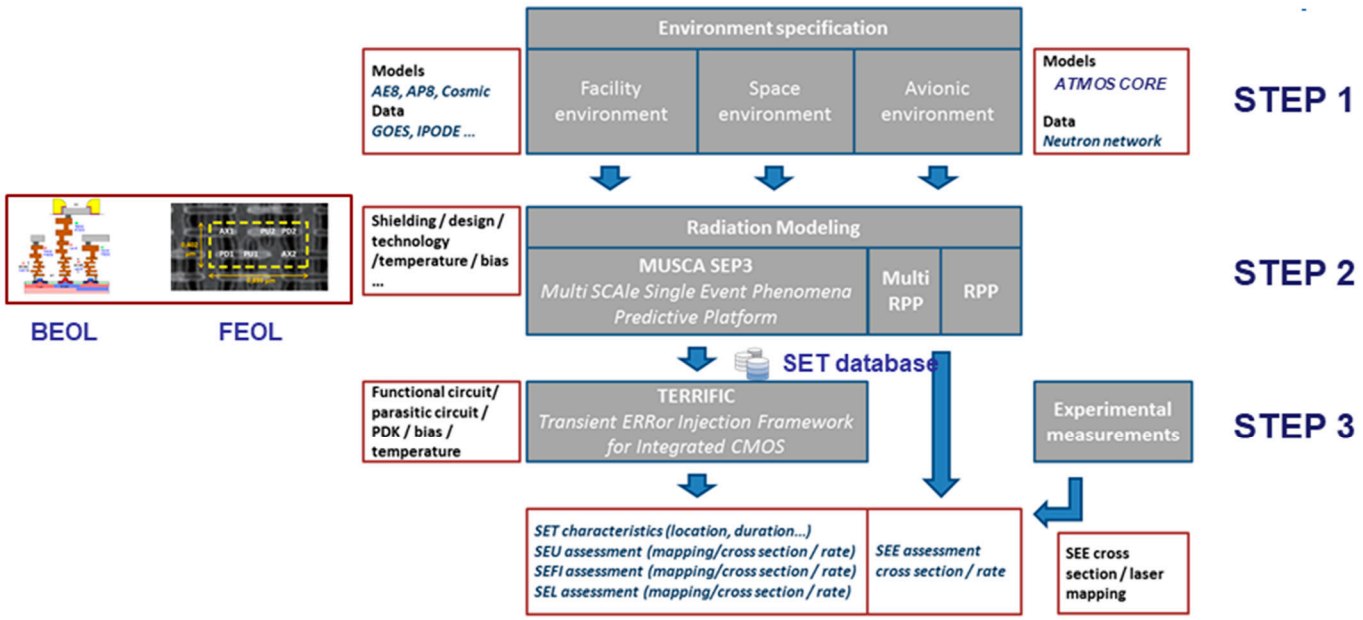


Figure 8. General simulation framework at transistor level based on MUSCA SEP3 and TERRIFIC tools.

The complete principle of the modelling is reported in previous works [5,9–12]. First, these simulations use GEANT4 databases (for nuclear, ionization, interactions . . .) in order to describe the deposition of free carriers by the radiation particle. Second, the parasitic SET

currents of each drain and source implant induced by transport and collection of the charges are calculated by analytical models implemented in the MUSCA SEP3 tool. The analytical 3D models capture the dynamic transport and multiple charge collection mechanisms such as the bipolar amplification, charge sharing effects, etc. Moreover, the shape of the SET is a function of the bias voltage, the layout, and the fabrication processes. The output from MUSCA SEP3 is a SET currents database. This SET database is used by TERRIFIC to perform the injections and the electrical simulations. Thus, the SETs are injected on each floating node at transistor level (on source and drain) for a transient electrical simulation performed by Spectr. It allows us to estimate the soft error response of the circuit. The standard n-MOS and p-MOS model cards are provided by PTM (Predictive Technology Model) [13]. However, because of process variations from one founder to another, these model cards have been calibrated with the aim of fitting with the technology used in the investigated SRAM cells, as presented in the previous section (Cf. Figures 3 and 4) [14].

4.1. Validation of SEU Prediction with Heavy Ion Test Data

The first step of validation is based on a comparison with experimental SEU cross sections for low LET (Linear Energy Transfer) obtained under heavy ions irradiation of the SPARTAN6 FPGA SRAM based on M. Gadlage et al. [15] and N. Sukhaseum et al. [16], and STMicroelectronics SRAMs from G. Gasiot et al. [17]. The LET is the energy lost by the radiation particle in the semiconductor by the Colombian effect. It defines the number of free carriers generated in the substrate which induces the parasite currents and a potential upset (SEU) in a memory cell.

The comparison between experimental data and SEU calculations is presented in Figure 9. A good correlation is shown between SEU measurements and MUSCA SEP3 simulations. Actually, the overestimation is lower than 10% with the calibrated model cards. However, an underestimation of the LET threshold is shown. This point could be due to hypotheses of capacitance characteristics used in the model cards of n-MOS and p-MOS transistors.

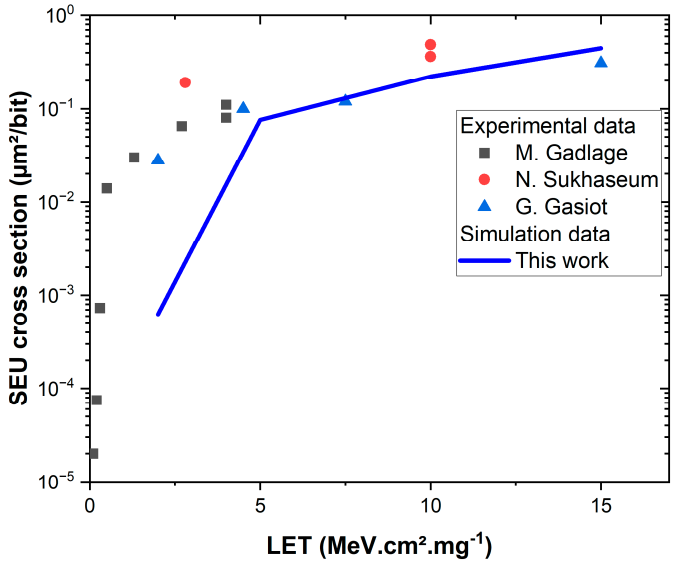


Figure 9. Validation of SEU prediction with experimental data of 45 nm 6T SRAM devices: SPARTAN6 FPGA SRAM based from M. Gadlage et al. [15] and N. Sukhaseum et al. [16], and STMicroelectronics SRAMs from G. Gasiot et al. [17].

In the next section, the impact of voltage scaling on the SEU sensitivity of the SRAM cells is investigated, while the interest in ST circuits as SEU hardening techniques is presented and discussed.

4.2. Impact of Voltage Scaling on SEU Sensitivity

Figure 10 shows the estimation of SEU cross sections of the standard 6T SRAM as a function of LET for a range of core voltage, from 1.2 V down to 0.4 V. As reported in [4,5], the decrease in the core voltage leads to an increase in the SEU sensitivity. A direct correlation between the decrease in SNM (observed in Figure 3) and the decrease in the upset threshold voltage (observed in Figure 10) is highlighted. This point is really interesting and it could allow for anticipating an enhancement or a degradation of the SEU robustness using these two static electrical metrics. Thus, a first global estimation of the SEU sensitivity of the SRAM cell could be determined without radiation data (from experimental tests or radiation simulation tools).

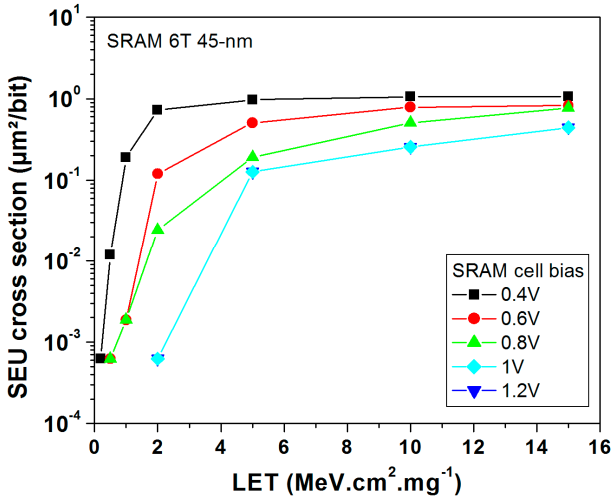


Figure 10. Estimated SEU cross-section of the standard 6T SRAM in 45 nm technology simulated for heavy ions irradiation as a function of the bias of the memory.

In terms of quantitative variations, it is possible to note that for the NT regime (0.4–0.5 V), the LET threshold decreases by a factor of 2. However, even if the decrease in the LET threshold is limited, it is important to note that, at 0.4 V, the saturation of the SEU cross section is reached at a LET of 2 MeV·cm^2·mg^{-1}. This weak variation is mainly due to the initial very high sensitivity of the SRAM cell at nominal bias (1.2 V).

4.3. Impact of Schmitt Trigger on Soft Error Robustness

Figure 11 highlights the improvement of the SEU robustness induced by the use of ST structures in the SRAM cell. The figure presents a comparison of the SEU cross-section of the standard 6T SRAM cell (red dots) and the optimized ST SRAM cell (black squares) obtained for a range of heavy ions from 0.2 MeV·cm^2·mg^{-1} up to 58.8 MeV·cm^2·mg^{-1}. The LET threshold is improved by a factor of 2.5 for the two biases (1 V and 0.4 V). Moreover, the maximal SEU cross-section is decreased by a factor of 4 at nominal bias (1 V). As reported previously, the enhancement is due to the competition of the two metrics: the SNM in hold mode and the upset threshold voltage. It seems that the upset threshold voltage induces a stronger effect than the SNM on the SEU cross-section of the Schmitt trigger SRAM cell. Actually, the SNM of the ST SRAM cell operating at 1 V is decreased by a factor of 0.5× in comparison to the standard 6T SRAM while the upset threshold voltage is increased by a factor of 1.35×.

Figure 12 shows the SEU/MBU ratio for the conventional 6T SRAM (top figures) and the optimized ST SRAM (bottom figures) operating at 1 V (left) and 0.4 V (right).

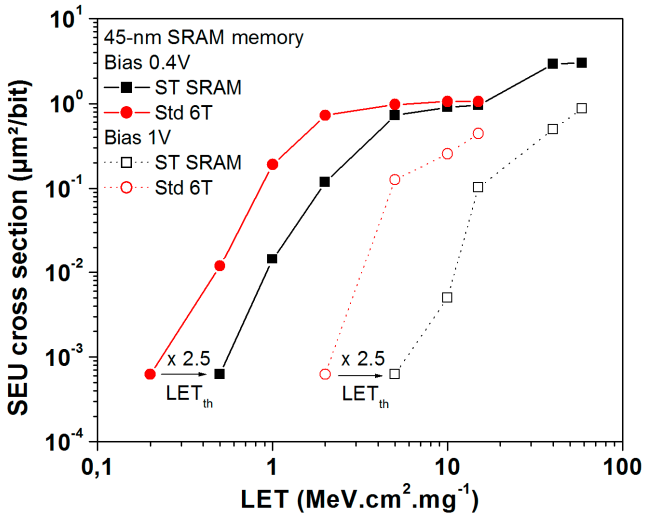


Figure 11. Enhancement of SEU cross section using ST structure in 45 nm SRAM cells operating at 1 V (empty symbols) and (filled symbols) 0.5 V as a function of the LET of heavy ions.

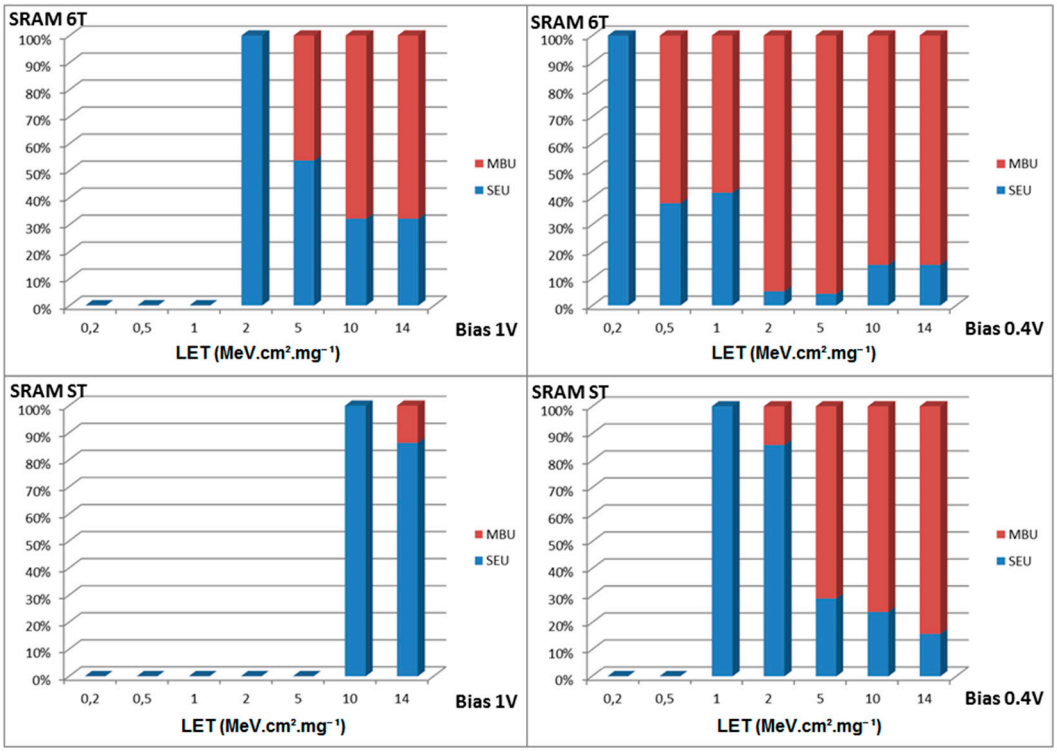


Figure 12. Calculated MBU (in red) and SEU (in blue) ratio as a function of the LET of heavy ions ($MeV{\cdot}cm^2{\cdot}mg^{-1}$) for 6T SRAM (**top**) and optimized ST SRAM (**bottom**) operating at 1 V (**left**) and 0.4 V (**right**).

The contributions of SEU (in blue) and MBU (in red) to the total SEU cross-section are presented as a function of LET. The figure emphasizes the interest in the use of optimized ST circuits for hardened SRAM cells at nominal and low power (0.4 V). The optimized ST SRAM is sensitive to MBU from 10 $MeV{\cdot}cm^2{\cdot}mg^{-1}$ at 1 V, while the memory is totally immune to SEU below 10 $MeV{\cdot}cm^2{\cdot}mg^{-1}$. For the highest LETs of heavy ions, i.e., 15 $MeV{\cdot}cm^2{\cdot}mg^{-1}$, the optimized ST circuit allows for reducing (by a factor of 6) the MBU occurrence from 95% down to 14%. Because the MBUs are more complex to detect and correct than SEUs, this is critical from a system/circuit point of view. Actually, correction circuit techniques such as EDAC (Error Detection and Correction) allow us to mitigate the

impact of SEU on the system, but it induces some drops in the global performance of the system onboard the satellite.

Thus, the optimized ST SRAM design is a great candidate (from a soft error point of view) to be used in embedded digital systems operating at very low power.

4.4. Discussion of Soft Error Rate on Nanosatellite

For the last section of this work, the impact of SRAM cell design on the operational SER is discussed with their use in nanosatellites in mind. The SER can be defined as the following equation:

$$\mathrm{SER} = \int \sigma_{seu}(let).\frac{d\Phi_{let}}{dlet}.dlet \tag{1}$$

where σ_{seu} is the SEU cross-section of the memory, and Φ_{let} is the flux of heavy ions with a given let.

The tool used for the SER computation is named SEE-U developed by ARTENUM [18]. The simulation tool allows for defining the position and the orientation of the device (in this case the SRAM) in a realistic geometry of the satellite. Figure 13a,b show a 2U nanosatellite platform used for this user case.

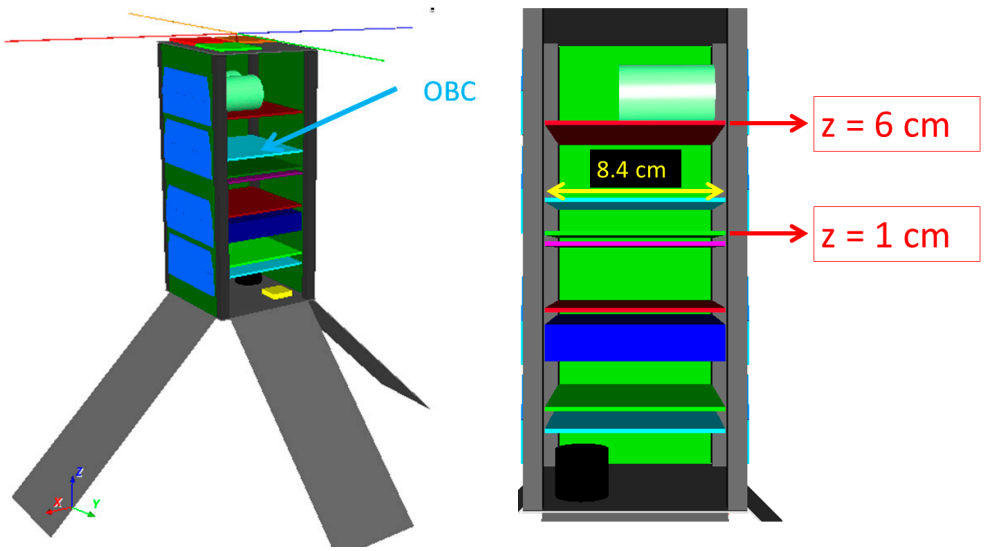


Figure 13. (**a**) The 2U nanosatellite platform with its different boards whose the OBC board, (**b**) potential locations of the OBC board simulated by the tool SEE-U.

This allows for taking into account the anisotropic thickness seen by the device and then the anisotropic flux after the shielding seen by the device.

For this discussion, the space environment has been defined as a geostationary orbit (GEO) with a solar min activity and modeled from CREME96 [19]. This radiation environment has been set because it corresponds to a majority contribution of heavy ions to the SER [20].

Several locations of the OBC (on-board computer) board (in the *Z*-axis) have been considered in the 2U satellite as shown in Figure 13b. For the four different configurations on the *Z*-axis, 25 locations (5×5) of the SRAM device have been simulated on the OBC board. The SEE-U simulations allow for generating SER mappings of the two SRAM designs as shown in Figure 14a,b for the standard SRAM and the optimized ST SRAM, respectively.

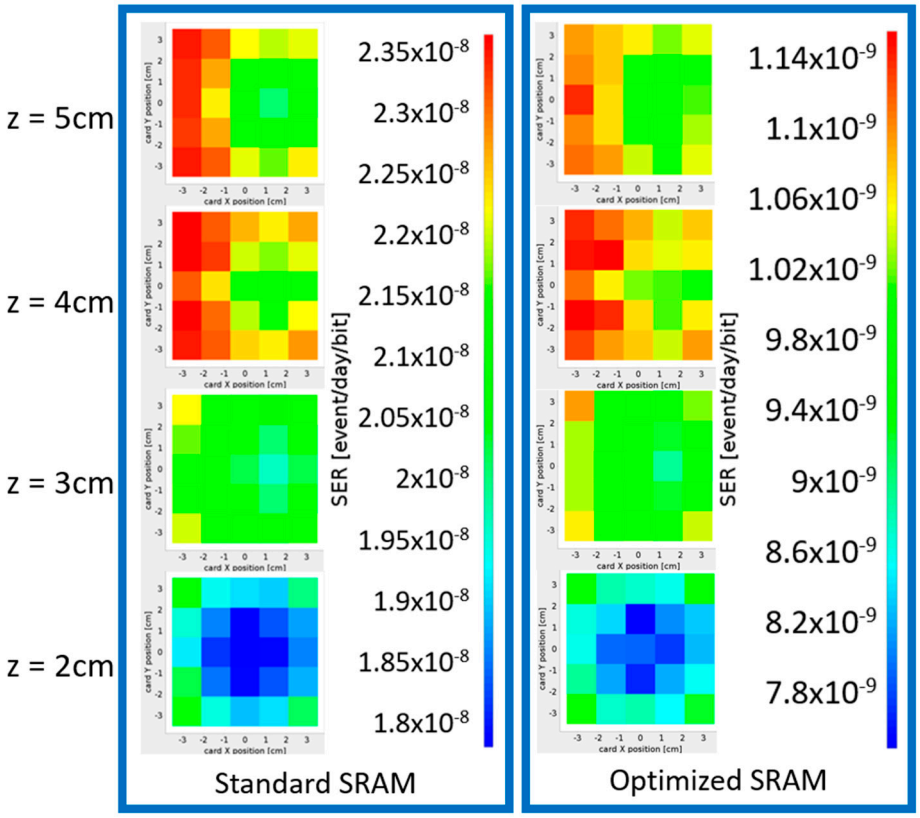


Figure 14. Simulation of the SER mapping as a function of the position of the OBC board in the 2U nanosatellite platform: (**a**) for the Standard SRAM, (**b**) for the optimized ST SRAM.

First, it is interesting to note for both SRAM designs, the minimum and the maximum values of the SER values are obtained on the same positions on the OBC board. More generally, all the SER values evolve the same way depending on the SRAM position in the nanosatellite. This is due to the location of the power board on the top of the nanosatellite structure and the very low dependence of the heavy ions angle on the SEU cross-section of the SRAM cells. Second, the difference of the SER as a function of the *Z*-axis is about 50% for the two SRAM designs as shown in Table 1.

Table 1. Synthesis of SER of the SRAM cells on-board the 2U nanosatellite in GEO orbit.

	Standard SRAM (Event/day/bit)	**ST SRAM (Event/day/bit)**	**Ratio (SER Standard SRAM/(SRA ST SRAM)**
Max SER value	2.35×10^{-8}	1.14×10^{-9}	25
Max SRAM value	1.8×10^{-8}	7.6×10^{-10}	21

The maximum value of the SER for standard SRAM is 2.35×10^{-8} event/day/bit, while it is 1.14×10^{-9} event/day/bit for the ST SRAM. At the same time, the minimum value of the SER for standard SRAM is 1.8×10^{-8} event/day/bit while it is 7.6×10^{-10} event/day/bit for the ST SRAM. Finally, the use of the Schmitt trigger design allows improvement in the SER by a factor of 25.

5. Conclusions

This paper presents the estimation by simulation of the SEU sensitivity of 45 nm SRAM cells at nominal and near-threshold regimes. Comparisons of experimental static noise margin and heavy ions and proton SEU cross section allow for validating the simulation flow.

Regarding the soft error sensitivity of the optimized ST memory, the LET threshold is improved by a factor of 2.5 while the maximum SEU cross-section is decreased by a factor of 4 at nominal bias (1 V). Moreover, the optimized ST circuit allows for reducing (by a factor of 6) the MBU occurrence from 95% down to 14%. This point is critical because the MBU is riskier than the SEU from the system/circuit point of view.

Finally, in order to quantify the interest in the use of the optimized ST SRAM design for nanosatellite applications, the soft error rates have been computed by the mean of the SEE-U tool. It appears that, in GEO orbit, the use of the optimized ST design allows for the improvement of the SER of the SRAM by a factor of 25.

For these reasons, the optimized ST SRAM design is a great candidate to be used in embedded digital systems operating at very low power, such as for nanosatellites, which have a very limited power budget.

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

CMOS	Complementary Metal Oxide Semiconductor
EDAC	Error Detection and Correction
FPGA	Field-Programmable Gate Array
GIDL	Gate Induce Drain Leakage
IoT	Internet-of-Things
LEO	Low Earth Orbit
LET	Linear Energy Transfer
MBU	Multiple Bit Upset
MEO	Medium Earth Orbit
MUSCASEP3	Multi SCAle Single Event Phenomena Prediction Platform
OBC	On Board Computer
PTM	Predictive Technology Model
SER	Soft Error Rate
SET	Single Event Transient
SEU	Single Event Upset
SNM	Static Noise Margin
SRAM	Static Random-Access Memory
ST	Schmitt Trigger
VLSI	Very Large Scale Integration

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