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A High-Power Density DC Converter for Medium-Voltage DC Distribution Networks

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Abstract: A DC converter is the core equipment of voltage conversion and power distribution in a DC distribution network. Its operating characteristics have a profound impact on the flexible regulation of distributed resources in an active distribution network. It is challenging for the existing single-stage conversion topology to meet the requirements of distributed renewable energy connected to a multi-voltage level, medium-voltage grid. It is necessary to study the multistage transform power unit topology further, which can satisfy high reliability, high efficiency, and wide input range. This paper proposes a high-power density DC converter for medium-voltage DC networks with wide voltage levels. It adopts Buck-LLC integrated modular composition. The input ends of the high isolation resonant power unit are connected in series to provide high voltage endurance, and the output ends are connected in parallel to meet the high-power demand and achieve high-power transmission efficiency. The proposed series dual Buck-LLC resonant power unit topology can adjust the duty cycle of series dual buck circuits to meet the needs of different levels of medium-voltage DC power grids. The soft switching problem within the wide input range of all switching tubes is solved by introducing auxiliary inductors, thereby improving energy transmission efficiency. The auxiliary circuit and control parameters are optimized based on the research of each switching tube's soft switching boundary conditions. Finally, an experimental prototype of a 6.25~7 kW power unit is designed and developed to prove the proposed topology's feasibility and effectiveness. Great breakthroughs have been made both in theoretical research and engineering prototype development.

Keywords: DC converter; DC distribution network; Buck-LLC; modular combination; soft switching

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1. Introduction

With the large-scale penetration of renewable energies, storage, and various types of power electronic devices in recent years, the construction of a new power system with renewable energy as the main body has attracted wide attention. Flexible DC distribution network technology, with high-power quality, high stability, and flexible control advantages, has become a research hotspot [1–5]. Among them, the DC transformer is indispensable as the hub of energy convergence and distribution in the DC power grid.

Unlike the AC transformer, through the electromagnetic induction voltage conversion principle, the DC transformer can only use power electronic devices to achieve DC voltage manipulation. Some DC converter topologies have been mature applications, but not all topologies meet the connection needs of different medium voltage levels. A clamp multilevel circuit was first introduced by A. Nabae et al. [6], in which a midpoint clamp topology is proposed. The voltage stress of each device is only half of the DC side voltage. It has been widely used in high-voltage and high-power situations. However, with the voltage levels increasing, the number of power devices also increases, and the number of diodes increases by the square of the voltage levels. Therefore, the current practical

application is mainly a three-level structure, which limits the voltage level of its application to generally less than 3 kV [7,8].

The concept of a modular multilevel structure was first proposed in 2001 by Rainer Marquardt, a scholar at the Bundeswehr University in Munich, Germany. The modular multilevel converter (MMC) adopts the cascade of sub-modules of half-bridge and full-bridge converter structures, which does not have the problems of dynamic voltage equalization and consistent triggering. It has been widely studied and applied in flexible DC transmission [9–15]. In [16], a compact MMC-DC/DC is proposed, which improves the integration of MMC-DC/DC, but the short-circuit fault on the DC side is not considered. When the DC side is short-circuited, a large number of submodule capacitors are short-circuited and discharged, resulting in a large short-circuit impulse current that endangers the safe operation of the transmission line. Thus, Professor Hui Li of Florida State University proposed the improved current source type MMC-DC/DC topology [17,18]. The bridge arm inductor is added based on the full-bridge submodule type MMC structure, and the high-frequency conversion port between the bridge arm inductor is led out. When there is a short-circuit fault on the DC side, the bridge arm inductor can limit the fault current well, and the whole bridge submodule can realize the DC side fault crossing.

The resonant converter and MMC topology combination have also received more and more attention in medium-voltage DC research [19]. A transformer-free resonant modular multilevel converter is proposed in [20], with inherent voltage-balance capability between modules. Moreover, it adopts phase-shift control between modules to obtain higher equivalent switching frequency and step-down ratios. However, the switching tube's high voltage and current stress limit its application in high-voltage and high-power situations. In addition, the lack of electrical isolation limits its potential for further expansion. Therefore, [21] added isolation transformers to the topology, which can achieve electrical isolation and bidirectional energy flow. The voltage gain can also be manipulated by adjusting the number of submodules involved in modulation.

In the modular combined DC converter, [22] describes the connection mode of a modular combined converter in detail. It puts forward the general control method of four series-parallel combined systems. In [23], the modular combined DC converter's operation characteristics and control methods are deeply studied, which is used to interconnect high and low-voltage DC power grids. In [24], the research of modular combined DC converters in flexible DC distribution is carried out. In [25], the modular combined DC converter is improved, and a topology based on four active full-bridge power modules is proposed. Due to its modular structure, high-frequency isolation, and other characteristics, modular combined DC converters have also been widely studied in AC-DC power electronic transformers [26–28].

In summary, the ISOP structure suits high-voltage and low-voltage output in medium-voltage conversion. The modular power unit can realize topology integration with a simple structure. It also has an immense capacity-expansion ability and can fully reflect the advantages of the power unit topology. Moreover, it can improve reliability, which is more suitable for the scenario of renewable energy access studied in this paper. However, with access requirements for broad voltage levels in medium-voltage power grids, single-stage conversion power units can hardly meet the criteria mentioned. The multistage conversion power unit topology with high reliability, high efficiency, and wide input range is required.

This paper proposes a Buck-LLC integrated modular combined DC converter for renewable energy access. A detailed analysis of the converter operating principles is performed to illustrate the features. A comparison with the current existing references and the proposed converter is presented in Table 1.

Table 1. Comparisons among different DC converters in references.

Refs.	Voltage Stress	ZVS Ability	Tracking Performance
[9]	Medium	Poor	Poor
[13]	Low	Medium	Good
[20]	High	Medium	Medium
[25]	Low	Medium	Good
Proposed	Low	Good	Good

Based on the analysis of the working principle of the proposed topology, its DC gain characteristics, power characteristics, and soft switch characteristics were derived. The boundary conditions of soft switching for each switch tube were studied. The auxiliary circuit and control parameters were optimized and designed. The experimental results of the prototype verify the analysis, as mentioned above.

2. Modular Combined DC Converter Topology Based on Buck-LLC Integration

The modular combined DC converter based on Buck-LLC integration in this paper is shown in Figure 1. A series dual-buck integrated LLC converter (SDBuck-LLC) is used as a power unit. The input terminals of each power unit bear high voltage in series and output terminals in parallel to provide stable DC output. Considering the redundancy requirements of power units, redundant switches are connected to the input front of each power unit, which has the advantages of quick cutting of power units, fault current limiting, etc.

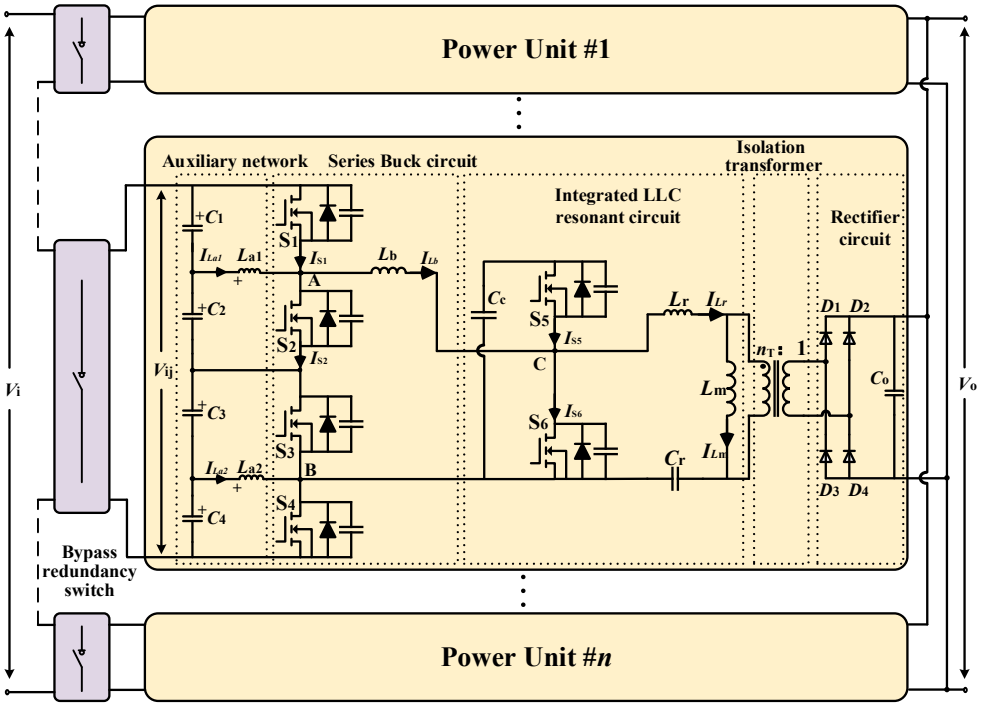

Figure 1. Modular combined DC-DC converter based on Buck-LLC integration.

The above SDBuck-LLC comprises an auxiliary network, series buck circuit, integrated LLC resonant circuit, isolation transformer, and rectifier circuit. The converter uses high-frequency SiC MOSFET S_1~S_6 as the main power switch tubes to meet the stable operation at the high-input voltage operating point. Moreover, all switch tubes can realize soft switching in a wide working range. The buck circuit uses S_1~S_4 as the power switches, withstanding the high input voltage stress in series, and realizes the voltage reduction through the previous stage circuit. The S_5 and S_6 are switching tubes in the rear LLC

resonant circuit, providing convenience for each switching tube's ZVS through the resonator. Input capacitors C_1~C_4 and auxiliary inductors L_{a1} and L_{a2} form an auxiliary network to provide a bias current for S_1~S_4 to meet the conditions of realizing ZVS. As the output inductor of the series buck circuit, L_b is connected with1 S_2 and S_1 at point A and S_5 and S_6 at point C.

The clamping capacitor C_c, S_5, and S_6 together form an integrated half-bridge circuit, which can not only work with the front-end buck inductor L_b to adjust the clamping capacitor voltage V_{Cc}, but also form a half-bridge resonant circuit with the back-end cavity. The resonator cavity comprises the resonant inductor L_r, the resonant capacitor C_r, the excitation inductor L_m, and the high-frequency isolation transformer. The isolation transformer is used to realize the electrical isolation of the input and output terminals, and then the required low-voltage DC is obtained by the rectifier diode D_1~D_4 rectification. The transformer ratio is n_T:1. I_{Lf}, I_{Lr}, I_{Lb}, I_{La1}, I_{La2} are the current flowing through the inductor L_f, L_r, L_b, L_{a1}, and L_{a2}, respectively. The forward reference direction of the currents is given in the form of an arrow in Figure 1.

3. SDBuck-LLC's Operating Principle and Steady-State Analysis

3.1. Analysis of Working Mode and Working Principle

The power unit SDBuck-LLC adopts a fixed-frequency and fixed-phase-shift pulse-width modulation strategy and adjusts the output voltage by controlling the duty cycle of S_1~S_4 in the series buck circuit. The phase-shift angle between S_1 and S_5 and the auxiliary network provides appropriate current bias to ensure all switching tubes can realize ZVS within a wide input voltage range. LLC resonators operate at a fixed frequency. Specifically, the driving signals G_1 and G_4 of switching tubes S_1 and S_4 are the same, and the duty cycle is D_1; the driving signals G_2 and G_3 of the switching tube S_2 and S_3 are the same. $S1$ and $S2$ are complementary switching on. The duty cycle D_2 of the switching tube $S5$ is fixed at 0.5. S_5 and $S6$ are complementary switching on. Define G_1 rising edge leading G_5 rising edge φT_s.

By analyzing the relationship between D_1 and φ, the working state of the converter can be divided into eight working modes, as shown in Table 2, and the brief waveform of each working mode is shown in Figure 2.

Table 2. Submodule SDBuck-LLC operational mode division.

Mode	1	2	3	4
X ($0 < D_1 \leq 0.5$)	$0 < \varphi \leq D_1$	$D_1 < \varphi \leq 0.5$	$0.5 < \varphi \leq D_1 + 0.5$	$D_1 + 0.5 < \varphi \leq 1$
Y ($0.5 < D_1 \leq 1$)	$0 < \varphi \leq D_1$–0.5	D_1–$0.5 < \varphi \leq 0.5$	$0.5 < \varphi \leq D_1$	$D_1 < \varphi \leq 1$

To ensure that the switching tube S_1~S_6 could meet the ZVS condition under various load conditions within a wide input voltage range, the buck inductor current I_{Lb} should be negative at the turn-on time of S_1, S_4, and S_6. The modes X4 and Y1 could not meet the current requirements above. Thus, modes X4 and Y1 are not included in the working range of the power unit. The proposed power unit adopts the fixed frequency and fixed phase-shift control scheme. To adapt to the power transmission in a wide range, the phase shift φT_s should not be too significant.

Thus, mode X3, mode Y3, and mode Y4 are excluded. In mode X2, $D_1 < \varphi$, the inductor L_b has two continuous current states in one cycle. Compared with mode X1, the RMS value of the buck inductor current ILb in mode X2 is slightly higher under the same voltage gain, transmission power, and ZVS conditions. Thus, Mode X2 will lead to higher loss. In summary, mode X1 and mode Y2 are the most suitable operating modes for the proposed SDBuck-LLC within the design requirements. Therefore, the two working modes are analyzed in detail in this paper. The critical waveforms of each mode are shown in Figure 3, and the corresponding equivalent circuits are shown in Figures 4–7. For simple analysis,

two assumptions are followed: (1) all devices, including switching tubes and capacitors, are ideal devices; and (2) the DC voltage ripple at both ends of the output capacitor is ignored.

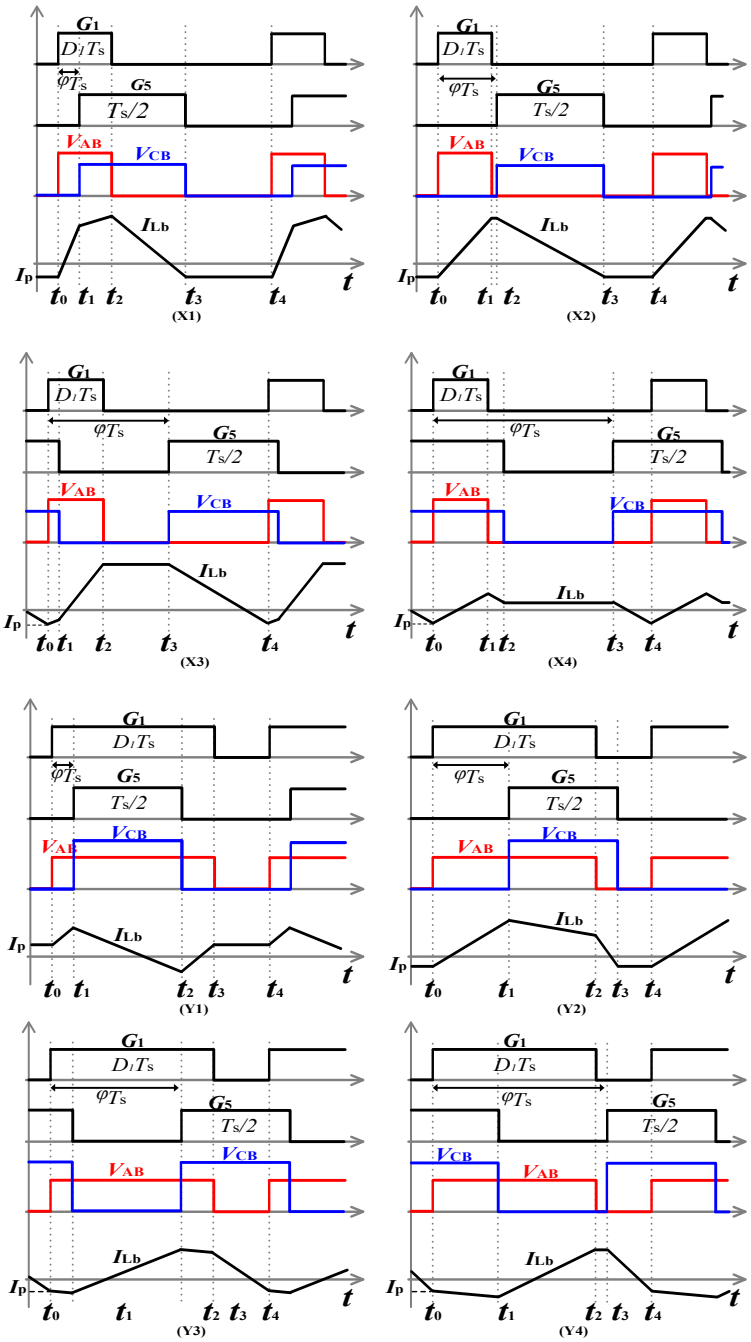

Figure 2. Waveforms of each operational mode of SDBuck-LLC.

(1) Mode X1:

Stage 1 (t_0~$t_{0'}$): Before time t_0, S_6 has been turned on. The driving signals G_1, G_4 of S_1, and S_4 rise at time t_0. Since the reverse diodes of S_1 and S_4 have been switched on, S_1 and S_4 realize ZVS, and V_{AB} rises from 0 to V_i. At this stage, the voltage of the auxiliary inductors L_{a1} and L_{a2} is $-V_{c1}$ and V_{c4}, which are both in the discharge and charging states, respectively. The input voltage V_{CB} of the resonator is 0, and the voltage applied at both ends of the buck inductor L_b is the difference between V_{AB} and V_{CB}, which is equal to Vi. L_b is in a state of high excitation, and I_{Lb} rises rapidly from the initial I_p value. The resonant current I_{Lr} increases by a sine wave at the resonant frequency f_r. The diodes D_2 and D_3 are

on. The excitation inductor voltage V_{Lm} is clamped by the reverse output voltage V_o, and the excitation inductor current I_{Lm} gradually decreases.

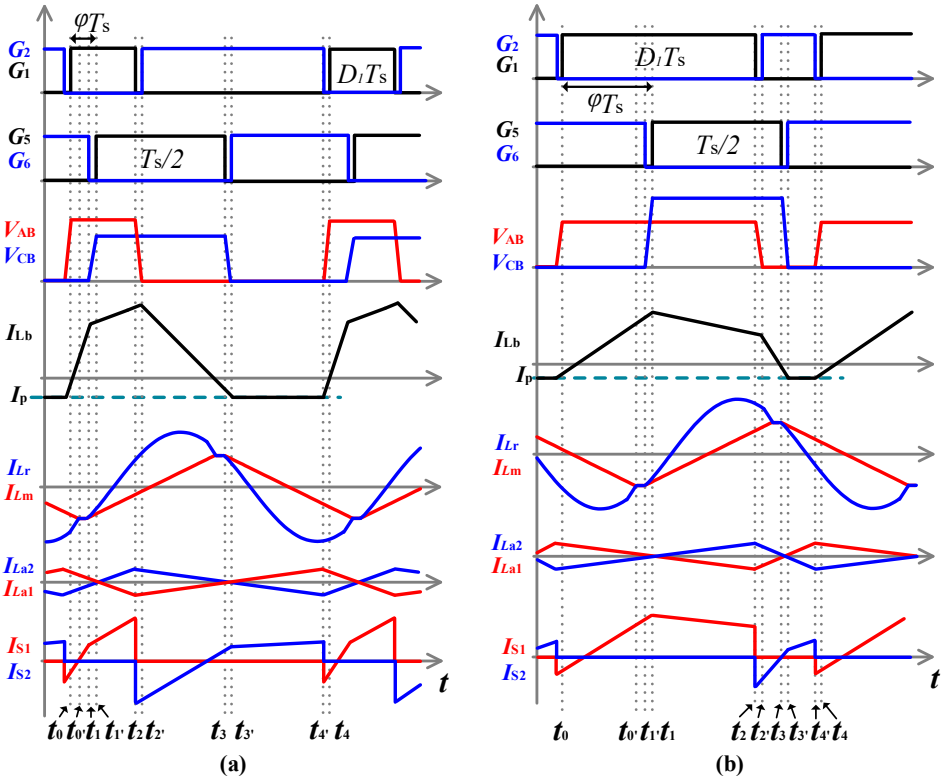

Figure 3. Key voltage and current waveforms of SDBuck-LLC (**a**) mode X1 and (**b**) mode Y2.

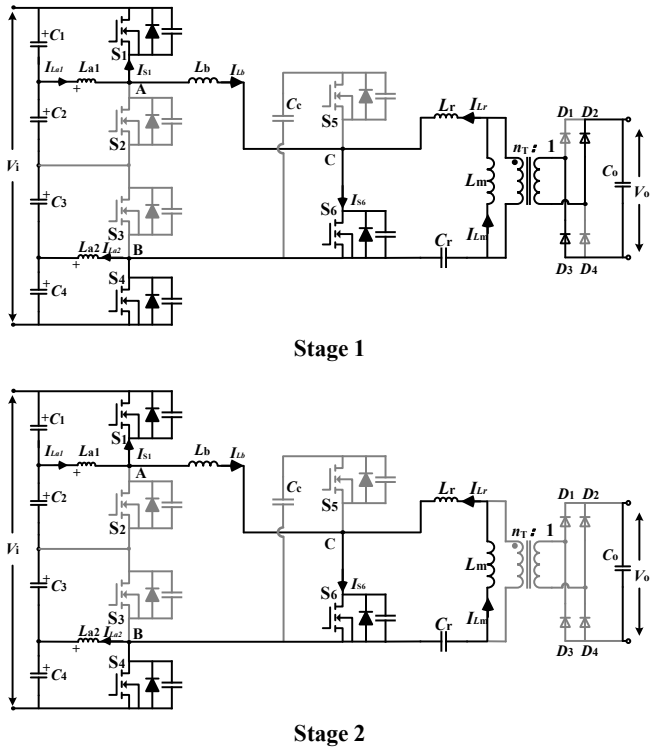

Figure 4. Equivalent circuits of stage 1 and stage 2 in mode X1.

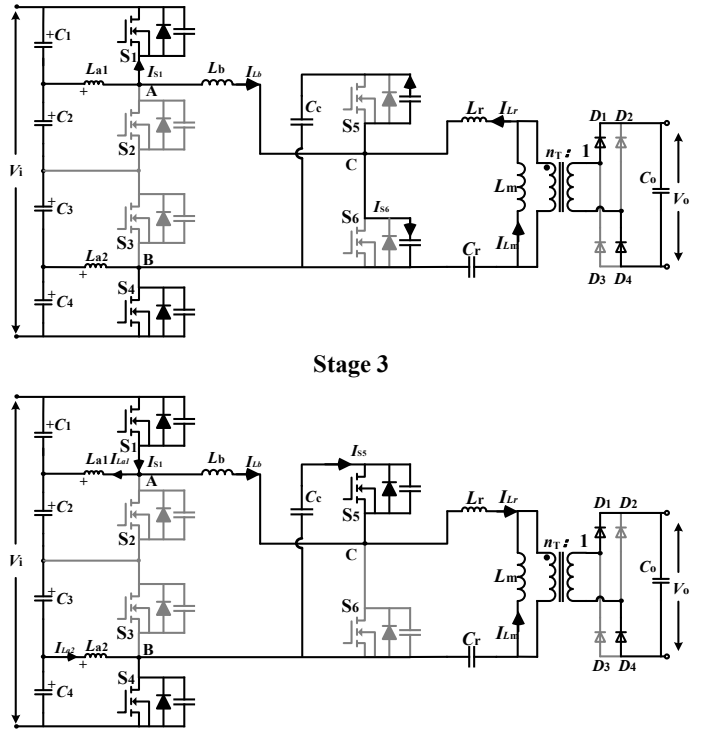

Figure 5. Equivalent circuits of stage 3 and stage 4 in mode X1.

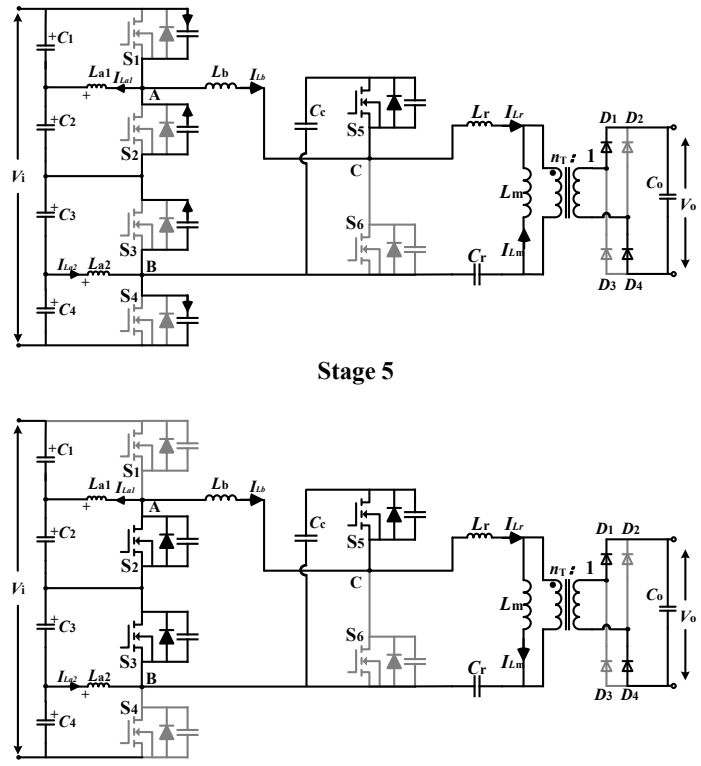

Figure 6. Equivalent circuits of stage 5 and stage 6 in mode X1.

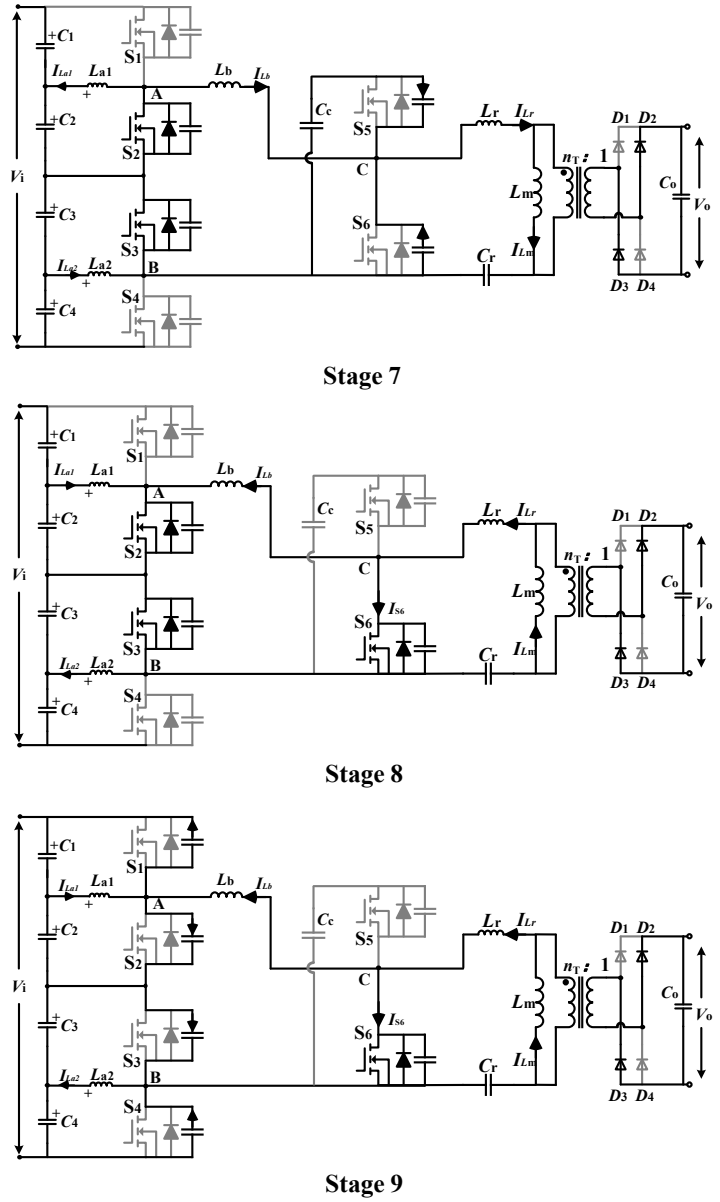

Figure 7. Equivalent circuits of stage 7, stage 8, and stage 9 in mode X1.

Stage 2 ($t_{0'}$~t_1): At $t_{0'}$, I_{Lr} equals I_{Lm}. Diodes D_1~D_4 are turned off at this stage, and no current passes through the transformer winding. No energy is transmitted to the secondary side through the transformer. The resonant inductor L_{r}, the excitation inductor L_{m}, and the resonant capacitor C, participate in the resonance, and the resonant frequency is f_{m}. Because the excitation inductor is higher than the resonant inductor in the LLC resonant design, the change of resonant current at this stage is minimal.

Stage 3 (t_1~$t_{1'}$): At t_1, S_6 is turned off, and S_1 and S_4 remain on. This phase is the dead time between S_6 and S_5. The junction capacitors of S_5 and S_6 begin to discharge and charge, respectively, laying the foundation for the ZVS of S_5. At the same time, D_1 and D_4 switch on, and the excitation inductor Lm exits the resonance link.

Stage 4 ($t_{1'}$~t_2): At $t_{1'}$, the driving signal G_5 of S_5 begins to rise, then S_5 realizes ZVS, and the current value passing through S_5 at the opening moment is the difference between I_{Lr} and I_{Lb}. The input voltage V_{CB} of the resonator rises and equals the clamp capacitor voltage V_{Cc}. The voltage applied at both ends of L_{b} equals V_{i}–V_{Cc}, L_{b} is in a low excitation state, and the growth rate of I_{Lb} slows down. The auxiliary inductor currents I_{La1} and I_{La2} fall and rise simultaneously, but the direction reverses at this stage. In the resonator cavity,

only the resonator inductor and the resonator capacitor participate in the resonance. I_{Lr} increases with the resonant frequency f_r as a sine wave, V_{Lm} is affected by V_o clamp, and I_{Lm} gradually increases.

Stage 5 (t_2~$t_{2'}$): at t_2, S_1 is turned off and S_5 remains open. I_{La1} and I_{La2}, respectively, reach the lowest and highest values. This phase is the dead time between S_2 and S_1, and the junction capacitors of S_1 and S_2 begin to charge and discharge, respectively, providing conditions for the ZVS of S_2.

Stage 6 ($t_{2'}$~t_3): at $t2'$, the driving signal $G2$ of $S2$ rises, and then $S2$ realizes ZVS. The current value passing through S_2 at the opening moment is the difference between I Lra1 and ILb. VAB drops to 0, and the voltage applied at both ends of Lb equals -VCc, which is in a deep demagnetization state. ILb drops rapidly. The voltage applied in the ports of La1 and La2 is Vc2 and -Vc3, respectively, in the charging and discharging state. In this stage, the resonator resonates at two resonant frequencies, fr and fm. The condition of resonant frequency fm is like that of the above stage 2.

Stage 7 (t_3~$t_{3'}$): at t_3, S_5 is turned off, S_2 and S_3 remain on, and the dead time between S_5 and S_6 is entered again. Then, the junction capacitors of S_5 and S_6 begin to charge and discharge, respectively, providing conditions for the ZVS of S_6. At the same time, in this stage, the rectifier bridge starts to reverse pilot, and the excitation inductor L_m exits the resonant link.

Stage 8 ($t_{3'}$~$t_{4'}$): at $t_{3'}$, the driving signal G_6 of S_6 rises, and then S_6 realizes ZVS. The current value passing through S_6 at the opening moment is the difference between the inductor current I_{Lb} and the resonant current I_{Lr}. The input voltage V_{CB} of the resonator drops to 0. The voltage applied at both ends of L_b is 0, and L_b is in the continuous current state. I_{Lb} remains unchanged. The rising and falling rates of I_{La1} and I_{La2} remain the same, but the direction reverses at this stage. In the resonator cavity, only the resonant inductor and the resonant capacitor participate in the resonance. The resonant current I_{Lr} decreases as a sine wave with the resonant frequency f_r. The excitation inductor voltage V_{Lm} is affected by the reverse output voltage V_o clamp, and I_{Lm} gradually decreases.

Stage 9 ($t_{4'}$~t_4): at $t_{4'}$, S_2 is turned off, S_6 remains open, and I_{La1} and I_{La2} reach the highest and lowest values, respectively. The dead time between S_2 and S_1 starts again. The junction capacitors of S_1 and S_2 begin to discharge and charge, respectively. At t_4, the driving signal of S_1 rises, and S_1 realizes ZVS. The current value passing through S_1 at the opening moment is the difference between I_{Lb} and I_{La1}; then, the next cycle is entered.

(2) Mode Y2:

The proposed power unit SDBuck-LLC works in mode Y2 roughly the same as in mode X1. The main differences are as follows:

(a) In stage 4 of mode Y2, the voltage applied at both ends of L_b is V_i-V_{Cc}, which is negative at this time, in a low demagnetization state, and I_{Lb} slowly decreases.
(b) The deep excitation state time corresponding to stages 1, 2, and 3 is lengthened, and the resonant negative half-cycle corresponding to this period is also lengthened.
(c) The deep demagnetization state time corresponding to stages 6 and 7 is shortened, and the resonant positive half-period corresponding to this period is also shortened.

3.2. Characteristics of DC Voltage Gain

The presence of the auxiliary network shown in Figure 1 does not affect the voltage gain of each mode of the power unit, and the overall gain of the converter can be obtained by analyzing the two-stage converter gain separately. Define M_{Buck} as the DC gain of the front-stage buck converter and M_{LLC} as the DC gain of the back-stage half-bridge LLC resonant converter; then, the gain of the power unit is:

$$M_{dc} = M_{Buck} \bullet M_{LLC} \quad (1)$$

Through the above modal analysis, V_{AB} is a square wave with a duty cycle of D_1 and an amplitude of V_i. V_{CB} is a square wave with a duty cycle of 0.5 and an amplitude of V_{Cc}. For buck inductor L_b, according to the volt-second balance principle, it can be obtained:

$$D_1 V_i = (1 - 0.5) V_{cc} \tag{2}$$

Namely:

$$M_{Buck} = V_{Cc} / V_i = 2D_1 \tag{3}$$

Based on fundamental wave analysis, the steady-state equivalent circuit of the SDBuck-LLC resonant converter studied in this paper is shown in Figure 8.

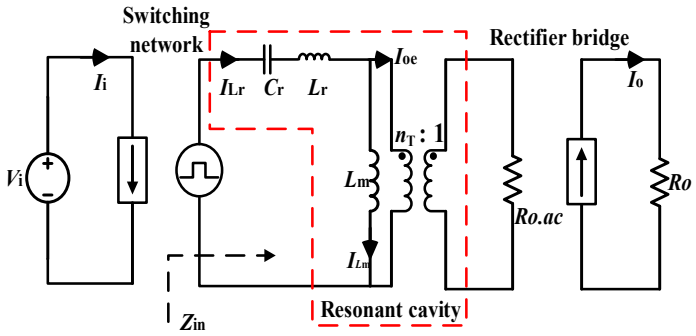

Figure 8. Steady-state equivalent circuit of SDBuck-LLC.

First, the following parameter definitions are listed below:

$$\text{Equivalent resistance } R_{\text{eq}}: \ R_{eq} = {n_{\text{T}}}^2 R_{o.ac} = \frac{8{n_{\text{T}}}^2}{\pi^2} R_o \tag{4}$$

$$\text{Quality Factor Q}: \ Q = \frac{1}{R_{\text{eq}}} \sqrt{\frac{L_{\text{r}}}{C_{\text{r}}}} \tag{5}$$

$$\text{Normalized frequency } f_{\text{n}}: \ f_n = f_s / f_{sn} \tag{6}$$

$$\text{Inductance coefficient } \lambda: \ \lambda = L_r / L_m \tag{7}$$

$$\text{Resonant angular } \omega_{\text{r}}: \ \omega_{\text{r}} = \sqrt{\frac{1}{L_{\text{r}} C_{\text{r}}}} \tag{8}$$

According to the steady-state equivalent circuit shown in Figure 8, the input impedance Zin can be calculated by Equation (9).

$$Z_{in}(j\omega) = jh\omega L_r - \frac{j}{h\omega C_r} + jh\omega L_m // R_{eq} \tag{9}$$

The transfer function of the h harmonic of the resonator can be calculated by Equation (10).

$$H_h(j\omega) = \frac{1}{n_T} \cdot \frac{jh\omega L_m // R_{eq}}{(jh\omega L_m // R_{eq}) + jh\omega L_r - \frac{j}{h\omega C_r}} \tag{10}$$

Therefore, the gain M_{LLC} of the half-bridge LLC resonant circuit can be obtained in Equation (11).

$$M_{LLC} = \frac{V_O}{V_{\text{Cc}}} = \frac{1}{2} \| H_1(j2\pi f_e) \| = \frac{1}{2n_T \sqrt{(1 + \lambda - \frac{\lambda}{f_n^2})^2 + Q^2 \cdot (f_n - \frac{1}{f_n})^2}} \tag{11}$$

LLC resonant converters mainly adjust the output voltage by changing the switching frequency. Thus, a wide input voltage range corresponds to a wide switching frequency adjustment range, reducing the converter efficiency. In practical application, for ZVS realization and efficiency improvement, the switching frequency of the switching tube should be near the resonant frequency f_r as far as possible. Thus, M_{LLC} is 0.5. The integrated converter proposed in this paper works at the resonant frequency point.

In summary, the ideal DC gain of the SDBuck-LLC converter is:

$$M_{dc} = \frac{D_1}{n_T} \tag{12}$$

3.3. Voltage Stress and Power Characteristics

The voltage stress of a power device is one of the critical theoretical bases for its selection. Based on the modal analysis of mode X1, the power unit's voltage stress of each power device is described in detail. In stage 1 and stage 2, the switching tubes S_1, S_6, S_4, and inductor L_b form a loop with the input end, and the output diode D_2 and D_3 are on. The switching tube S_2 and S_3 need to jointly withstand the input voltage V_i, and the voltage at both ends of the inductor L_b is also V_i. The diode D_1 and D_4 must withstand the output voltage V_o, and the switching tube S_5 must withstand the capacitor voltage V_{Cc}.

In stage 6, the switch tube S_2, S_3, S_5, buck inductor L_b, and capacitor C_c form a voltage loop, and the output diodes D_1 and D_4 are on. The switching tubes S_1 and S_4 must withstand the input voltage V_i jointly, and the voltage at both ends of the inductor L_b is V_{Cc}. The diode D_2 and D_3 must withstand the output voltage V_o, and the switch tube S_6 must withstand the capacitor voltage V_{Cc}.

Therefore, the voltage stress of the switching tube S_1~S_4 is:

$$V_{S1\text{-}max} = V_{S2\text{-}max} = V_{S3\text{-}max} = V_{S4\text{-}max} = V_i/2 \tag{13}$$

The voltage stress of the switching tube S_5, S_6 is:

$$V_{S5\text{-}max} = V_{S6\text{-}max} = V_{Cc} = 2D_1V_i \tag{14}$$

The voltage stress of diode D_1~D_4 is:

$$V_{D1\text{-}max} = V_{D2\text{-}max} = V_{D3\text{-}max} = V_{D4\text{-}max} = V_o = D_1V_i \tag{15}$$

According to the above modal analysis, the current expression of inductor L_b in mode X1, Y2 can be obtained as follows; I_p is the current value of the buck inductor when S_1 is turned on, and it is also the minimum current value in its cycle.

$$I_{Lb\text{-}X1Y2}(t) = \begin{cases} I_p + V_i t/L_b & 0 \le t \le \varphi T_s \\ I_p + (V_{Cc}\varphi T_s + (V_i - V_{Cc})t)/L_b & \varphi T_s \le t \le D_1 T_s \\ I_p + (V_{Cc}\varphi T_s + V_i D_1 T_s - V_{Cc}t)/L_b & D_1 T_s \le t \le (\varphi + 0.5)T_s \\ I_p & (\varphi + 0.5)T_s \le t \le T_s \end{cases} \tag{16}$$

It shows that the inductance L_b and phase-shift angle affect the inductor current's peak value. The larger the inductance L_b, the smaller the peak value of inductance current and its effective value, and the smaller the on-loss of the converter.

$$P_i = P_o = \frac{1}{T_s}\int_{t_0}^{t_4} V_{AB}(t)I_{Lb}(t)dt = \frac{1}{T_s}\int_{t_0}^{t_4} V_{CD}(t)I_{Lb}(t)dt \tag{17}$$

$$P_{X1Y2} = 0.5I_pV_{Cc} + \frac{V_{Cc}^2 T_s}{4L_b}\left(-\frac{\varphi^2}{D_1} + 2\varphi - D_1 + 0.5\right) \tag{18}$$

According to Equation (17), the transmission power of the converter under the ideal conditions of mode X1, Y2 can be obtained, as shown in Equation (18).

It can be seen from the above equations that P, Ip, $D1$, and φ are mutually restricted under the premise that the other parameters of the converter device are determined. When the input voltage is determined, the duty cycle $D1$ is also determined, and Ip is closely related to the transmission power P and phase shift φT_s.

Figure 9 shows the relationship between output power P, duty cycle $D1$, and inductance Lb under different phase shifts φT_s when fs = 80 k, Vo = 400 V, and I_p = 3 A in modes X1 and Y2. Obviously, with the increase in phase shift φT_s, the modes X1 and Y2 of the converter gradually tend to work at a higher duty cycle, and the power that can be transmitted also increases. Moreover, the value of inductance L_b also affects the power that can be transmitted; the more significant the L_b, the weaker the power transmission capacity.

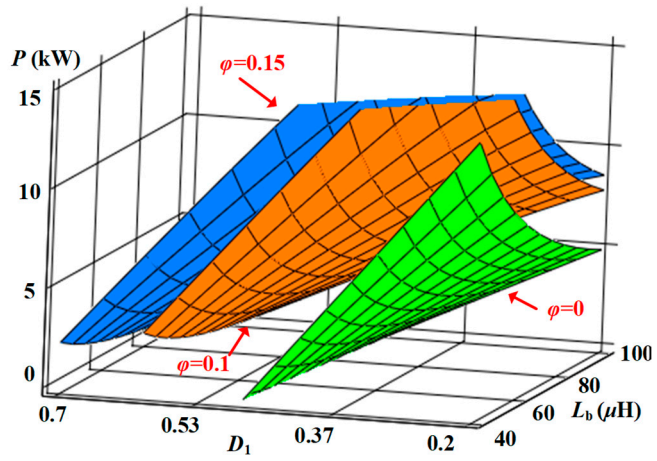

Figure 9. The relationship between power P and D_1, L_b under different phase shifts φT_s.

3.4. Soft-Switching Characteristics

Through modal analysis, it can be found that the ZVS realization of switching tube S_1~S_4 is mainly determined by inductor current I_{Lb}, I_{La1}, and I_{La2}. The ZVS realization of switching tube S_5~S_6 is mainly determined by inductor current I_{Lb} and resonant current I_{Lr}. Taking mode X1 as an example, the switching tubes S_2 and S_3 are off at $t_{4'}$ time. Before the switching tube S_4 and S_1's driving signal rises, the auxiliary inductors L_{a1} and L_{a2} will provide a reverse bias current. The junction capacitance of the switching tube S_4 and S_1 gradually begins to discharge, and the drain-source voltage V_{ds1} and V_{ds4} rapidly drops to 0. From that point, the driving signal of the switching tubes S_1 and S_4 begins to rise, and S_1 and S_4 realize ZVS. For the switching tube S_2 and S_3, the switching tubes S_1 and S_4 are off at t_2 time. Before the switching tube S_2 and S_3's driving signal rises, the inductors L_{a1}, $L_{a2,}$ and L_b provide reverse currents. The junction capacitance of the switching tube S_2 and S_3 gradually begins to discharge, and the drain-to-source voltage V_{ds2} and V_{ds3} rapidly drops to 0. From that point, the driving signal of the switching tube S_2 and S_3 begins to rise, and S_2 and S_3 realize ZVS. For the switching tube S_5, the switching tube S_6 is off at $t_{1'}$, and before the drive signal of S_5 rises, the buck inductor L_b will provide a reverse current for S_5. The junction capacitance of S_5 gradually discharges, and the drain-to-source voltage V_{ds5} rapidly drops to 0. After that, the drive signal of S_5 begins to rise, and S_5 realizes ZVS. For the switching tube S_6, the switching tube S_5 is off at t_3, and before the driving signal of the switching tube S_6 rises, the reverse current comes from the resonant inductor L_r. The junction capacitance of the switching tube S_6 gradually begins to discharge, and the drain-to-source voltage V_{ds6} rapidly drops to 0. After that, the driving signal of the switching tube S_6 begins to rise, and S_6 realizes ZVS. It is defined that the complete charge and discharge current of the junction capacitor is ΔI_{ZVS}. To ensure that the junction capacitor can discharge to 0 to meet ZVS in each switching dead time, the instantaneous current value of the switching tubes at the opening time must be less than $-\Delta I_{ZVS}$.

Therefore, the ZVS condition of each switching tube in the power unit can be expressed by the following equation:

$$I_{\text{S1-on}} = I_{\text{S4-on}} = I_{\text{Lb}}(t_0) - I_{\text{La1}}(t_0) \leq -\Delta I_{\text{ZVS}} \tag{19}$$

$$I_{\text{S2-on}} = I_{\text{S3-on}} = I_{\text{La1}}(t_{2'}) - I_{\text{Lb}}(t_{2'}) \leq -\Delta I_{\text{ZVS}} \tag{20}$$

$$I_{\text{S5-on}} = I_{\text{Lr}}(t_1) - I_{\text{Lb}}(t_1) \leq -\Delta I_{\text{ZVS}} \tag{21}$$

$$I_{\text{S6-on}} = I_{\text{Lb}}(t_{3'}) - I_{\text{Lr}}(t_{3'}) \leq -\Delta I_{\text{ZVS}} \tag{22}$$

By extension of the power expression mentioned above, Equation (23) can be obtained.

$$I_{\text{p}} = \frac{2P_{\text{X1Y2}}}{V_{\text{Cc}}} - \frac{V_{\text{Cc}}^2 T_{\text{s}}}{2L_{\text{b}} V_{\text{Cc}}}\left(-\frac{\varphi^2}{D_1} + 2\varphi - D_1 + 0.5\right) \tag{23}$$

Then, Equation (24) can be obtained:

$$I_{\text{Lb}}(t_{3'}) = I_{\text{Lb}}(t_0) = I_{\text{p}} \tag{24}$$

According to the above analysis, when the converter is in the half-load or no-load state, its ZVS condition is easier to achieve than the full-load state. Therefore, the following analysis only considers the ZVS condition of the converter at full load. $I_{\text{La1}}(t_{2'})$ and $I_{\text{Lb}}(t_{2'})$ are constant negative and positive values, respectively, so the inherent characteristics of S_3 and S_2 meet the ZVS condition in a wide operating range. The ZVS conditions of S_1, S_4, S_5, and S_6 need to be analyzed according to specific working conditions.

The Fourier expansion expression of the input voltage V_{CB} of the resonator is shown as follows:

$$V_{\text{CB}} = (1 - D_2)V_{\text{Cc}} + V_{\text{sh}} \tag{25}$$

$$V_{sh} = \sum_{h=1}^{\infty} \frac{\sqrt{2}V_{\text{Cc}}}{h\pi}\sqrt{1 - \cos(2h\pi D_2)} \cdot \sin(2h\pi f_{\text{s}} t + \theta_h) \tag{26}$$

Among them,

$$\theta_h = \tan^{-1}\left(\frac{\sin(2h\pi D_2)}{1 - \cos(2h\pi D_2)}\right) = \frac{\pi}{2} - hD_2 \cdot \pi$$

According to the resonator transfer function shown in Equation (10), the expressions of excitation inductance current I_{Lm} and equivalent load current I_{oe} in the steady-state equivalent circuit shown in Figure 8 can be easily derived.

$$I_{\text{Lm}} = n \cdot \sum_{\text{h}=1}^{\infty} \frac{H_{\text{h}} V_{\text{CBh}}}{jh\omega L_m} \tag{27}$$

$$I_{\text{oe}} = n \cdot \sum_{h=1}^{\infty} \frac{H_h V_{\text{CBh}}}{R_{eq}} \tag{28}$$

The resonant current I_{Lr} can be obtained by adding the above two formulas.

$$\begin{aligned} I_{Lr}(t) &= \sum_{h=1}^{\infty} \frac{\sqrt{2}V_{\text{Cc}}}{h\pi}\sqrt{1 - \cos(2h\pi D_2)} \\ &\cdot\left\{\frac{|n_{\text{T}} \cdot H_h|}{R_{eq}} \sin(2h\pi f_{\text{s}} t + \theta_h + \angle(n_{\text{T}} \cdot H_h))\right. \\ &\left. - \frac{|n_{\text{T}} \cdot H_h|}{h\omega L_m} \cos(2h\pi f_{\text{s}} t + \theta_h + \angle(n_{\text{T}} \cdot H_h))\right\} \end{aligned} \tag{29}$$

When fs = 80 k, P = 6.25 kW, and V_o = 400 V, the relationship between the opening current I_{S5on} of S_5 and I_{S6on} of S_6, duty cycle D_1, phase shift φT_s, and buck inductance L_b can be obtained by combining the inductance expression (16) derived above, as shown in Figures 10 and 11, respectively. Considering the transmission power and voltage level comprehensively, the value of ΔI_{ZVS} is 1.5 A, and the dark-colored plane in the figure is the reference plane of $I_{on} = -1.5$ A. It can be found that the ZVS range of S_6 and S_5 is relatively wide. When φ is less than 0.1, ZVS of S_5 cannot be realized under the condition of a low-duty cycle. The increase in inductance L_b causes the opening current of S_5 to increase. When the duty cycle of S_6 is more significant than 0.3, there are working points where S_6 cannot realize ZVS. But with the increase of phase shift φT_s or the decrease of inductance L_b, the working range meeting the ZVS condition will gradually expand.

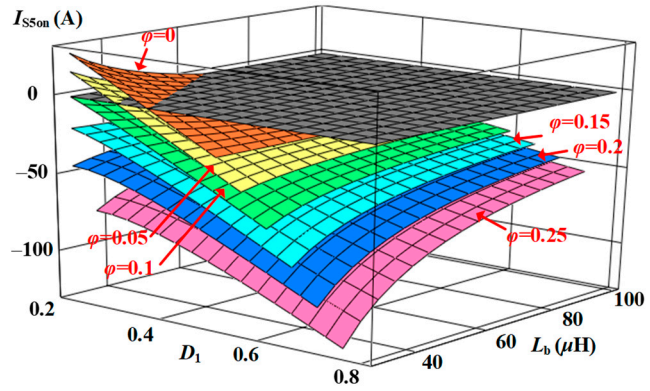

Figure 10. The relationship between I_{S5on} and D_1, L_b under different phase shifts φT_s.

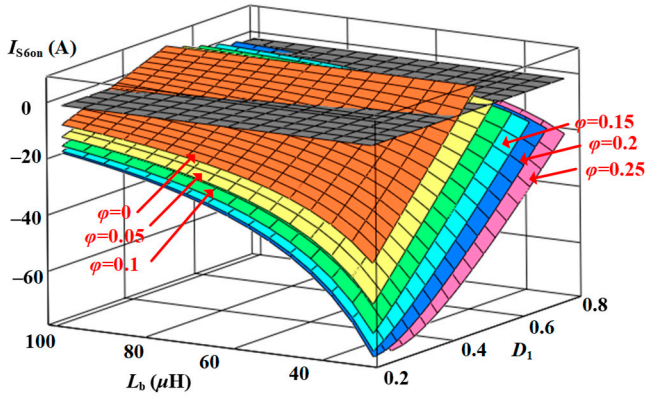

Figure 11. The relationship between I_{S6on} and D_1, L_b under different phase shifts φT_s.

According to the volt-second balance of L_{a1}, namely $(1 - D_1)T_s V_{c2} = D_1 T_s V_{c1}$, and the symmetry of the series-type double-buck circuit ($V_{c1} + V_{c2} = V_{c3} + V_{c4} = V_i/2$), it can be calculated:

$$V_{c1} = (1 - D_1)V_i/2 \tag{30}$$

$$V_{c2} = D_1 V_i/2 \tag{31}$$

The peak value of the auxiliary inductance current can be calculated by the following equation:

$$\left|i_{La1-pk+}\right| = \left|i_{La1-pk-}\right| = \frac{1}{L_{a1}} \int_{D_1 T_s/2} V_{c1} dt = \frac{D_1(1 - D_1)}{4 f_s L_{a1}} V_i \tag{32}$$

$$I_{S1\text{-}on} = I_{S4\text{-}on} = I_p - \frac{D_1(1 - D_1)}{4 f_s L_{a1}} V_i \tag{33}$$

When f_s = 80 k, P = 6.25 kW, V_o = 400 V, and L_b = 75 µH, the relationship between the opening current I_{S1on} and I_{S4on} of S_1 and S_4, duty cycle D_1, phase shift φT_s, and auxiliary inductance L_{a1} can be obtained, as shown in Figure 12. The gray plane in the figure is the reference plane of I_{on} = −1.5 A. The increase in phase shift φT_s reduces the ZVS difficulty of S_1 and S_4; the decrease of auxiliary inductance L_{a1} increases the negative bias current when the switching tube is opened, making ZVS easier to realize. At the same time, the introduced bias current will lead to a slight increase in the conduction loss. From this point of view, the value of the auxiliary inductance L_{a1} should not be too small.

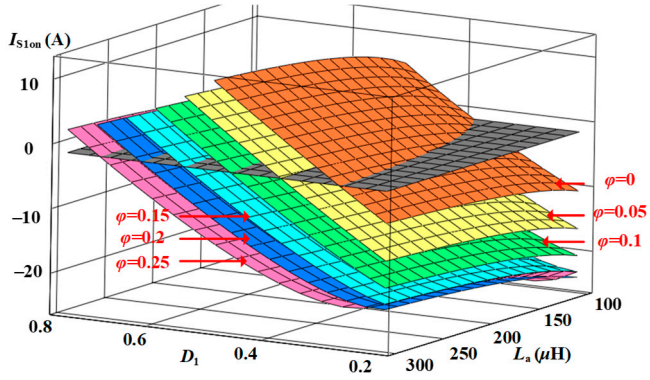

Figure 12. The relationship between I_{S1on}, I_{S4on}, and D_1, L_b under different phase shifts φT_s.

4. Experimental Verification

4.1. Experimental Prototype

An experimental prototype of 6.25~7 kW was designed and developed to prove the feasibility of the proposed power unit topology and the correctness of the above analysis. It meets the requirements of a wide input voltage range of 750 V~1430 V. Table 3 shows the device parameters of the experimental prototype, and Figure 13 shows the experimental prototype.

Table 3. Experimental prototype parameters.

Parameters	Values	Parameters	Values
Input voltage (V_i)	750 V~1430 V	Rated output power (P_o*)	6.25~7 kW
Output voltage (V_o)	400 V	Rated switching frequency (f_{sn})	80 kHz
Resonant inductor (L_r)	14.3 µH	Transformer turns ratio (n_T)	1:1
Input capacitance (C_1~C_4)	50 µF	Auxiliary inductors (L_{a1}, L_{a2})	180 µH
Phase shift (φ)	0.15	Resonant inductor (L_b)	75 µH
Clamp capacitor (C_c)	55 µF	Resonant capacitance (C_r)	276.6 nF

4.2. Experimental Scheme

The DC converter engineering prototype meets the needs of 6–10 kV medium-voltage DC power grid access, including eight power units, with one power unit redundancy switching capability. When eight power units operate, the input voltage range of a single power unit is 750~1250 V, the output voltage is 400 V, and the output power is 6.25 kW. When seven power units operate, the input voltage range of a single power unit is 860~1430 V, and the output power is 7.15 kW.

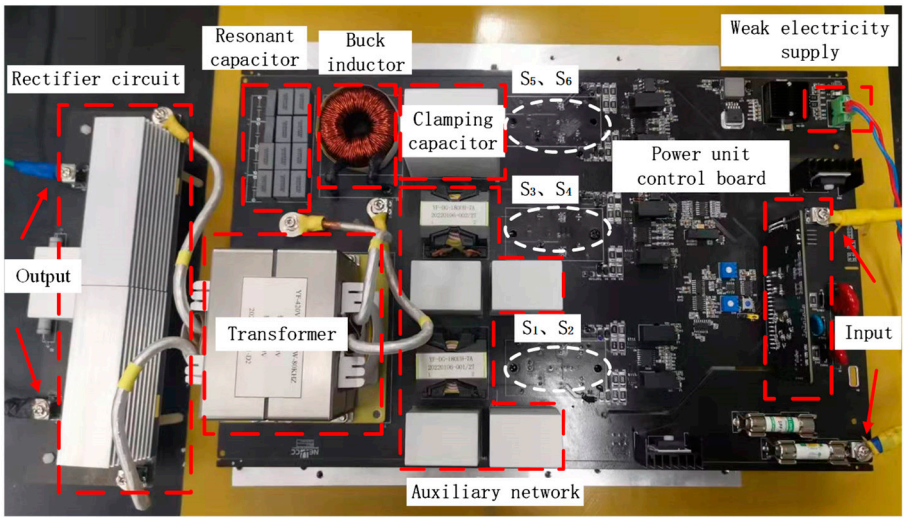

Figure 13. Experimental prototype of SDBuck-LLC.

Figure 14 shows the steady-state experimental waveforms under different input voltages and rated power conditions when eight power units work. V_{Tp} is the input voltage on the primary side of the transformer. Figure 14a,b corresponds to the steady-state waveforms when the input voltage of the power unit is 750 V and D_1 = 0.55. The power unit works in mode Y2. As shown in the figure, the amplitude of V_{AB} is equal to the input voltage, which is 750 V. The amplitude of V_{CB}, the input voltage of the resonator, is equal to the clamp capacitor voltage V_{Cc}, which is 800 V. Under D_2 = 0.5 and nT = 1, the output voltage is stable at 400 V. Currently, the current offset provided by the auxiliary network is the lowest, and it is the most difficult with which to realize ZVS. Figure 14c,d corresponds to the steady-state waveforms when the input voltage of the power unit is 1250 V, D_1 = 0.34, and mode X1. As shown in the figure, the V_{AB} amplitude equals the input voltage, which is 1250 V. V_{CB} amplitude, namely the input voltage of the resonator, is equal to the clamp capacitor voltage V_{Cc}, which is still 800 V. In these two operating modes, each electrical parameters of the LLC resonator are the same. Figure 15 shows the steady-state experimental waveforms when the input voltage of the power unit is 1400 V when seven power units operate. The output power is 7 kW, D_1 = 0.29, and the power unit works in mode X1. As shown in the figure, the V_{AB} amplitude equals the input voltage, which is 1400 V. The V_{CB} amplitude is equal to the clamp capacitor voltage V_{Cc}, which is still 800 V.

Figure 16 shows the ZVS waveforms of each switching tube at different input voltages under full load conditions. Due to the symmetric relationship between S_1 and S_4, and S_2, and S_3, only related waveforms of S_1 and S_2 are shown in this paper. Figure 16a,c,e,g respectively shows the drain-source voltage and gate-source voltage waveforms of S_1, S_2, S_5, and S_6 when the input voltage is 750 V under full-load conditions. It can be seen that S_1 and S_6 are in the most difficult ZVS condition in the whole working range. The time difference between the falling edge of drain-source voltage and the rising edge of gate-source voltage of S_1 is less than 100 ns. The time difference between the falling edge of drain-source voltage and the rising edge of gate-source voltage of S_6 is only 20 ns. Figure 16b,d,f,h respectively show the drain-source voltage and gate-source voltage waveforms of S_1, S_2, S_5, and S_6 when the input voltage is 1250 V under full-load conditions. The time difference between the drain-source voltage falling edge and the gate-source voltage rising edge of each switching tube is more incredible than 160 ns, which can quickly achieve ZVS.

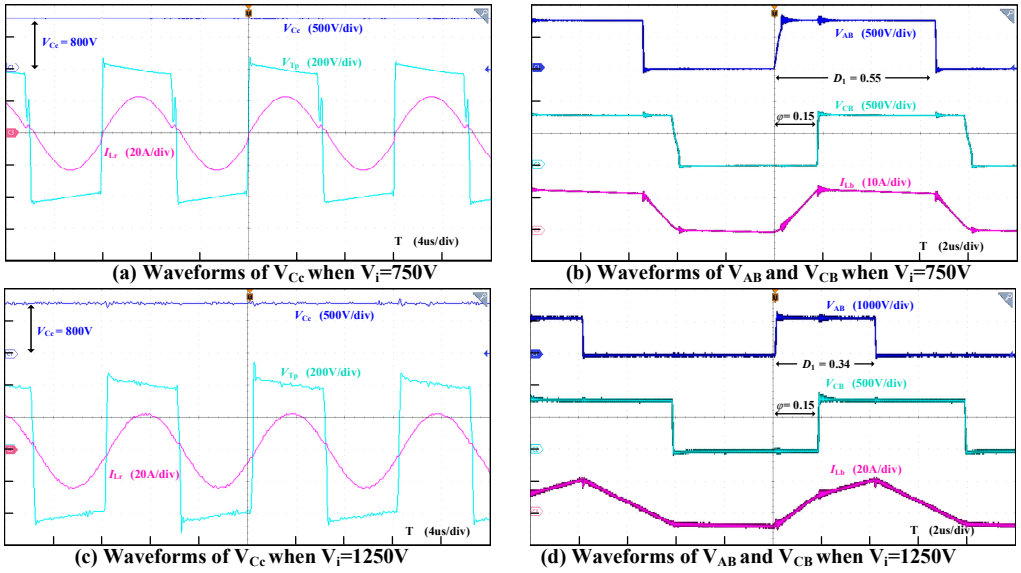

Figure 14. Steady-state experimental waveform of SDBuck-LLC with an output power of 6.25 kW under different V_i.

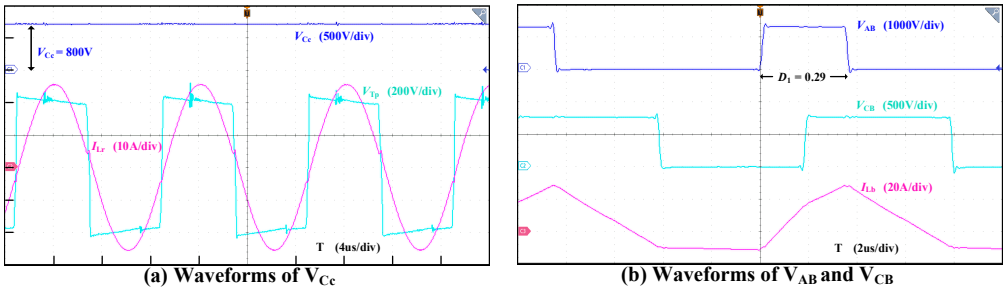

Figure 15. Steady-state experimental waveforms of SDBuck-LLC with an output power of 6.25 kW and input voltage of 1400 V.

Figure 17 shows the ZVS waveforms of each switching tube at different input voltages under a 20% load condition (1200 W). Figure 17a,c,e,g respectively corresponds to the ZVS waveforms of S_1, S_2, S_5, and S_6 when the input voltage is 750 V. Figure 17b,d,f,h respectively corresponds to the ZVS waveforms of S_1, S_2, S_5, and S_6 when the input voltage is 1250 V. It can be seen that under light load conditions, there is a long-time difference between the drain-source voltage falling edge and the gate-source voltage rising edge. Thus, ZVS can be easily realized. In summary, ZVS can be realized in a wide input voltage and output power range for all switching tubes for the proposed SDBuck-LLC resonant converter. Figure 18 shows the efficiency comparison of the power unit under different input voltages. The variation curves of converter efficiency with output power are shown under input voltage 750 V, 950 V, and 1250 V, respectively. The power of each operating point is measured by the power analyzer HIOKI-PW6001. As seen in Figure 18, the efficiency of the power unit decreases slightly with the increase in the input voltage. Still, the efficiency under full-load conditions is higher than 95% in a wide input voltage range.

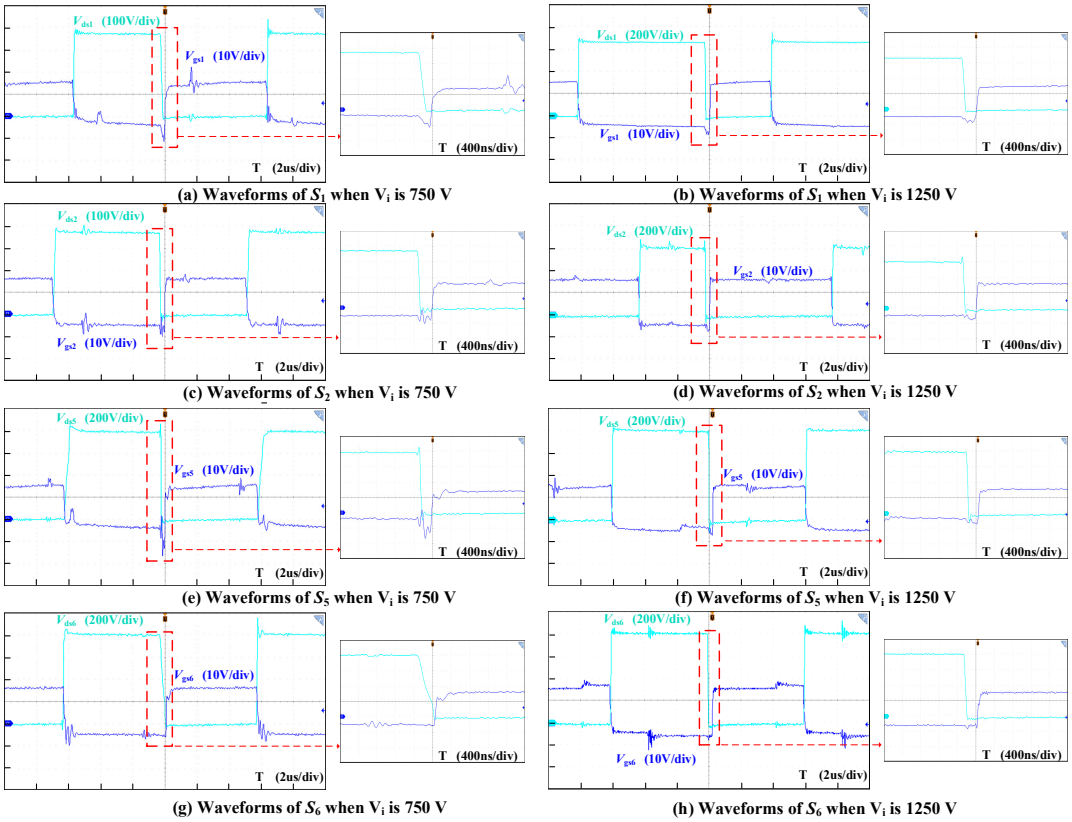

Figure 16. ZVS waveforms of each switch under full load and different input voltages V_i.

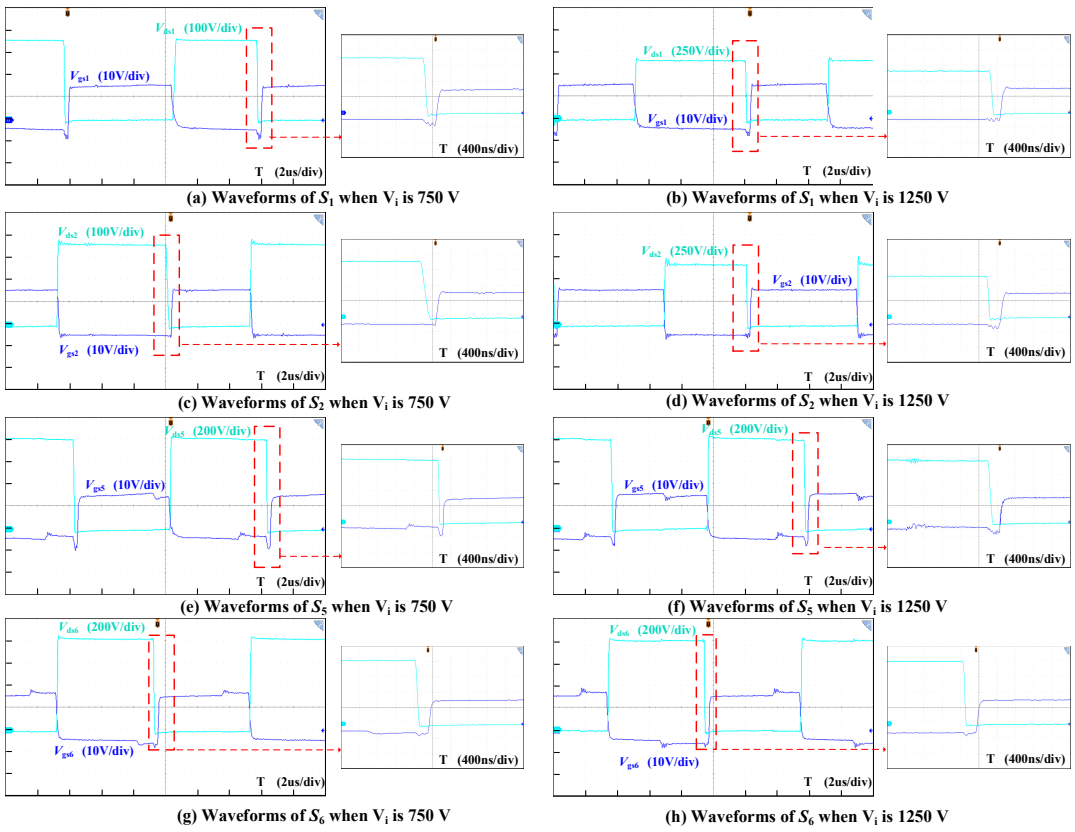

Figure 17. ZVS waveforms of each switch under light load and different input voltages V_i.

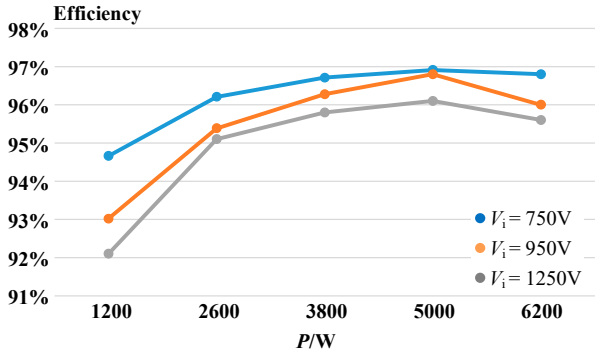

Figure 18. Efficiency curves of SDBuck-LLC under different input voltages V_i.

5. Conclusions

A DC transformer is an efficient power electronic equipment with DC voltage conversion and DC energy distribution abilities, which is the key technology for the development and construction of a DC power grid. This paper studied the DC converter for renewable energy access, and a Buck-LLC integrated modular combined DC converter was proposed. Great breakthroughs were made in theoretical research and engineering prototype development. The topology can meet the requirements of a wide voltage range on the medium voltage side. The converter takes SDBuck-LLC as its power unit, which consists of an auxiliary network, series buck, integrated LLC resonant circuit, isolation transformer, and rectifier circuit. The circuit structure adopts an integrated design and has a high-power density. The duty cycle of a series double-buck circuit can be adjusted to suit the application of a wide input voltage range. Through the auxiliary circuit and the phase shift φT_s introduced, all the switching tubes can realize ZVS in a wide input voltage range. Thus, the turn-on loss is eliminated, and the overall conversion efficiency of the converter is improved. The experimental prototype of the power unit was designed, the experimental results of the prototype were shown, and the feasibility of the proposed power unit was verified. The work in this paper is helpful for subsequent research on DC converters, such as the analysis of the electromagnetic energy interaction mechanism inside the DC converter, the construction of a complete and accurate loss model of the DC converter, and the exploration of the core factors affecting the operation efficiency of the DC converter. Therefore, this work lays a foundation for proposing a globally oriented theory and method for the optimization of the operation efficiency of the DC converter.

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Conflicts of Interest: The authors declare no conflict of interest.

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