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Comparison of 2L + 2M and 6L SVPWM for Five-Phase Inverter to Reduce Common Mode Voltage

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Abstract: Multiphase drives have received a lot of interest because of their several features over traditional three-phase systems for high-power applications. Pulse-width modulation (PWM) approaches are necessary to regulate the supply for multiphase ac drives. As a result, it is vital to continually improve the modulation and control approaches used to upgrade output power converters' quality. This paper offers a comparative analysis of the 2L + 2M and 6L space vector pulse-width modulation (SVPWM) techniques applied to a five-phase two-level voltage source inverter (VSI) fed an inductive (R-L) load. The comparative evaluation is based on measuring the inverter switching losses, the total harmonic distortion (THD) values, and the common mode voltage (CMV) under different operation scenarios. A system model is carried out by MATLAB/Simulink. An experimental prototype is constructed in the lab to validate the theoretical analysis. Simulation results for the system based on the two SVPWM techniques are obtained at different modulation indices and different output frequencies and are confirmed by the experimental results. It has been found that the peak-to-peak CMV of the 6L method is 80% lower than that of the 2L + 2M method. Moreover, 6L SVPWM offers better DC-link utilization compared to 2L + 2M SVPWM.

Keywords: multiphase; voltage source inverter (VSI); space vector pulse-width modulation (SVPWM); common mode voltage (CMV); five-phase inverter; switching techniques

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1. Introduction

Multiphase power electronic converters and drive systems have recently gained popularity due to various benefits over typical three-phase systems for high-current/high-power applications [1,2]. The multiphase topologies of ac drives over three-phase systems, in particular, allow for amplitude reduction, a fault-tolerance capability, an increase in the torque-pulsation frequency, and a decrease in the rotor harmonic losses in electrical machines. As a result, the rating of the semiconductor switches in power electronic converters is reduced [3–6]. They are highly suited for abundant applications, including marine electric propulsion, electrical and hybrid vehicles, locomotive traction, aircrafts, wind electric systems, etc. [7–10]. However, in recent years, applications have been built on a five-phase approach [11–13]. Due to the recent increased growth in multiphase drive systems, it is necessary to continuously enhance the modulation and control approaches used to enhance the goodness of output power converters [14–16].

A two-level multiphase voltage source inverter (VSI) is the most common power electronic converter for these applications, without regard to the sort of ac machine or the number of machine phases [17]. However, the voltage quality and the total harmonic distortion (THD) of the output voltage of two-level VSIs is poor. Hence, many researchers present multilevel VSIs [18–21]. These multilevel VSIs showed a lower THD and a better

voltage quality than conventional two-level VSIs. However, multilevel VSIs require more semiconductor switches than two-level VSIs besides the requirements of a complex control.

To manage the supply for the multiphase ac drives, adopting pulse-width modulation (PWM) techniques is required [22]. For multiphase voltage source inverters, a variety of PWM approaches are studied and described in the literature [22–29].

Different PWM algorithms inevitably result in different behaviors in terms of the performance metrics that may be utilized to create output sinusoidal waveforms, to minimize inverter switching losses, and to decrease the harmonic distortion. Several approaches have been considered for multiphase converters to generate the required sinusoidal output voltage. PWM techniques based on continuous carriers (CPWM) and continuous space vectors (SVPWM) were developed in [22,23]. These methods include sinusoidal PWM (SPWM), elimination of fifth harmonic SPWM, triangular zero-sequence elimination PWM, and four active space trajectory PWM. A comparison between the continuous CPWM and SVPMW techniques with respect to their similarities and distinctions was investigated in [24]. Discontinuous PWM techniques are also developed in [25,26] to be suitable for multiphase converters based on the two-large (2L) and the two-large and two-medium (2L + 2M) modulation techniques, and a comparison between the distinct continuous and discontinuous PWM schemes was reported in [29] based on the 2L + 2M and the four-large (4L) modulation approaches.

The majority of these methods are linked with modest common mode voltage values (CMV) and high dv/dt rates. This has major consequences for machine drives. It produces an increase in the bearing current in a motor drive, which damages the bearing and shortens the motor's life. Furthermore, the CMV can exacerbate electromagnetic interference (EMI) problems. As a result, the system's reliability suffers [20,30,31]. Therefore, it is essential to minimize the CMV level and dv/dt rates in the inverter circuit.

A wide range of physical and computer program methods have been offered to lower the CMV. Most physical techniques include filters or adding additional legs in inverter circuits, which make the structure bulkier and more expensive. The most popular method to minimize the CMV is software solutions using enhanced PWM techniques [32].

Different techniques are used to suppress the CMV, such as multicarrier SPWM, space vector modulation (SVM), shifting phase techniques, and model predictive control (MPC) [33–36]. However, the approaches described above result in an increased leakage current and system cost. Two-dimensional, three-dimensional, and four-dimensional SVM schemes were developed to reduce the CMV and obtain sinusoidal output voltage [37–39]. The controlled continuous and noncontinuous SVPWM methods were introduced in [40] to minimize the switching losses in a VSI fed five-phase induction motor drives. The six-large (6L) SVPWM technique was introduced in [41] to diminish the bearing current. Some of these methods increase the time calculation of switching. A modified SVPWM approach that reduces the CMV compared with conventional SVPWM was developed in [42]. However, the modified method increased the THD of both the phase voltage and current.

In general, with the different PWM approaches, SVPWM gives a better performance for all types of power converter circuits. In addition, SVPWM can perform significantly better than MPC in controlling a five-phase VSI fed a load without requiring knowledge of the load model. The majority of enhanced PWM methods are improved SVPWM approaches that use voltage vectors with a negligible CMV effect [43].

The 6L SVPWM technique was described in [41] with a single focus on the influence of the bearing current and shaft voltage. The comparison in [41] did not take into account the effect on the switching losses, the THD of the output current, and the output voltage. Furthermore, the comparison was performed at the unity modulation index. To establish a fair comparison between the 6L approach presented in [41] and the 2L + 2M method introduced in [29], a thorough comparison at various modulation indices and characteristics, such as the switching losses, THD, and CMV, must be performed.

This paper presents a comparative study of the 2L + 2M and 6L SVPWM techniques applied to a five-phase two-level VSI fed an inductive (R-L) load. In this study, the CMV, inverter switching, conduction, and total losses as well as the output voltage THD are used as measuring tools to investigate the performance of the studied SVPWM methods at different modulation index values and different output frequencies. Several simulation and experimental results of the 2L + 2M and 6L SVPWM techniques controlling a five-phase two-level VSI fed an R-L load at different modulation indices and different output frequency values are presented under different situations.

After the introduction section, this article is ordered as follows: Section 2 discusses the essentials of the 2L + 2M and 6L SVPWM techniques, and Sections 3 and 4 introduce the simulation and experimental results, respectively. Finally, the conclusion is presented in Section 5.

2. PWM Techniques for a Five-Phase VSI

Two-level VSIs are widely utilized in motor drives to convert the DC input voltage to an AC output voltage with a controlled frequency and controlled ac voltage magnitudes using different PWM techniques.

Figure 1 shows a graphic representation of a two-level five-phase VSI. The top and bottom switches on each leg could not be closed at the same time, as this would shorten the DC supply. Each leg is represented by a one or a zero: one if the top switch is on and zero if the bottom switch is on. The five-phase VSI has 32 (2^5) allowed switching voltage vectors for connecting the output load endings to the dc-link voltage. The switching voltage vectors are divided into ten zones, each extending the angle of the ($\pi/5$) radian in the α–β plane as illustrated in Figure 2. The thirty-two space vectors are split into thirty active vectors ($V_1 - V_{30}$) and two null vectors (V_z). The active voltage vectors can be divided into three levels according to their voltage vector magnitude. The active and zero vectors and their magnitudes with respect to the DC-link voltage can be as follows: ten large vectors (0.6472 V_{DC}), ten medium vectors (0.4 V_{DC}), ten small vectors (0.2472 V_{DC}), and two null vectors (0), respectively [40], where V_{DC} is the average value of the DC-link voltage.

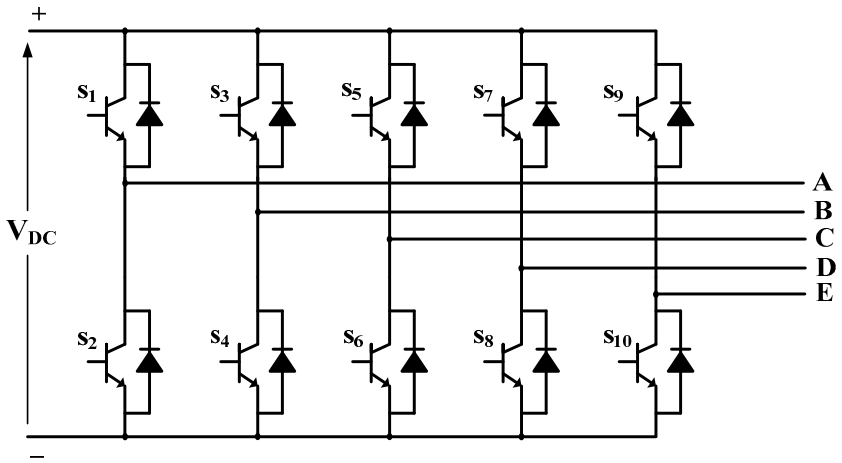


Figure 1. Two-level five-phase VSI.

This section discusses two SVPWM techniques that use these voltage space vectors in different patterns to achieve the command sinusoidal output voltage.

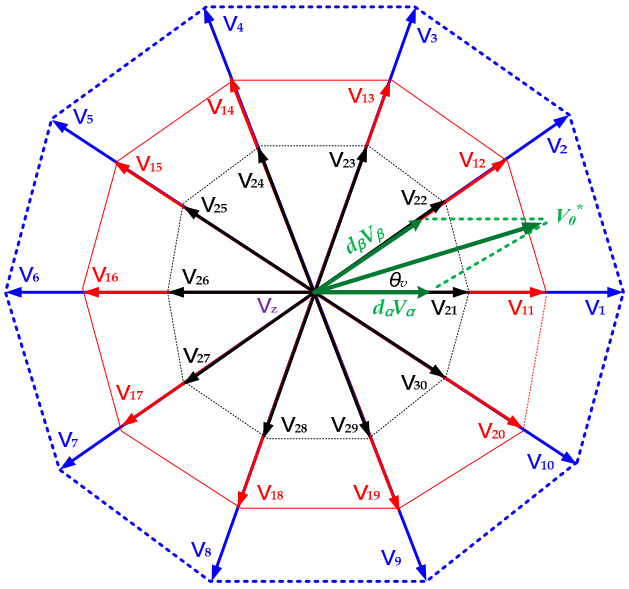


Figure 2. Switching voltage space vectors in the α–β plane.

2.1. 2L + 2M SVPWM Technique

In this method, two large and two medium voltage vectors are used with the zero vectors to achieve the command output voltage vector. The command output voltage vector (V_o^*) can be configured using the adjacent voltage vectors (V_α , V_β , V_z) as determined by Equation (1).

$$V_O^* = d_\alpha V_\alpha + d_\beta V_\beta + d_z V_z \tag{1}$$

The active- and zero-vector duty cycles (d_α , d_β , d_z) are calculated as in Equations (2)–(4).

$$d_\alpha = m_v . \sin\left(\frac{\pi}{5} - \theta_v\right) \tag{2}$$

$$d_\beta = m_v . \sin(\theta_v) \tag{3}$$

$$d_z = 1 - d_\alpha - d_\beta \tag{4}$$

where m_v represents the required output voltage modulation index value and θ_v is the angle of the command voltage vector within the actual decagon zone [44,45]. The highest value of the command voltage vector does not exceed 0.6155 V_{DC} [44,45]. The switching pattern of the 2L + 2M method uses the outer and intermediate vectors, which minimize the switching event number. Therefore, the corresponding large-, medium-, and zero-vector duty cycles in the α–β plane are as follows:

$$d_{\alpha l} = d_\alpha \frac{V_l}{V_l + V_m} \tag{5}$$

$$d_{\alpha m} = d_\alpha \frac{V_m}{V_l + V_m} \tag{6}$$

$$d_{\beta l} = d_\beta \frac{V_l}{V_l + V_m} \tag{7}$$

$$d_{\beta m} = d_\beta \frac{V_m}{V_l + V_m} \tag{8}$$

$$d_z = 1 - d_{\alpha l} - d_{\alpha m} - d_{\beta l} - d_{\beta m} \tag{9}$$

This subdivision devotes 61.8% of the whole active time to large vectors and 38.2% to medium vectors. As a result of this subdivision, the maximum value of the fundamental output voltage does not pass 0.5257 V_{DC} [44,45].

To reduce the count of switching, the switching pattern and space vector sequence for the approach employing 2L + 2M space vectors for the first zone are as those in Equation (10). Table 1 reveals the switching vectors that reduce the switching losses in diverse zones. The switching state V_{15} (00100) in Table 1 signifies that inverter switches S_2, S_4, S_5, S_8, and S_{10} are turned on, while switches S_1, S_3, S_6, S_7, and S_9 are turned off.

Table 1. The switching vectors of the 2L + 2M method for the inverter in all zones to reduce switching losses.

Sector No.	$V_{\alpha m}$	$V_{\alpha l}$	$V_{\beta m}$	$V_{\beta l}$	V_{z1}	V_{z2}
1	V_{11} (10000)	V_1 (11001)	V_{12} (11101)	V_2 (11000)	V_{31} (00000)	V_{32} (11111)
2	V_{13} (01000)	V_2 (11000)	V_{12} (11101)	V_3 (11100)		
3	V_{13} (01000)	V_4 (01100)	V_{14} (11110)	V_3 (11100)		
4	V_{15} (00100)	V_4 (01100)	V_{14} (11110)	V_5 (01110)		
5	V_{15} (00100)	V_6 (00110)	V_{16} (01111)	V_5 (01110)		
6	V_{17} (00010)	V_6 (00110)	V_{16} (01111)	V_7 (00111)		
7	V_{17} (00010)	V_8 (00011)	V_{18} (10111)	V_7 (00111)		
8	V_{19} (00001)	V_8 (00011)	V_{18} (10111)	V_9 (10011)		
9	V_{19} (00001)	V_{10} (10001)	V_{20} (11011)	V_9 (10011)		
10	V_{11} (10000)	V_{10} (10001)	V_{20} (11011)	V_1 (11001)		

Figure 3 illustrates the switching pattern for the top switches of the five-phase VSI in the first zone. It is worth noting that just one of the top switches' states will be altered among two side by side switching states.

$$0.5\,d_{z1} \rightarrow 0.5\,d_{\alpha m} \rightarrow 0.5\,d_{\beta l} \rightarrow 0.5\,d_{\alpha l} \rightarrow 0.5\,d_{\beta m} \rightarrow d_{z2} \rightarrow 0.5\,d_{\beta m} \rightarrow 0.5\,d_{\alpha l} \rightarrow 0.5\,d_{\beta l} \rightarrow 0.5\,d_{\alpha m} \rightarrow 0.5\,d_{z1} \tag{10}$$

$$d_{z1} = d_{z2} = 0.5\,d_z \tag{11}$$

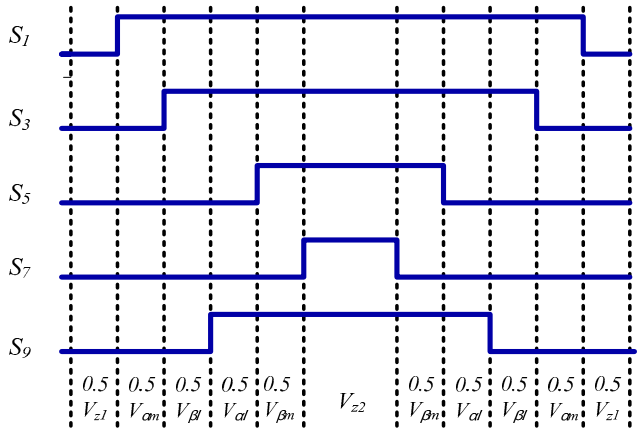


Figure 3. The 2L + 2M switching pattern for the top switches of the five-phase VSI in the first sector.

2.2. 6L SVPWM Technique

As previously indicated, each switching cycle must have a minimum of five vectors. More vectors might be employed, but the switching losses must be considered. The switching losses are relatively substantial in five large (5L) vectors. An extra vector may be added to maintain the switching losses at as low as is feasible. In each switching cycle, six neighboring large vectors with no zero vectors are employed. A cycle will include five

switching events using 6L vectors, while 4L and 5L vectors will have switching counts of seven and six, respectively [41].

The switching pattern of the 6L method uses the outer vectors, which minimize the switching event number. If the vector group chosen is 9, 10, 1, 2, 3, and 4, as illustrated in Figure 4, the corresponding large-vector duty cycles in the α–β plane are as follows [41]:

$$d_9 = 0.5 - \frac{(15 + 5\,g_0)\,V_\alpha + (g_1 + 2\,g_2)\,V_\beta}{2\,V_{DC}\,{g_1}^2} \tag{12}$$

$$d_{10} = \frac{10\,V_\alpha - (3\,g_1 + g_2)\,V_\beta}{V_{DC}\,{g_1}^2} \tag{13}$$

$$d_1 = \frac{(5\,g_0 - 5)\,V_\alpha + (g_1 + 2\,g_2)\,V_\beta}{V_{DC}\,{g_1}^2} \tag{14}$$

$$d_2 = \frac{10\,V_\alpha + (g_1 - 3\,g_2)\,V_\beta}{V_{DC}\,{g_1}^2} \tag{15}$$

$$d_3 = \frac{(2\,g_1 + 4\,g_2)\,V_\beta}{V_{DC}\,{g_1}^2} \tag{16}$$

$$d_4 = d_9 \tag{17}$$

where the values of the three constants g_0, g_1, and g_2 are $\sqrt{5}$, $4\,sin(2\pi/5)$, and $4\,sin(\pi/5)$, respectively.

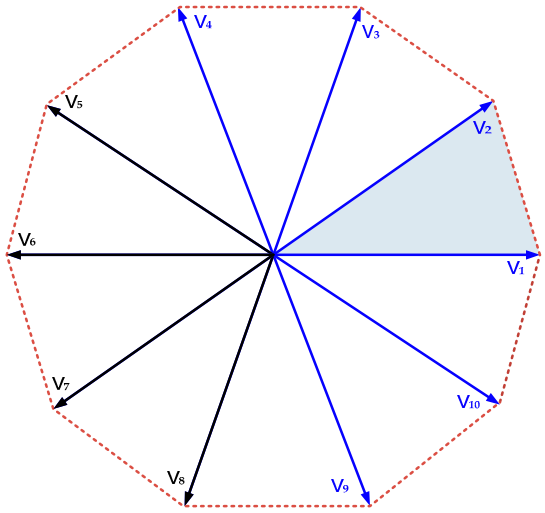


Figure 4. The 6L switching pattern in the α–β plane.

The current sector for a reference voltage of magnitude V_{ref}^* and angle θ is given by Equation (18), where the *ceil* function rounds numbers towards positive infinity to the closest integer and the angle θ lies between 0 and 2π.

The current voltage sector's V_α and V_β values could be determined as in Equations (19) and (20), respectively.

$$k = ceil\left(\theta / \frac{\pi}{5}\right) \tag{18}$$

$$V_\alpha = V_{ref}^*\,cos\left(\theta - (k-1)\,\frac{\pi}{5}\right) \tag{19}$$

$$V_\beta = V_{ref}^*\,sin\left(\theta - (k-1)\,\frac{\pi}{5}\right) \tag{20}$$

The switching pattern and space vector sequence for the approach employing 6L vectors for the first sector are as those in in Equation (21). Table 2 illustrates the switching vectors that reduce the switching losses in different zones.

Table 2. The 6L switching vectors for the vector group chosen are 9, 10, 1, 2, 3, and 4.

Sector No.	V_9	V_{10}	V_1	V_2	V_3	V_4
1	10011	10001	11001	11000	11100	01100
2	10001	11001	11000	11100	01100	01110
3	11001	11000	11100	01100	01110	00110
4	11000	11100	01100	01110	00110	00111
5	11100	01100	01110	00110	00111	00011
6	01100	01110	00110	00111	00011	10011
7	01110	00110	00111	00011	10011	10001
8	00110	00111	00011	10011	10001	11001
9	00111	00011	10011	10001	11001	11000
10	00011	10011	10001	11001	11000	11100

Figure 5 illustrates the switching pattern for the top switches of the five-phase VSI in the first zone for the approach employing 6L vectors. It is also noteworthy that, between two adjacent switching states, only one of the top switches' conditions will be altered as stated in the 2L + 2M switching pattern.

$$0.5\,d_9 \rightarrow 0.5\,d_{10} \rightarrow 0.5\,d_1 \rightarrow 0.5\,d_2 \rightarrow 0.5\,d_3 \rightarrow\ d_4 \rightarrow 0.5\,d_3 \rightarrow 0.5\,d_2 \rightarrow 0.5\,d_1 \rightarrow 0.5\,d_{10} \rightarrow 0.5\,d_9 \quad (21)$$

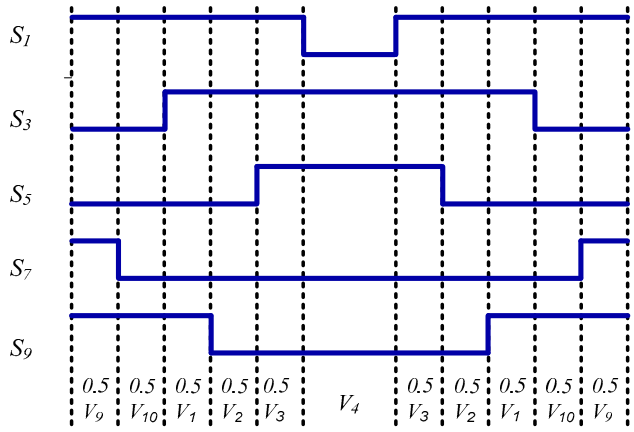


Figure 5. The 6L switching arrangement for the top switches of the five-phase VSI in the first zone.

3. Simulation Results

This part describes and compares the simulation results of the 2L + 2M and 6L SVPWM approaches of the five-phase inverter. The DC supply voltage is set to 100 V, and the switching frequency is 10 kHz, with a sampling time of 1 µs. An inductive load (R = 17 ohm, and L = 0.25 H) has been tied to the five-phase output terminals of the VSI. Figure 6 compares the CMV of the two SVPWM methods at the unity modulation index and a 50 Hz output frequency. This comparison shows that the peak-to-peak CMV of the 6L method is 80% lower than that of the 2L + 2M method. This reduces the shaft voltage and the bearing current in the case of the 6L method.

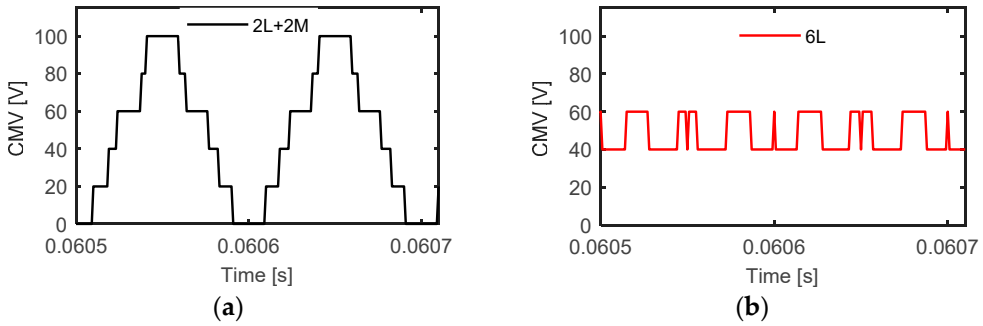


Figure 6. Simulation results of the CMV at unity modulation index and 50 Hz for (**a**) 2L + 2M and (**b**) 6L methods.

Figures 7 and 8 show the simulation results of the phase and line voltages of the two SVPWM methods at the unity modulation index and a 50 Hz output frequency, respectively. A 72° phase shift between each phase has been observed in the two SVPWM methods with a 0.02 s time period. The voltage quality of the line and phase voltage is not good because the two PWM methods have been applied to the conventional five-phase two-level VSI. To enhance the voltage quality and to reduce the THD of the phase and line voltages, it is recommended to apply a multilevel VSI instead of a conventional two-level VSI as discussed in this paper.

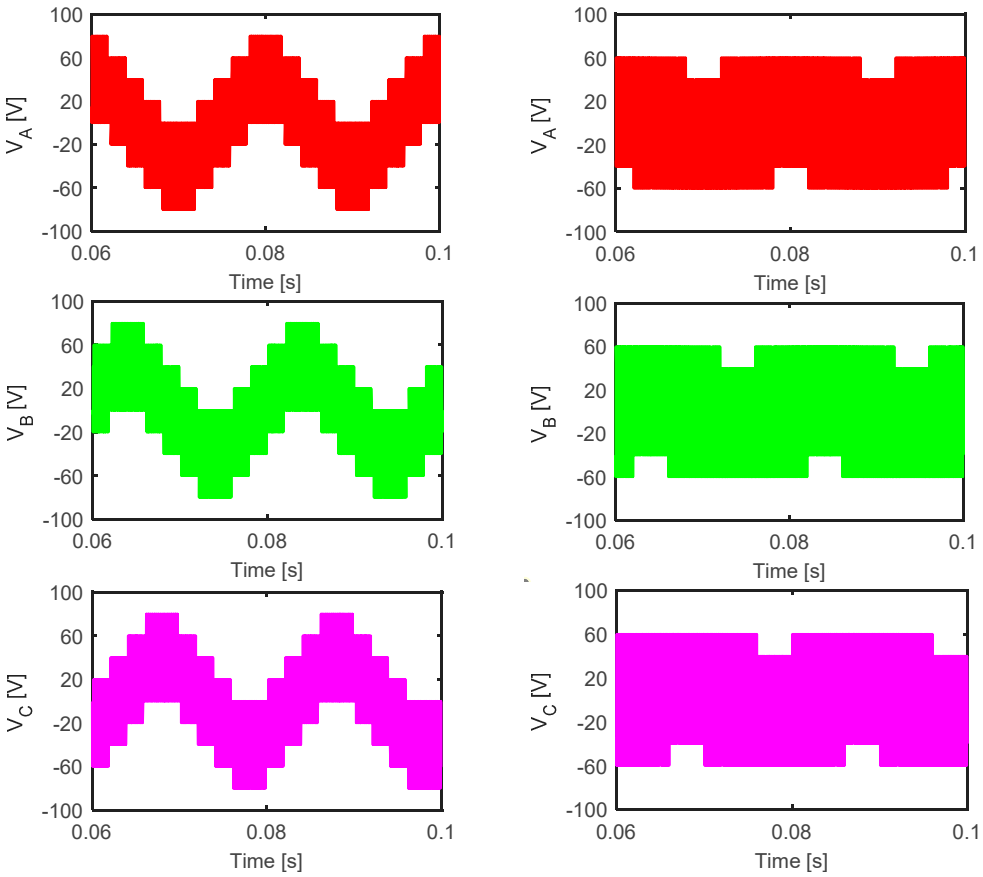


Figure 7. *Cont.*

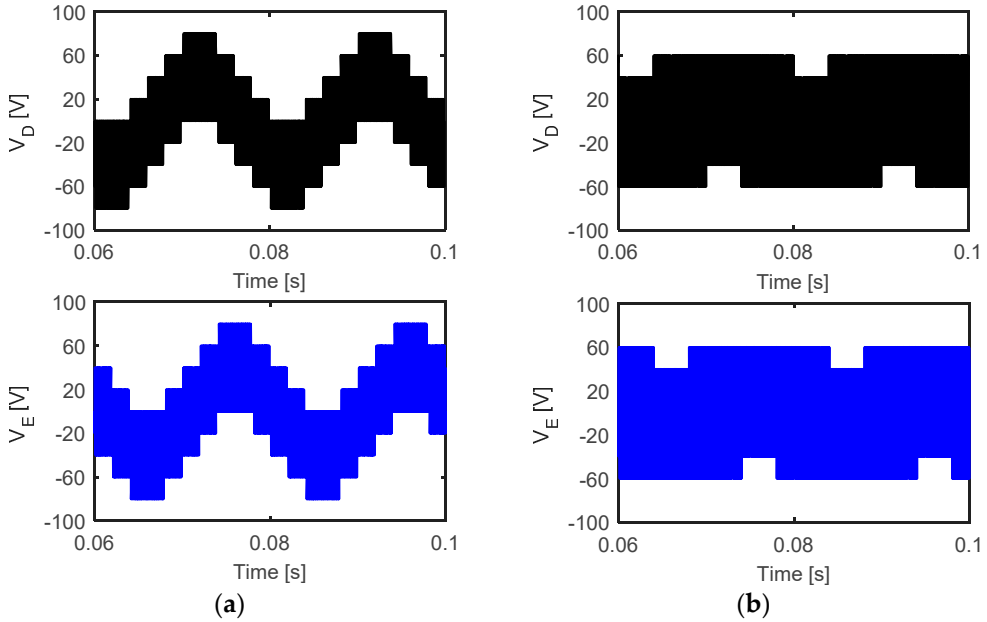


Figure 7. Simulation results of the output phase voltages at unity modulation index and 50 Hz for (**a**) 2L + 2M and (**b**) 6L methods.

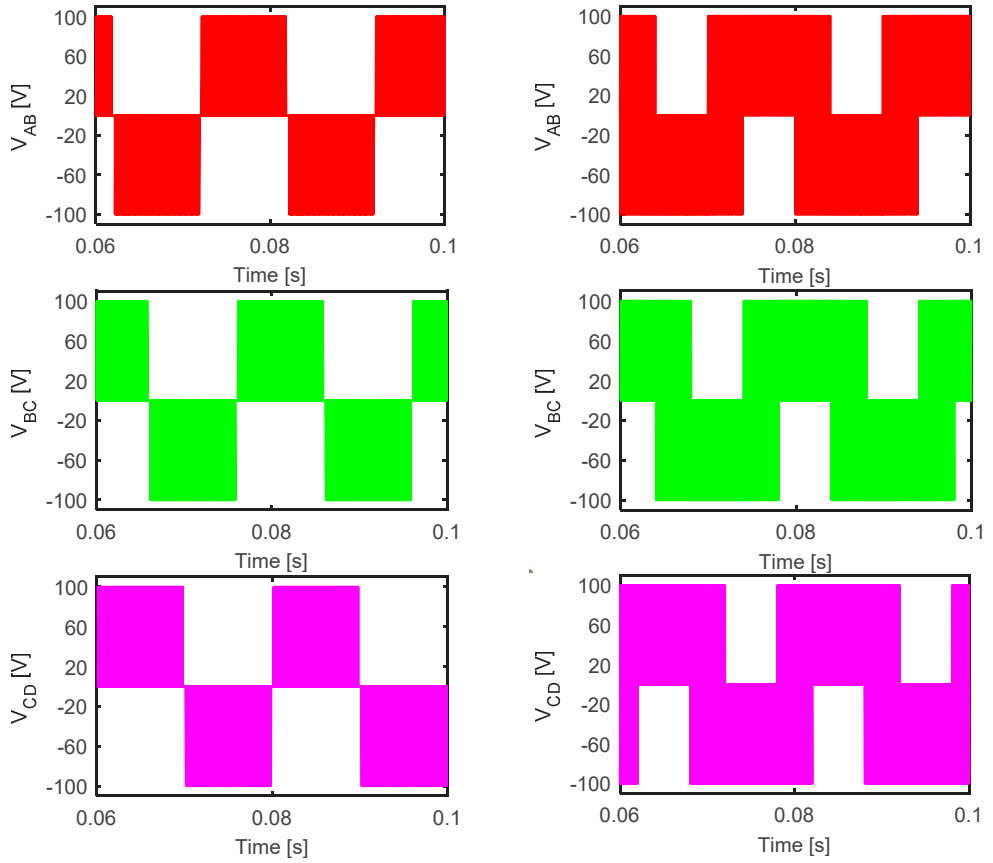


Figure 8. *Cont*.

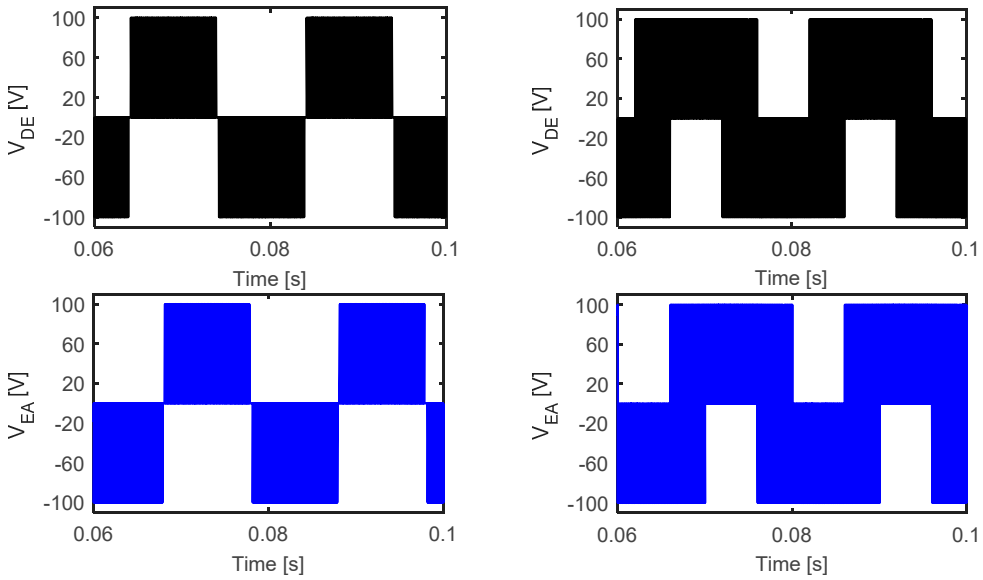


Figure 8. Simulation results of the output line-to-line voltages at unity modulation index and 50 Hz for (**a**) 2L + 2M and (**b**) 6L methods.

Figure 9 indicates the output five-phase currents at the unity modulation index and a 50 Hz output frequency. It has been found that the peak value of the output current in the 6L method is greater than that in the 2L + 2M approach. This means that the 6L method offers better utilization of the DC link compared to the 2L + 2M method. Figure 10 displays the percent THD of the five-phase currents and the 50 Hz output frequency for two modulation indices, e.g., 1 and 0.5. The THD of the five-phase current is comparable between the two SVPWM methods.

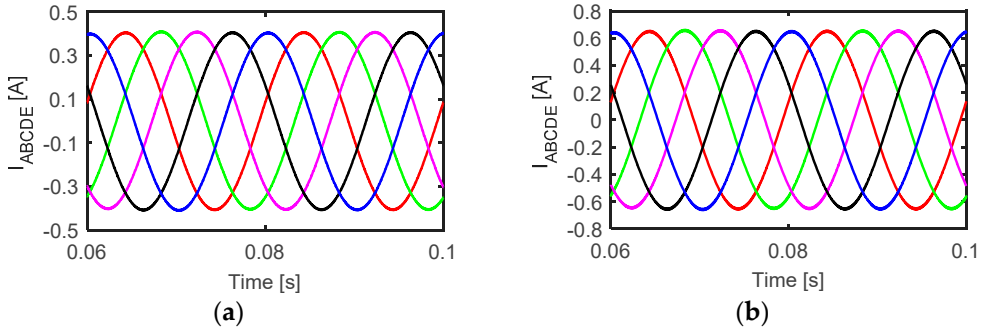
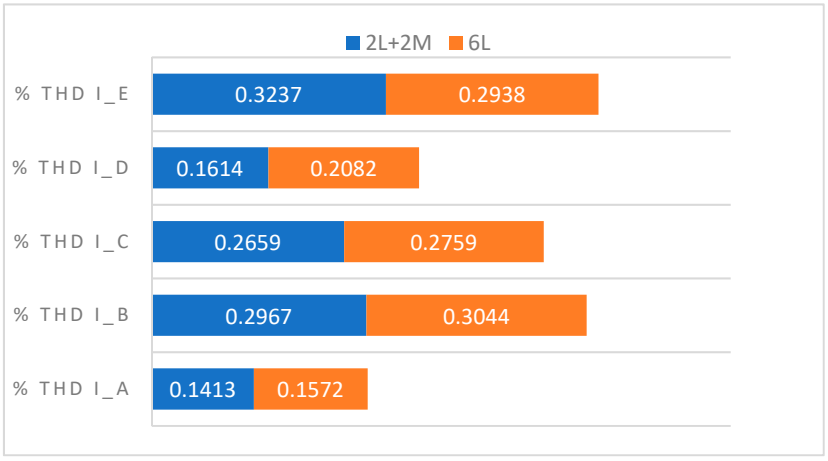
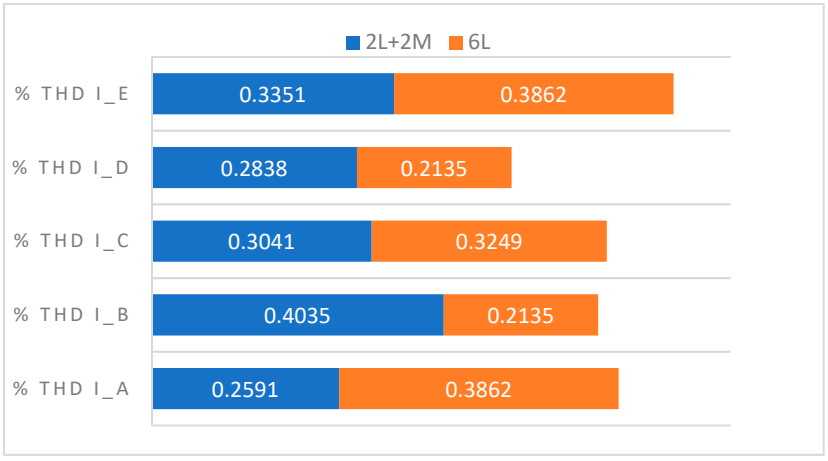


Figure 9. Simulation results of the output phase currents at unity modulation index and 50 Hz for (**a**) 2L + 2M and (**b**) 6L methods.

Figure 11 compares the switching, conduction, and total losses of the inverter for the two SVPWM methods at the unity modulation index and a 50 Hz output frequency. The conduction losses in the 6L method are 78.66% higher than those in the 2L + 2M approach. This is because of the higher current and better DC-link utilization. The switching losses, which are the significant dominant part of the inverter loss, are nearly the same between the two SVPWM methods. The total losses of the 6L method are 3.8% higher than those of the 2L + 2M method.



(**a**)



(**b**)

Figure 10. Simulation results of the THD of the output phase currents for 2L + 2M and 6L methods at 50 Hz and modulation indices of (**a**) 1 and (**b**) 0.5.

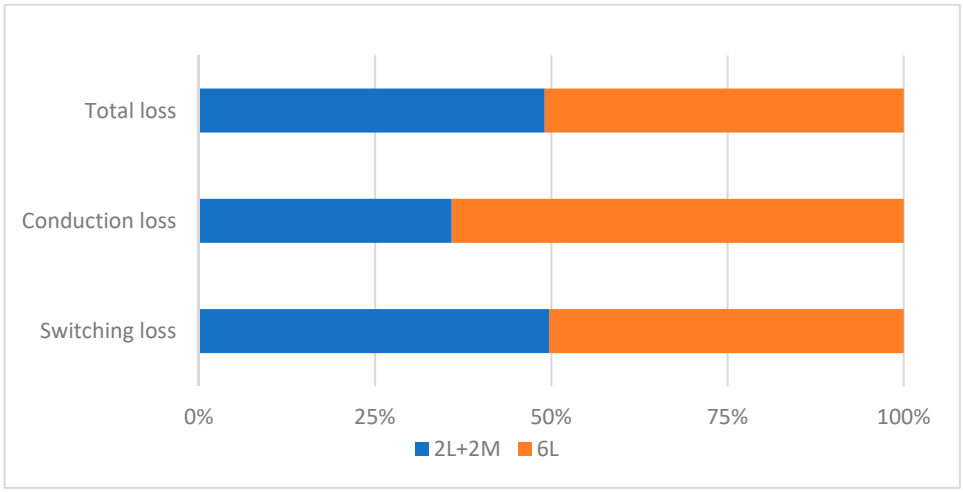


Figure 11. Simulation results of the inverter switching and conduction losses at unity modulation index and 50 Hz.

Figure 12 shows the output five-phase currents at the unity modulation index and a 25 Hz output frequency. As has been found at a 50 Hz output frequency, the peak value of the output current in the 6L approach is greater than that in the 2L + 2M approach at a

25 Hz output frequency. This means that the 6L method offers better utilization of the DC link compared to the 2L + 2M method. Figure 13 shows the output line voltage at the unity modulation index and a 25 Hz output frequency.

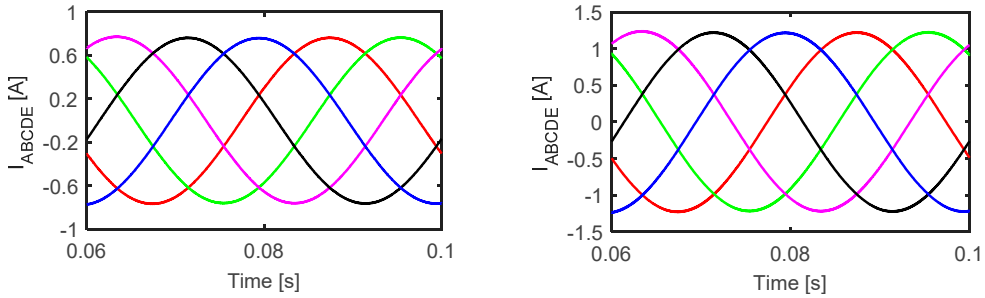


Figure 12. Simulation results of the output phase currents at unity modulation index and 25 Hz for (**a**) 2L + 2M and (**b**) 6L methods.

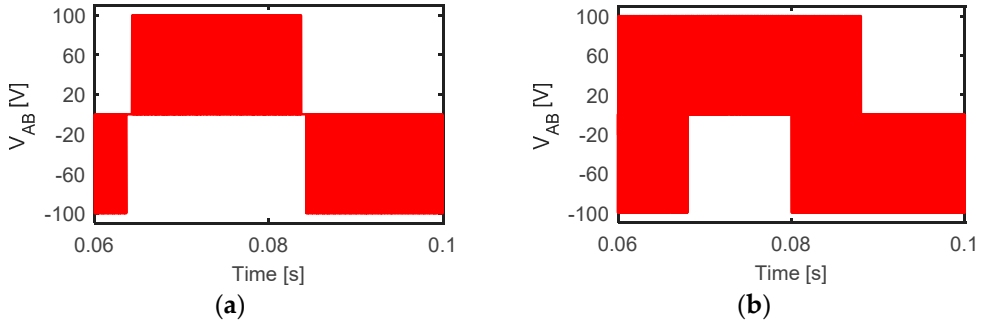


Figure 13. Simulation results of the output line-to-line voltage at unity modulation index and 25 Hz for (**a**) 2L + 2M and (**b**) 6L methods.

4. Comparison of Experimental and Simulation Results

The experimental setup described in Figure 14 has been used to validate the simulation results of the two SVPWM methods. The previous section compared the simulation results of the two PWMs at a high switching frequency (10 kHz) and a lower sampling time step of 1 µs. This is to obtain accurate results for the comparison. However, the conditions of the simulation results introduced in the previous section (a 1 µs solver time step and a 10 kHz switching frequency) cannot be implemented in the experimental results. This is because of the capabilities of the DS pace and the computer processor. Hence, the comparison of the simulation results and the experimental results has been performed in this section at a 1 kHz switching frequency and a 50 µs sampling time. The performance of the two SVPWM methods has been experimentally examined at a 100 V DC supply and an inductive R-L load of 17 ohm, and 0.25 H has been connected to the five-phase inverter.

Figure 15 likens the experimental and the simulation results of the CMV of the two SVPWM methods at the unity modulation index and at a 50 Hz output frequency. The simulated and experimental results are very close, and the 6L method provides an 80% lower peak-to-peak value of the CMV as has been observed in the simulation results.

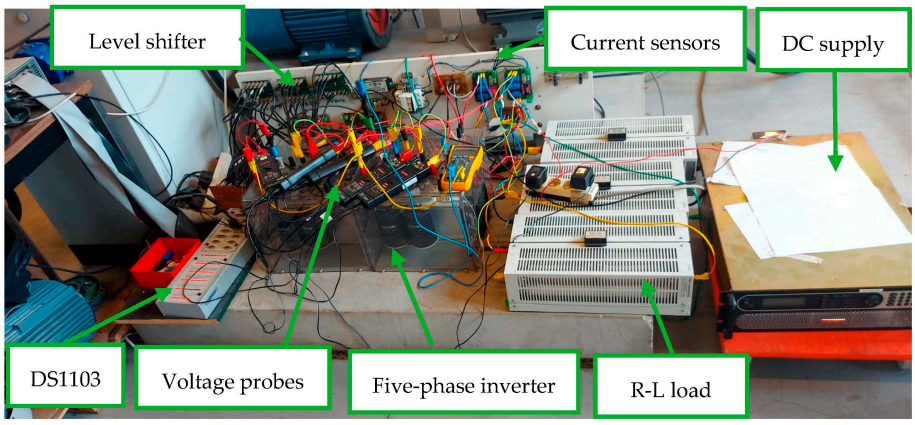


Figure 14. Photo of the experimental setup.

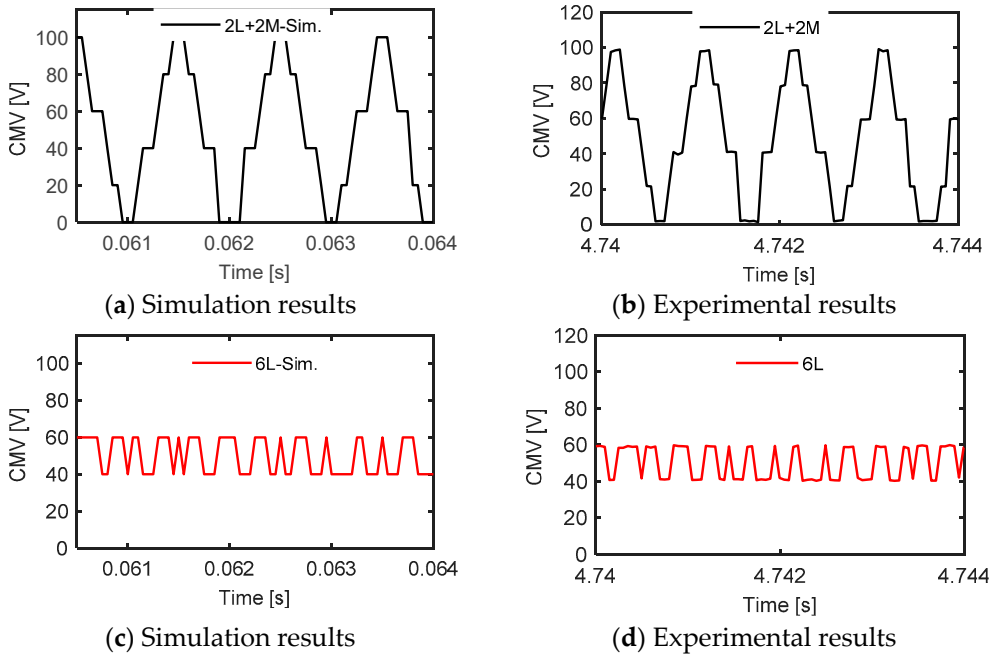
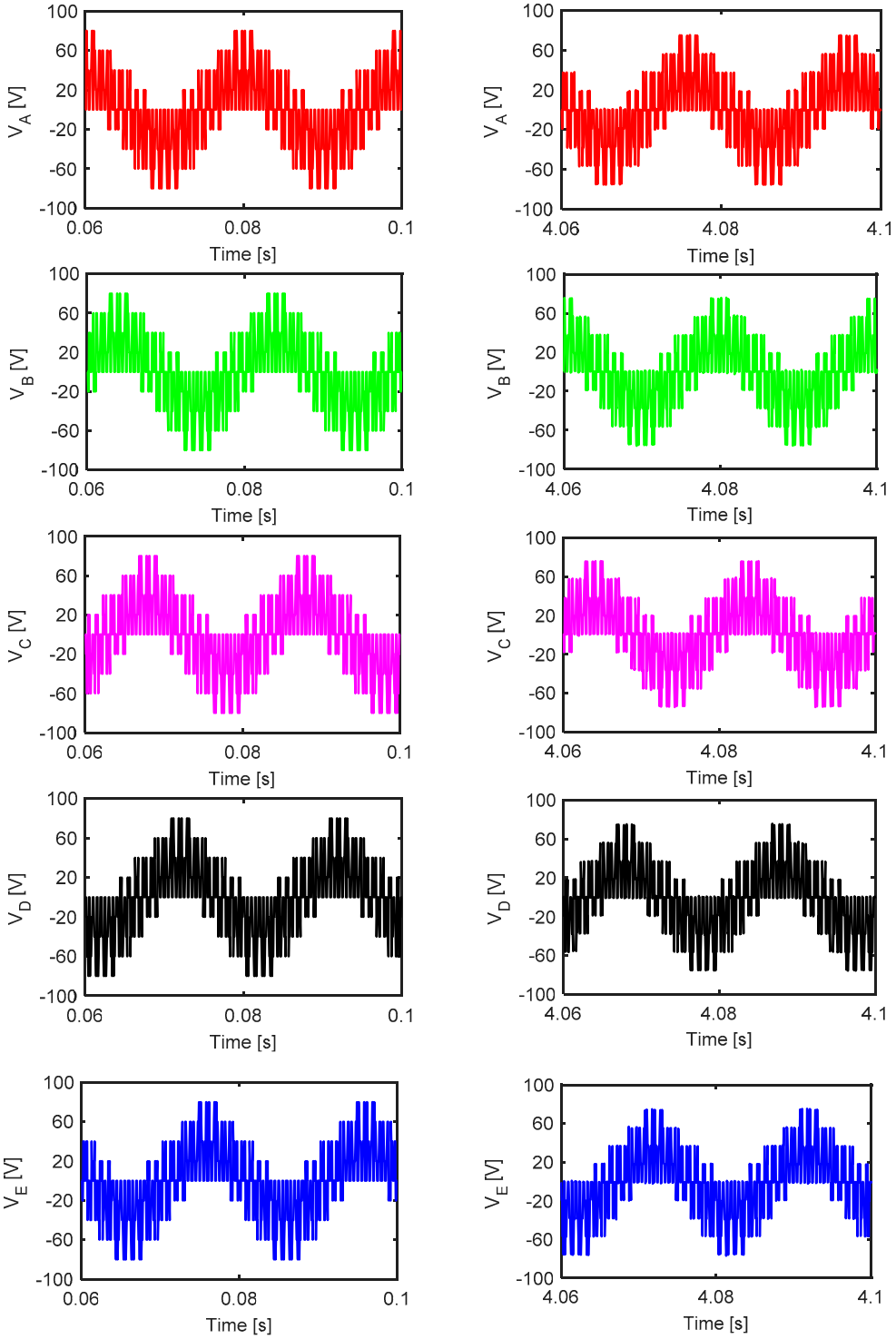


Figure 15. Experimental and simulation results of the CMV at unity modulation index and 50 Hz for (**a**) simulation of 2L + 2M method, (**b**) experiment of 2L + 2M method, (**c**) simulation of 6L method, and (**d**) experiment of 6L method.

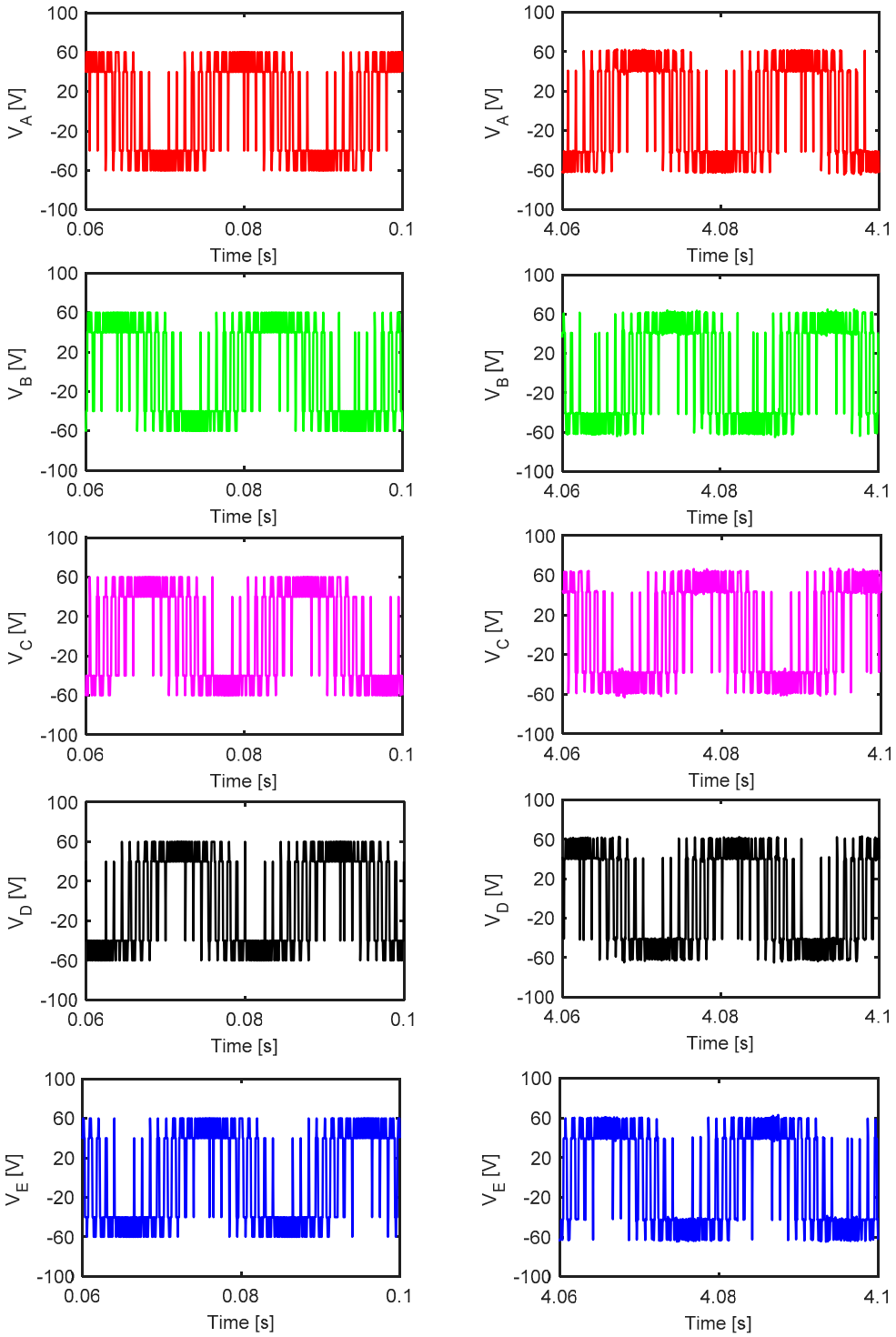
Figure 16 likens the experimental and the simulation results of the phase voltages of the 2L + 2M method at the unity modulation index and a 50 Hz output frequency. There is an acceptable match between the experimental and simulation results. Figure 17 compares the experimental and the simulation results of the phase voltages of the 6L approach at the unity modulation index and a 50 Hz output frequency. There has been an acceptable match between the experimental and simulation results. Figure 18 depicts the experimental and the simulation results of the phase voltages of the 2L + 2M method at the unity modulation index and a 50 Hz output frequency. There has been an acceptable match between the experimental and simulation results. Figure 19 introduces the experimental and the simulation results of the phase voltages of the 6L method at the unity modulation index and a 50 Hz output frequency. There has been an acceptable match between the experimental and simulation results. The voltage quality of the line and phase voltage is not good because the two PWM methods have been applied to the conventional five-phase two-level VSI. To enhance the voltage quality and reduce the THD of the phase and line

voltages, it is recommended to apply a multilevel VSI instead of a conventional two-level VSI as discussed in [46–49].



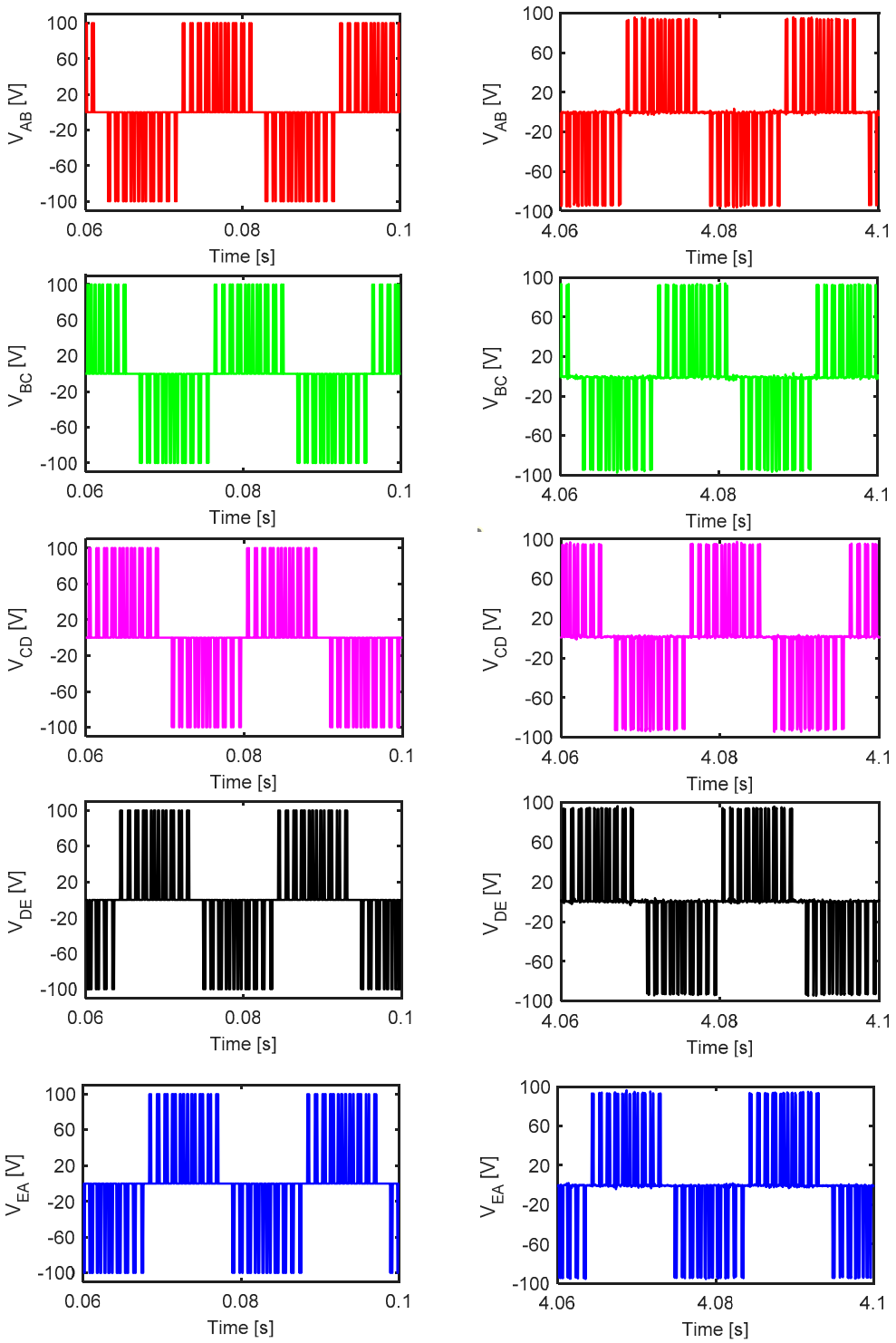
(**a**) Simulation results (**b**) Experimental results

Figure 16. Experimental and simulation results of the output phase voltages at unity modulation index and 50 Hz for 2L + 2M (**a**) simulation and (**b**) experiment.



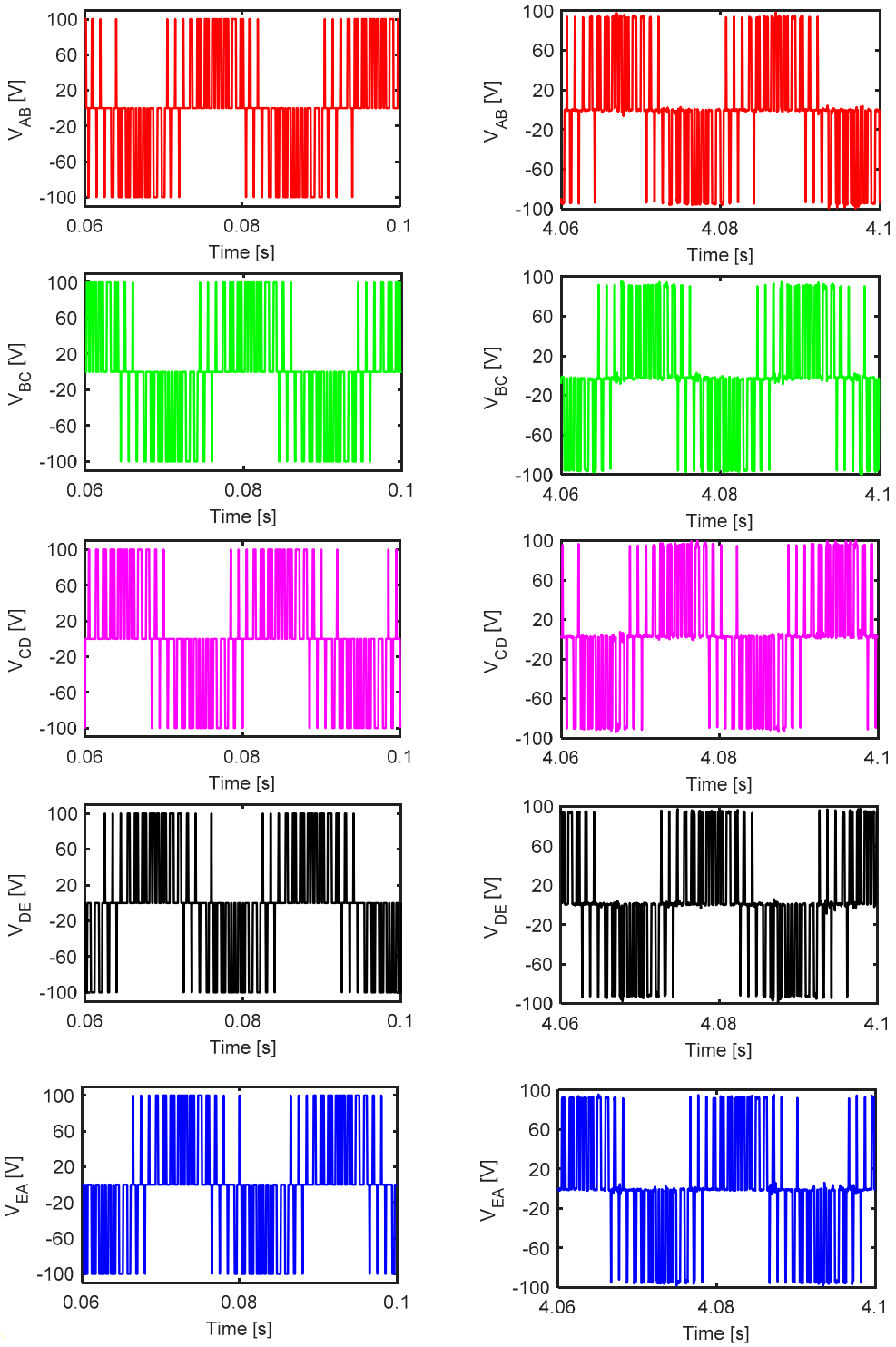
(**a**) Simulation results (**b**) Experimental results

Figure 17. Experimental and simulation results of the output phase voltages at unity modulation index and 50 Hz for 6L (**a**) simulation and (**b**) experiment.



(**a**) Simulation results (**b**) Experimental results

Figure 18. Experimental and simulation results of the output line-to-line voltages at unity modulation index and 50 Hz for 2L + 2M method's (**a**) simulation results and (**b**) experimental results.

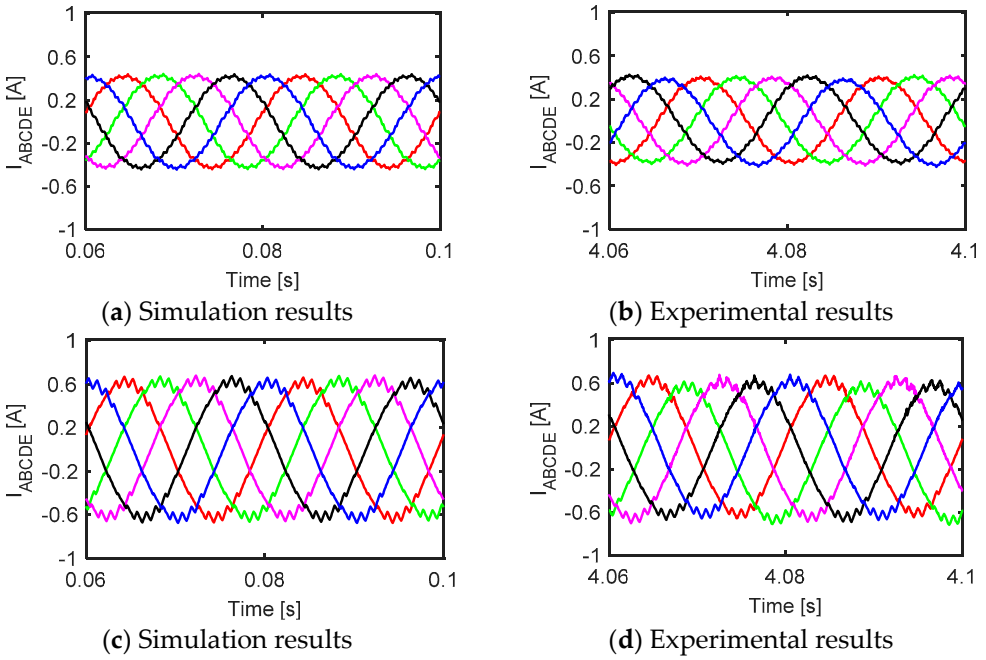


(**a**) Simulation results (**b**) Experimental results

Figure 19. Experimental and simulation results of the output line-to-line voltages at unity modulation index and 50 Hz for 6L method's (**a**) simulation results and (**b**) experimental results.

Figure 20 shows the measured and the simulation results of the five-phase currents of the inverters of the two SVPWM methods at the unity modulation index and a 50 Hz output frequency. It has been found that the experimental results are comparable with the simulation results. Figure 21 shows the experimental and simulation results of the five-phase currents of the two SVPWM methods at the unity modulation index and a 25 Hz output frequency. There is an excellent match between the experimental and simulation

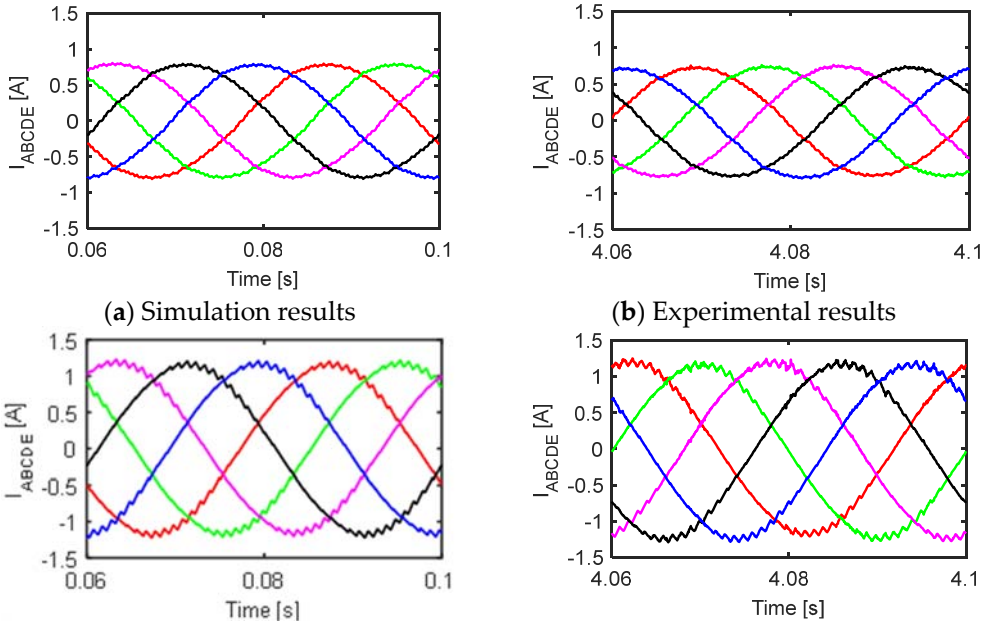
results. The distortion in the currents in the simulation and experimental results in this section (Section 4) is higher compared to the simulation results in the previous section (Section 3) because of the lower switching frequency.



(**a**) Simulation results (**b**) Experimental results

(**c**) Simulation results (**d**) Experimental results

Figure 20. Experimental and simulation results of the output phase currents at unity modulation index and 50 Hz: (**a**) simulation results of 2L + 2M method, (**b**) experimental results of 2L + 2M method, (**c**) simulation results of 6L method, and (**d**) experimental results of 6L method.



(**a**) Simulation results (**b**) Experimental results

(**c**) Simulation results (**d**) Experimental results

Figure 21. Experimental results of the output phase currents at unity modulation index and 25 Hz: (**a**) simulation results of 2L + 2M method, (**b**) experimental results of 2L + 2M method, (**c**) simulation results of 6L method, and (**d**) experimental results of 6L method.

5. Conclusions

This study compares the 2L + 2M and 6L SVPWM algorithms applied to a five-phase two-level voltage source inverter fed by an inductive load. The comparison is based on testing the inverter switching losses, CMV, and THD values under various operation conditions. MATLAB/Simulink creates a system model. In the laboratory, an experimental model is produced to confirm the theoretical analysis. The simulation findings for the system based on the two SVPWM approaches are produced at different modulation indices and output frequencies and are validated by the experimental data. It was found that the peak-to-peak CMV of the 6L approach is 80% lower than that of the 2L + 2M method. Furthermore, 6L SVPWM outperforms 2L + 2M SVPWM in terms of DC-link utilization.

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