electronics

MDPI

Article

A Double-Edge-Triggered Digital LDO with Built-In Adaptive VCO Clock for Fast Transient Response and Low Power Consumption

Xin Xin, Dongdong Wei and Xingyuan Tong *

School of Electronic Engineering, Xi'an University of Posts & Telecommunications, Xi'an 710121, China; xinxin@xupt.edu.cn (X.X.); weidongdong@stu.xupt.edu.cn (D.W.)
* Correspondence: tongxingyuan@xupt.edu.cn

Abstract: A double-edge-triggered digital low dropout regulator (DLDO) is proposed with a built-in adaptive voltage-controlled oscillator (VCO) clock (AVC) for a system-on-chip (SoC) application. To achieve a fast transient response, the main comparator generates the comparison result at the rising edge of the AVC, and this result is sampled by the coarse or fine bidirectional shifter register at the falling edge of the AVC. Furthermore, the clock frequency can be boosted from 8 MHz at the steady state to 50 MHz by the AVC when the output current suffers from a sudden change, and it can also be adjusted in real-time according to the output voltage, which avoids the oscillation phenomenon and decreases the power consumption during the recovery process. To further lower the power consumption, the self-clock comparator replaces the conventional static comparator in the transient detector. The post-simulation results show that the proposed DLDO consumes a quiescent current of 95.13 µA in the steady state, and drives a maximum load current of 25 mA at the supply power of 0.6 V with an active area of 0.053-mm^2 in a 180 nm CMOS process. When the load current jumps from 0.5 mA to 25 mA at the edge of 100 ps, the undershoot voltage and overshoot voltage are only 335 mV with the recovery time of 2.7 µs and 47.6 mV with the recovery time of 2.1 µs at the total on-chip capacitor of 50 pF, respectively, resulting in two competitive figures of merits (FoMs) than the previous works.

Keywords: DLDO; adaptive voltage-controlled oscillator clock; double-edge trigger; fast transient response; low power consumption

Citation: Xin, X.; Wei, D.; Tong, X. A Double-Edge-Triggered Digital LDO with Built-In Adaptive VCO Clock for Fast Transient Response and Low Power Consumption. *Electronics* **2023**, *12*, 4100. https://doi.org/10.3390/electronics12194100

Academic Editors: Andrea Ballo, Gaetano Palumbo and Orazio Aiello

Received: 19 August 2023
Revised: 21 September 2023
Accepted: 28 September 2023
Published: 29 September 2023

1. Introduction

In Internet of Things (IoT) and system-on-chip (SoC) application scenarios, energy-efficient fine-grained power management systems are indispensable for self-power wireless sensors due to the limited power capability of the supply and energy harvester. At high supply voltages (e.g., 1.2 V and above), analog low-dropout regulators (LDOs) can regulate a constant voltage for analog and RF modules due to their excellent noise performance and high PSRR characteristics, which maximize the performance and energy efficiency [1,2]. With CMOS process scaling, the intrinsic gain of the transistors is smaller, leading to an analog circuit accuracy reduction. Although the multistage operational transconductance amplifier improves the gain, it also introduces stability issues and considerable power consumption. In addition, in the near-threshold range (62 mV to 0.6 V), the analog LDO (ALDO) also fails to show excellent energy efficiency. Recently, the digital LDO (DLDO) features low voltage operation, process scalability, and other benefits associated with digital-oriented design, which has received the attention of many researchers [3].

Compared with the DLDO with the power PMOS transistors, the DLDO with the power NMOS transistor can provide additional current through their intrinsic loop (V_{gs}) to optimize the undershoot voltage and the response time during the output voltage recovery process. Nevertheless, this type of DLDO requires a charge pump circuit and the level

shifter to ensure that the gate voltage of the power NMOS transistor is higher than the supply voltage [4]. This leads to extra area and power consumption in the level shifter, charge pump, and capacitance. The classic digital LDOs improve the clock frequency of the dynamic comparator and the bidirectional shift register (S/R) for a better transient response, but increase the static power I_q in the steady state [5]. Therefore, it is crucial to enhance the transient response while simultaneously reducing the power consumption.

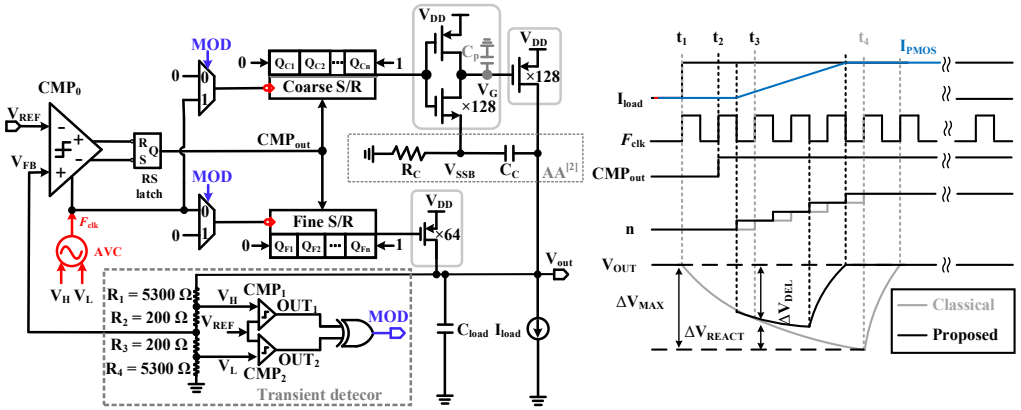
There are various approaches to enhance the dynamic response of digital LDOs. One method is to use asynchronous clocking [6] or the self-clock technique [7] instead of the synchronous clock as the trigger method of the comparator and the S/R. However, asynchronous clocking can make the logic design more intricate and susceptible to voltage and temperature variations, which compromises the robustness of the system. Another strategy involves modifying the structure of the power PMOS transistor array, for instance, a binary-weighted PMOS capacitor array. Because the most significant bit PMOS transistor always offers the maximum current whether large or small jumps occur in the output voltage, this leads to the oscillation phenomenon and a long recovery time when a small output voltage change occurs [8]. Dual-loop regulation is an effective way to avoid the oscillation phenomenon by utilizing an extra transient detector (TD) to check the output changes. The coarse loop is used to quicken the output level recovery when the output exceeds the detection boundaries, and when the threshold level is not surpassed, the PMOS transistor in the fine loop is switched at each clock edge for high accuracy and current efficiency. However, the continuous-time (CT) comparator in the TD can increase the static power consumption of the digital LDO [9]. The analog-assisted (AA) technique uses a coupling capacitor C_C with a resistance R_1 that forms a high-pass filter to compensate the transient current to the gate of the PMOS transistor, which is a promising technology as there is no additional static power consumption [10]. However, the performance is degraded in the light-to-heavy load transient case because the transconductance of the PMOS transistors is too small to fully compensate for the load transient current. Fortunately, the light load current can reach about several hundred μA. The only fly in the ointment is that the transient response can be boosted at the expense of area (C_C = 120 pF). Finally, the fifth technique is adaptive clocking, which selects the clock frequency of the comparator and the S/R. However, the glitch during the fast/slow clock switching process may affect the performance of the circuit [11].

To address the above-mentioned issues, the comparator and bidirectional S/R were controlled with different trigger methods without extra circuit assistance and robustness issues in our work. Specifically, the comparator obtains the quantization result at the rising edge, while the bidirectional S/R then samples and shifts this quantization result at the falling edge. As a result, the transient response can be enhanced because the PMOS array can adjust the output current in the current cycle. In other words, this trigger technology can relax the clock frequency at the steady state by 2×. In addition, a built-in adaptive voltage-controlled oscillator (VCO) clock (AVC) is proposed to reduce both the static and transient power consumption by adjusting the clock frequency of the comparator and bidirectional S/R in real-time according to the output voltage. When the output current change jumps from 0.5 mA to 25 mA within 100 ps, the clock frequency of the AVC is boosted from 8 MHz in the steady state to 50 MHz, which lowers the undershoot voltage and the recovery time in the undershoot case and overshoot case to 335 mV, 2.7 μs, and 2.1 μs. To boost the current efficiency, the self-clock comparator in the transient detector is employed. The post-simulation results show that the proposed DLDO can provide a load current from 0.5 mA to 25 mA and achieve a peak current efficiency of 99.6% at the supply voltage of 0.6 V with an active area of 0.053 mm^2 in a standard 0.18 μm CMOS process, leading to the FoM_1 and FoM_2 of 2.654 ps and 0.13 pF, respectively.

The rest of this paper is organized as follows. Section 2 describes the architecture and working principle of the proposed DLDO. Section 3 demonstrates the circuit implementations and design considerations of each circuit module. Section 4 presents the simulation results and comparisons. Section 5 concludes this work.

2. Architecture and Working Principle

Figure 1a presents the overall architecture of the proposed DLDO with an AA loop from Ref. [4]. The proposed DLDO consists of the main comparator CMP_0 with an RS latch, two selectors controlled by the MOD signal, the coarse and fine bidirectional S/R, the coarse and fine power PMOS transistor arrays, the AVC, and the TD.



(**a**) (**b**)

Figure 1. (**a**) Block diagram of the proposed DLDO. (**b**) Transient response comparison between the classical and proposed DLDO.

To trade off the power and transient response, the PMOS array is divided by 128 coarse PMOS transistors with a size of 100 µm/0.18 µm and 64 fine PMOS transistors with a size of 10 µm/0.18 µm. The total size of the coarse PMOS array is mainly determined by the maximum load current, while the size of the unit for the fine PMOS transistor is decided by the minimum load current. Under the same maximum output current capability, as the bits of the coarse PMOS array increases, for example, 256 bits, the output current of every unit of the coarse PMOS transistor is halved, which not only increases the area of the coarse bidirectional SR, but also prolongs the recovery time. In contrast, with the decrease in the bit of the coarse PMOS array such as 64 bits, the transient current provided by every coarse PMOS transistor is increased by more than two times at a large undershoot in the output voltage since the source to drain voltage (V_{sd}) of every coarse PMOS transistor increases from 50 mV in the steady state to several hundred mV in the transient response. The simulation shows that the output current of every coarse PMOS transistor with a size of 400 µm/0.18 µm is 924 µA and 1.8 mA at the V_{sd} of 50 mV and 300 mV, which is much higher than the total current (828 µA) provided by the fine PMOS array. However, by doing this, the output suffers from the overshoot voltage after the undershoot voltage, which still prolongs the recovery time. More significantly, the proposed DLDO cannot switch from the coarse loop to the fine loop during the output recovery process. Furthermore, the RS latch can protect or temporarily store the main comparator result during the comparator reset phase.

It can be seen from Figure 1 that the gate voltage of the power PMOS transistors is determined by the coarse/fine loop bidirectional S/R and the AA loop. When the output current increases suddenly, the output voltage of the proposed DLDO decreases sharply, and the output voltage change is assumed as ΔV_{out}. The AA loop has a faster response than the main loop of the DLDO, and thus the gate voltage can reduce $C_C \cdot \Delta V_{out}/(C_C + C_P)$ immediately to lower the undershoot voltage, where C_P is the parasitic gate capacitor of the power PMOS transistors. In the proposed work, the total size of the fine PMOS array is only 1/20 of that of the coarse PMOS array. Therefore, the undershoot voltage dominantly relies on the coarse PMOS array. Furthermore, even if the AA loop is employed in the fine PMOS array, the undershoot voltage cannot be optimized obviously because the parasitic capacitance of the fine PMOS array is contained and the gate voltage change of all PMOS transistors is reduced under the identical C_C. Therefore, the AA loop is only used for the

coarse PMOS array by trading off the undershoot voltage and gate voltage change of the power PMOS transistors.

Figure 1b shows the transient response comparison between the classical DLDO [5] and the proposed DLDO. When the load current (I_{load}) steps up at t_1 within a rapid edge time, the CMP_0 and the SR latch hardly provide a correct comparison result (CMP_{out}) due to the limited comparison time ($1/(2{\cdot}F_{clk})$). At t_2, the CMP_{out} turns to the high level at the rising edge of F_{clk}. Now, the coarse S/R is selected by the MOD because the V_{OUT} exceeds the threshold boundary, unlike the S/R of the classical DLDO [5] and the conventional coarse-fine loop DLDO [9], which is triggered in the next cycle t_3. The S/R in the proposed DLDO is triggered at the falling edge to turn on the power PMOS transistor to supplement the output current to reduce the ΔV_{DEL} until the I_{PMOS} is equal to I_{load}. In other words, the transient response can be enhanced by triggering the comparator CMP_0 and the S/R at the rising and falling edge, respectively, without the clock frequency increment and any hardware cost.

Unlike the conventional TD [12], the self-clocked comparators CMP_1 and CMP_2 replace two CT comparators to lower the power consumption, and the operation frequency of these two comparators is enhanced to 58 MHz to diminish the comparator's delay effect on the DLDO at a supply voltage of 0.6 V. The four resistors R_1, R_2, R_3, and R_4 in the TD have resistance values of 5300 Ω, 200 Ω, 200 Ω, and 5300 Ω, respectively. Therefore, V_H, V_{FB}, and V_L can be calculated as follows:

$$\begin{cases} V_H = \frac{R_2+R_3+R_4}{R_1+R_2+R_3+R_4} \cdot V_{out} \\ V_{FB} = \frac{R_3+R_4}{R_1+R_2+R_3+R_4} \cdot V_{out} \\ V_L = \frac{R_4}{R_1+R_2+R_3+R_4} \cdot V_{out} \end{cases} \quad (1)$$

According to Equation (1), even if there is a resistance mismatch, V_H must be larger than V_{REF}, while V_L must be smaller than V_{REF}. If the TD range is too small (2 mV), the proposed DLDO will jump from the fine loop to the coarse loop with a slight change in the output voltage. As a result, the output voltage will oscillate during output recovery due to multiple overshoots and undershoots, resulting in a long recovery time. If the TD range is too large (200 mV), it is difficult to switch the proposed DLDO from the fine loop to the coarse loop with a large jump in the output. As a consequence, this situation also leads to a long recovery time since the current provided by each PMOS transistor in the fine loop is small. In our design, the TD range was designed to be 20 mV by compromising the recovery time in the case of the large jump and the small jump in the output voltage. In addition, the V_H and V_L were designed for 285 mV and 265 mV, respectively, by the series resistor ladder instead of the voltage reference for the dynamic voltage scaling. The voltage reference operating in the subthreshold region or the 2T solution in [13] can dramatically reduce the static power consumption. However, the series resistor ladder was used in our work for two reasons. Firstly, V_H, V_L, and V_{FB} vary with the supply voltage to achieve a fixed V_{drop}. The voltage reference (2T solution) can only provide a fixed level under different PVT conditions, which shrinks the supply voltage range. Secondly, we assumed that a voltage reference with the value of 285 mV was designed with the nanowatt level power consumption. An external operational amplifier is still required to generate a voltage reference value of 265 mV, resulting in additional power consumption and increased circuit complexity. When the load current changes sharply, the overshoot voltage or undershoot voltage exceeds the threshold voltage V_H or V_L, and then the MOD outputs 1. The AVC generates a high-frequency clock. At the same time, the comparator and coarse bidirectional S/R, controlled by this high-frequency clock, can quickly recover the output voltage through a coarse PMOS array until V_{FB} is recovered between the V_H and V_L levels. More importantly, because the clock frequency (F_{clk}) is controlled by the V_H and V_L associated with the output of the DLDO (V_{out}), it will decrease with the decrease in the undershoot voltage. Therefore, the oscillation at V_{out} can effectively be avoided during the signal recovery process. When the circuit output is at a steady state or when the overshoot voltage or undershoot voltage is small, MOD outputs 0, and the AVC produces a corresponding low-frequency clock to control the CMP_0 and the

fine-loop bidirectional SR for the output voltage recovery. Meanwhile, the coarse bidirectional SR is idle to lower the power consumption.

3. Design Results and Comparison

3.1. Dynamic Comparator Design

The self-clock comparators CMP_1 and CMP_2 in the TD shown in Figure 2 consist of a double-tail comparator (DTC), an XOR, and an SR latch. Assuming that the initial outputs Out_p and Out_n are at the low level at the reset state, the CLK becomes the high level after the delay of the XOR (t_{XOR}), and then the comparator starts to compare the feedback signals (V_H and V_L) and V_{REF} to generate the new results Out_p and Out_n after the delay of the comparator (t_{cmp}). By performing an XOR for the new results Out_p and Out_n, the CLK becomes the low level after the t_{NOR}, and the comparator can also be reset after the reset time of the comparator. Hence, the operation frequency of the self-clock comparator can be written as:

$$f_{clk} = 1/\left(2 \cdot t_{XOR} + t_{reset} + t_{cmp}\right) \tag{2}$$

Compared to the strong-arm comparator, the DTC is made up of the preamplifier stage (preamp) and the second latch stage, and the kickback noise can be isolated by the preamplifier stage in the low-voltage operation. The main comparator CMP_0 is controlled by the AVC to enhance the transient response, while the comparators CMP_1 and CMP_2 are controlled by the clocks CLK_1 and CLK_2 separately for the output voltage detection in real-time. To analyze the delay of the comparator (t_{cmp}), the operation process of the DTC is divided into three phases: the reset phase, the integrated phase, and the latch phase. The delay in the integrated phase (t_0) and the latch phase (t_{latch}) of the comparator is the dominant factor. t_0 represents the charging process to the load capacitor (C_{out}) until the first n-channel transistor (NM_3/NM_4) turns on. t_{latch} stands for the latching delay of two cross-coupled inverters (PM_3, PM_4, NM_3, and NM_4 transistors), which is from an initial output voltage difference V_0 (The final state of the integral phase) to a voltage swing of $V_{outp} - V_{outn} = V_{DD}/2$. The total delay ($t_{cmp}$) of this comparator can be evaluated as follows [14]:

$$\begin{aligned} t_{cmp} &= t_0 + t_{latch} = 2\frac{V_{thnm5,6} \cdot C_{out}}{I_{tail2}} + \frac{C_{out}}{g_{m,inv}} \cdot ln\left(\frac{V_{DD}/2}{\Delta V_0}\right) \\ &= 2\frac{V_{thnm5,6} \cdot C_{out}}{I_{tail2}} + \frac{C_{out}}{g_{m,inv}} \cdot ln\left(\frac{V_{DD} \cdot I_{tail2}^2 \cdot C_X}{8 \cdot g_{mnm1,2} \cdot g_{mnm5,6} \cdot C_{out} \cdot V_{thnm5,6}^2 \cdot \Delta V_{in}}\right) \end{aligned} \tag{3}$$

where C_X is the output parasitic capacitor at the nodes f_n and f_p, $g_{mnm1,2}$, $g_{mnm5,6}$, and $g_{m,inv}$ are the transconductance of the NM_1, NM_2, NM_5, and NM_6 transistors, and the two cross-coupled inverters, I_{tail2} and $V_{thnm5,6}$ stand for the tail current of the M_{tail2} transistor at the latch phase and the threshold voltage of the NM_5 and NM_6 transistors. It can be seen from Formula (3) that the delay of the comparator can be affected by the input level difference and the process corners.

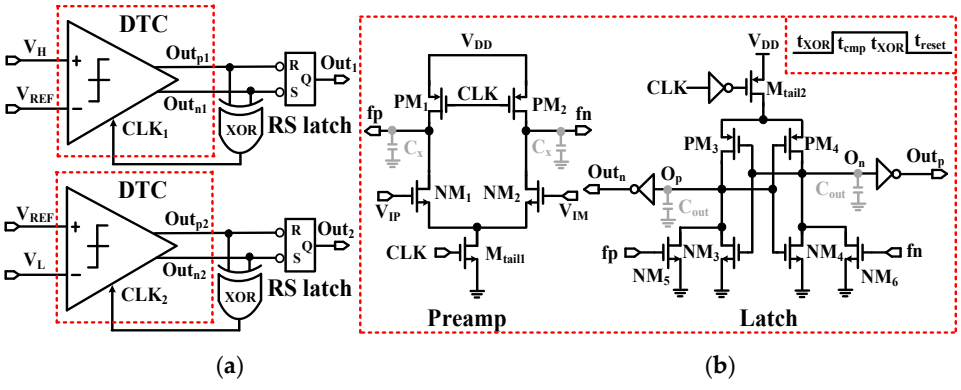


Figure 2. (**a**) Schematic of the comparator with the self-clocked technology. (**b**) Schematic of the double-tail dynamic comparator.

The effect of the offset voltage of the comparator on the proposed DLDO can be equivalent to the effect on the accuracy of the voltage reference (V_{REF}). The offset voltage can be calculated as follows:

$$V_{os} = V_{os,\ preamp} + \frac{1}{A_{preamp}} V_{os,\ latch} \tag{4}$$

where $V_{os,\ preamp}$ and $V_{os,\ latch}$ are the offset of the preamplifier stage and the second latch stage. A_{preamp} represents the gain of the preamplifier stage. Since the $V_{os,\ latch}$ is damped by the preamplifier stage, the offset voltage of the dynamic comparator is dominated by that of the preamplifier stage and the $V_{os,\ preamp}$ can be expressed as follows [15]:

$$V_{os,preamp} = \Delta V_{thNM1,2} + \frac{(V_{gs} - V_{th})_{NM1,2}}{2} \cdot \left(\frac{\Delta S_{NM1,2}}{S_{NM1,2}} + \frac{\Delta R_{NM1,2}}{R_{NM1,2}} \right) \tag{5}$$

where $\Delta V_{thNM1,2}$, $\Delta S_{NM1,2}$, and $\Delta R_{NM1,2}$ indicate the threshold voltage mismatch, the parameter ($\mu C_{OX} W/L$) mismatch of the NM_1 and NM_2 transistors, and the equivalent load mismatch at the nodes f_p and fn, respectively. $(V_{gs}\text{-}V_{th})_{NM1,2}$ stands for the overdrive voltage of the NM_1 and NM_2 transistors. Therefore, the W/L of the input transistor NM_1 and NM_2 needs to be increased to suppress the offset voltage of the DTC. When the positive side of the comparator is increased linearly from 265 mV to 285 mV in 20 µs, and the negative side of the comparator is fixed at 275 mV, Figure 3 shows the 500-run Monte Carlo simulation of the offset voltage at the clock frequency of 8 MHz and 50 MHz. The type of Monte Carlo simulation is "process and mismatch". The mean and standard deviation of the comparator's offset voltage are independent of the clock frequency and are about 700 µV, which can match the theoretical calculation.

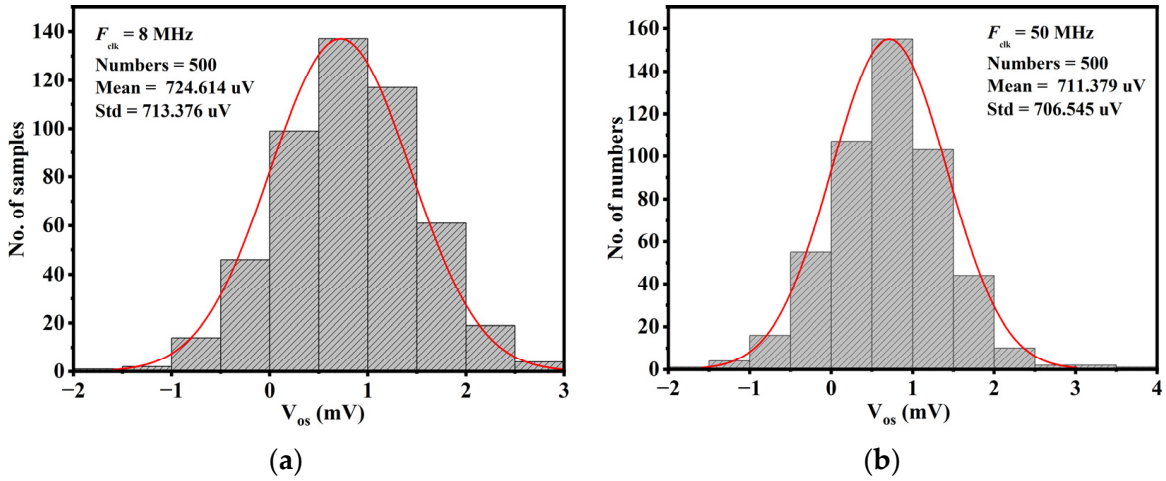


Figure 3. The 500-run Monte Carlo simulation about the offset voltage. (**a**) F_{clk} = 8 MHz; (**b**) F_{clk} = 50 MHz.

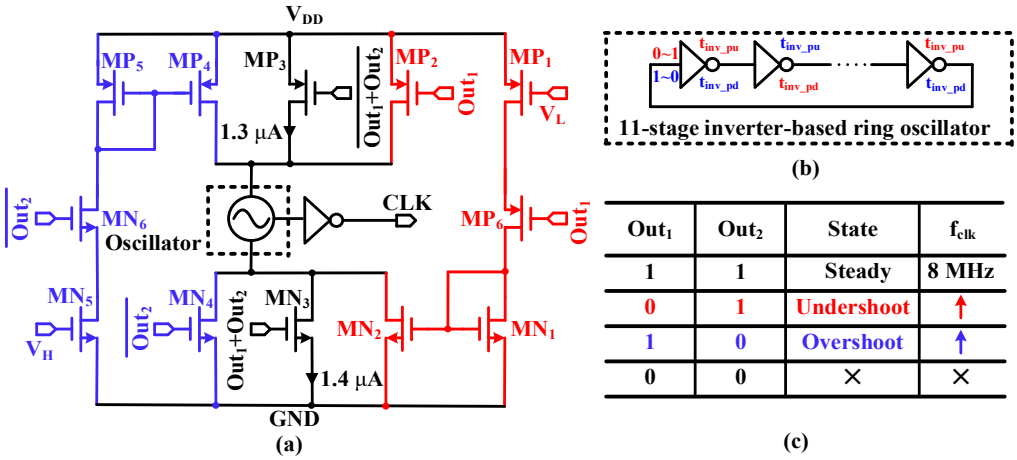
3.2. Built-In Adaptive VCO Clock

Figure 4a presents the schematic of the AVC, which is composed of the 11-stage inverter-based ring oscillator in Figure 4b, the pull-down controlled transistors (MN_1-MN_6), and the pull-up-controlled transistor (MP_1-MP_6). The working state of the AVC is decided by the TD. When the proposed DLDO is in the steady state ($V_H > V_{REF} > V_L$), the outputs Out_1 and Out_2 of the self-clocked comparator CMP_1 and CMP_2 are high level, and the oscillation frequency of the AVC is determined by the pull-up current of 1.3 µA from the MP_3 transistor and the pull-down current of 1.4 µA from the MN_3 transistor. If the pull-up current is equal to the pull-down current in the steady state, the AVC will generate a clock with a duty cycle of 50%. Because the reset time (T_{res}) at the low level of the main comparator (CMP_0) is independent of the input signal amplitude, it can be less than the

quantization time (T_{quan}) at the high level to improve the operating frequency of the CMP_0. That is to say, it is not necessary to design the clock duty ratio of 50% under the steady state. Because the pull-up current is less than the pull-down current, the pull-up time is greater than the pull-down time for every inverter in Figure 4b. The T_{res} at the low level and the T_{quan} at the high level can be calculated as follows:

$$\begin{cases} T_{res} = 6 \cdot t_{inv\_pu} + 5 \cdot t_{inv\_pd} \\ T_{quan} = 5 \cdot t_{inv\_pu} + 6 \cdot t_{inv\_pd} \end{cases} \quad (6)$$

It can be seen from Formula (6) that the reset time of the comparator is just less than the quantization time of the comparator.



Out_1	Out_2	State	f_{clk}
1	1	Steady	8 MHz
0	1	Undershoot	↑
1	0	Overshoot	↑
0	0	×	×

Figure 4. (**a**) Schematic of the AVC. (**b**) Schematic of the oscillator. (**c**) Working state.

This oscillation frequency of the AVC can be calculated as 8.13 MHz, which can match the simulation result (8 MHz). When the output (V_{out}) of the proposed DLDO encounters a large undershoot in the transient response ($V_H < V_{REF}$), the Out_1 turns to the low level and the Out_2 remains at the high level. The pull-down current from the current mirror (the MN_1 and MN_2 transistors) and the extra pull-up current from the MP_2 transistor can boost the oscillation frequency of the AVC. Meanwhile, the pull-down current is controlled by the V_L, and the larger the undershoot voltage, the higher the I_{MN2} current and oscillation frequency of the AVC. Similarly, when the overcharge voltage occurs ($V_L > V_{REF}$), the oscillation frequency of the AVC is also enhanced by the pull-up current from the MP_4 transistor and the extra pull-down current from the MN_4 transistor. Figure 4c summarizes the working state and the oscillation frequency of the AVC in different conditions of the DLDO. Figure 5a shows that the clock frequency of the AVC varies with the V_L and V_H. F_{clk} is only 8 MHz at the steady state; the F_{clk} can be boosted up to about 50 MHz at the transient response at a 0.6 V supply through the PSS simulation.

The clock frequency of the AVC at different temperatures and corners at the steady state and transient state is presented in Table 1. The slowest frequency and fastest clock frequency occur at the −40 °C@ss corner and 85 °C@ff corner. Furthermore, the clock frequency ratio between the steady state and the transient state is almost 1:6.25 at any process corner and temperature. Figure 5b shows the 500-run Monte Carlo simulation of the clock frequency at the steady state and transient state. The mean value and standard deviation of the clock frequency at the steady state are 8.21 MHz and 2.48 MHz, respectively, while those of the clock frequency at the undershoot case and overshoot case are nearly 52 MHz and 11.61 MHz, and 50.82 MHz and 13.12 MHz, respectively.

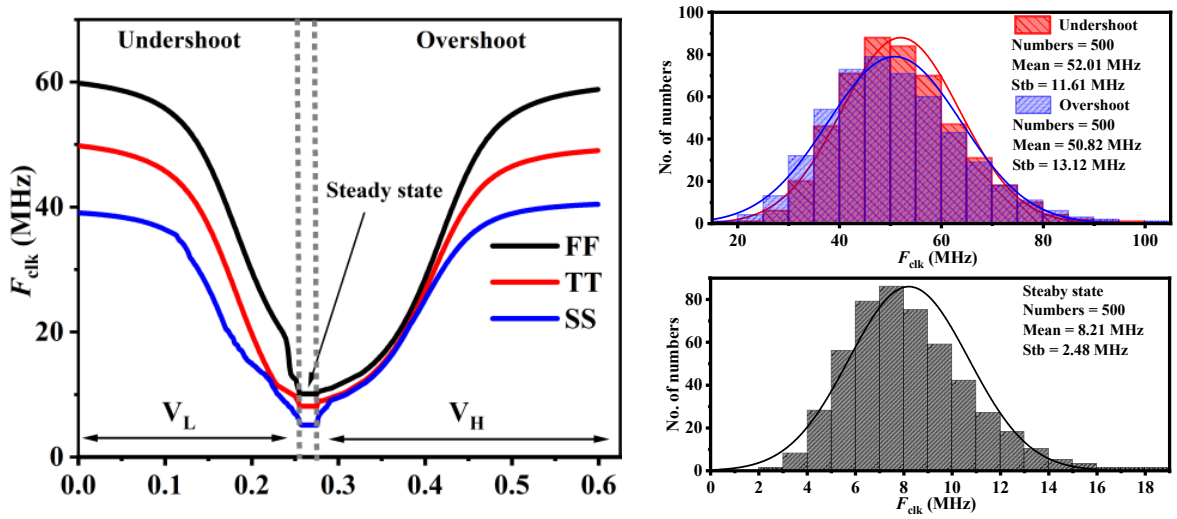


Figure 5. The clock frequency (F_{clk}) of the AVC. (**a**) Different process corners. (**b**) The 500-run Monte Carlo simulation.

Table 1. F_{clk} at different temperature and process corners.

Temp [°C]		**−40**			**27**			**85**	
Corner	**FF**	**TT**	**SS**	**FF**	**TT**	**SS**	**FF**	**TT**	**SS**
Steady state @ F_{clk} [MHz]	7.86	5.97	4.12	10.05	8.01	5.10	13.13	10.96	7.15
Undershoot @ F_{clk} [MHz]	52.31	40.28	29.97	60.11	51.23	39.58	70.23	61.34	49.22
Overshoot @ F_{clk} [MHz]	51.03	39.24	28.92	57.88	49.54	38.37	69.58	60.77	48.64

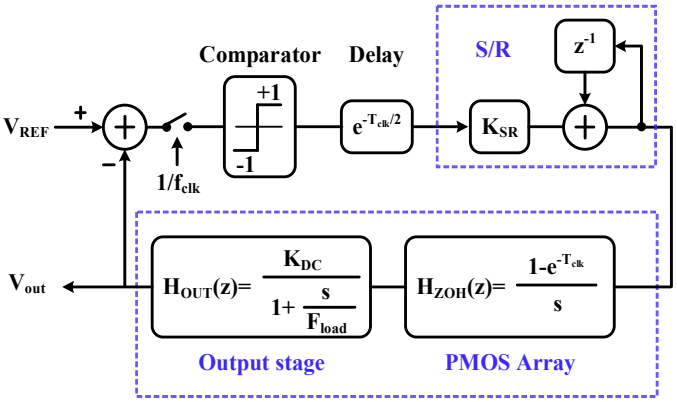
3.3. Loop Stability Analysis

Following a similar analysis presented in [4,10], the small signal model and the zero-pole distribution are demonstrated in Figure 6a and 6b, respectively. The bidirectional S/R acts as an ideal discrete-time integrator with a dc pole (p_0) with the gain of K_{SR}. The PMOS array outputs a constant current and provides a gain of K_{DC} until the next negative clock edge, thus a zero-order hold (ZOH) is placed in front of the output stage, which is modeled by the load resistor (R_{load}) and the load capacitor (C_{load}). Hence, the second pole p_2 and the third parasitic pole p_3 are located at the output node V_{out} and the gate of the power transistor (V_G), where R_{on1} and R_{on2} stand for the output resistance of the turn-on power transistors and the output resistance of the inverter in the coarse loop and the S/R in the fine loop at node V_G. The p_3 is far away from the unit gain-bandwidth product, which does not affect the loop stability. Furthermore, the AA loop in Figure 6b introduces a dc zero z_0 and a pole p_{AA}, and it does not work in the steady state of the DLDO. Therefore, the open-loop transfer function $H(s)_{open\_loop}$ and closed-loop transfer function $H(s)_{close\text{-}loop}$ in the steady state can be expressed respectively as follows:

$$\begin{aligned} H(s)_{open\_loop} &= e^{-sT_{clk}/2} \cdot K_{SR} \cdot \frac{1}{1-z^{-1}} \cdot \frac{1-e^{T_{clk}}}{s} \cdot \frac{K_{DC}}{1+s/F_{load}} \\ &= \frac{K_{forward}}{z-1} \cdot \frac{1-e^{-F_{load}/F_{clk}}}{z-e^{-F_{load}/F_{clk}}} \end{aligned} \tag{7}$$

$$\begin{aligned} H(s)_{close\_loop} &= \frac{H(s)_{open\_loop}}{1+H(s)_{open\_loop}} \\ &= \frac{K_{forward}\left(1-e^{-F_{load}/F_{clk}}\right)}{(z-1)\left(z-e^{-F_{load}/F_{clk}}\right)+K_{forward}\left(1-e^{-F_{load}/F_{clk}}\right)} \end{aligned} \tag{8}$$

where the forward gain $K_{forward} = K_{SR} \cdot K_{DC}$, and F_{load} and F_{clk} are the output pole frequency $((R_{on1} \,||\, R_{load}) \cdot C_{Load})^{-1}$ and the adaptive clock frequency, respectively. Unlike the analog LDO, the DLDO cannot directly reflect the zero-pole point position and the phase characteristics by the AC simulation. The DLDO judges the stability by the distribution of poles in the z plane. As analyzed in Equation (7), one pole is located on the unit circle, which is derived from the S/R. The other pole is determined by the F_{load} and F_{clk} together. The worst case of stability is at the light load due to a large output resistance. In the pre-simulation, the F_{clk} of the AVC was 8 MHz and the F_{load} was 36.4 MHz. In the post-simulation, the F_{clk} was reduced to 7.8 MHz, and the F_{load} was reduced to 35.8 MHz. Hence, the second pole was almost unchanged and hardly affected the stability. Based on the MATLAB model, under the condition of the constant sampling rate F_{clk}, with the decrease in the load current, the decrease in F_{load} makes the two poles ($z = 1$ and $z = e^{-Fload/Fclk}$) closer in Figure 7a, and easily leads to the instability of the system because the phase margin (PM) is decreased from 84.8° to 45.1°, as shown in Figure 7b. The stability of the proposed DLDO benefits from the AVC technology because the clock frequency of F_{clk} can drop down to 8 MHz whether under a heavy or light load.

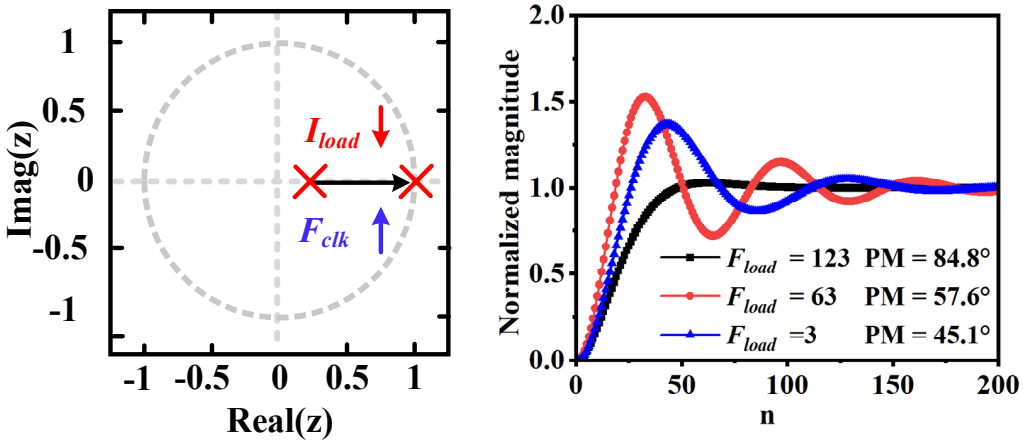


(a)

	Value	From
p_1	0	S/R
p_2	$1/(R_{on1} \| R_{load} \cdot C_{load})$	Load
P_3	$1/(R_{on2} \cdot C_G)$	V_G
p_{AA}	$1/(R_c \cdot C_c)$	AA
z_0	0	AA

(b)

Figure 6. (**a**) Small signal equivalent model; (**b**) pole-zero analysis.



(a) (b)

Figure 7. (**a**) Root locus plot of the proposed DLDO. (**b**) Step response curve at the different F_{load} with a F_{clk} of 1.

3.4. LCO Issues at the Steady State

The intrinsic quantization noise of the DLDO causes the output ripple at the steady state, which is also known as the limit cycle oscillation (LCO) phenomenon. Normally,

the LCO period is 2M times the clock period (T_{clk}), where M is the mode of the LCO. In the classical DLDO, since the bidirectional S/R always samples the quantization result of the previous cycle in Figure 8, the response time of the power PMOS array has a period delay, resulting in the obvious voltage ripple in the conventional DLDO. With the double-edge-trigger method, the comparator performs quantization at a high level, and the S/R outputs and shifts the comparator result at the falling edge in the same cycle. Therefore, the proposed digital LDO can prompt the output timelier than the classical DLDO.

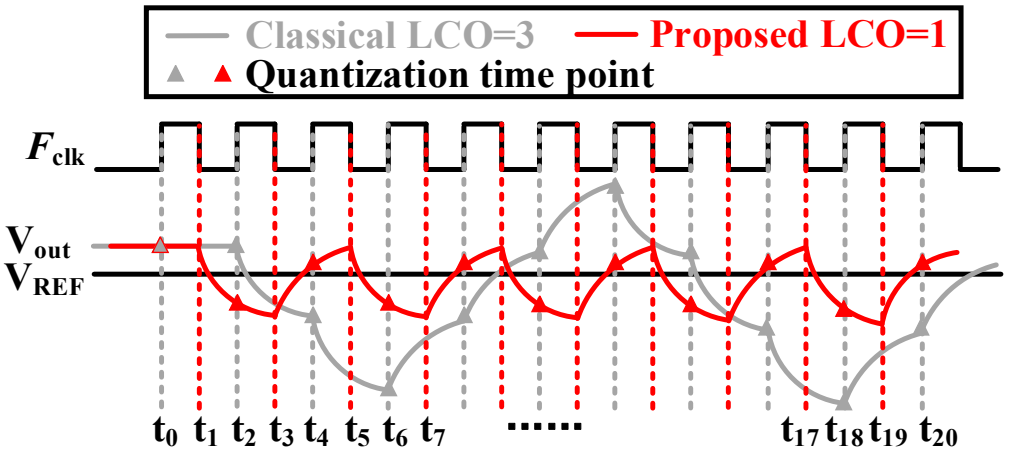


Figure 8. Conceptual transient waveform of the LCO phenomenon.

As shown in Figure 8, when V_{out} is slightly higher than the V_{REF} in the steady state, the comparator performs quantization at t_0, a single PMOS power transistor controlled by the fine bidirectional S/R can be switched off to reduce the output current at t_1, and the output begins to be pulled down. If the settling time τ, decided by the output pole, is less than half of the sampling clock cycle ($T_{clk}/2$), the output voltage can be stable at the next quantization point t_2. According to the comparator result, the PMOS array turns on a single PMOS transistor to provide the output current from the moment t_3, and then the output voltage begins to be stretched to a level higher than V_{REF}, like the moment t_0. As depicted in Figure 8, the mode of the LCO can be reduced from 3 to 1. Compared with the auxiliary redundant PMOS power transistor in the feedforward path [16,17], the proposed LDO can reduce the LCO mode to 1 without adding any extra power consumption or design complexity.

4. Simulation Results and Comparisons

Figure 9 shows that the proposed DLDO occupies an active area of 0.053 mm^2 in a standard 0.18 µm CMOS process including the CMP_0, the AVC, the TD with two self-clocked comparators (CMP_1 and CMP_2), the AA circuit, and the coarse and fine S/R and the power PMOS transistor array. Figure 10 shows the simulation setup of the proposed DLDO. The total on-chip capacitor (C_C) was 50 pF and the resistors R_{a1} and R_{a2} were served for the heavy load and light load, which were designed as 22.5 Ω and 1100 Ω, respectively. The switch (S_w) and the inverter (inv_1) are employed to generate the falling and rising edge time of 100 ps for the load transient.

All parasitic effects were considered including the parasitic capacitance from the metal wires to the substrate, the parasitic capacitance among different metal wires, and the parasitic resistance of the wires. The parasitic resistance of the entire proposed DLDO was reduced by the minimum spacing between modules and the multilayer metal interconnection technology. Because the static current of the proposed DLDO was less than 100 µA, the effect of the parasitic resistance was almost negligible. In addition, the offset of the dynamic comparator and resistance mismatch in the TD circuit were suppressed by good matching and dummy technology.

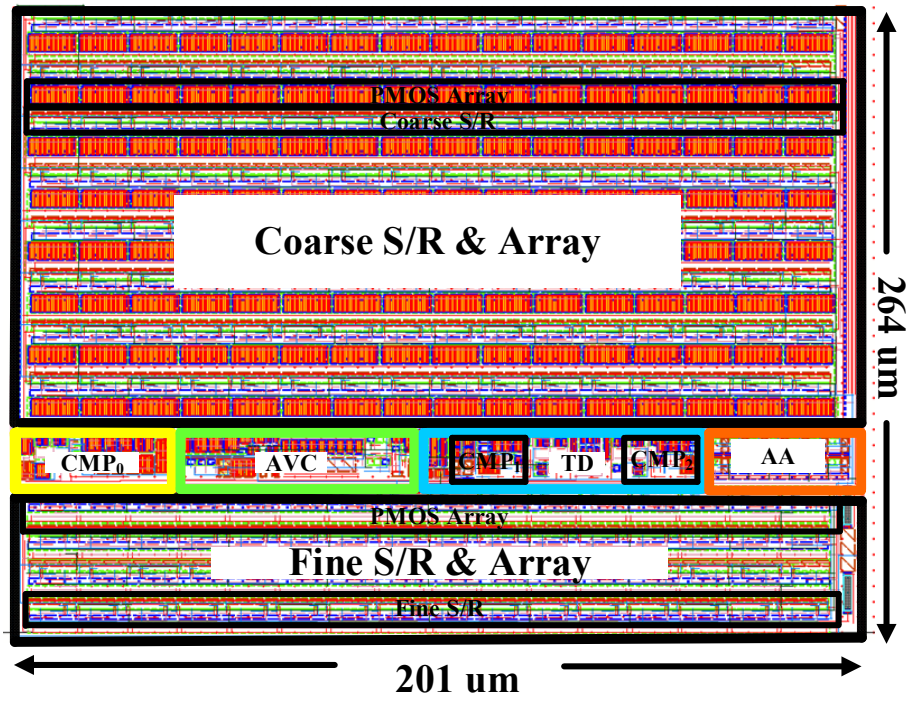


Figure 9. Layout of the proposed DLDO.

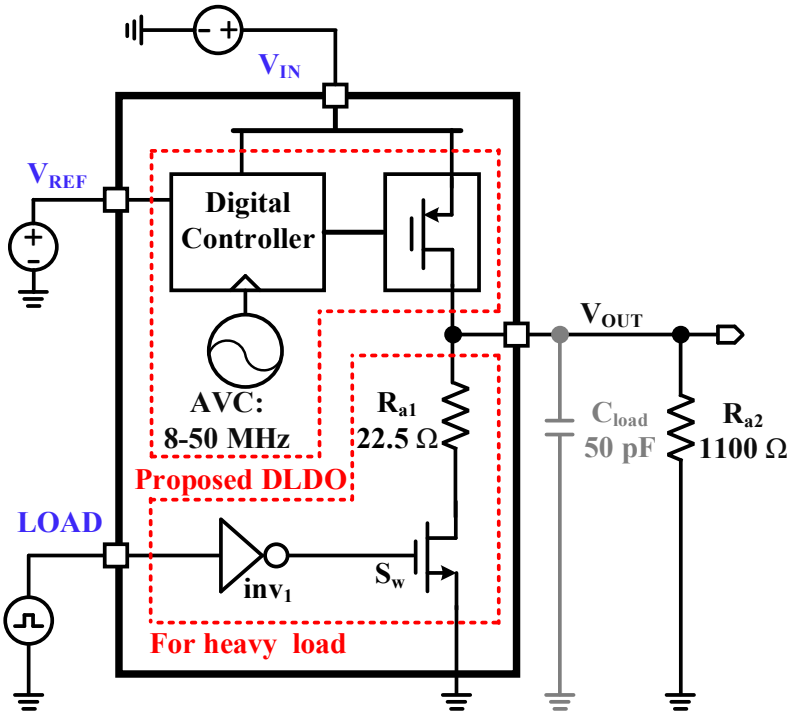


Figure 10. Simulation setup.

The proposed DLDO provides a load current from 500 µA to 25 mA and consumes a quiescent current of 95.13 µA at the heavy load of 25 mA under a low supply of 0.6 V, resulting in a peak current efficiency of 99.6%. The power consumption is independent of the I_{load}, and Figure 11 illustrates the power breakdown of the proposed DLDO in the steady state where the resistors in the TD occupy more than 50% of the total power, and the power of the AVC is only 2.5% of the total power.

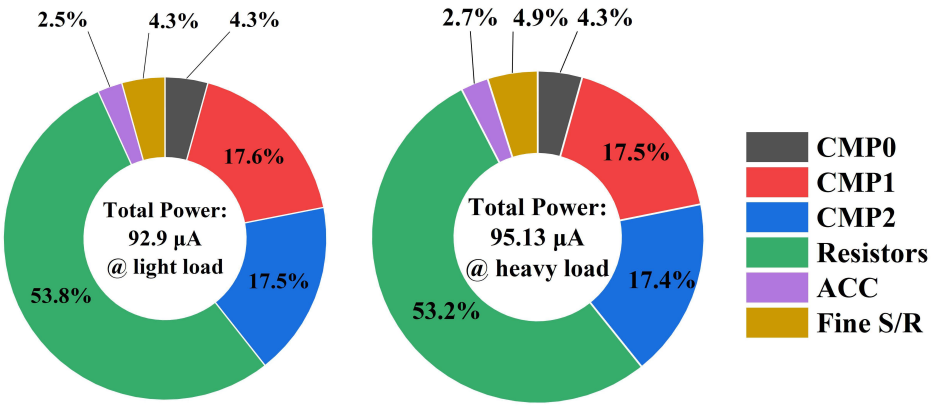


Figure 11. Power breakdown.

The proposed DLDO can regulate V_{OUT} from 550 mV to 1050 mV with the V_{DD} varying from 0.6 V to 1.1 V with a dropout voltage of 50 mV. Figure 12a shows that the line regulation (LR) was 5.8 mV/V at the load current of 0.5 mA and 4.3 mV/V at the heavy load of 25 mA, respectively, while Figure 12b shows that the best and worst LR were 4.2 mV/V and 6.6 mV/V at the V_{REF} of 0.75 V and 0.5 V, respectively. Figure 12c shows that the fluctuation of the load regulation (LD) varied the supply voltage, and the LD as 0.1265 mV/mA at the supply of 0.6 V. Figure 12d,e verified the LR at the light load of 0.5 mA and LD at the 0.6 V supply at different corners, and the LR and LD remained at the same order of magnitude. To evaluate the transient performance of the proposed DLDO, the proposed DLDO regulator was operated at the V_{DD} of 600 mV with the V_{OUT} of 550 mV and the C_C of 50 pF.

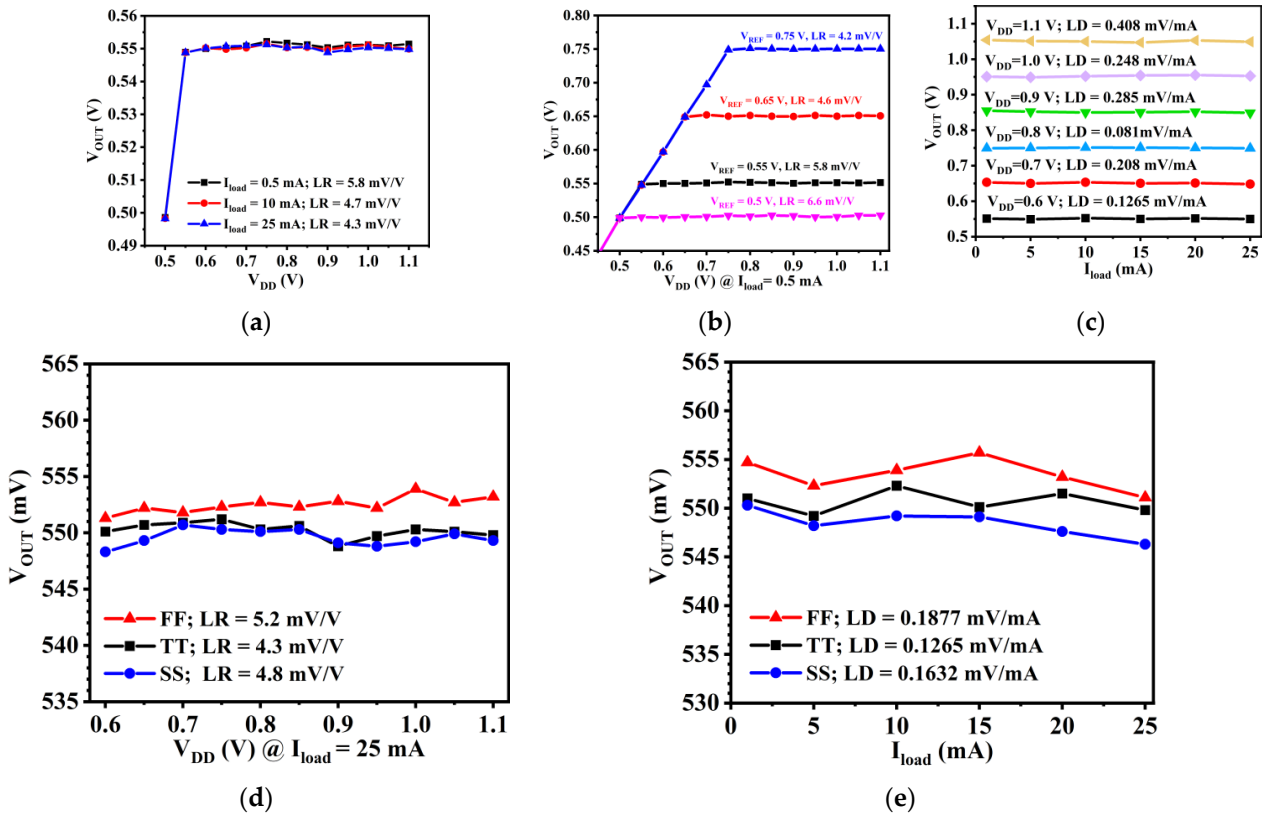


Figure 12. (**a**) Simulated LR at the different loads. (**b**) Simulated LR at different V_{REF} values. (**c**) Simulated LD at different supplies. (**d**) Simulated LR at different corners. (**e**) Simulated LD at different corners.

Regardless of the analog LDO or the digital LDO, the shorter the T_{edge}, the more it can reflect the worst undershoot voltage and overshoot voltage of the LDO. Therefore, T_{edge} was designed to be 100 ps to reflect the worst undershoot voltage and overshoot voltage. The advantage of the capacitor C_C in the AA technology is that the off-chip load capacitor can be reduced to 0 [10]. In order to intuitively reflect the transient effects of parasitic capacitance and resistance, Figure 13 shows that the overshoot voltage and undershoot voltage of the proposed DLDO were almost unchanged, and the recovery time of the undershoot and overshoot was extended by 70 ns and 60 ns, respectively.

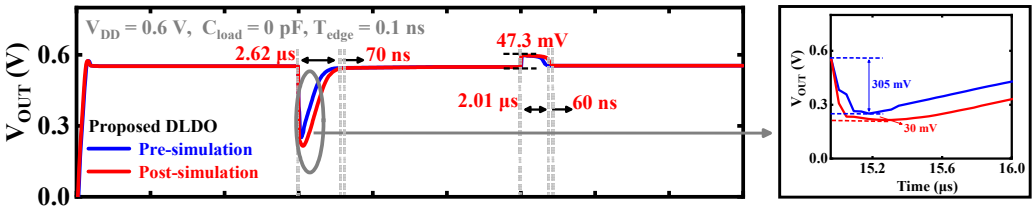


Figure 13. Simulated transient comparison between the pre-simulation and post-simulation.

Figure 14 shows the transient response comparison among the conventional LDO, the DLDO with the AA loop, and the proposed double-edge-triggered DLDO with the AA loop and the AVC. At the external clock frequency of 8 MHz, the undershoot voltage of the conventional DLDO with the AA technology decreased by 66 mV than that of the conventional DLDO when the load current stepped up from 0.5 mA to 25 mA at the edge time (I_{load}) of 100 ps. Compared with the conventional DLDO with the AA technology, the undershoot voltage with the proposed double-edge-triggered DLDO can be reduced from 438 mV to 335 mV, and the recovery time was optimized from 14.8 µs to 2.7 µs in the undershoot case and from 10.5 µs to 2.1 µs in the overshoot case. Meanwhile, it can be seen from Figure 14 that the clock frequency was enhanced from 8 MHz to 50 MHz by the AVC. Figure 14 also shows the transient response of the proposed DLDO with and without a load capacitor at a supply of 0.6 V at the different T_{edge}. As can be seen from Figure 14, the undershoot voltage with the load capacitor was only 21 mV smaller than that without the load capacitor, while the overshoot voltage was almost constant whether the load capacitor exists or not. This verifies that the C_C in the AA technology can reduce the off-chip load capacitor to 0. Furthermore, when the T_{edge} was 400 ns as in [18], the undershoot voltage and overshoot voltage were decreased to 274 mV and 46.51 mV. Figure 15 shows the transient response of the proposed DLDO with and without a load capacitor at a supply of 1.1 V. The undershoot voltage and overshoot voltage were 230 mV and 46 mV without the load capacitor, respectively. When a load capacitor (C_{load}) of 50 pF was added, the undershoot voltage and overshoot voltage decreased to 232 mV and 44.8 mV, respectively. Furthermore, the transient response was also enhanced due to the improvement in the clock frequency of the AVC. Overall, the undershoot voltage and overshoot voltage were optimized with a longer T_{edge} and a load capacitor.

To verify the robustness of the transient responses, the simulation at different process corners and temperatures is depicted in Table 2. The undershoot voltage and overshoot voltage at the FF corner had a smaller spike, and the recovery time became faster than the performances at the TT corner with the same temperature, while the performances at the SS corner behaved just right, in contrast. As a result, the worst undershoot voltage and overshoot voltage were 399 mV with a recovery time of 2.7 µs and 48.3 mV with a recovery time of 2.1 µs, respectively. The reason why the overshoot voltage was almost constant is that V_{out} jumped to almost the supply voltage when the output voltage suddenly dropped from 25 mA to 0.5 mA.

Table 2. Transient response at different temperatures and process corners.

Temp [°C]	−40 °C @I_{load} from 0.5 to 25 mA			27 °C @I_{load} from 0.5 to 25 mA			85 °C @I_{load} from 0.5 to 25 mA		
Corner	**FF**	**TT**	**SS**	**FF**	**TT**	**SS**	**FF**	**TT**	**SS**
Undershoot	329	354	399	292	335	378	268	296	342
@ T_r [mV/µs]	2.46	4.22	8.58	1.8	2.7	4.3	1.22	1.3	3.01
Overshoot	47.5	47.9	48.3	46.8	47.6	48.1	45.3	47.1	47.9
@ T_r [mV/µs]	2.12	3.78	7.57	1.31	2.1	4.03	0.92	1.02	2.88

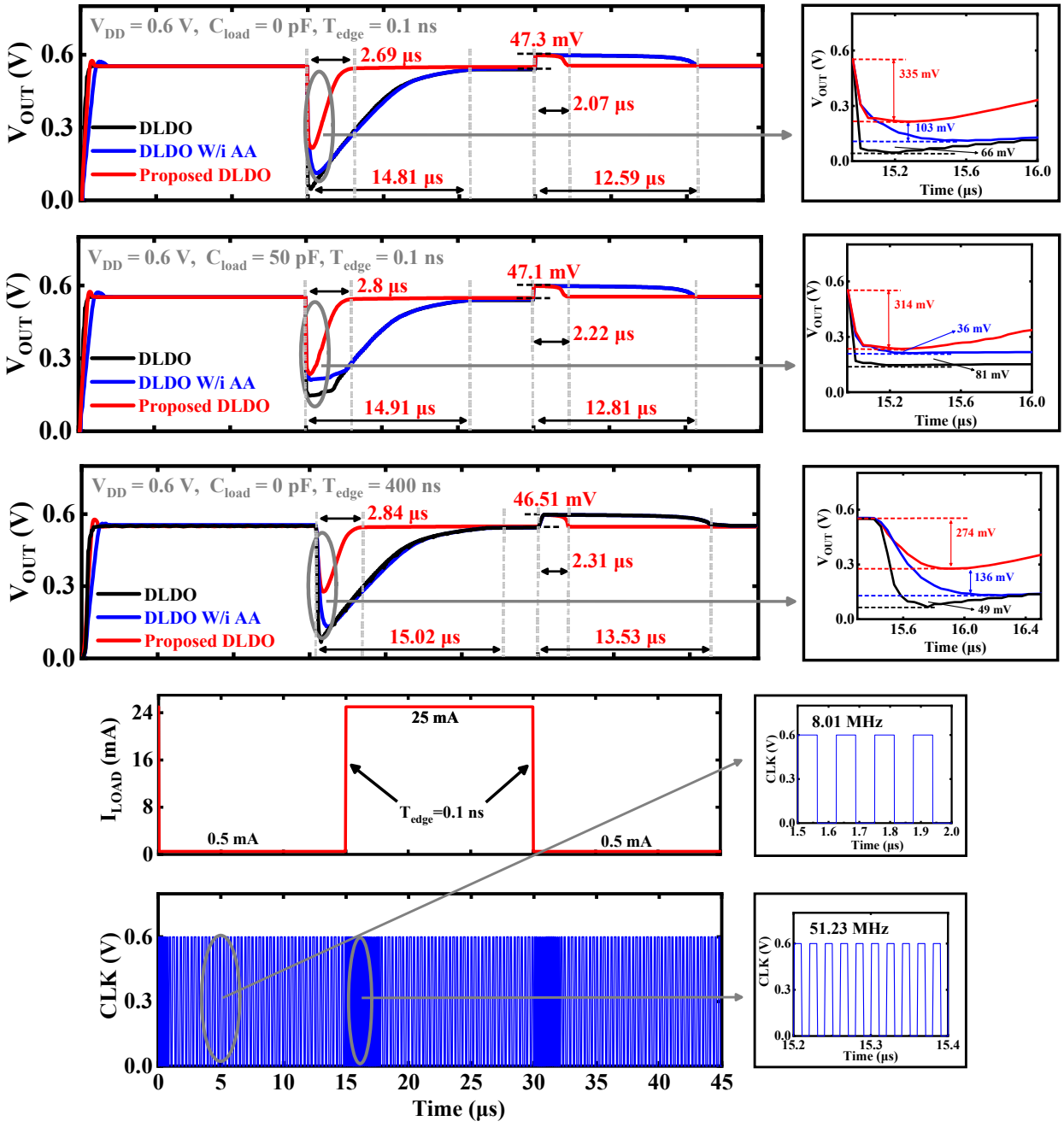


Figure 14. Simulated transient response comparison with Refs [5,10] at a supply voltage of 0.6 V.

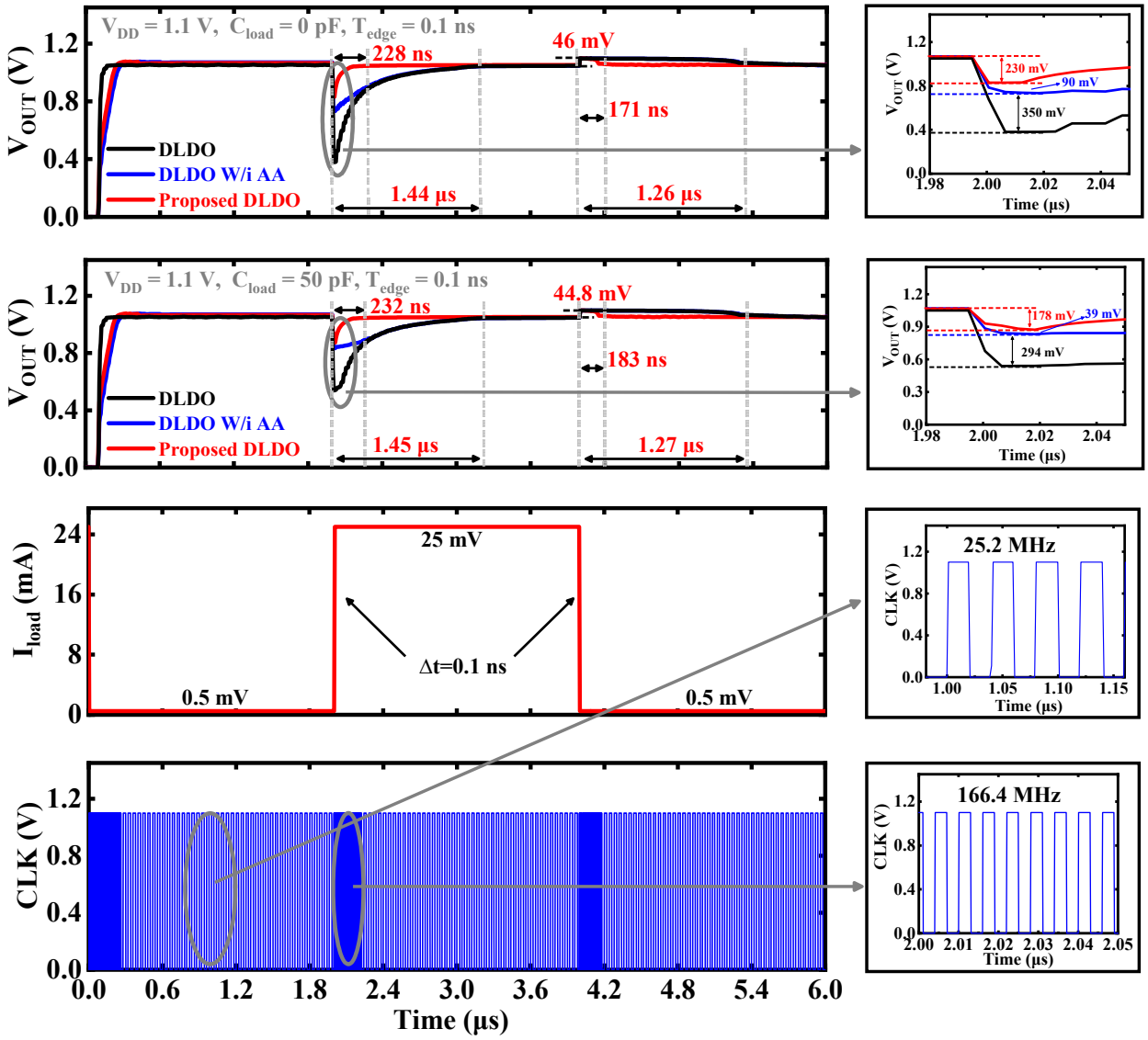


Figure 15. Simulated transient response comparison with Refs [5,10] at a supply voltage of 1.1 V.

Table 3 illustrates the performance parameters of the proposed DLDO in this paper and compares the simulation performances with the state-of-the-art DLDO architectures. In the steady state, the V_{drop} voltage is always 50 mV for any supply voltage. Specifically, when the supply voltage is 1.1 V, the output voltage is 1.05 V, while the supply voltage is 600 mV and the output voltage is 550 mV. Compared with [18,19], these DLDOs still need a large load capacitor to suppress the voltage fluctuation within 100 mV during the transient response. Compared to works with a fixed clock frequency [9,19–21], the AVC between the steady state and the transient response could better balance the transient responses and static current. Although the load current change could achieve a change of 28 mA in [22] at the only load capacitor of 9.5 pF, the DLDO consumed up to the quiescent current of about 1 mA, which degraded the current efficiency. The proposed DLDO can fix the stability issues at any load current and thus allows the output change from the minimum to the maximum load current within an edge time of 100 ps because the clock frequency can be adaptively adjusted based on the output voltage in time. Moreover, even though the power of the AVC is included, the quiescent current of the entire DLDO is still very low, resulting in the two FoMs. Meanwhile, we provide a comparison of the related simulation results with the previous publications [1,2,23,24] in Table 4 regarding the analog LDOs in electronics. It can be seen from Table 4 that the static power consumption of the recent

analog LDOs is comparable to that of the proposed DLDO. Furthermore, the area of these analog LDOs did not include the area of the load capacitor (C_{load}). The analog LDO could achieve better FoMs than the proposed DLDO because of the small undershoot voltage and overshoot voltage due to a larger load capacitor and a looser T_{edge}. The main advantages of the proposed DLDO are the ability to achieve an adjustable output voltage, completely circumvent the load capacitor, and a rigorous T_{edge} of only 0.1 ns at a low power supply (V_{DD} < 1.2 V).

Table 3. Performance summary and comparison with other DLDOs.

	JSSC′ 18 [19] [b]	**TCAS-II′ 20 [9] [b]**	**TCAS-II′ 20 [11] [b]**	**TPE′ 20 [18] [b]**	**AEU′ 21 [20] [a]**	**TPE′ 22 [21] [b]**	**TCAS-II′ 23 [22] [b]**	**This Work [a]**
Process [nm]	65	65	28	40	45	65	65	**180**
Gen method of clock	External clock	External clock	External clock	External clock	External clock	VCO	External clock	**VCO**
Trigger method	Asyn/ SET	Syn/ SET	Syn/ SET	Asyn/ SET	Syn/ SET	Syn/ SET	Asyn/ SET	**Syn**/ DET
Clock Adaptive	Yes	NO	Yes	NO	NO	Yes	Yes	**Yes**
F_{clk} [MHz]	1–240	10	4–64	100	10	500	NA	**8–50**
V_{DD} [V]	0.5–1	0.6–1.0	0.5–1	0.6–1.1	0.5–1	0.9–1.2	0.7–1.3	**0.6–1.1**
V_{out} [V]	0.3–0.45	0.55–0.95	0.45–0.95	0.5–1	0.45–0.95	0.5–1.1	0.65–1.25	**0.55–1.05**
V_{drop} [mV]	50	50	50	100	50	100	50	**50**
C_{load} [pF]	400	1000	100	4700	50	200	0	**0**
C_{total} [pF]	400	1000	100	4700	50	200.5	9.5	**50**
I_Q [μA]	14	10.2	20.1	19.6	22	131	1050	**95.13**
$I_{load,\ max}$ [mA]	5.6	4.5	6.5	20	2	6	80	**25**
$I_{load,\ min}$ [mA]	0.0001	0.1	1	0.4	0.5	0.15	5	**0.5**
ΔI_{Load} [mA]	1.06	-	2	19	1.5	3	28	**24.5**
Line regulation [mV/V]	2.3	-	-	-	23.8	-	2.63	**4.3**
Load regulation [mV/mA]	5.6	4.4	0.0196	1	1.007	0.15	-	**0.1265**
T_{edge} [ns]	15.1	10	5	400	1	5	0.1	**0.1**
ΔV_{OUT} [mV]	40	118	92	40	140	80	275	**335**
Settling Time [μs]	0.1	5.9	0.083	1.3	1.2	0.09	0.0018	**2.7**
Peak current efficiency [%]	99.8	99.7	99.8	99.9	99.98	99.3	99.7	**99.6**
Area [mm^2]	0.0023	0.0896	0.04173	0.18	0.0064	0.059	0.0925	**0.053**
FoM_1 [ps] [4]	199.359	62.16	46.23	10.2	6.84	232.88	3.498	**2.654**
FoM_2 [pF] [11]	0.7	0.683	0.205	0.387	0.228	1.397	0.15	**0.13**

[a] Simulation results, [b] Measurement results; SET: Single-edge trigger, DET: Double-edge trigger; $FoM_1 = C_{total} \times \Delta V_{out} \times I_Q/\Delta I_{load}{}^2$; $FoM_2 = C_{total} \times \Delta V_{out} \times I_Q/(V_{out} \times \Delta I_{load})$.

Table 4. Performance summary and comparison with other analog LDOs.

	Electronics' 21 [23] [a]	**Electronics' 22 [24] [a]**	**Electronics' 23 [1] [a]**	**Electronics' 23 [2] [a]**	**This Work [a]**
Process [nm]	180	180	180	180	**180**
Architecture	ALDO	ALDO	ALDO	ALDO	**DLDO**
V_{DD} [V]	1.297–3.3	1.2–1.8	1.8	2–5	**0.6–1.1**
V_{out} [V]	1.2	1	1.5	1.8	**0.55–1.05**
V_{drop} [mV]	97	200	300	200	**50**
C_{load} [pF]	50	100	50	5	**0**
C_{total} [pF]	56.1	107.5	1050	5	**50**
$Power_Q$ [μW]	11.15	12.36	28.98	132.8	57.07
$I_{load,\ max}$ [mA]	50	100	50	300	**25**
$I_{load,\ min}$ [mA]	1	1	0.2	3	**0.5**
ΔI_{Load} [mA]	50	99	49.8	297	**24.5**
Line regulation [mV/V]	0.065	2.74	-	0.55	**4.3**
Load regulation [mV/mA]	0.006	0.034	1450	0.00194	**0.1265**
T_{edge} [ns]	1000	100	10	300	**0.1**
ΔV_{OUT} [mV]	666	47	129	153	**335**
Settling Time [μs]	6.7	0.19	0.2	0.4	**2.7**
Peak current efficiency [%]	99.9	99.9	99.9	99.9	**99.6**
Area [mm^2]	0.103	0.01524	0.046	0.085	**0.053**
FoM_1 [ps] [4]	0.11	0.005	0.879	0.005	**2.654**
FoM_2 [pF] [11]	0.005	0.0005	0.029	0.0001	**0.13**

[a] Simulation results.

5. Conclusions

A double-edge-triggered DLDO was proposed with a built-in adaptive VCO clock. With the double-edge-trigger technology, the transient response can be enhanced by 2× without any power increment in the DLDO. In addition, the stability is also relaxed due to the low clock frequency, and the mode of the LCO is optimized as 1. Moreover, the built-in adaptive clock can accelerate the clock frequency from 8 MHz to 50 MHz, which balances the recovery time in the transient response and the power consumption in the steady state. The post-simulation results using a standard 0.18 μm CMOS process demonstrated that the maximum current is 99.6% with the self-clock comparators. Furthermore, benefiting from the process scaling, the proposed DLDO will be very suitable for ultra-low-voltage and ultra-low-power integrated digital circuits and systems.

Author Contributions: Conceptualization, X.X., D.W. and X.T.; Methodology, X.X. and D.W.; Validation, X.X. and D.W.; Formal analysis, D.W.; Investigation, X.X.; Resources, X.X. and X.T.; Writing—original draft preparation, X.X.; Writing—review and editing, D.W. and X.T.; Supervision, X.T.; Project administration, X.T.; Funding acquisition, X.X. and X.T. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported in part by the National Natural Science Foundation of China (No. 62104193, and No. 62271389) and the Key Scientific Research Program of Shaanxi Provincial Department of Education (No. 22JY058).

Data Availability Statement: Data sharing is not applicable to this article as no datasets were generated or analyzed during the current study.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Li, Y. A Low-Power, Fast-Transient FVF-Based Output-Capacitorless LDO with Push–Pull Buffer and Adaptive Resistance Unit. *Electronics* **2023**, *12*, 1285. [CrossRef]
2. Gao, M. Fully Integrated 1.8 V Output 300 mA Load LDO with Fast Transient Response. *Electronics* **2023**, *12*, 1409. [CrossRef]
3. Wang, Z.; Kim, S.J.; Bowman, K.; Seok, M. Review, Survey, and Benchmark of Recent Digital LDO Voltage Regulators. In Proceedings of the 2022 IEEE Custom Integrated Circuits Conference (CICC), Newport Beach, CA, USA, 24–27 April 2022; Volume 52, pp. 1–8.
4. Ma, X.; Lu, Y.; Li, Q.; Ki, W.H.; Martins, R.P. An NMOS Digital LDO With NAND-Based Analog-Assisted Loop in 28-nm CMOS. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2020**, *67*, 4041–4052. [CrossRef]
5. Okuma, Y. 0.5-V input digital LDO with 98.7% current efficiency and 2.7-μA quiescent current in 65nm CMOS. In Proceedings of the 2010 IEEE Custom Integrated Circuits Conference (CICC), San Jose, CA, USA, 19–22 September 2010; Volume 54, pp. 1–4.
6. Yang, F.; Mok, P.K. A Nanosecond-Transient Fine-Grained Digital LDO With Multi-Step Switching Scheme and Asynchronous Adaptive Pipeline Control. *IEEE J. Solid-State Circuits* **2017**, *52*, 2463–2474. [CrossRef]
7. Akram, M.A.; Hong, W.; Hwang, I.C. Capacitorless Self-Clocked All-Digital Low-Dropout Regulator. *IEEE J. Solid-State Circuits* **2019**, *54*, 266–276. [CrossRef]
8. Shi, J.; Zhao, B.; Tang, Z.; Ma, P.; Di, Z. A self-clocked binary-seaching digital low-dropout regulator with fast transient response. *IEICE Electron. Express* **2020**, *17*, 20200297. [CrossRef]
9. Qian, L.; Li, D.; Qian, K.; Ye, Y.; Xia, Y.; Mak, T. A Fast-Transient Response Digital Low-Dropout Regulator with Dual-Modes Tuning Technique. *IEEE Trans. Circuits Syst. II* **2020**, *67*, 2943–2947. [CrossRef]
10. Huang, M.; Lu, Y.; Seng-Pan, U.; Martins, R.P. An analog-assisted tri-loop digital low-dropout regulator. *IEEE J. Solid-State Circuits* **2018**, *53*, 20–34. [CrossRef]
11. Oh, J.; Park, J.E.; Jeong, D.K. A Highly Synthesizable 0.5-to-1.0-V Digital Low-Dropout Regulator with Adaptive Clocking and Incremental Regulation Scheme. *IEEE Trans. Circuits Syst. II* **2020**, *67*, 2174–2178. [CrossRef]
12. Babayan-Mashhadi, S.; Lotfi, R. Analysis and Design of a Low-Voltage Low-Power Double-Tail Comparator. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2014**, *22*, 343–352. [CrossRef]
13. Albano, D.; Crupi, F.; Cucchi, F.; Iannaccone, G. A Sub-kT/q Voltage Reference Operating at 150 mV. *IEEE Trans. Very Large-Scale Integr. (VLSI) Syst.* **2015**, *23*, 1547–1551. [CrossRef]
14. Huang, M.; Lu, Y.; Sin, S.W.; Seng-Pan, U.; Martins, R.P. A Fully Integrated Digital LDO with Coarse–Fine-Tuning and Burst-Mode Operation. *IEEE Trans. Circuits Syst. II* **2016**, *63*, 683–687. [CrossRef]
15. Xu, H.; Abidi, A.A. Analysis and Design of Regenerative Comparators for Low Offset and Noise. *IEEE Trans. Circuits Syst. I* **2019**, *66*, 2817–2830. [CrossRef]
16. Huang, M.; Lu, Y.; Sin, S.W.; Seng-Pan, U.; Martins, R.P.; Ki, W.H. Limit Cycle Oscillation Reduction for Digital Low Dropout Regulators. *IEEE Trans. Circuits Syst. II* **2016**, *63*, 903–907. [CrossRef]
17. Cai, G.; Zhan, C.; Lu, Y. A Fast-Transient-Response Fully-Integrated Digital LDO With Adaptive Current Step Size Control. *IEEE Trans. Circuits Syst. I* **2019**, *66*, 3610–3619. [CrossRef]
18. Lin, J.H.; Yang, S.H.; Muniandi, B.; Ma, Y.S.; Huang, C.M.; Chen, K.H. A High Efficiency and Fast Transient Digital Low-Dropout Regulator with the Burst Mode Corresponding to the Power-Saving Modes of DC–DC Switching Converters. *IEEE Trans. Power Electron.* **2020**, *35*, 3997–4008. [CrossRef]
19. Salem, L.G.; Warchall, J.; Mercier, P.P. A Successive Approximation Recursive Digital Low-Dropout Voltage Regulator with PD Compensation and Sub-LSB Duty Control. *IEEE J. Solid-State Circuits* **2018**, *53*, 35–49. [CrossRef]
20. Sood, L.; Agarwal, A. A CMOS standard-cell based fully-synthesizable low-dropout regulator for ultra-low power applications. *AEU-Int. J. Electron. Commun.* **2021**, *141*, 153958. [CrossRef]
21. Kang, J.G.; Park, J.; Jeong, M.G.; Yoo, C. Digital Low-Dropout Regulator with Voltage-Controlled Oscillator Based Control. *IEEE Trans. Power Electron.* **2022**, *37*, 6951–6961. [CrossRef]
22. Cherivirala, Y.K.; Wentzloff, D.D. A Capacitor-Less Digital LDO Regulator with Synthesizable PID Controller Achieving 99.75% Efficiency and 93.3-ps Response Time in 65 nm. IEEE Trans. *Circuits Syst. II* **2023**, *70*, 1769–1773. [CrossRef]
23. Perez-Bailon, J.; Calvo, B.; Medrano, N. A Fully-Integrated 180 Nm CMOS 1.2 V Low-Dropout Regulator for Low-Power Portable Applications. *Electronics* **2021**, *10*, 2108. [CrossRef]
24. Jiang, Y.; Wang, L.; Wang, S.; Cui, M.; Zheng, Z.; Li, Y. A Low-Power, Fast-Transient Output-Capacitorless LDO with Transient Enhancement Unit and Current Booster. *Electronics* **2022**, *11*, 701. [CrossRef]