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Design of Cost-Efficient SRAM Cell in Quantum Dot Cellular Automata Technology

Soha Maqbool Bhat [1,*], Suhaib Ahmed [2], Ali Newaz Bahar [3,4,*], Khan A. Wahid [4], Akira Otsuki [5,6,7,*] and Pooran Singh [1]

[1] Department of Electrical and Electronics Engineering, Mahindra University, Hyderabad 500043, India
[2] Department of Electronics and Communication Engineering, Baba Ghulam Shah Badshah University, Rajouri 185234, India
[3] Department of Information and Communication Technology (ICT), Mawlana Bhashani Science and Technology University, Tangail 1902, Bangladesh
[4] Department of Electrical and Computer Engineering, University of Saskatchewan, Saskatoon, SK S7N5A9, Canada
[5] Facultad de Ingeniería y Ciencias, Universidad Adolfo Ibáñez, Diagonal Las Torres 2640, Peñalolén, Santiago 7941169, Chile
[6] Waste Science & Technology, Luleå University of Technology, SE 971 87 Luleå, Sweden
[7] Neutron Beam Technology Team, RIKEN Center for Advanced Photonics, RIKEN, Wako 351-0198, Japan
* Correspondence: soha.bhat@outlook.com (S.M.B.); ali.bahar@usask.ca (A.N.B.); akira.otsuki@uai.cl (A.O.)

Abstract: SRAM or Static Random-Access Memory is the most vital memory technology. SRAM is fast and robust but faces design challenges in nanoscale CMOS such as high leakage, power consumption, and reliability. Quantum-dot Cellular Automata (QCA) is the alternative technology that can be used to address the challenges of conventional SRAM. In this paper, a cost-efficient single layer SRAM cell has been proposed in QCA. The design has 39 cells with a latency of 1.5 clock cycles and achieves an overall improvement in cell count, area, latency, and QCA cost compared to the reported designs. It can therefore be used to design nanoscale memory structures of higher order.

Keywords: QCA cell; memory cell; QCADesigner; low power dissipation; cost-efficient

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1. Introduction

There are several parameters that determine a CMOS-based device's characteristics: the gate-source voltage, drain-source voltage, oxide capacitance, threshold voltage, and drain-source current. When any of the above-mentioned parameters are altered, several quantum effects result in decreased performance of a device at the nanoscale. Small feature sizes associated with current CMOS technology will have many limitations in the near future [1]. In addition to leakage currents, power dissipation and oxide thickness scaling can also result in electron migration and cross-talk [1,2]. There are several examples of DIBL (drain induced barrier lowering), a decrease in gate oxide thickness, the merging of source and drain that produces punch-through conditions, and excessive current flow from a physical perspective [1]. The effects mentioned above violate the laws of physics and hinder the device from working properly. Furthermore, industries function according to the principle of cost-benefit analysis. Since the number of components on a single chip is increasing, excessive heat is generated in the chip and the small size of the chip causes it to be difficult to remove. The chip is thus destroyed under operative conditions as a result of the power dissipation [1]. To combat the consequences and effects discussed above, CMOS in nano regime needs to adopt alternate paradigms. Quantum dot Cellular Automata (QCA) nanotechnology is one of the most promising new technologies [1,2]. It provides high operational speed/frequency (in the range of THz) [3,4], high device density [5], and low power dissipation [6]. Therefore, QCA is attracting researchers to design various digital circuits, such as adders, multipliers, multiplexers, encoders, decoders, flip flops,

shift registers, content addressable memory, etc., in QCA technology to overcome the issues faced by CMOS [7–14].

QCA uses quantum dots or metal islands in place of transistors when designing digital circuits. There are four quantum dots in a QCA cell. This is one of the key components of QCA circuits [1,7,8]. Located at the corners of the cell, these quantum dots measure 18 nm by 18 nm. A pair of free electrons reside in the quantum dots diagonal to one another. It is not possible for these electrons to move between the cells, but they can tunnel between the dots. The electrons can be seen as having two polarization states [7]. The values can be either '0' or '1'. It is because of the Columbic repulsion between the cells that the cells exhibit these polarization states and information flows between them. Figure 1 shows the basic QCA cell and its polarization states.

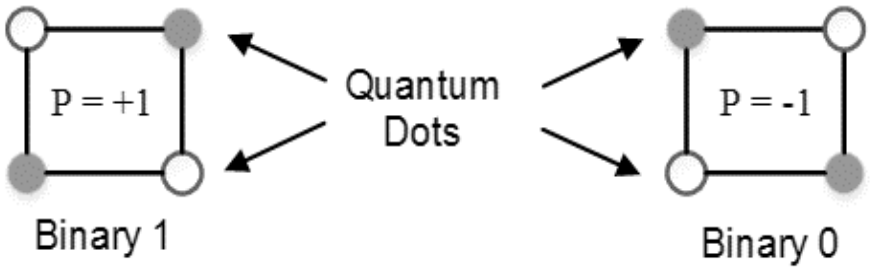


Figure 1. Representation of polarization states of QCA cell [7,8].

QCA can be implemented using four approaches, which are semiconductor [15,16], metal-island [17,18], magnetic [19,20], and molecular [21,22]. The first concept of QCA was demonstrated by fabrication of a metal island, wherein quantum dots were built using aluminum islands. However, this method was not suitable for higher order scalable circuits due to low speed of operation [17]. Semiconductor QCAs implementations are possible using highly advanced semiconductor serial lithography processes available for CMOS devices [15]. Magnetic QCA (MQCA) uses the concept of magnetic exchange interactions between nano participles for operation [19,20], whereas molecular implementation theoretically provides highly dense, symmetrical, and high speed designs. However, selection of molecules and clocking is a challenge [21,22]. In this paper, thus, semiconductor QCA based implementations have been presented.

A QCA cell has four clock levels to ensure that the signal power is dissipated in the right direction. These are Switch, Hold, Release, and Relax [7,8]. This QCA clocking is depicted in Figure 2. During the switch phase, the cell switches polarity when the barrier between dots increases, and it maintains its polarity after reaching the barrier during the hold phase. When the cell releases its polarity, it loses its orientation. When the cell reaches the relaxation phase, electrons are free to transfer within [8]. An identical clock signal is sent to the cells within a zone and a sub-array is formed. A maximum of 100 MHz frequency is attainable theoretically in magnetic QCA, up to 1 GHz in semiconductor and 1 THz in molecular QCA [23].

A memory cell is the basic unit of a memory array. Static Random Access Memory (SRAM) is the fundamental and most vital memory technology. It is fast and robust and finds its application in microprocessors and microcontrollers. The scaling of transistors has increased the demand for larger and faster microprocessors and the demand for high-density and high-speed SRAM. Hence, there is a need to design efficient SRAMs for low-power and ultra-dense applications. In this paper, an optimized design of SRAM is presented using semiconductor QCA; however, theoretical power consumption and throughput calculations have also been performed for molecular QCA implementation of the same design, since it has a higher speed of operation.

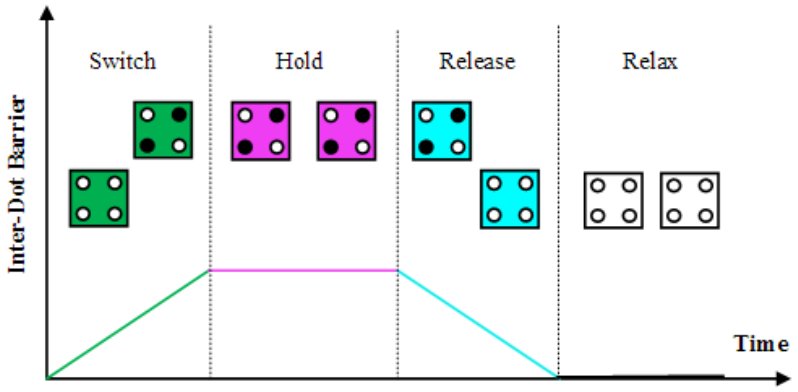


Figure 2. Clocking in QCA [7,8].

1.1. Paper Contributions

i. Design of optimized SRAM cell in QCA using majority voter gates and inverters.
ii. Energy dissipation evaluation at different kink energy levels.
iii. Theoretical analysis of power consumption and throughput for semiconductor and molecular QCA techniques.

1.2. Paper Organziation

The rest of the paper is organized as follows: various design parameters needed for comparison of QCA circuits are discussed in Section 2, followed by a discussion on various simulation parameters in Section 3. A brief review of existing SRAM designs in QCA along with motivation of this work is presented Section 4. The proposed logic design, its operating table, and QCA implementation are presented in Section 5. The simulation waveform needed for verification of proposed QCA design is presented in Section 6 along with energy dissipation analysis, theoretical comparison of power dissipation, throughput for semiconductor and molecular QCA techniques, and performance comparison with existing designs. This is followed by a conclusion in Section 6.

2. Design Parameters in QCA

The parameters of QCA circuits which are necessary for designing efficient circuits are as follows [1]:

i. *Cell Count:* While designing a circuit layout, the number of cells used determines the QCA cell count. Circuits should have as few cells as possible.
ii. *Cell Area:* The cell area is calculated by multiplying the area of a single cell by the total number of cells in the design. The cell area is 18 nm $\times$ 18 nm. Using this calculation result, it is possible to determine how many semiconductor or metal materials are needed for fabrication.
iii. *Total Area:* By multiplying the length by the width of the cellular area, the area occupied by the cellular arrangement is given. Since it incorporates the intercellular gap of 2 nm, it is different from the cell area parameter. It determines how much space a particular cell architecture will consume on a die (wafer), and as a result, how big the entire chip will be.
iv. *Latency:* Using the input–output route with the most phase shifts in the clock, the delay between the input signal and output signal is calculated by dividing the number by four.
v. *Hardware Complexity:* The hardware complexity can be determined by the total number of majority voters, inverters, and crossovers used in a QCA layout. The explicit interaction of cells in a circuit, on the other hand, does not take this parameter into account.
vi. *Energy dissipation:* Electronic devices have been severely restricted by energy dissipation. As the cells are more closely packed in QCA, they do not return to their

ground state after the clocking has been removed, since they are in close proximity to the surrounding cells. As a result of this, more energy is needed to stimulate the cell in the opposite polarization. Therefore, more energy is lost. The increase in energy dissipation can be attributed to factors including temperature and kink energy. All these factors are triggered by a non-energy lowering to the ground state.

3. Simulation Parameters in QCA

The simulation parameters that are required for verifying the operation of any QCA circuit are as follows [1]:

i. *Simulation Engine:* The coherence vector and bistable approximation simulation engines are available in QCA designer. In the first one, the speed is better, but the accuracy is decreased, while in the second one, the speed is better, but the accuracy is decreased.
ii. *Relative Permittivity:* QCA circuits can be manufactured with Ga-As, which has a permittivity of 12.9. Therefore, in the simulation of QCA circuits, this value was used.
iii. *Layer Separation:* The layered QCA design supports multilayer crossovers and reduces the overall circuit area.
iv. *Clock Amplitude Factor:* By default, the clock amplitude factor was set to 2 V (peak-to-peak).
v. *Temperature:* The temperature in QCA designer tool was 1 K by default. However, the temperature can be changed easily in the simulation settings.

4. Literature Review of SRAM Cell in QCA

Extensive research has been undertaken in the area of QCA to design SRAM memory cells. Loop-based structures are used in QCA technology for memory cell design. The data are stored within a closed loop of the QCA cell. Researchers have designed memory cells using various techniques such as SR latch, D-latch, multiplexer based, and majority—voter-based cells [23–32] in QCA technology.

Walus et al. proposed a RAM cell design using the D-latch [32]. Coplanar wire crossing is used in this design, and the QCA cell layout does not optimize the area, latency, or cell count. Another D-latch memory cell was proposed by Dehkordi et al. in [25]. They proposed two QCA layouts, one of which was better in terms of cell count than the second. The first design required 100 cells with a latency of eight clock zones and the second one required 63 cells and a latency of four clock zones.

Kianpour et al. proposed a RAM cell design [23] that requires only 53 cells, a latency of 1.5 clock zones, and occupies 0.05 μm^2 of area. The design dissipates more energy which adds to its disadvantage. Another loop-based memory cell proposed by Fan and Navimipour in [24] required 55 cells and occupies 0.06 μm^2 of area. This design dissipated less energy, but the latency was high.

Hashemi et al. proposed a RAM cell using a 2×1 multiplier in [31]. This layout was more optimal than the D-latch and SR-latch based memory cells, in terms of cell count, total area, and output stability. Using a majority voter gate that has five inputs and three inputs, Angizi et al. in [30] proposed a RAM cell with set/reset capabilities. Having features and full functionality of a memory cell, this design was optimal in terms of number of cells, total area, and stability of output. Khosroshahy et al. proposed a RAM cell using four three-input majority gates and one five-input majority gate with four control lines in [26]. The memory cell has achieved high performance, low-complexity, and is energy efficient.

These designs [23–32] were having the problem of a high count of QCA cells, inverters, and majority voters, which led to increased circuit cost and complexity. Moreover, they have low throughput, more energy dissipation, and high latency. Considering these shortcomings, in this paper, an optimized and efficient RAM cell with one inverter and four majority voter gates is designed in QCA to achieve low cell count, low power dissipation, and high speed of operation.

5. Proposed Design of Memory Cell

An optimized design of a memory cell in QCA is presented in this section. In this memory cell, when *Read_Enable* is equivalent to logic 1, the output is enabled and when the *Read_Enable* is equivalent to logic 0, the output will be logic 0. When *Read'/Write* is equivalent to logic 1, the write state is enabled and the memory loop will save the value of *Data*_Write. Whenever *Read'/Write* is equivalent to logic 0, the read state is enabled and the previously stored bit is given as the result of the output. The operation of this memory cell is given in Table 1. Figure 3 represents the logic level representation of the memory cell and the QCA implementation is given in Figure 4. The design was optimized to 39 cells along with a reduction in total area and QCA cost. This was achieved by using efficient three-input majority voter gates (for AND and OR operations) and an inverter in the proposed design. The throughput of a molecular QCA based proposed circuit is 42 GB/s and 42 MB/s for a semiconductor based QCA circuit. This throughput was calculated as the number of outputs multiplied by the number of stages divided by twice the initial latency [23]. The number of outputs and number of stages is 1 and the initial latency was 1.5 for the proposed design. The theoretical frequency of semiconductor and molecular QCA is 1 GHz and 1 THz, respectively [23].

Table 1. Operation of Memory Cell.

Mode	Read'/Write	Read_Enable	Data_Write	Memory Loop	Output
Read	0	0 1	x	No Change	0 Previous Value
Write	1	x	0 1	0 1	Don't Care

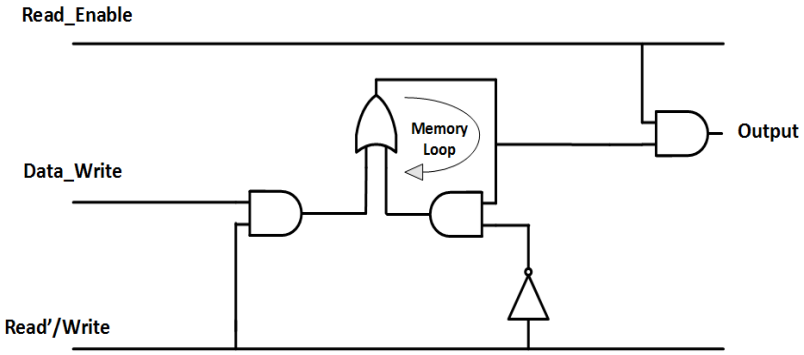


Figure 3. Logical representation of memory cell.

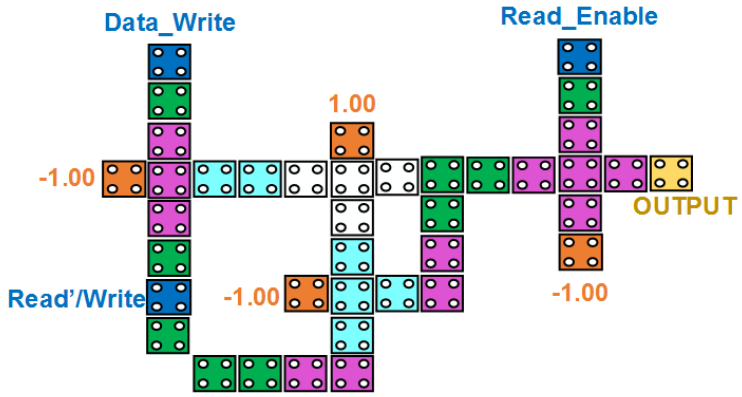


Figure 4. Implementation of a memory cell in QCA.

6. Results and Discussion

In this section, the simulation results are presented for the proposed memory cell design in QCA. The simulation was performed using QCA Designer 2.0.3 tool [33]. The engine setup used for the simulation was coherence vector.

As shown in Figure 5, the output of a memory cell is reached after 1.5 clock cycles in QCA, and it contributes to the latency design. It is validated that when *Read'/Write* is equal to logic 1, the write state is enabled and the memory loop saves the value of *Data_Write*. Whenever *Read'/Write* is equal to logic 0, the read state is enabled and the previously stored bit is given to the output.

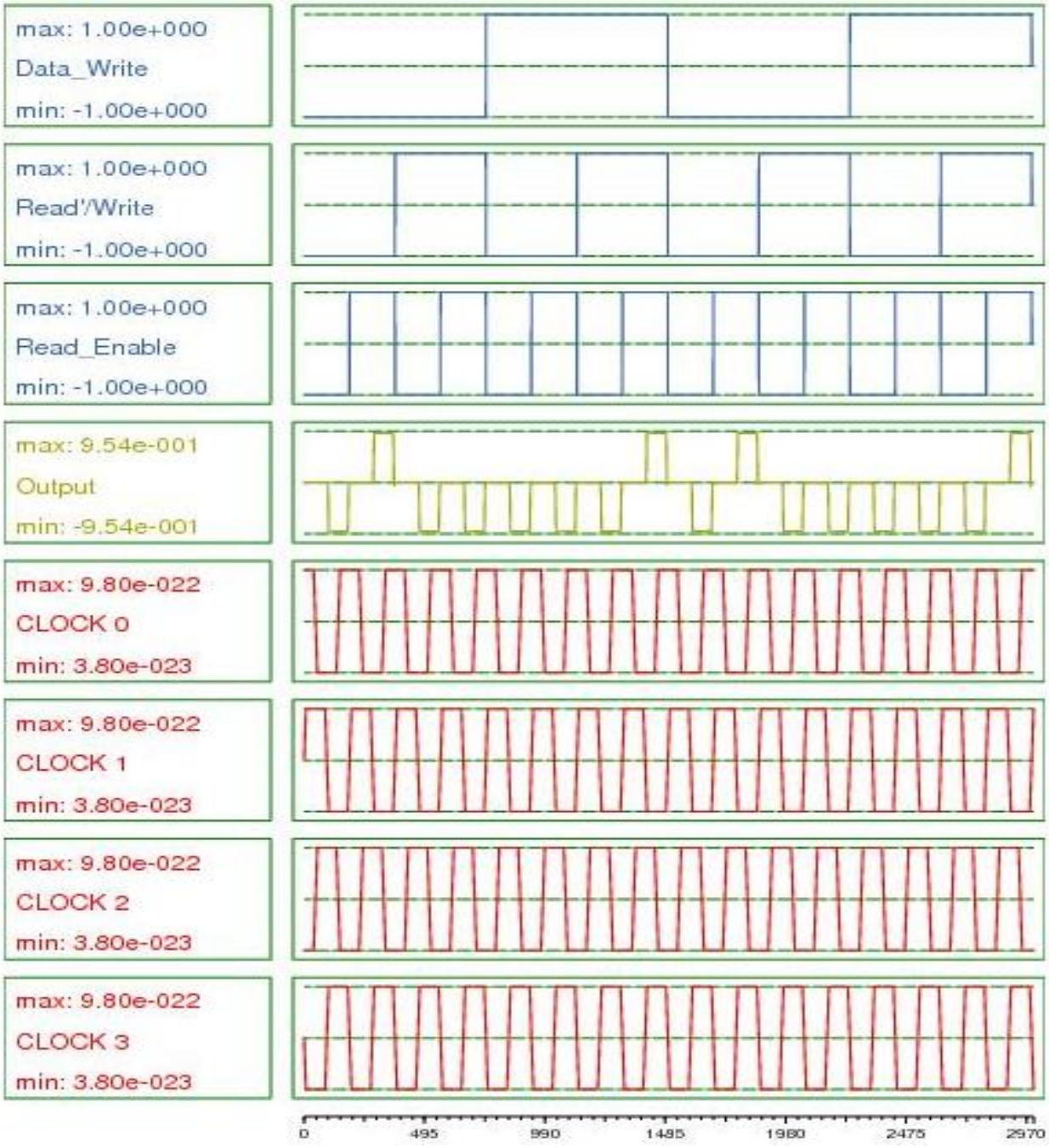


Figure 5. Simulation result of the memory cell in QCA.

The energy dissipation was investigated using the QCAPro tool [34]. The investigation was performed at 0.5, 1.0, and 1.5 Ek, which were the three different tunneling levels. Figure 6 shows the energy dissipation maps at 2 Kelvin temperature for the proposed design. At 0.5, 1.0, and 1.5 kink energy levels, the total energy dissipated by the proposed design was 60.38, 77.47, and 98.35 meV, respectively.

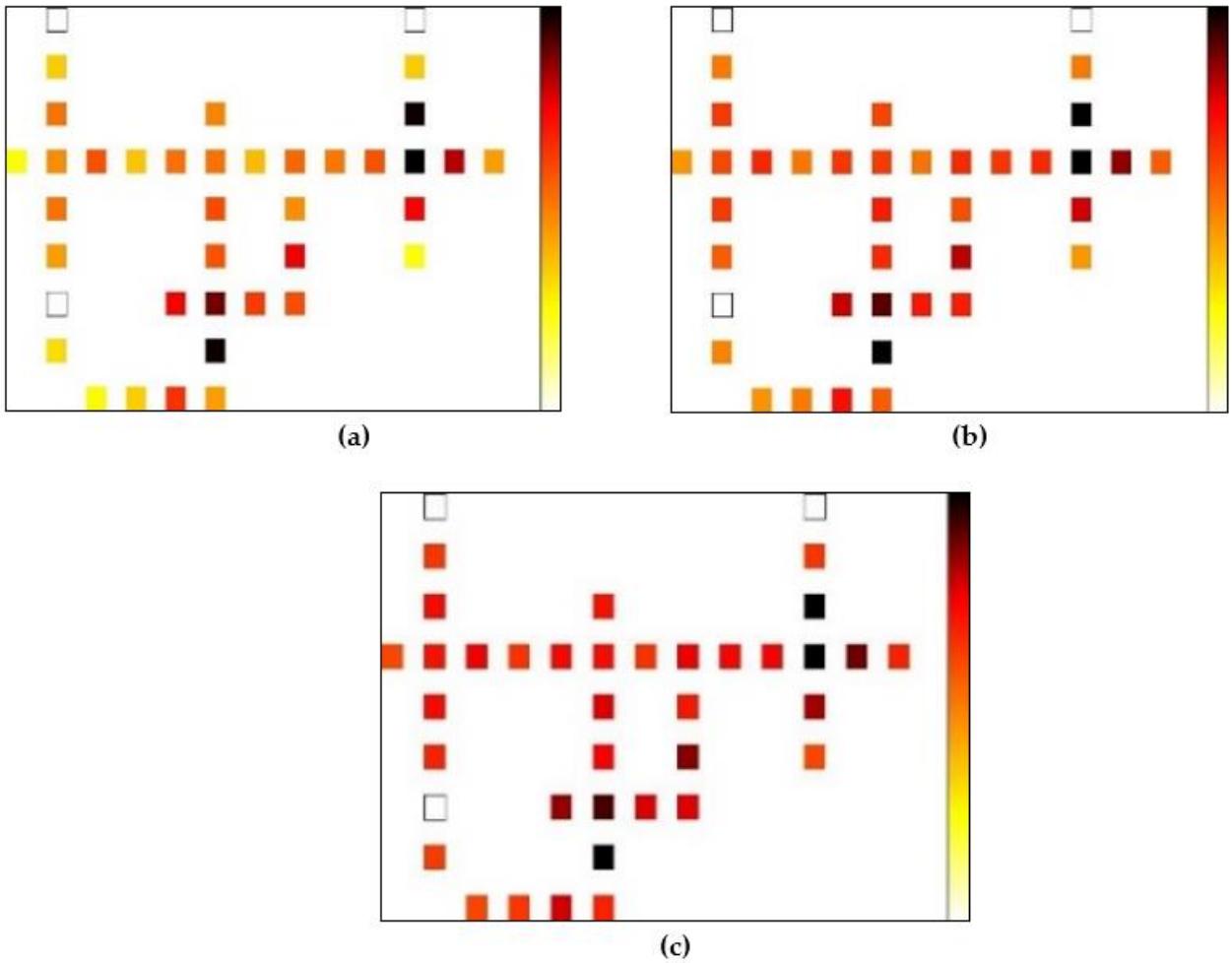


Figure 6. Energy dissipation map of the memory cell at (**a**) 0.5, (**b**) 1.0, and (**c**) 1.5 Ek levels.

Energy dissipation of the RAM cell was also calculated by simulations using the QCADesigner-E tool [35], which is an extension of the QCADesigner tool [33] and works on the principles discussed in [36–38]. It is found that total energy dissipation is 2.38×10^{-2} eV with an error of $\pm 2.38 \times 10^{-3}$ eV) and average energy dissipation per cycle is 2.16×10^{-3} eV with an error of $\pm 2.17 \times 10^{-4}$ eV.

Table 2 shows the performance of the memory cell proposed in this study and finds that the cost-effectiveness of the proposed design is evident. The proposed design has the least cell count of only 39 cells and 0.1035 QCA cost, which is much less than the previously reported designs. Furthermore, in Table 3, we can observe the performance improvement of up to 75.31% in cells utilized by the design, 75.34% in the area occupied by the cells, 71.25% in the total area utilized by the circuit, 62.5% in latency, and 92.95% in the cost of the QCA circuit.

Table 2. Performance Comparison of Memory Cell.

Design	Cell Count	Cell Area (μm^2)	Total Area (μm^2)	Latency	QCA Cost
Proposed	39	0.0126	0.046	1.5	0.1035
[23]	53	0.0168	0.052	1.5	0.117
[24]	55	0.0178	0.06	2.5	0.375
[25]	63	0.0204	0.092	4	1.472
[27]	75	0.0243	0.098	1.5	0.2205
[28]	87	0.0281	0.12	1.25	0.1875
[29]	87	0.0281	0.13	1.75	0.398
[30]	88	0.0285	0.08	1.5	0.18
[31]	109	0.0353	0.13	1.75	0.398
[32]	158	0.0511	0.16	2	0.64

Table 3. Performance Improvement of Proposed Memory Cell Compared to Existing Designs.

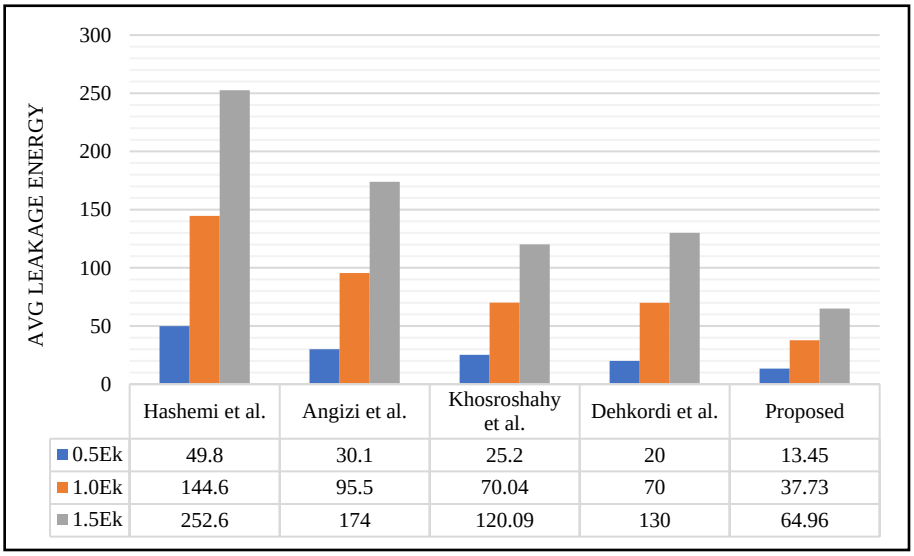
Design	Cell Count	Cell Area	Total Area	Latency	QCA Cost
[23]	26.41%	25%	11.53%	0%	11.53%
[24]	29.09%	29.21%	23.33%	40%	72.4%
[25]	38.09%	38.23%	50%	62.5%	92.96%
[27]	48%	48.14%	53.06%	0%	53.06%
[28]	55.17%	55.16%	61.66%	-20%	44.8%
[29]	55.17%	55.16%	64.61%	14.29%	73.99%
[30]	55.68%	55.78%	42.5%	0%	42.5%
[31]	64.22%	64.3%	64.61%	14.29%	73.99%
[32]	75.31%	75.34%	71.25%	25%	83.82%

Table 4 shows the performance analysis of throughput and power consumption for molecular and semiconductor QCA. The power consumption was calculated by dividing energy and time. For instance, the energy dissipation in the proposed design was 0.06 eV at 0.5 Ek, and 1 eV was equal to 1.60217×10^{-19} Ws. The theoretical frequency for molecular QCA is 1 THz, and 1 GHz for semiconductor QCA. Therefore, the power consumption was 0.961×10^{-8} W and 0.961×10^{-11} W for molecular and semiconductor QCA, respectively.

Table 4. Performance Comparison of Throughput and Power Consumption.

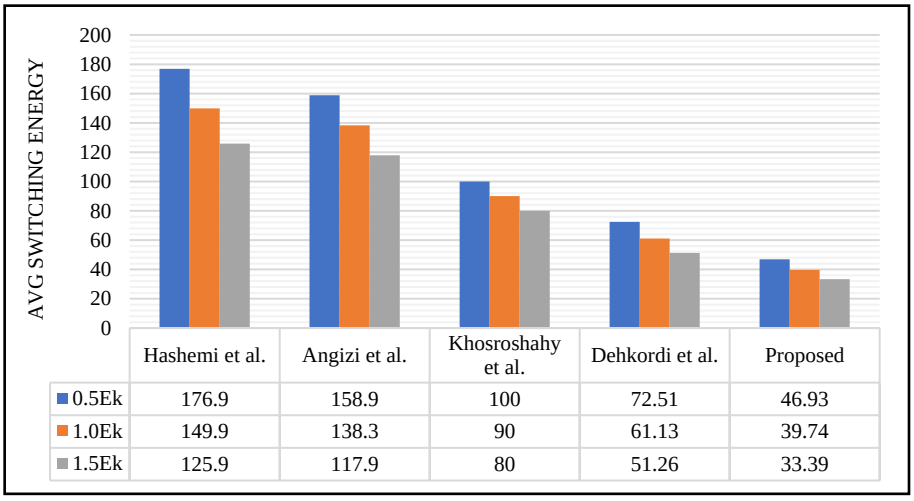
Design	Throughput (byte/sec)		Power Consumption	
	Semiconductor	Molecular	Semiconductor	Molecular
Proposed	42 MB/s	42 GB/s	0.961×10^{-11} W	0.961×10^{-8} W
[23]	42 MB/s	42 GB/s	3×10^{-10} W	3×10^{-7} W
[31]	36 MB/s	36 GB/s	3.633×10^{-11} W	3.633×10^{-8} W
[26]	36 MB/s	36 GB/s	1.56×10^{-11} W	1.56×10^{-8} W
[30]	32 MB/s	32 GB/s	3.02×10^{-11} W	3.02×10^{-8} W
[25]	16 MB/s	16 GB/s	1.92×10^{-11} W	1.92×10^{-11} W

The graphical comparison of the energy dissipation of the proposed memory cell is presented in Figure 7, which validates the low-power operation of the proposed QCA design. The improvement in energy dissipation is depicted in Table 5. Energy dissipation is reduced by up to 74.01% by the proposed design.



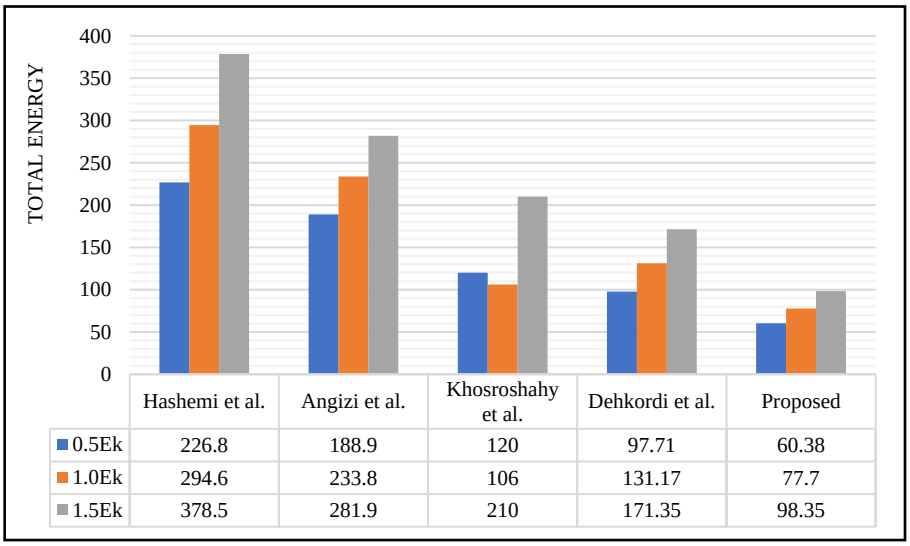
	Hashemi et al.	Angizi et al.	Khosroshahy et al.	Dehkordi et al.	Proposed
0.5Ek	49.8	30.1	25.2	20	13.45
1.0Ek	144.6	95.5	70.04	70	37.73
1.5Ek	252.6	174	120.09	130	64.96

(**a**)



	Hashemi et al.	Angizi et al.	Khosroshahy et al.	Dehkordi et al.	Proposed
0.5Ek	176.9	158.9	100	72.51	46.93
1.0Ek	149.9	138.3	90	61.13	39.74
1.5Ek	125.9	117.9	80	51.26	33.39

(**b**)



	Hashemi et al.	Angizi et al.	Khosroshahy et al.	Dehkordi et al.	Proposed
0.5Ek	226.8	188.9	120	97.71	60.38
1.0Ek	294.6	233.8	106	131.17	77.7
1.5Ek	378.5	281.9	210	171.35	98.35

(**c**)

Figure 7. Graphical comparison of (**a**) average leakage, (**b**) average switching dissipation, and (**c**) total energy dissipation (meV) of the memory cell at different kink energy levels with designs Hashemi et al. [31], Angizi et al. [30], Khosroshahy et al. [26], Dehkordi et al. [25].

Table 5. Performance Improvement of Energy Dissipated by Proposed Memory Cell.

Design	γ-Factor Level		
	0.5 Ek	1.0 Ek	1.5 Ek
[31]	73.37%	73.62%	74.01%
[30]	68%	66.76%	65.11%
[26]	49.68%	26.96%	53.16%
[25]	38.2%	40.76%	42.6%

7. Conclusions

In this study, an SRAM cell was proposed in QCA with low cell count, area, and QCA cost. It was coplanar in nature with high output polarization and validated using QCADesigner's coherence vector engine. A total of 39 cells were included in the design with a clock cycle latency of 1.5 cycles. An improvement of 25% in the cell count was achieved along with an 11.54% improvement in the area of the design and QCA cost, respectively achieved by the proposed design compared to the previously reported best design. In the future, this work can be extended further to design an M × N memory array with minimum latency to achieve a high speed of operation for different applications.

Author Contributions: Conceptualization, S.M.B. and P.S.; methodology, S.M.B. and S.A.; software, S.M.B. and S.A.; validation, S.A. and P.S.; formal analysis, A.N.B.; writing—original draft preparation, S.M.B. and S.A.; writing—review and editing, S.A., P.S., A.N.B., K.A.W. and A.O.; supervision, S.A. and P.S.; funding acquisition, A.O. All authors have read and agreed to the published version of the manuscript.

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References

1. Fazili, M.M.; Shah, M.F.; Naz, S.F.; Shah, A.P. Survey, taxonomy, and methods of QCA-based design techniques—Part II: Reliability and security. *Semicond. Sci. Technol.* **2022**, *37*, 063002. [CrossRef]
2. Lent, C.S.; Tougaw, P.D.; Porod, W.; Bernstein, G.H. Quantum cellular automata. *Nanotechnology* **1993**, *4*, 49. [CrossRef]
3. Lu, Y.; Liu, M.; Lent, C. Molecular quantum-dot cellular automata: From molecular structure to circuit dynamics. *J. Appl. Phys.* **2007**, *102*, 034311. [CrossRef]
4. Lu, Y.; Liu, M.; Lent, C. Molecular electronics-from structure to circuit dynamics. In Proceedings of the Sixth IEEE Conference on Nanotechnology, Cincinnati, OH, USA, 17–20 July 2006; pp. 62–65.
5. Frost, S.E.; Rodrigues, A.F.; Janiszewski, A.W.; Rausch, R.T.; Kogge, P.M. Memory in motion: A study of storage structures in QCA. In Proceedings of the First Workshop on Non-Silicon Computing, Cambridge, MA, USA, 3 February 2002; pp. 1–8.
6. Blair, E.P.; Yost, E.; Lent, C.S. Power dissipation in clocking wires for clocked molecular quantum-dot cellular automata. *J. Comput. Electron.* **2010**, *9*, 49–55. [CrossRef]
7. Ahmed, S.; Baba, M.I.; Bhat, S.M.; Manzoor, I.; Nafees, N.; Ko, S.-B. Design of reversible universal and multifunctional gate-based 1-bit full adder and full subtractor in quantum-dot cellular automata nanocomputing. *J. Nanophotonics* **2020**, *14*, 036002. [CrossRef]
8. Nafees, N.; Ahmed, S.; Kakkar, V.; Bahar, A.N.; Wahid, K.A.; Otsuki, A. QCA-Based PIPO and SIPO Shift Registers Using Cost-Optimized and Energy-Efficient D Flip Flop. *Electronics* **2022**, *11*, 3237. [CrossRef]
9. Almatrood, A.; George, A.K.; Singh, H. Low-Power Multiplexer Structures Targeting Efficient QCA Nanotechnology Circuit Designs. *Electronics* **2021**, *10*, 1885. [CrossRef]
10. Safoev, N.; Jeon, J.-C. Design and evaluation of cell interaction based vedic multiplier using quantum-dot cellular automata. *Electronics* **2020**, *9*, 1036. [CrossRef]
11. Yan, A.; Liu, R.; Huang, Z.; Girard, P.; Wen, X. Designs of Level-Sensitive T Flip-Flops and Polar Encoders Based on Two XOR/XNOR Gates. *Electronics* **2022**, *11*, 1658. [CrossRef]
12. Bahar, A.N.; Wahid, K.A. Design of an efficient N× N butterfly switching network in quantum-dot cellular automata (QCA). *IEEE Trans. Nanotechnol.* **2020**, *19*, 147–155. [CrossRef]

13. Seyedi, S.; Pourghebleh, B.; Jafari Navimipour, N. A new coplanar design of a 4-bit ripple carry adder based on quantum-dot cellular automata technology. *IET Circuits Devices Syst.* **2022**, *16*, 64–70. [CrossRef]
14. Enayati, M.; Rezai, A.; Karimi, A. Efficient circuit design for content-addressable memory in quantum-dot cellular automata technology. *SN Appl. Sci.* **2021**, *3*, 1–10. [CrossRef]
15. Mitic, M.; Cassidy, M.; Petersson, K.; Starrett, R.; Gauja, E.; Brenner, R.; Clark, R.; Dzurak, A.; Yang, C.; Jamieson, D. Demonstration of a silicon-based quantum cellular automata cell. *Appl. Phys. Lett.* **2006**, *89*, 013503. [CrossRef]
16. Agrawal, P.; Ghosh, B. Innovative design methodologies in quantum-dot cellular automata. *Int. J. Circuit Theory Appl.* **2015**, *43*, 253–262. [CrossRef]
17. Liu, M.; Lent, C.S. High-speed metallic quantum-dot cellular automata. In Proceedings of the Third IEEE Conference on Nanotechnology (IEEE-NANO), San Francisco, CA, USA, 12–14 August 2003; pp. 465–468.
18. Bhattacharjee, P.; Das, K.; De, M.; De, D. SPICE modeling and analysis for metal island ternary QCA logic device. In *Information Systems Design and Intelligent Applications*; Springer: Berlin/Heidelberg, Germany, 2015; Volume 339, pp. 33–41.
19. Vacca, M.; Graziano, M.; Zamboni, M. Majority voter full characterization for nanomagnet logic circuits. *IEEE Trans. Nanotechnol.* **2012**, *11*, 940–947. [CrossRef]
20. Alam, M.T.; DeAngelis, J.; Putney, M.; Hu, X.S.; Porod, W.; Niemier, M.; Bernstein, G.H. Clocking scheme for nanomagnet QCA. In Proceedings of the 7th IEEE Conference on Nanotechnology (IEEE-NANO), Hong Kong, China, 2–5 August 2007; pp. 403–408.
21. Pulimeno, A.; Graziano, M.; Sanginario, A.; Cauda, V.; Demarchi, D.; Piccinini, G. Bis-ferrocene molecular QCA wire: Ab initio simulations of fabrication driven fault tolerance. *IEEE Trans. Nanotechnol.* **2013**, *12*, 498–507. [CrossRef]
22. Liza, N.; Lu, Y.; Blair, E.P. Designing boron-cluster-centered zwitterionic Y-shaped clocked QCA molecules. *Nanotechnology* **2022**, *33*, 465201. [CrossRef]
23. Kianpour, M.; Sabbaghi-Nadooshan, R. A novel quantum-dot cellular automata X-bit x 32-bit SRAM. *IEEE Trans. Very Large Scale Integr. Syst.* **2015**, *24*, 827–836. [CrossRef]
24. Fam, S.R.; Navimipour, N.J. Design of a loop-based random access memory based on the nanoscale quantum dot cellular automata. *Photonic Netw. Commun.* **2019**, *37*, 120–130. [CrossRef]
25. Dehkordi, M.A.; Shamsabadi, A.S.; Ghahfarokhi, B.S.; Vafaei, A. Novel RAM cell designs based on inherent capabilities of quantum-dot cellular automata. *Microelectron. J.* **2011**, *42*, 701–708. [CrossRef]
26. Khosroshahy, M.B.; Moaiyeri, M.H.; Navi, K.; Bagherzadeh, N. An energy and cost efficient majority-based RAM cell in quantum-dot cellular automata. *Results Phys.* **2017**, *7*, 3543–3551. [CrossRef]
27. Sasamal, T.N.; Singh, A.K.; Ghanekar, U. Design and implementation of QCA D-flip-flops and RAM cell using majority gates. *J. Circuits Syst. Comput.* **2019**, *28*, 1950079. [CrossRef]
28. Heydari, M.; Xiaohu, Z.; Lai, K.K.; Afro, S. A cost-aware efficient RAM structure based on quantum-dot cellular automata nanotechnology. *Int. J. Theor. Phys.* **2019**, *58*, 3961–3972. [CrossRef]
29. Mubarakali, A.; Ramakrishnan, J.; Mavaluru, D.; Elsir, A.; Elsier, O.; Wakil, K. A new efficient design for random access memory based on quantum dot cellular automata nanotechnology. *Nano Commun. Netw.* **2019**, *21*, 100252. [CrossRef]
30. Angizi, S.; Sarmadi, S.; Sayedsalehi, S.; Navi, K. Design and evaluation of new majority gate-based RAM cell in quantum-dot cellular automata. *Microelectron. J.* **2015**, *46*, 43–51. [CrossRef]
31. Hashemi, S.; Navi, K. New robust QCA D flip flop and memory structures. *Microelectron. J.* **2012**, *43*, 929–940. [CrossRef]
32. Walus, K.; Vetteth, A.; Jullien, G.; Dimitrov, V. RAM design using quantum-dot cellular automata. In Proceedings of the Nanotechnology Conference, San Francisco, CA, USA, 23–27 February 2003; pp. 160–163.
33. Walus, K.; Dysart, T.J.; Jullien, G.A.; Budiman, R.A. QCADesigner: A rapid design and simulation tool for quantum-dot cellular automata. *IEEE Trans. Nanotechnol.* **2004**, *3*, 26–31. [CrossRef]
34. Srivastava, S.; Asthana, A.; Bhanja, S.; Sarkar, S. QCAPro-an error-power estimation tool for QCA circuit design. In Proceedings of the IEEE international symposium of circuits and systems (ISCAS), Rio de Janeiro, Brazil, 15–18 May 2011; pp. 2377–2380.
35. Torres, F.S.; Wille, R.; Niemann, P.; Drechsler, R. An energy-aware model for the logic synthesis of quantum-dot cellular automata. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* **2018**, *37*, 3031–3041. [CrossRef]
36. Timler, J.; Lent, C.S. Power gain and dissipation in quantum-dot cellular automata. *J. Appl. Phys.* **2002**, *91*, 823–831. [CrossRef]
37. Timler, J.; Lent, C.S. Maxwell's demon and quantum-dot cellular automata. *J. Appl. Phys.* **2003**, *94*, 1050–1060. [CrossRef]
38. Lent, C.S.; Liu, M.; Lu, Y. Bennett clocking of quantum-dot cellular automata and the limits to binary logic scaling. *Nanotechnology* **2006**, *17*, 4240. [CrossRef] [PubMed]