electronics

Article

Integrated Circuit Design of Fractional-Order Chaotic Systems Optimized by Metaheuristics

Martin Alejandro Valencia-Ponce [1,†], Astrid Maritza González-Zapata [1,†], Luis Gerardo de la Fraga [2,†], Carlos Sanchez-Lopez [3,†] and Esteban Tlelo-Cuautle [1,*,†]

[1] Department of Electronics, INAOE, Luis Enrique Erro No. 1, Tonantzintla, Puebla 72840, Mexico
[2] Computer Science Department, CINVESTAV, Av. IPN 2508, Mexico City 07360, Mexico
[3] Department of Electronics, UATx, Av. Universidad No. 1, Tlaxcala 90070, Mexico
* Correspondence: etlelo@inaoep.mx; Tel.: +52-222-2663100
† These authors contributed equally to this work.

Abstract: Nowadays, a huge amount of research is done on introducing and implementing new fractional-order chaotic systems. In the majority of cases, the implementation is done using embedded hardware, and very seldom does it use integrated circuit (IC) technology. This is due to the lack of design automation tools ranging from the system level down to layout design. At the system level, the challenge is guaranteeing chaotic behavior by varying all parameters while optimizing dynamical characteristics, such as the Lyapunov spectrum and the Kaplan–Yorke dimension. Using embedded hardware, the implementation is straightforward, but one must perform a scaling process for IC design, in which the biases may be lower than 1 volt but the amplitudes of the state variables of the chaotic systems can have values higher than one. In this manner, this paper describes three levels of abstraction to design fractional-order chaotic systems: The first one shows the optimization of a case study, the mathematical model of the fractional-order Lorenz system to find the fractional-orders of the derivatives, and the coefficients that generate better chaotic behavior. The second level is the block description of a solution of the mathematical model, in which the fractional-order derivatives are approximated in the Laplace domain by several approximation methods. The third level shows the IC design using complementary metal–oxide–semiconductor (CMOS) technology. The transfer functions approximating the fractional-order derivatives are synthesized by active filters that are designed using operational transconductance amplifiers (OTAs). The OTAs are also used to design adders and subtractors, and the multiplication of variables is done by designing a CMOS four-quadrant multiplier. The paper shows that the simulation results scaling the mathematical model to have amplitudes lower than ±1 are in good agreement with the results using CMOS IC technology of 180 nm.

Keywords: chaos; CMOS design; operational transconductance amplifier; fractional-order derivative; active filter; particle swarm optimization

Citation: Valencia-Ponce, M.A.; González-Zapata, A.M.; de la Fraga, L.G.; Sanchez-Lopez, C.; Tlelo-Cuautle, E. Integrated Circuit Design of Fractional-Order Chaotic Systems Optimized by Metaheuristics. *Electronics* **2023**, *12*, 413. https://doi.org/10.3390/electronics12020413

Academic Editors: Fábio Passos, Nuno Lourenço and Ricardo Martins

Received: 23 November 2022
Revised: 30 December 2022
Accepted: 11 January 2023
Published: 13 January 2023

1. Introduction

There is a wide variety of natural phenomena in science and engineering applications that exhibit chaotic behavior, whose main property is a high sensitivity to initial conditions. Such phenomena can be modeled by integer or fractional-order chaotic systems, and their randomness can be exploited to develop engineering applications. In particular, the electronic design of chaotic systems is generally performed using embedded systems, such as field-programmable gate arrays (FPGAs), due to its popularity for fast prototyping. It has also been shown that the mathematical models of either integer or fractional-order chaotic systems can be optimized to generate better chaotic behavior, as shown in [1], where the authors show how the optimized models can be implemented using commercially available amplifiers, field-programmable analog arrays (FPAA), FPGAs, micro-controllers,

and nanometer technology of integrated circuits (ICs). The big challenge is the development of an electronic design automation (EDA) tool with the capabilities of optimizing the mathematical model, macro-modeling of the chaotic system, and designing of the blocks using complementary metal–oxide–semiconductor (CMOS) IC technology. In this manner, this paper summarizes recent advances on the development of EDA tools for analog design of chaotic systems that require the design of filters, adders, subtractors, multipliers, and comparators. A case study is given to show the optimization, block description, and CMOS design of a fractional-order chaotic system.

Recently developed EDA tools perform the design of electronic systems in a hierarchical fashion, as shown in [2], where the authors cover the device, circuit, and system levels for radio-frequency ICs. This is a big problem known as physical design that requires a massive amount of computer resources in order to meet the tape-out schedule [3] and to mainly accomplish target specifications that support process variations, for instance. Some works introduce systematic and multilevel approaches [4], and others pay special attention to the placement of the circuit blocks [5,6]. Modern EDA tools include optimization [7,8] and machine learning [9]. These combinations of design methods allow one to guarantee the layout generation [10], which sometimes requires one to have the lowest silicon area [11–13]. The authors of [14] introduced the automated design of analog circuits, whose algorithm not only successfully reaches unique, valid, and practical performances, but also does so in state-of-the-art run time, achieving target specifications post-layout for the folded cascode amplifier. Such a task was also performed by some authors applying multi-objective optimization algorithms [15–17], and recently by applying many-objective algorithms [18]. Those EDA tools include process variations and statistical analyses to guarantee robust design. Others put emphasis on the layout generation [19] and yield-aware optimization in nanometer-scale technologies [20]. These EDA tools inspired this work to use three levels of abstraction to design fractional-order chaotic systems: The first one is devoted to showing the application of metaheuristics to find the coefficients and the fractional-orders of the derivatives that generate better chaotic behavior from a mathematical model. The second level is the block description of the mathematical model, in which the fractional-order derivatives are approximated in the Laplace domain. The third level shows the IC design using CMOS technology of 180 nm.

Researchers involved in real applications of chaotic systems, such as the design and synchronization of random number generators (RNGs) [21], generally use FPGAs to verify the generation of a chaotic attractor, as already shown in [1,22–24]. However, for low power consumption and wireless applications, the design of CMOS ICs is recommended, as they can be fabricated in a very-low silicon environment. The CMOS design of chaotic systems is not new; it was done three decades ago for the introduction of the IC chip of Chua's circuit [25], using 2 μm technology, occupying a silicon area of 2.5 mm $\times$ 2.8 mm, and biased with a single 9V battery. The authors highlighted that the CMOS IC can be employed as a basic component in the design of complex circuits making use of chaotic signals, including a class of cellular neural networks and secure communication systems. By the same time, the authors of [26], introduced a CMOS IC design of a chaotic discrete-time system for the generation of broadband white noise using 3 μm technology. From recent times, one can find CMOS designs of chaotic systems using CMOS technology of 180 nm, provided from different fabrication companies [27–32]. These IC designs can be improved by performing variation analyses of the process (voltage and temperature) and Monte Carlo simulations [33]. Further, those robust designs can be used to design random number generators [34,35], which have shown real engineering applications, such as for the design of a CMOS high-data-rate true random bit generator through delta sigma modulation [36]. Other applications of CMOS chaotic systems are the design of high-precision analog-to-digital converter (ADC) calibration systems [37], a 1 Gbps chaos-based stream cipher [38], and a chaos-key based data encryption system, in which the data secrecy is compared to the advanced encryption standard (AES) [39]. Regarding fractional-order

chaotic systems, there have been very few trials generating CMOS designs, as shown in [18,40,41].

The organization of the paper is as follows: Section 2 shows the adaptation of an optimization algorithm to fractional-order chaotic systems, Section 3 shows the approximation of the fractional-order derivatives in the Laplace domain, Section 4 shows the CMOS design of a fractional-order chaotic system, and Section 5 summarizes the results and shows the suitability for the development of an EDA tool for the design of CMOS fractional-order chaotic systems. Finally, the conclusions are given in Section 6.

2. Simulation and Optimization of Fractional-Order Chaotic Systems

This section shows the optimization of two chaotic systems taken as case studies, namely, those of Chen and Liu [42]. They are fractional-order Lorenz-type systems. Each system is optimized to maximize the chaotic characteristic known as the Kaplan–Yorke dimension (D_{KY}) by applying the particle swarm optimization (PSO) algorithm.

2.1. Optimization of Chaotic Systems by PSO

As already shown in [1], every chaotic system can be optimized in its dynamical characteristics, e.g., by maximizing the positive or maximum Lyapunov exponent and D_{KY}. Afterwards, one can implement the optimized systems using commercially available electronic devices, FPAAs, FPGAs, and micro-controllers, or by designing an IC using CMOS nanometer technology, as shown here. All these tasks can be automated to develop an EDA tool ad hoc for fractional-order chaotic systems. In addition, the first challenge is determining whether or not a mathematical model generates chaotic behavior. To that end, the authors of [43] introduced a method based on the Fourier transform to evaluate if the generated time series is chaotic or not. The Fourier spectrum of a chaotic time series has several peaks surpassing a determined threshold, and they are not multiples of a fundamental frequency, as happens for a periodic signal. Evaluating the Fourier spectrum of a time series saves computing time in an optimization loop, and therefore, not all the time series are used to evaluate dynamical characteristics as Lyapunov exponents and D_{KY}, which can be performed by using the free time-series analysis (TISEAN) software. The dynamical characteristics are evaluated, generating about 30,000 data points from a mathematical model, but the transient must be eliminated, and it associates with the first 10,000 data. In this manner, a chaotic system can be optimized by maximizing Lyapunov exponents and D_{KY} using TISEAN within PSO. The majority of people agree that PSO is an easy algorithm to implement, and we provide the main pseudocode for the optimization of fractional-order chaotic systems. PSO consists of a set of n possible solutions called particles, which represents a potential solution in D-dimensional space [44]. It requires the definition of the population size N_p and the number of generations G in which the potential solutions are evolved, and the algorithm is calibrated until generating good, feasible solutions.

From a mathematical model of a fractional-order chaotic system, the derivatives have fractional-order values that can be a fraction of unity. In this work, the fractional-orders are considered to be in the range $[0.3, 0.9]$ and can vary in steps of 0.1. During the optimization task, the coefficients and fractional-orders of the derivatives are the design variables, for which random values are generated within PSO, and their associated time series are analyzed with the Fourier spectrum [43] to determine if they can go to TISEAN to evaluate D_{KY}. The iterations within PSO are performed until a determined number of generations, and the last particles are saved and considered feasible solutions.

The pseudocode of PSO is given in Algorithm 1. It begins by initializing a random population, and the speed and position of each particle are updated according to (1) and (2) [45]. In these equations, i is the index of the particle, j its dimension, p_i the best position found

for it initially, and p_g the best position found during the optimization [43]. In this work: $c_1 = 0.5$, $c_2 = 0.9$, $N_p = 30$ (population), and $G = 10$ (number of generations).

$$v_{ij} = v_{ij} + c_1 \text{rand}()(p_{ij} - x_{ij}) + c_2 \text{rand}()(g_j - x_{ij}) \quad (1)$$

$$x_{ij} = x_{ij} + v_{ij} \quad (2)$$

Algorithm 1 Optimization of a fractional-order chaotic system by PSO.

1: Initialize the first particle i of the population N_p with known parameters, and the rest randomly $(\mathbf{x})$
2: Initialize the velocity of the particles vs.
3: **for** $(counter = 1; counter \leq G; counter + +)$ **do**
4: **for** $(i = 1; i \leq N_p; i + +)$ **do**
5: **for** $(j = 1; j \leq D; j + +)$ **do**
6: **if** the sum of the fractional order of all particles is ≥ 2.1 **then**
7: Evaluate the position of the particles to find the eigenvalues.
8: **if** at least one eigenvalue is greater than zero, **then**
9: Evaluate the position of the particles to generate the chaotic time series.
10: Calculate the Fourier transform of the time series.
11: **if** Fourier amplitude $>$ Range **then**
12: Evaluate D_{KY}
13: Initialize the particle's best position $p_i \leftarrow x_i$
14: **else**
15: Do not calculate D_{KY} because the system is not chaotic.
16: $D_{KY} = 0$.
17: **end if**
18: **else**
19: Evaluate the next particle, go to step 26.
20: $D_{KY} = 0$.
21: **end if**
22: **else**
23: Evaluate the next particle, go to step 26.
24: $D_{KY} = 0$.
25: **end if**
26: Evaluate the new velocity using (1)
27: Evaluate the new position using (2)
28: **end for**
29: $f_x \leftarrow func(x_i)$
30: **if** f_x is better than $score_i$ **then**
31: $score_i \leftarrow f_x$
32: $p_i \leftarrow x_i$
33: **if** p_i is better than g **then**
34: $g \leftarrow p_i$
35: **end if**
36: **end if**
37: **end for**
38: **end for**
39: **return** x, p, g and $score$

2.2. Optimization of the Fractional-Order Chen System

The fractional-order Chen system is given in (3). According to [42], it is a Lorenz-type system that generates chaotic behavior by setting $a = 35$, $b = 3$, and $c = 28$, with commensurate fractional-order equal to $q_1 = q_2 = q_3 = 0.9$. The simulation of this system and using initial conditions $x_0 = -9, y_0 = -5, z_0 = 14$, led us to generate the chaotic attractor shown in Figure 1. As one can see, the amplitudes of the state variables are higher than

20, but for a CMOS design, it is required to be in the range of about ± 1, which can be accomplished by scaling the optimized values of the mathematical model, as shown in the following section.

$$\begin{aligned} D_t^{q_1} x(t) &= a(y(t) - x(t)) \\ D_t^{q_2} y(t) &= (c - a)x(t) - x(t)z(t) + cy(t) \\ D_t^{q_3} z(t) &= x(t)y(t) - bz(t) \end{aligned} \tag{3}$$

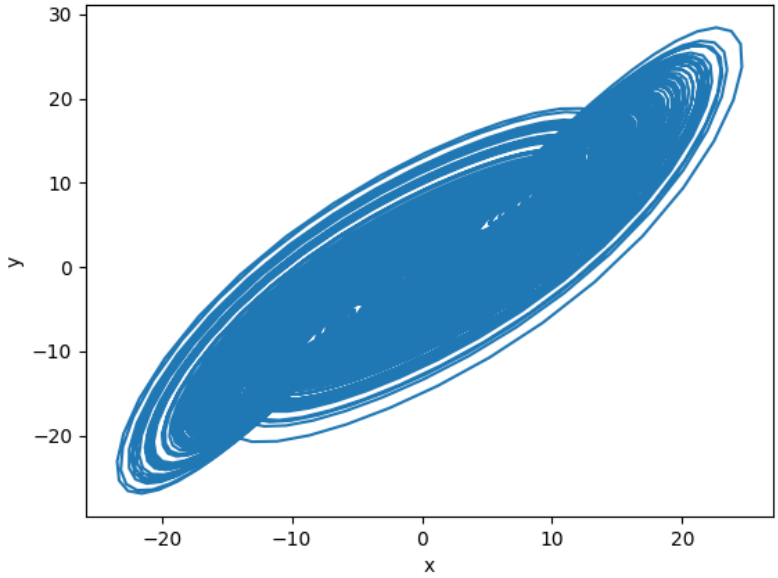


Figure 1. Chen attractor generated from (3) by setting $a = 35$, $b = 3$, $c = 28$, and $q_1 = q_2 = q_3 = 0.9$, and using initial conditions $x_0 = -9, y_0 = -5$, and $z_0 = 14$.

The execution of PSO with a population of 30 particles and evolved during 10 generations for the maximization of D_{KY} provided the five solutions given in Table 1. As one can see, the fractional orders are 0.8 and 0.9 to have a D_{KY} higher than 2.2240, which is the value evaluated by TISEAN using the non-optimized parameters, the original ones, and the optimal solutions have values somewhat similar to the original coefficients a, b, c. The fractional orders of the derivatives are approximated in the Laplace domain in the following section.

Table 1. Five solutions of the optimization of Chen system (3) applying PSO.

Parameter	a	b	c	q_1	q_2	q_3	D_{KY}
Original	35	3	28	0.9	0.9	0.9	2.2240
Solution 1	34.5379	2.4909	28.4066	0.9	0.9	0.9	2.2859
Solution 2	33.5356	3.1781	28.2312	0.8	0.8	0.9	2.3091
Solution 3	34.3726	3.0313	27.8618	0.9	0.9	0.9	2.2721
Solution 4	33.5929	3.2233	28.7034	0.8	0.8	0.9	2.3506
Solution 5	33.3714	3.3152	28.4679	0.8	0.8	0.9	2.3333

2.3. Optimization of the Fractional-Order Liu System

The fractional-order Liu system is given in (4). It was simulated to generate the attractor shown in Figure 2, by setting $a = 10, b = 2.5, c = 40$, $k = 1$, $h = 4$, and $q_1 = q_2 = q_3 = 0.9$; and using initial conditions $x_0 = 0.2, y_0 = 0.3$, and $z_0 = 0.5$. The time series were introduced to TISEAN to evaluate $D_{KY} = 2.1917$. Five optimal solutions are given in Table 2, where it can be appreciated that the fractional orders are 0.8 and 0.9, and the values of the coefficients are slightly similar to the original ones, but D_{KY} has been

increased. The fractional orders of the derivatives are approximated in the Laplace domain in the following section.

$$\begin{aligned} D_t^{q_1} x(t) &= a(y(t) - x(t)) \\ D_t^{q_2} y(t) &= cx(t) - kx(t)z(t) \\ D_t^{q_3} z(t) &= -bz(t) + hx^2(t) \end{aligned} \tag{4}$$

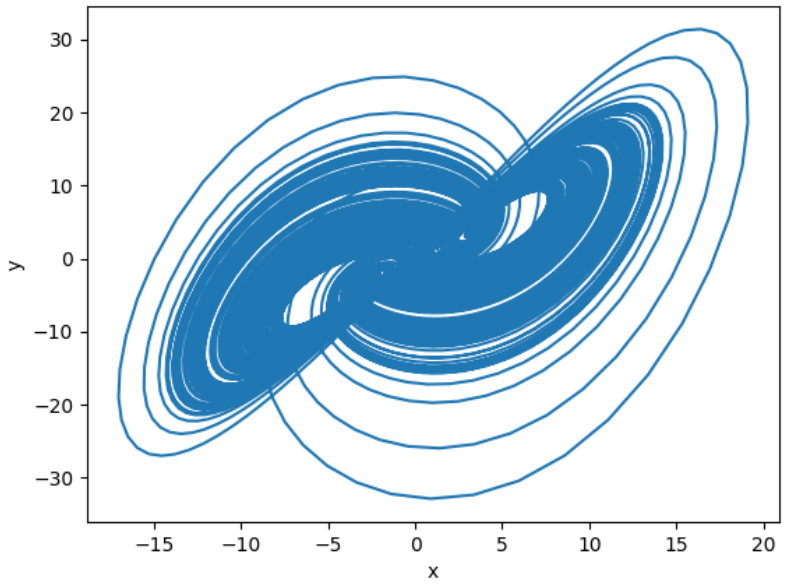


Figure 2. Liu attractor generated from (4) by setting $a = 10, b = 2.5, c = 40$, $k = 1$, $h = 4$, and $q_1 = q_2 = q_3 = 0.9$; and using initial conditions $x_0 = 0.2, y_0 = 0.3$, and $z_0 = 0.5$.

Table 2. Five solutions of the optimization of Liu system (4) applying PSO.

Parameter	a	b	c	k	h	q_1	q_2	q_3	D_{KY}
Original	10	2.5	40	1	4	0.9	0.9	0.9	2.1917
Solution 1	9.413323	2.322034	40.139001	1.029814	4.008886	0.8	0.8	0.8	2.2331
Solution 2	9.724684	2.436013	39.808277	0.987385	4.017011	0.8	0.8	0.8	2.3304
Solution 3	9.770579	2.615027	39.844751	1.094766	4.054294	0.9	0.9	0.8	2.2505
Solution 4	10.057213	2.985930	40.071543	0.890802	3.873207	0.9	0.9	0.8	2.2444
Solution 5	10.069213	2.877164	39.450604	0.829341	4.084662	0.9	0.9	0.8	2.2419

3. Frequency Approximation of the Fractional-Order Chaotic Systems

This section shows the amplitude scaling of Chen and Liu fractional-order systems to allow CMOS design. Taking an optimal solution given in the previous section, one can see the fractional orders of the derivatives as 0.8 and 0.9; these orders are approximated herein, and therefore, the scaled attractors are shown for the Chen and Liu systems.

3.1. Scaling the Amplitudes of the Chen System

The CMOS design performed in the following section requires that the state variables have amplitudes of ± 1 or smaller. In this manner, the amplitude scaling is done by changing variables. In this case, we propose (5) to be replaced in (3). It introduces k_1, k_2, and k_3 that update the Chen system as in (6). By setting $k_1 = 45, k_2 = 50$, and $k_3 = 70$, the new amplitudes of the state variables are shown in Figure 3; as one can see, they are lower than ± 0.6. By reordering (6), one gets (7), where $\frac{ak_2}{k_1} = m$, $(c-a)\frac{k_1}{k_2} = n$, $\frac{k_1 k_3}{k_2} = p$, and $\frac{k_1 k_2}{k_3} = r$.

$$\begin{aligned} x(t) &= k_1 u(t) \\ y(t) &= k_2 v(t) \\ z(t) &= k_3 w(t) \end{aligned} \tag{5}$$

$$\begin{aligned} D_t^{q_1}u(t) &= \tfrac{ak_2}{k_1}v(t) - au(t) \\ D_t^{q_2}v(t) &= (c-a)\tfrac{k_1}{k_2}u(t) - \tfrac{k_1k_3}{k_2}w(t) + cv(t) \\ D_t^{q_3}w(t) &= \tfrac{k_1k_2}{k_3}u(t)v(t) - bw(t) \end{aligned} \tag{6}$$

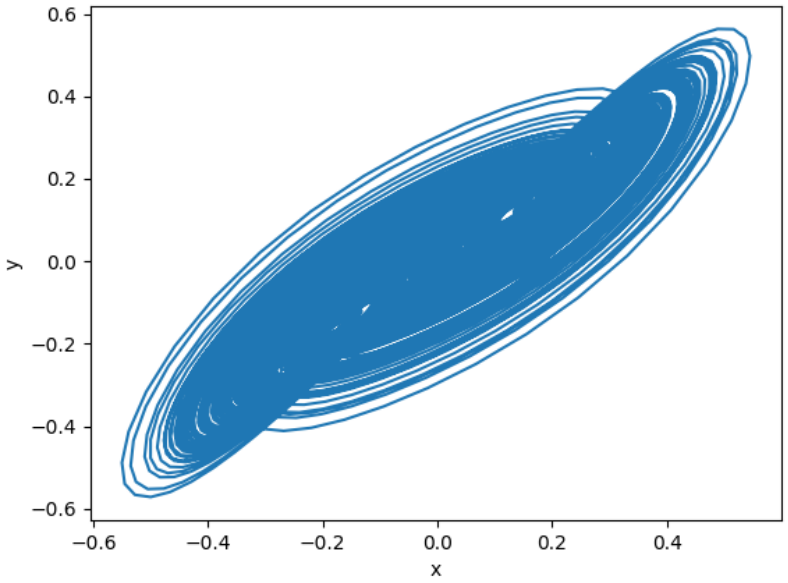


Figure 3. Chen attractor after scaling to allow CMOS design.

$$\begin{aligned} D_t^{q_1}u(t) &= mv(t) - au(t) \\ D_t^{q_2}v(t) &= nu(t) - pw(t) + cv(t) \\ D_t^{q_3}w(t) &= ru(t)v(t) - bw(t) \end{aligned} \tag{7}$$

The scaling parameters m, n, p, r introduced by (7) do not modify the D_{KY} values, as shown in Table 3, and now, one can appreciate the maximum amplitude values of the state variables x, y, and z that are lower values than ± 1, so that they allow a CMOS design, as shown in the following section.

Table 3. The scaling parameters m, n, p, and r introduced by (7) provide maximum amplitudes of x, y, and z within ± 0.71, while maintaining the values of the associated D_{KY}.

Param.	*a*	*b*	*c*	*m*	*n*	*p*	*r*	Max *x*	Max *y*	Max *z*	D_{KY}
Original	35	3	28	38.89	−6.3	63	32.14	0.55	0.57	0.64	2.2397
Solution 1	34.53	2.49	28.41	38.37	−5.51	63	32.14	0.56	0.59	0.68	2.2973
Solution 2	33.53	3.17	28.23	37.26	−4.77	63	32.14	0.65	0.69	0.68	2.3153
Solution 3	34.37	3.03	27.86	38.19	−5.86	63	32.14	0.57	0.59	0.66	2.2748
Solution 4	35.59	3.22	28.70	37.32	−4.4	63	32.14	0.66	0.71	0.71	2.3303
Solution 5	33.37	3.31	28.46	37.08	−4.42	63	32.14	0.65	0.70	0.69	2.3329

3.2. Scaling the Amplitudes of Liu System

The scaling of Liu system is performed by replacing (5) in (4), thereby providing (8). In a similar way, the parameters are reordered as: $m = \frac{ak_2}{k_1}$, $n = \frac{ck_1}{k_2}$, $p = \frac{kk_1k_3}{k_2}$, $r = \frac{hk_1^2}{k_3}$, giving (9). Table 4, shows the scaled values using initial conditions equal to $x_0 = 0.2$, $y_0 = 0.3$ and $z_0 = 0.5$. Figure 4, shows the scaled values of the Liu attractor.

$$\begin{aligned} D_t^{q_1}u(t) &= \tfrac{ak_2}{k_1}v(t) - au(t) \\ D_t^{q_2}v(t) &= \tfrac{ck_1u(t)}{k_2} - \tfrac{kk_1k_3u(t)w(t)}{k_2} \\ D_t^{q_3}w(t) &= -bw(t) + \tfrac{hk_1^2u^2(t)}{k_3} \end{aligned} \tag{8}$$

$$\begin{aligned} D_t^{q_1} u(t) &= mv(t) - au(t) \\ D_t^{q_2} v(t) &= nu(t) - pu(t)w(t) \\ D_t^{q_3} w(t) &= -bw + ru^2(t) \end{aligned} \tag{9}$$

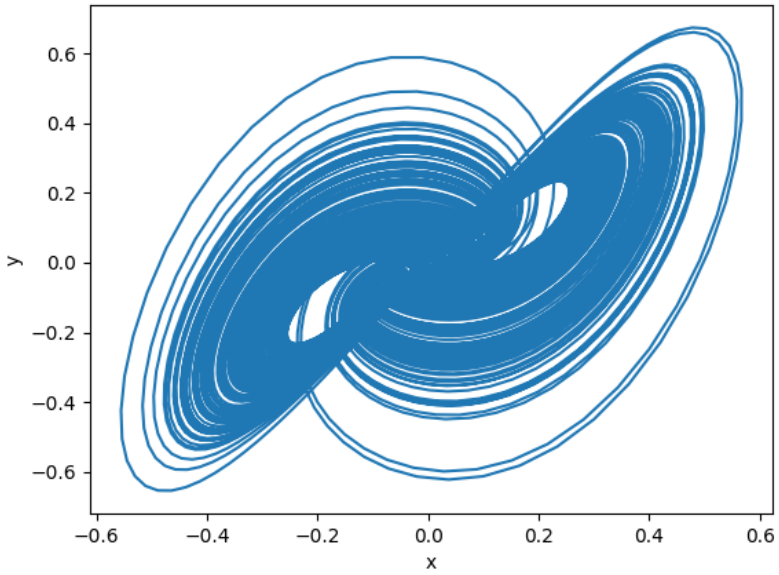


Figure 4. Liu attractor after scaling to allow CMOS design.

Table 4. The scaling parameters m, n, p, r introduced by (9) provide maximum amplitudes of x, y, z within ± 0.74, while maintaining the values of the associated D_{KY}.

Param.	a	b	c	k	h	m	n	p	r	Max x	Max y	Max z	D_{KY}
Orig.	10	2.5	40	1	4	13.33	30.0	105.0	25.71	0.57	0.67	0.70	2.1938
Sln. 1	9.41	2.32	40.14	1.03	4.01	12.55	30.11	108.15	25.78	0.46	0.56	0.54	2.2169
Sln. 2	9.72	2.44	39.81	0.99	4.02	12.96	29.86	103.95	25.84	0.47	0.57	0.55	2.2211
Sln. 3	9.77	2.62	39.84	1.09	4.05	13.03	29.88	114.45	26.04	0.44	0.52	0.56	2.2392
Sln. 4	10.06	2.99	40.07	0.89	3.87	13.41	30.05	93.45	24.88	0.51	0.59	0.67	2.2304
Sln. 5	10.07	2.88	39.45	0.83	4.08	13.43	29.59	87.15	26.23	0.52	0.61	0.74	2.2331

The scaled values of the parameters listed in Tables 3 and 4 must be tested to choose the one with the lowest sensitivity, which is correlated with the CMOS implementation given in the following section.

3.3. Approximation of the Fractional-Order Derivatives in the Laplace Domain

Lets us consider the fractional order chaotic system given by (10) [32]. The scaled system has the parameters $a = 0.35$, $b = 0.03$, and $c = 0.28$; and its simulation with initial conditions $x_0 = y_0 = z_0 = 0.1$ produces amplitudes of the state variables within ± 0.5, as shown in Figure 5.

$$\begin{aligned} s^{0.8} X(s) &= a(Y(s) - X(s)) \\ s^{0.8} Y(s) &= (c - a)X(s) - X(s) * Z(s) + cY(s) \\ s^{0.9} Z(s) &= X(s) * Y(s) - bZ(s) \end{aligned} \tag{10}$$

By describing (10), one can infer the use of amplifiers, adders, subtractors, and multipliers. In addition, two fractional-order integrators are also necessary; they have fractional-orders of 0.8 and 0.9, which can be approximated in the Laplace domain by applying Charef's method [46], so that (11) describes $H_1(s) = 1/s^{0.8}$ and (12) describes $H_2(s) = 1/s^{0.9}$. These transfer functions are suitable to be designed in CMOS IC technology, as shown in the following section.

$$H_1(s) = \frac{1}{s^{0.8}} \approx \frac{5.3088(s + 0.1334)(s + 2.371)(s + 42.17)(s + 749.9)}{(s + 0.01334)(s + 0.2371)(s + 4.217)(s + 74.99)(s + 1334)} \tag{11}$$

$$H_2(s) = \frac{1}{s^{0.9}} \approx \frac{2.2675(s+1.292)(s+215.4)}{(s+0.01292)(s+2.154)(s+359.4)} \tag{12}$$

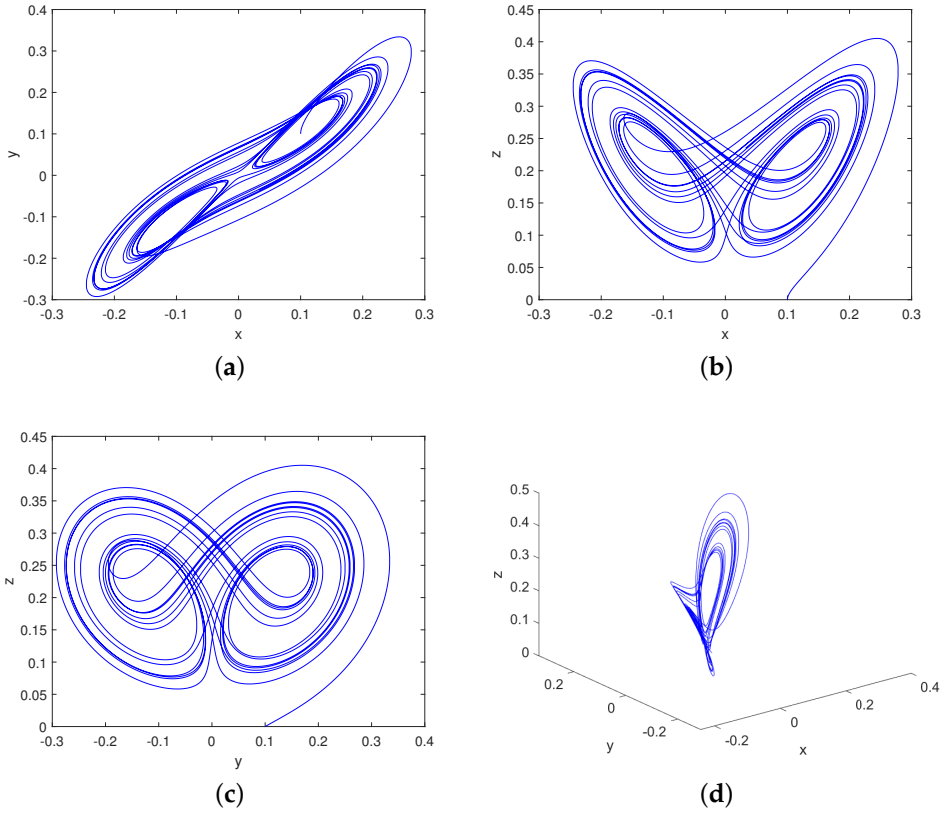
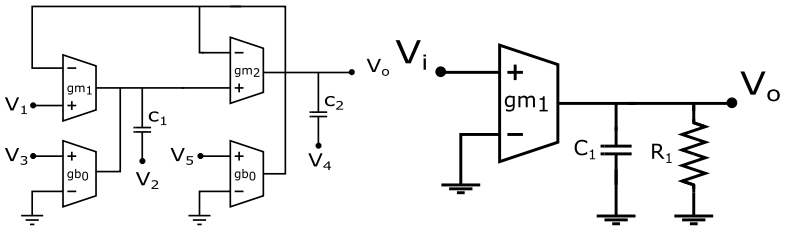


Figure 5. Portraits of the chaotic Chen system given in (10), by setting $a = 0.35$, $b = 0.03$, and $c = 0.28$, and using initial conditions $x_0 = y_0 = z_0 = 0.1$. (**a**) x-y, (**b**) x-z, (**c**) y-z, and (**d**) x-y-z planes.

4. CMOS Design of a Fractional-Order Chaotic System

This section shows the CMOS design of the fractional-order integrators to implement Chen system given in (10) that was proposed by [32]. As shown above, in order to design a CMOS IC, the coefficients are set to: $a = 0.35$, $b = 0.03$, and $c = 0.28$ to reduce the amplitudes of the state variables to be within ± 1 or lower. As observed in Figure 5, the portraits show amplitudes of around ± 0.5, good enough to design the fractional-order Chen system using CMOS technology of 180nm from UMC. The first step of the design process is the synthesis of the fractional-order integrators that have been proposed in [47] and given in (11) and (12). Both fractional-order integrators can now be approximated by using bi-quadratic and low-pass filters, which are shown in Figure 6a and Figure 6b, respectively, and the topologies use operational transconductance amplifiers (OTAs). These OTA-based filters are taken from [48], which have the transfer functions given in (13) for the bi-quadratic filter, and (14) for the low-pass filter.



(**a**) Bi-quadratic filter. (**b**) Low-pass filter.

Figure 6. OTA-based active filters.

$$Vo = \frac{\frac{gm_1gm_2}{C_1C_2}V_1 + s\frac{gm_2}{C_2}V_2 + \frac{gb_0gm_2}{C_1C_2}V_3 + s^2V_4 + s\frac{gb_1}{C_2}V_5}{s^2 + \frac{gm_2}{C_2}s + \frac{gm_1gm_2}{C_1C_2}} \tag{13}$$

$$Vo = \frac{gm_1/C}{s + gm_2/C}Vi \tag{14}$$

The transfer function given in (11) approximates the fractional-order integrator $H_1(s) = 1/s^{0.8}$. As the denominator is of order five, it can be separated into two functions of second-order, and one of first-order. In this manner, (11) can be decomposed by the functions given in the right-hand sides of (15)–(17), which are synthesized by the OTA-based active filters as follows.

In (13), one can set $V_1 = V_2 = 0$ and $V_3 = V_4 = V_5 = V_i$, so that the resulting transfer function of the circuit shown in Figure 6a can be described by (15), which is associated with the first second order transfer function taken from (11). If $gb_0 = gb_1 = 500$ µA/V, then $C_2 = gb_1/2.50 = 200$ µF and $gm_2 = 4.45C_2 = 886$ µA/V. Additionally, $C_1 = gb_0gm_2/0.31C_2 = 7.4$ mF and $gm_1 = 0.99C_1C_2/gm_2 = 1.58$ mA/V.

$$H(s) = \frac{s^2 + \frac{gb_1}{C_2}s + \frac{gb_0gm_2}{C_1C_2}}{s^2 + \frac{gm_2}{C_2}s + \frac{gm_1gm_2}{C_1C_2}} = \frac{s^2 + 2.50s + 0.31}{s^2 + 4.45s + 0.99} \tag{15}$$

The second quadratic function given in (16) is solved by also setting $gb_0 = gb_1 = 500$ µA/V, but now the circuit elements are evaluated as: $C_2 = gb_1/792.07 = 631$ nF and $gm_2 = 1408.99C_2 = 889.43$ µA/V. Additionally, $C_1 = gb_0gm_2/31{,}623.28C_2 = 22.27$ µF and $gm_1 = 100{,}036.66C_1C_2/gm_2 = 1.58$ mA/V.

$$H(s) = \frac{s^2 + \frac{gb_1}{C_2}s + \frac{gb_0gm_2}{C_1C_2}}{s^2 + \frac{gm_2}{C_2}s + \frac{gm_1gm_2}{C_1C_2}} = \frac{s^2 + 792.07s + 31{,}623.28}{s^2 + 1408.99s + 100{,}036.66} \tag{16}$$

The first-order low-pass filter shown in Figure 6b, is used to synthesize (17). If $gm_1 = 500$ µA/V, the capacitor value will be $C_1 = gm_1/5.30 = 94.33$ µF, and therefore, $R_1 = 1/0.01292C = 796$ KΩ.

$$H(s) = \frac{gm_1C}{s + gm_2C} = \frac{5.3088}{s + 0.01334} \tag{17}$$

To carry out the design of the fractional-order integrator described in (12), in which $H_2(s) = 1/s^{0.9}$, the transfer function can be split into two functions, one of second-order and one of first-order, as given in (18) and (19), respectively.

$$H_2(s) = \frac{s^2 + 216.6920s + 278.2968}{s^2 + 361.5540s + 774.1476} \tag{18}$$

$$H_3(s) = \frac{2.2675}{s + 0.01292} \tag{19}$$

From (18) and (13) and by setting again $V_1 = V_2 = 0$ and $V_3 = V_4 = V_5 = V_i$, one gets (20). If $gb_0 = gb_1 = 500$ µA/V, the capacitor and transconductance values are obtained as: $C_2 = gb_1/216.6920 = 2.3$ µF and $gm_2 = 361.5540C_2 = 830$ µA/V; and $C_1 = gb_0gm_2/278.2968C_2 = 650$ µF and $gm_1 = 774.1476C_1C_2/gm_2 = 1.4$ mA/V. In a similar way, the low-pass filter shown in Figure 6b is synthesized by the circuit element

values evaluated as: if $gm_1 = 500$ µA/V, the capacitor value will be $C_1 = gm_1/2.2675 = 220$ µF, and therefore, $R_1 = 1/0.01292C = 350$ KΩ.

$$H_2(s) = \frac{s^2 + \frac{gb_1}{C_2}s + \frac{gb_0 gm_2}{C_1 C_2}}{s^2 + \frac{gm_2}{C_2}s + \frac{gm_1 gm_2}{C_1 C_2}} = \frac{s^2 + 216.6920s + 278.2968}{s^2 + 361.5540s + 774.1476} \tag{20}$$

Figure 7 shows the gain and phase behaviors of the approximated fractional order integrators of orders 0.8 and 0.9, and the responses are compared with MatLab simulations of (11) and (12), which show very low error, so that the OTA-based designs are suitable to perform the CMOS design of the fractional-order system given in (10).

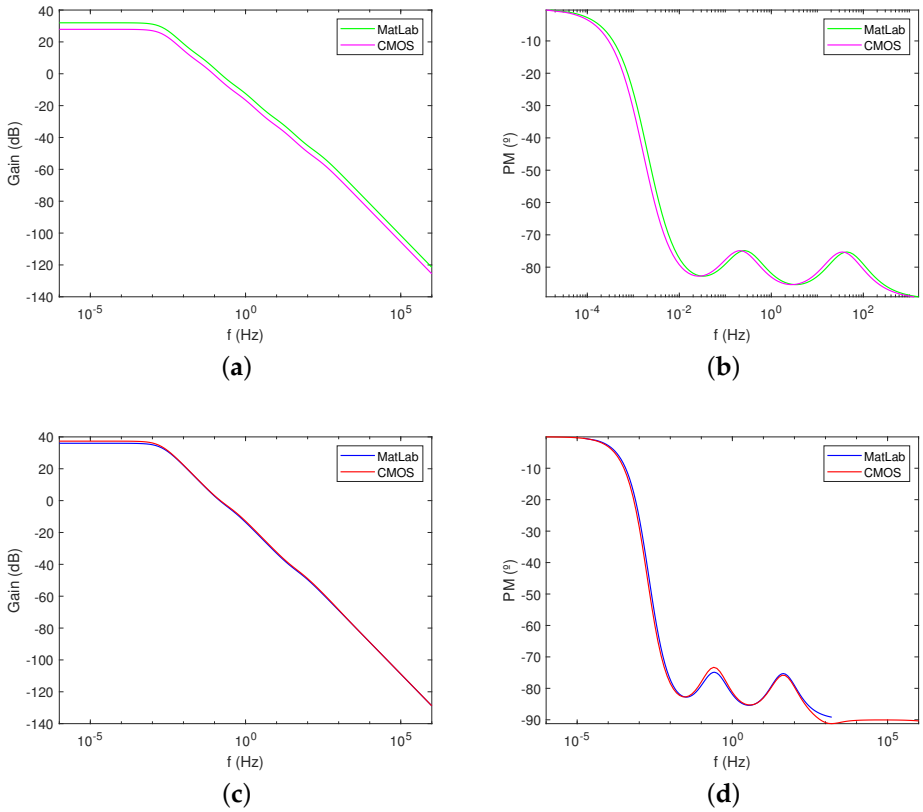


Figure 7. Frequency responses of the two fractional-order integrators considering ideal transfer function approximation in MatLab^{TM} and HSPICE^{TM} simulation using CMOS transistor models. (**a**) Gain and (**b**) phase of the fractional-order 0.8, and (**c**) fain and (**d**) phase of the fractional-order 0.9.

To complete the CMOS design of (10), the need for designing two two-input adders and one three-input adder can be inferred; these are shown in Figure 8 using OTAs. To explain how these adders work, let us consider the adder in Figure 8a: the output of this adder must be equal to $x = ay - ax$, so that y is connected to the positive input of the OTA gm_a and the variable x to the negative input of the OTA gm_b. However, these OTAs must scale the values of the variables y and x by $a = 0.35$. Therefore: if gm_c is equal to 500 µA/V, then gm_a and gm_b should be equal to 175 µA/V. A similar analysis should be performed for the other adders. It is important to mention that one of the most important characteristics of an OTA to design these adders and active filters is its transconductance (gm) value. In this work, the designed OTA is shown in Figure 9. This topology allows controlling the value of the transconductance through the resistances in the sources of the MOS transistors, i.e., those forming the differential pair. The Rs can be designed with MOS transistors, as detailed in [33]. Table 5 shows the electrical characteristics for different gm values of the OTA that is used for the design of the CMOS fractional-order chaotic system. Figure 10

shows the layout of the OTA providing $g_m = 500$ µA/V, and Figure 11 shows the layout of the fractional-order integrator of 0.9.

The convolutions given in (10) ($X(s) * Y(s)$ and $X(s) * Z(s)$) were implemented using a four-quadrant multiplier, as the one already given in [49]. As a result, the attractors of the CMOS design of the fractional-order chaotic system given in (10), and using CMOS technology of 180nm are shown in Figure 12.

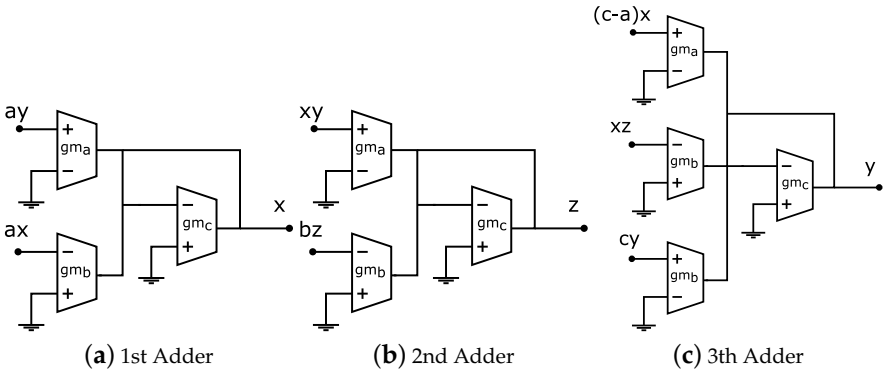


Figure 8. OTA adders.

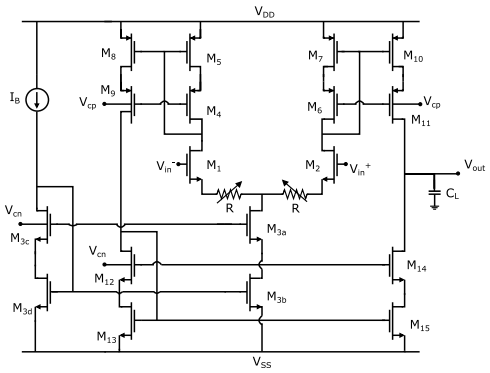


Figure 9. One-Stage OTA.

Table 5. Electrical characteristics and feasible W/L sizes of the OTA shown in Figure 9.

gm (µA/V)	50	200	500	830	890	1400	1500	3000
FoM$_s$	1500	1504	1469	1269	1284	1251	1236	1398
DCGain (dB)	80	80.2	80.1	75.8	76.2	71	73	60
Power dissipation (µW)	36	37.8	93.6	171	174.6	288	297	540
CMRR (dB)	115	117	110	103	105	106	109	93
GBW (MHz)	15	15.84	38.27	60.29	62.3	99	102	209
PM (°)	68	68	61	62	62	52	52	55
PSRR+ (dB)	102	105	100	97	97	80	80	74
PSRR− (dB)	79	81	81	77	77	75	75	61
SR+ (V/µs)	5	5	11	34	34	33	33	74
SR- (V/µs)	5	5	13	13	14	31	31	49
Vmax (V)	0.59	0.59	0.62	0.63	0.63	0.62	0.62	0.6
Vmin (V)	−0.5	−0.5	−0.55	−0.56	−0.55	−0.58	−0.58	−0.6
W1 [M1,M2] (µm)	27.9	30.42	49.32	81.81	81.81	90	90	261
W2 [M3a-M3d,M12-M15] (µm)	7.29	7.29	10.08	9.54	9.54	18.9	18.9	37.8
W3 [M4-M11] (µm)	18.27	18.2 7	23.22	36.99	36.99	27.9	27.9	31.5
W4 [Mn1-Mn4] (µm)	9.45	9.45	15.3	90	90	90	90	189
L1 [M1,M2] (µm)	1.08	1.08	0.72	0.81	0.81	0.81	0.81	0.54
L2 [M3a-M3d,M12-M15] (µm)	1.8	1.8	1.62	0.99	0.99	0.99	0.99	0.9
L3 [M4-M11] (µm)	0.9	1.17	0.9	0.72	0.72	0.72	0.72	0.18
L4 [Mn1-Mn4] (µm)	0.27	0.27	0.18	1.53	1.53	0.18	0.18	0.18
Ib (µA)	20	21	52	95	97	160	165	300
Vc (V)	0.7	0.7	0.8	0.9	0.9	0.9	0.9	0.9

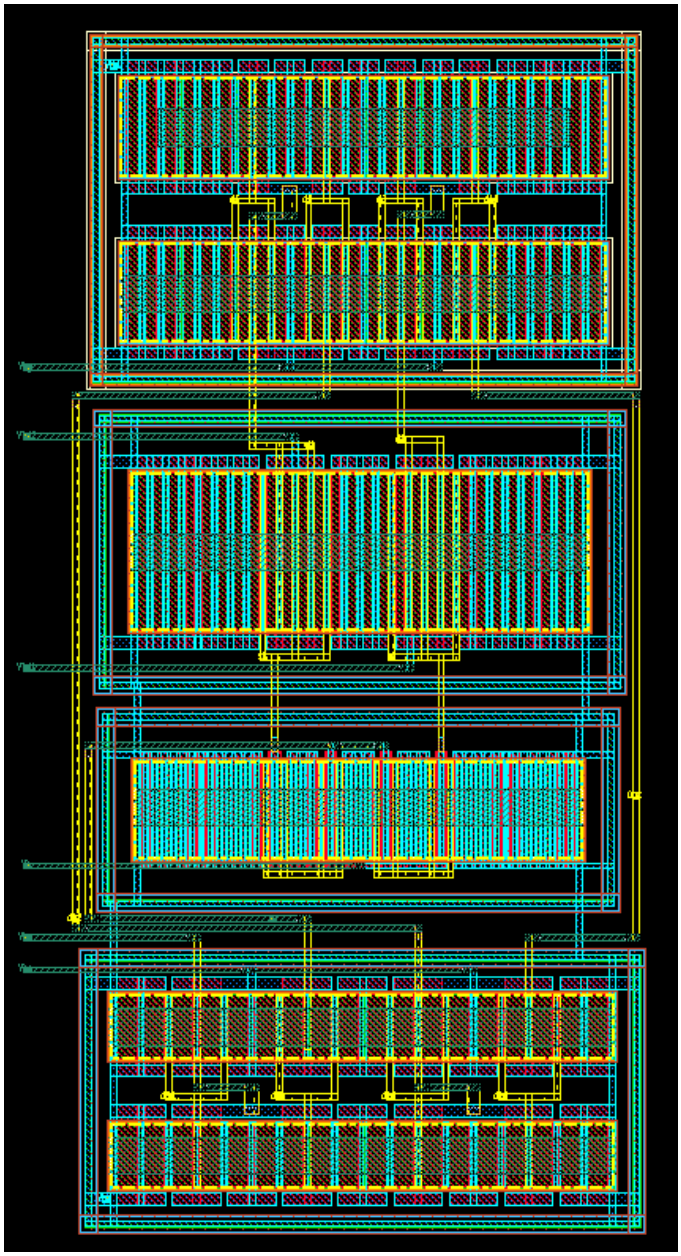


Figure 10. Layout of the OTA providing $g_m = 500$ µA/V.

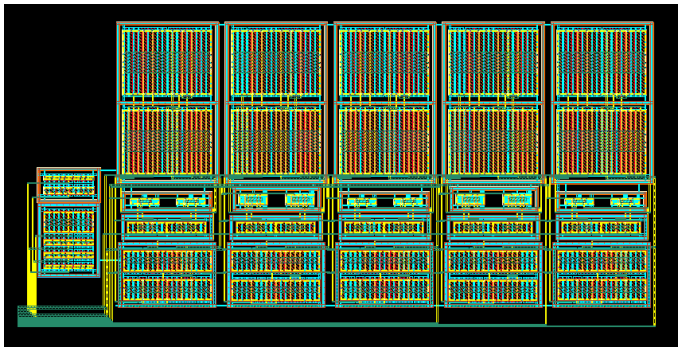
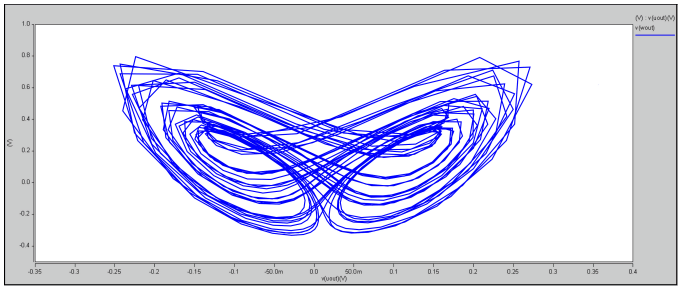
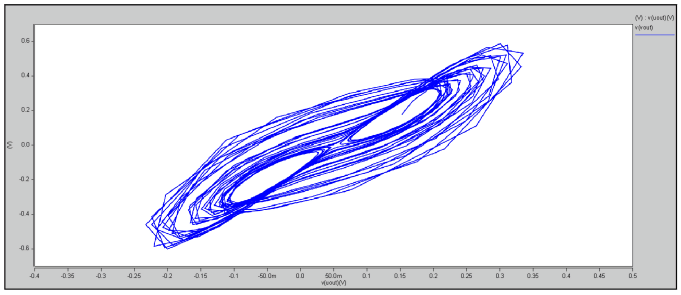


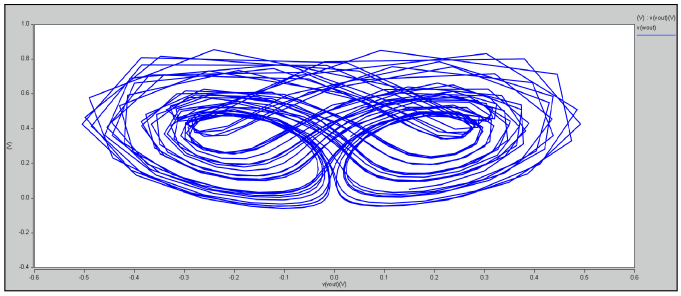
Figure 11. Layout of the fractional-order integrator of 0.9.



(**a**) x vs. z



(**b**) x vs. y



(**c**) y vs. z

Figure 12. Phase portraits of the CMOS OTA-based fractional-order chaotic system given in (10) and using CMOS technology of 180 nm.

5. Discussion of Results

As shown in the previous sections, the IC design of fractional-order chaotic systems by using CMOS technology can be performed through the optimization of the mathematical model by metaheuristics. The design process can then be performed considering three major levels of abstraction; each one can be considered as a challenge to develop EDA tools. The highest level has been highlighted in Section 2, describing the adaptation of an optimization algorithm to optimize fractional-order chaotic systems from the mathematical model, in order to maximize dynamical characteristics, such as Lyapunov spectrum and Kaplan–Yorke dimensions. It has been appreciated that in this level of abstraction, the amplitudes of the state variables of a mathematical model can have large values, higher than those supported by a CMOS design, which in this case the CMOS technology of 180 nm leads us to scale the mathematical model to provide amplitudes within ± 1 or lower.

Optimizing the mathematical model of a fractional-order system, as for the ones given in (3) and (4), includes varying the values of the orders of the derivatives, which are higher than zero but lower than one. More case studies are already given in recent works and in the book [1], where one can find a summary on the single, multi, and many-objective optimization algorithms applied to chaotic systems of integer and fractional-order. One can also associate this optimization process with the system level when considering the design of electronic systems, as described in [2].

The second level of abstraction proposed in this work is described in Section 3, which highlights the block description of a mathematical model, and the particular interest is the approximation of the fractional-order derivatives in the Laplace domain. This is not a trivial task, so several authors have been introduced different methods to perform the rational approximations of arbitrary order, as recently done in [50], where the authors summarize several rational approximations of arbitrary order for differentiators and integrators in the frequency domain. Basically, similar works that introduce methods to approximate and arbitrary order, use the basic definitions already given by Riemann–Liouville, Grünwald–Letnikov and Caputo. One can think on the exactness of each method along with their advantages and disadvantages, since each method approximates the arbitrary order with polynomials of high order, thereby generating different errors. Some authors also introduce methods to reduce the polynomial orders; those methods are known as model-order-reduction (MOR) ones and are quite suitable in the design of very large scale integration (VLSI) systems, as shown in [51]. In fact, MOR techniques reduce the complexity of VLSI designs, paving the way to higher operating speeds and smaller feature sizes. In this paper, the fractional-orders of the derivatives, i.e., 0.8 and 0.9, were approximated by applying Charef's method [46]. Those transfer functions are different from the ones that can be obtained applying other methods to approximate an arbitrary order, as detailed in [50]. In the case of approximating an arbitrary order in the Laplace domain, higher-order polynomials can be reduced to have third or even second order, by allowing an increase in the error. This is still a challenge focused on the reduction of the polynomial order and generating low error in the band of interest.

The third level of abstraction described herein is oriented to the design of a fractional-order chaotic system using CMOS technology. In this manner, the transfer functions approximating the fractional-order derivatives are implemented using topologies of active filters, and due to the exactness and reduced numbers of transistors, filters, adders, and subtractors, were designed using OTAs, as detailed in Section 4. The first design step consists of scaling the amplitudes of the state variable to be within ± 1 Volt or lower, as required by the CMOS IC technology of 180 nm. The next step is identifying the operations such as addition, subtraction, and multiplication, which can be designed using CMOS technology, and in some cases OTAs. The rational approximations of arbitrary order can then be designed using active filters, but the challenge is for the decomposition of higher-order polynomials to have second-order and first-order polynomials that can be associated with bi-quadratic and single pole/zero filters. The task of dealing with high-order polynomials can be solved by performing a partial fraction expansion, as shown in [52]. The transfer functions can also be implemented using FPAAs, as shown in [53].

Once a CMOS design is verified at the transistor level of abstraction, one can proceed to generate the layout [10,12], for which another problem in VLSI design is the placement and routing of the designed blocks [5,6,13]. Recall that the first integrated chaotic system was introduced three decades ago [25], so that the layout was not as complex as for VLSI circuits. Therefore, the authors conclude that working with these three levels of abstraction makes possible the design of CMOS ICs for fractional-order chaotic systems.

6. Conclusions

The electronic implementation of fractional-order chaotic systems can be performed by using commercially available devices, FPAAs, FPGAs, and microcontrollers. However, for low power and wireless applications, they are not as suitable as a CMOS IC, the design of which is not a trivial task. In this manner, this work proposed the design of CMOS fractional-order chaotic systems performing three main tasks, associated with three levels of abstraction. The first one, the high-level, was oriented to optimizing the mathematical model to guarantee chaotic behavior, which was verified evaluating the Fourier transform of the chaotic time series. In this level of abstraction, the coefficients and orders of the derivatives were varied to maximize the dynamical characteristics D_{KY}. As one can infer, this task can be performed using other metaheuristics to optimize a mathematical model.

The second level of abstraction was focused on the block description of a mathematical model, in which the arbitrary order of each of the derivatives was approximated in the Laplace domain. The challenge is still guaranteeing chaotic behavior during the approximation of the fractional-orders, since a slight error may mitigate chaotic behavior, and this influences the CMOS design of the chaotic system. Another important issue is the scaling process of the mathematical model to have amplitudes of the state variables within ranges that can be suitable for CMOS design. In this work, the amplitudes of the state variables of Chen and Liu systems were scaled to have values in the range lower than ± 1.

From the block description and Laplace approximation of the arbitrary orders, one can go to the third level proposed herein, the CMOS design, and layout generation. The case study was designed using OTAs, but one can think of using other active devices and also other active filter topologies. These could lead to designing robust CMOS chaotic systems that can support process and temperature variations. Finally, it was discussed that the layout generation is a challenge for sensitive systems, as for the chaotic ones.

The phase portraits of the CMOS fractional-order Chen system shown in Figure 12 are in good agreement with the theoretical results. One can also perform variation analyses as already done in [33]. Finally, from the results of the CMOS design, one can conclude on the suitability of performing the three levels of abstraction, which can lead to the development of EDA tools for chaotic systems.

Author Contributions: Conceptualization, E.T.-C., L.G.d.l.F. and C.S.-L.; methodology, M.A.V.-P.; software, M.A.V.-P. and A.M.G.-Z.; validation, L.G.d.l.F.; formal analysis, M.A.V.-P. and A.M.G.-Z.; writing—original draft preparation, M.A.V.-P., A.M.G.-Z. and E.T.-C.; writing—review and editing, M.A.V.-P., E.T.-C., L.G.d.l.F. and C.S.-L. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Data Availability Statement: Not applicable.

Acknowledgments: M.A.V.-P. and A.M.G.-Z. thanks to CONACyT-Mexico for the PhD scholarship at INAOE. C.S.-L. thanks to CONACyT-Mexico for the sabbatical fellowship at INAOE.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Tlelo-Cuautle, E.; De La Fraga, L.G.; Guillén-Fernández, O.G.; Silva-Juárez, A. *Optimization of Integer/Fractional Order Chaotic Systems by Metaheuristics and Their Electronic Realization*; CRC Press: Boca Raton, FL, USA, 2021.
2. Canelas, A.; Passos, F.; Lourenço, N.; Martins, R.; Roca, E.; Castro-López, R.; Horta, N.; Fernández, F.V. Hierarchical Yield-Aware Synthesis Methodology Covering Device-, Circuit-, and System-Level for Radiofrequency ICs. *IEEE Access* **2021**, *9*, 124152–124164. [CrossRef]
3. Hosny, A.; Reda, S. Characterizing and Optimizing EDA Flows for the Cloud. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* **2022**, *41*, 3040–3051. [CrossRef]
4. Passos, F.; Roca, E.; Castro-López, R.; Fernández, F.V. *Automated Hierarchical Synthesis of Radio-Frequency Integrated Circuits and Systems: A Systematic and Multilevel Approach*; Springer: Cham, Switzerland, 2020.
5. de Gusmão, A.P.L.; Horta, N.C.G.; Lourenço, N.C.C.; Martins, R.M.F. Scalable and order invariant analog integrated circuit placement with Attention-based Graph-to-Sequence deep models. *Expert Syst. Appl.* **2022**, *207*, 117954. [CrossRef]
6. Gusmão, A.; Póvoa, R.; Horta, N.; Lourenço, N.; Martins, R. DeepPlacer: A custom integrated OpAmp placement tool using deep models. *Appl. Soft Comput.* **2022**, *115*, 108188. [CrossRef]
7. Elbadry, M.M.; Makkey, M.Y.; Atef, M. Design framework for inverter cascode transimpedance amplifier using Gm/I-D based PSO applying design equations. *AEU Int. J. Electron. Commun.* **2021**, *142*, 153985. [CrossRef]
8. Kumar, S.B.V.; Rao, V.P.; Singh, M.K. Optimal floor planning in VLSI using improved adaptive particle swarm optimization. *Evol. Intell.* **2022**, *15*, 925–938. [CrossRef]
9. Budak, A.F.; Gandara, M.; Shi, W.; Pan, D.Z.; Sun, N.; Liu, B. An Efficient Analog Circuit Sizing Method Based on Machine Learning Assisted Global Optimization. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* **2022**, *41*, 1209–1221. [CrossRef]
10. Martins, R.; Lourenço, N.; Póvoa, R.; Horta, N. Shortening the gap between pre-and post-layout analog IC performance by reducing the LDE-induced variations with multi-objective simulated quantum annealing. *Eng. Appl. Artif. Intell.* **2021**, *98*, 104102. [CrossRef]

11. Sasikumar, A.; Subramaniyaswamy, V.; Jannali, R.; Rao, V.S.; Ravi, L. Design and area optimization of CMOS operational amplifier circuit using hybrid flower pollination algorithm for IoT end-node devices. *Microprocess. Microsyst.* **2022**, *93*, 104610. [CrossRef]
12. Wei, P.H.; Murmann, B. Analog and Mixed-Signal Layout Automation Using Digital Place-and-Route Tools. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2021**, *29*, 1838–1849. [CrossRef]
13. Nohtanipour, M.; Maghami, M.H.; Radmehr, M. A Placement and Routing Method for Layout Generation of CMOS Operational Amplifiers Using Multi-Objective Evolutionary Algorithm Based on Decomposition. *Inf. Midem J. Microelectron. Electron. Components Mater.* **2021**, *51*, 181–191. [CrossRef]
14. Settaluri, K.; Liu, Z.; Khurana, R.; Mirhaj, A.; Jain, R.; Nikolic, B. Automated Design of Analog Circuits Using Reinforcement Learning. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* **2022**, *41*, 2794–2807. [CrossRef]
15. Touloupas, K.; Sotiriadis, P.P. LoCoMOBO: A Local Constrained Multiobjective Bayesian Optimization for Analog Circuit Sizing. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* **2022**, *41*, 2780–2793. [CrossRef]
16. Zhang, S.; Yang, F.; Yan, C.; Zhou, D.; Zeng, X. An Efficient Batch-Constrained Bayesian Optimization Approach for Analog Circuit Synthesis via Multiobjective Acquisition Ensemble. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* **2022**, *41*, 1–14. [CrossRef]
17. Liao, T.; Zhang, L. High-Dimensional Many-Objective Bayesian Optimization for LDE-Aware Analog IC Sizing. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2022**, *30*, 15–28. [CrossRef]
18. Valencia-Ponce, M.A.; Tlelo-Cuautle, E.; de la Fraga, L.G. On the Sizing of CMOS Operational Amplifiers by Applying Many-Objective Optimization Algorithms. *Electronics* **2021**, *10*, 3148. [CrossRef]
19. Park, M.J.; Lee, J.; Cho, K.; Park, J.; Moon, J.; Lee, S.H.; Kim, T.K.; Oh, S.; Choi, S.; Choi, Y.; et al. A 192-Gb 12-High 896-GB/s HBM3 DRAM With a TSV Auto-Calibration Scheme and Machine-Learning-Based Layout Optimization. *IEEE J. Solid-State Circuits*. **2023**, *58*, 256–269. [CrossRef]
20. Canelas, A.M.L.; Guilherme, J.M.C.; Horta, N.C.G. *Yield-Aware Analog IC Design and Optimization in Nanometer-Scale Technologies*; Springer: Cham, Swizterland, 2020.
21. Karimov, T.; Rybin, V.; Kolev, G.; Rodionova, E.; Butusov, D. Chaotic communication system with symmetry-based modulation. *Appl. Sci.* **2021**, *11*, 3698. [CrossRef]
22. Liao, T.L.; Wan, P.Y.; Yan, J.J. Design and Synchronization of Chaos-Based True Random Number Generators and Its FPGA Implementation. *IEEE Access* **2022**, *10*, 8279–8286. [CrossRef]
23. Sayed, W.S.; Mohamed, S.M.; Elwakil, A.S.; Said, L.A.; Radwan, A.G. Numerical Sensitivity Analysis and Hardware Verification of a Transiently-Chaotic Attractor. *Int. J. Bifurc. Chaos* **2022**, *32*, 2230015. [CrossRef]
24. Andreev, V.; Ostrovskii, V.; Karimov, T.; Tutueva, A.; Doynikova, E.; Butusov, D. Synthesis and Analysis of the Fixed-Point Hodgkin–Huxley Neuron Model. *Electronics* **2020**, *9*, 434. [CrossRef]
25. Cruz, J.; Chua, L. An ic chip of chua circuit. *IEEE Trans. Circuits Syst. II Analog. Digit. Signal Process.* **1993**, *40*, 614–625. [CrossRef]
26. Rodriguezvazquez, A.; Delgado, M.; Espejo, S.; Huertas, J. Switched-capacitor broad-band noise generator for cmos vlsi. *Electron. Lett.* **1991**, *27*, 1913–1915. [CrossRef]
27. Joshi, M.; Ranjan, A. Low power chaotic oscillator employing CMOS. *Integr. VLSI J.* **2022**, *85*, 57–62. [CrossRef]
28. Raj, N.; Ranjan, R.K.; James, A. Chua's Oscillator With OTA Based Memcapacitor Emulator. *IEEE Trans. Nanotechnol.* **2022**, *21*, 213–218. [CrossRef]
29. Duan, Z.; Wang, H.; He, S.; Li, S.; Yan, S.; Zhao, X.; Yu, X.; Yang, G.; Tan, H. A fully integrated chaos generator based on voltage controlled oscillator. *Microelectron. J.* **2022**, *126*, 105514. [CrossRef]
30. Jin, J.; Zhao, L. Low Voltage Low Power Fully Integrated Chaos Generator. *J. Circuits Syst. Comput.* **2018**, *27*, 1830005. [CrossRef]
31. Choubey, C.K.; Paul, S.K. Systematic realisation of inductorless and resistorless Chua's chaotic oscillator using VDGA. *Int. J. Electron.* **2022**. [CrossRef]
32. Ouyang, Z.; Jin, J.; Yu, F.; Chen, L.; Ding, L. Fully Integrated Chen Chaotic Oscillation System. *Discret. Dyn. Nat. Soc.* **2022**, *2022*, 8613090. [CrossRef]
33. Hugo Carbajal-Gomez, V.; Tlelo-Cuautle, E.; Manuel Munoz-Pacheco, J.; Gerardo de la Fraga, L.; Sanchez-Lopez, C.; Vidal Fernandez-Fernandez, F. Optimization and CMOS design of chaotic oscillators robust to PVT variations: INVITED. *Integr. Vlsi J.* **2019**, *65*, 32–42. [CrossRef]
34. Nguyen, N.; Kaddoum, G.; Pareschi, F.; Rovatti, R.; Setti, G. A fully CMOS true random number generator based on hidden attractor hyperchaotic system. *Nonlinear Dyn.* **2020**, *102*, 2887–2904. [CrossRef]
35. Addabbo, T.; Fort, A.; Mugnaini, M.; Petra, N.; Takaloo, H.; Vignoli, V. Self-tunable chaotic true random bit generator in current-mode CMOS circuit with nonlinear distortion analysis. *Int. J. Circuit Theory Appl.* **2019**, *47*, 1877–1892. [CrossRef]
36. Wannaboon, C.; Tachibana, M.; San-Um, W. A 0.18-mu m CMOS high-data-rate true random bit generator through Delta Sigma modulation of chaotic jerk circuit signals. *Chaos* **2018**, *28*, 063126. [CrossRef]
37. Dong, S.; Wang, Y.; Xin, X.; Tong, X. A chaos-based true random number generator based on OTA sharing and non-flipped folded Bernoulli mapping for high-precision ADC calibration. *Microelectron. J.* **2021**, *116*, 105259. [CrossRef]
38. Garcia-Bosque, M.; Diez-Senorans, G.; Perez-Resa, A.; Sanchez-Azqueta, C.; Aldea, C.; Celma, S. A 1 Gbps Chaos-Based Stream Cipher Implemented in 0.18 mu m CMOS Technology. *Electronics* **2019**, *8*, 623. [CrossRef]
39. Nguyen, N.; Pham-Nguyen, L.; Nguyen, M.B.; Kaddoum, G. A Low Power Circuit Design for Chaos-Key Based Data Encryption. *IEEE Access* **2020**, *8*, 104432–104444. [CrossRef]

40. Dar, M.R.; Kant, N.A.; Khanday, F.A. Realization of Fractional-Order Double-Scroll Chaotic System Using Operational Transconductance Amplifier (OTA). *J. Circuits Syst. Comput.* **2018**, *27*, 1850006. [CrossRef]
41. Dar, M.R.; Kant, N.A.; Khanday, F.A. Realization of Integrable Incommensurate-Fractional-Order-Rossler-System Design Using Operational Transconductance Amplifiers (OTAs) and Its Experimental Verification. *Int. J. Bifurc. Chaos* **2017**, *27*, 1750077. [CrossRef]
42. Petráš, I. The fractional-order Lorenz-type systems: A review. *Fract. Calc. Appl. Anal.* **2022**, *25*, 362–377. [CrossRef]
43. Tlelo-Cuautle, E.; González-Zapata, A.M.; Díaz-Muñoz, J.D.; de la Fraga, L.G.; Cruz-Vega, I. Optimization of fractional-order chaotic cellular neural networks by metaheuristics. *Eur. Phys. J. Spec. Top.* **2022**, *231*, 2037–2043. [CrossRef]
44. Bai, Q. Analysis of particle swarm optimization algorithm. *Comput. Inf. Sci.* **2010**, *3*, 180. [CrossRef]
45. Shi, Y. Particle swarm optimization. *IEEE Connect.* **2004**, *2*, 8–13.
46. Charef, A. Modeling and analog realization of the fundamental linear fractional order differential equation. *Nonlinear Dyn.* **2006**, *46*, 195–210. [CrossRef]
47. Ahmad, W.M.; Sprott, J.C. Chaos in fractional-order autonomous nonlinear systems. *Chaos Solitons Fractals* **2003**, *16*, 339–351. [CrossRef]
48. Geiger, R.L.; Sanchez-Sinencio, E. Active filter design using operational transconductance amplifiers: A tutorial. *IEEE Circuits Devices Mag.* **1985**, *1*, 20–32. [CrossRef]
49. Valencia-Ponce, M.A.; Castañeda-Aviña, P.R.; Tlelo-Cuautle, E.; Carbajal-Gómez, V.H.; González-Díaz, V.R.; Sandoval-Ibarra, Y.; Nuñez-Perez, J.C. CMOS OTA-based filters for designing fractional-order chaotic oscillators. *Fractal Fract.* **2021**, *5*, 122. [CrossRef]
50. Colín-Cervantes, J.D.; Sánchez-López, C.; Ochoa-Montiel, R.; Torres-Muñoz, D.; Hernández-Mejía, C.M.; Sánchez-Gaspariano, L.A.; González-Hernández, H.G. Rational Approximations of Arbitrary Order: A Survey. *Fractal Fract.* **2021**, *5*, 267. [CrossRef]
51. Tan, S.; He, L. *Advanced Model Order Reduction Techniques in VLSI Design*; Cambridge University Press: Cambridge, UK, 2007.
52. Bertsias, P.; Psychalinos, C.; Maundy, B.J.; Elwakil, A.S.; Radwan, A.G. Partial fraction expansion–based realizations of fractional-order differentiators and integrators using active filters. *Int. J. Circuit Theory Appl.* **2019**, *47*, 513–531. [CrossRef]
53. Kapoulea, S.; Psychalinos, C.; Elwakil, A.S. FPAA-based realization of filters with fractional Laplace operators of different orders. *Fractal Fract.* **2021**, *5*, 218. [CrossRef]