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Self-Rectifying Resistive Switching Memory Based on Molybdenum Disulfide for Reduction of Leakage Current in Synapse Arrays

DongJun Jang and Min-Woo Kwon *

Department of Electronic Engineering, Gangneung-Wonju National University, Gangneung 25457, Republic of Korea; shys0901@gwnu.ac.kr
* Correspondence: mwkwon@gwnu.ac.kr

Abstract: Resistive random-access memory has emerged as a promising non-volatile memory technology, receiving substantial attention due to its potential for high operational performance, low power consumption, temperature robustness, and scalability. Two-dimensional nanostructured materials play a pivotal role in RRAM devices, offering enhanced electrical properties and physical attributes, which contribute to overall device improvement. In this study, the self-rectifying switching behavior in RRAM devices is analyzed based on molybdenum disulfide nanocomposites decorated with Pd on SiO_2/Si substrates. The switching layer integration of Pd and MoS_2 at the nanoscale effectively mitigates leakage currents decreasing from cross-talk in the RRAM array, eliminating the need for a separate selector device. The successful demonstration of the expected RRAM switching operation and low switching dispersion follows the application of a Pd nanoparticle embedding method. The switching channel layer is presented as an independent (Pd nanoparticle coating and MoS_2 nanosheet) nanocomposite. The switching layer length (4000 µm) and width (7000 µm) play an important role in a lateral-conductive-filament-based RRAM device. Through the bipolar switching behavior extraction of RRAM, the formation of the conductive bridges via electronic migration is explained. The fabricated Pd-MoS_2 synaptic RRAM device results in a high resistive current ratio for a forward/reverse current higher than 60 at a low resistance state and observes a memory on/off ratio of 10^3, exhibiting stable resistance switching behavior.

Keywords: resistive random-access memory (RRAM); molybdenum disulfide (MoS_2); palladium (Pd); self-rectifying; resistive current ratio

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1. Introduction

The traditional architectures based on von Neumann systems have long encountered a problem with the "memory wall"—a bottleneck resulting from data transmission between the memory and processing units. Recently, neuromorphic system technology, drawing inspiration from the human brain, has emerged as a potential solution to this issue. The intricate human brain performs computing, learning, and memory functions in parallel, consuming approximately 10 W of energy within a volume of around 1 L. The neural network of the human brain is designed with 10^{15} synapses and 10^{11} neurons, and the strength of neuron–synapse connections is adjusted through a process known as spike-timing-dependent plasticity (STDP). In the field of neuromorphic non-volatile memory technology, the emerging resistive random-access memory (RRAM) device is attracting significant attention due to its excellent properties, including low operation voltage, low power consumption, scalability, and compatibility with complementary metal oxide semiconductor (CMOS) technologies. STDP-mechanism-based synaptic RRAM devices offer the ability to store and retrieve data by altering their resistance states through the application of voltage pulses. This mechanism enables the realization of compact and energy-efficient

memory solutions for various applications, including data storage and computing, artificial intelligence, and internet of things devices.

However, RRAM devices face challenges in cross-bar array architectures due to leakage currents caused by interference between nearby cells. To alleviate the cross-talk in memristive RRAM devices, a new concept of operational and structural solutions has been developed. Conventional synapse-based RRAM devices have been adopted in one-transistor and one-resister (1T1R) structures or one-selector and one-resister (1T1S) structures, where each RRAM cell is integrated with a non-linear circuit device known as a selector device [1,2]. These approaches have disadvantages, including larger cell sizes, increased operating voltages, and complex fabrication processes. As an alternative, research has been conducted to develop memory cells with self-rectifying properties to suppress leakage current interference in RRAM cells [3–5].

As shown in Figure 1, the vertical sandwich structure of the RRAM device serves as an indicator for thin film materials and various switching mechanisms. The conventional RRAM device structures typically comprise metal-oxide metal or metal-oxide-doped Si. Generally, the electrical performance of RRAM relies on the thin film materials used for the electrode and the switching layer. Various materials have been explored for the application of self-rectifying RRAM, including nanomaterials, carbon-based materials [6,7], metal oxides (MXs) [8], and transition metal dichalcogenides (TMDs), which have been used as switching channel layers in various memory platforms. MXs-based RRAM devices exhibit inherent and favorable properties for the switching behavior. The deposition of the switching layer using MXs, such as titanium dioxide [9], zinc oxide, zirconium dioxide, hafnium oxide [10–12], tin dioxide [13], and aluminum oxide [14], among others, is compatible with CMOS materials, making them suitable candidates for the development of high-performance RRAM and electronic synaptic devices. However, despite the thin nature of the MXs-based switching layers in RRAM devices, ultra-fine film deposition often results in significant leakage currents and a limited memory window [15]. Recently, various approaches have been conducted to reduce the operating voltage of the RRAM, except for the method of reducing the thickness of the switching layer. To achieve low-power operation in RRAM, diverse techniques can be employed, including embedding metal nanoparticles to enhance the electric field, incorporating nanostructured materials into the switching channel layer, and altering the electrode [16]. While decorating the switching layer with metal nanoparticles has been effective in reducing the SET voltage, it has been observed that this approach does not necessarily lead to an improvement in the memory window [3].

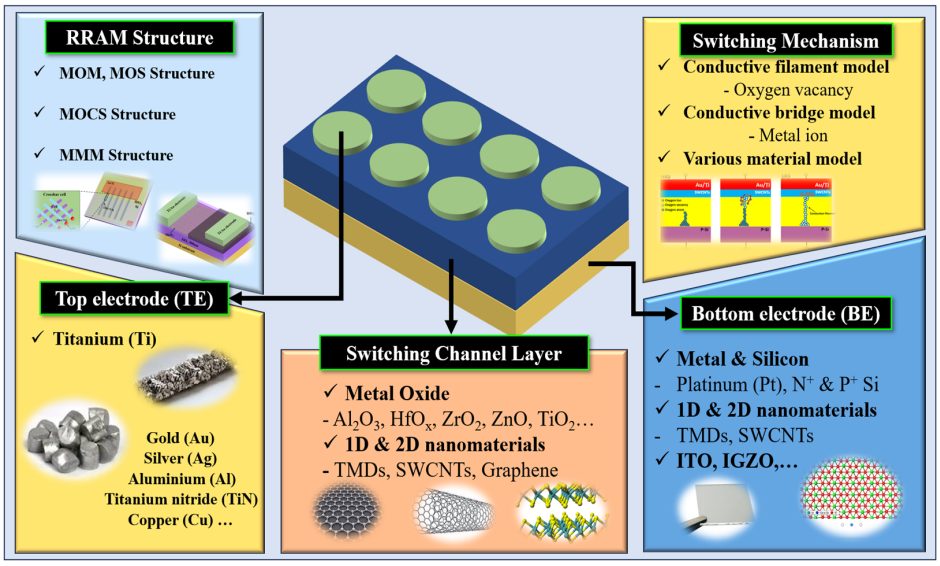

Figure 1. Illustration of structures, switching mechanisms, and various materials for RRAM device applications.

2. Nanomaterials for Switching Channel Layer

The synthesis of one-dimensional (1D) and two-dimensional (2D) nanostructured materials has unveiled their potential for applications in memory device platforms and toxic gas detection sensors. RRAM devices employing nanostructured materials as the switching layer induce the formation of conductive filaments in thin switching channel layers, resulting in excellent electrical characteristics relative to the deposition area density. The manufacturing process of nanomaterial-based RRAM devices offers insights into the low-power operation and memristive switching properties. It is imperative to propose solutions, which simultaneously reduce leakage current and enhance memory window characteristics. Nanostructured materials have gained attention in the fabrication of flexible RRAM devices due to their ability to uniformly form nanostructures at room temperature [17]. Memristive switching channel layers utilizing carbon-based nanomaterials, such as graphene, graphene oxides, carbon nanotubes (CNTs), single-walled carbon nanotubes, and multi-walled carbon nanotubes, have been reported [18]. On the other hand, 1D CNTs can be categorized into metallic or semiconducting based on the orientation of particles, chirality, and diameter, which significantly affect their electrical and physical properties. One-dimensional CNTs are attracting attention due to their thermal stability and excellent electrical properties. The physical advantages of CNTs are high elasticity and durability, high current density ($\approx 10^9$ A/cm^2), and high thermal conductivity ($\approx$3000 W/mK). Among the CNTs deposition methods, achieving the synthesis of semiconducting CNTs through the dip-coating technology is exceptionally challenging [18]. A semiconducting bandgap is necessary to exhibit RRAM self-rectifying diode characteristics as a switching channel layer. Consequently, 2D TMDs nanostructured materials are structurally similar to graphene materials but offer an adjustable bandgap [19]. The junction between the switching channel layer and the electrode facilitates the formation of a Schottky barrier, imparting diode characteristics. Two-dimensional TMDs present promising opportunities to optimize the deposition thickness and leverage unique electrical and physical properties to enhance the performance of RRAM devices. Well-known 2D TMDs layered materials, such as tungsten disulfide, tungsten diselenide, molybdenum diselenide, and MoS_2, have garnered interest as suitable materials for RRAM thin film layers [20]. MoS_2 exhibits favorable characteristics as a switching channel layer, including flexibility, transparency, and good electron mobility, compared to other materials. Various deposition methods have been employed to achieve high-quality MoS_2 nanosheets. Many studies have attempted the deployment of physical vapor deposition or chemical vapor deposition (CVD) technologies to grow thin MoS_2 layers [18,19]. MoS_2 is of particular interest in RRAM applications due to its self-rectifying switching behavior—a phenomenon in which the direction of the current flow is effectively controlled by the device structure. These memristive switching behavior mechanisms eliminate the need for external diodes or selectors, simplifying device structures and reducing power consumption. Meanwhile, nanoparticles and nanosheets hold promise for use in emerging memory devices and intelligent memristors through the synthesis technology. The fabrication process of nanocomposite-based RRAM devices provides insights into the low-power operation and resistance switching characteristics [21,22].

To showcase high-performance RRAM devices, there have been reports of nanocomposite-based MoS_2 RRAM devices using materials such as poly(4-vinylphenol) [23], reduced graphene oxide (rGO) [24], and polymethylmethacrylate (PMMA) [25]. It is worth noting that these RRAM devices were fabricated on substrates such as indium tin oxide (ITO) coated glass and polyethylene naphthalate (PEN). While there have been advancements in vertically stacking MXs and nanocomposites as switching channel materials, the field of RRAM devices based on metal nanoparticle MoS_2 switching layers remains relatively unexplored. Recent investigations have focused on the impact of nanoparticles embedded in the switching channel layer on the RRAM switching mechanism. One promising approach to generating stable electric fields and reducing switching dispersion within the RRAM's switching channel layer is the doping of transition metals, such as palladium (Pd), platinum (Pt), ruthenium (Ru), and nickel (Ni). The Pd nanoparticle coating method demonstrates

excellent transparency, low SET voltage, and a wide switching memory window [3]. Introducing Pt nanoparticles into the electric field has been shown to reduce the operating voltage, enhance stable resistive switching (RS) operation, and decrease switching dispersion [26]. Furthermore, decorating the RS layer with Ru nanoparticles has been employed to improve device yield and retention performance [27]. Ni nanoparticles have been found to enhance the local electric field, resulting in reduced switching dispersion [28].

Therefore, the independent fabrication process of nanocomposite switching layer RRAM holds promise for applications in emerging memory devices and intelligent memory components. Horizontal conductive filaments (CFs)-based RRAM devices formed within the switching layer are proposed to alleviate the cross-talk between cells due to current leakage during the SET/RESET process in the memory array. A novel approach to achieving self-rectifying switching behavior in RRAM devices is proposed in this study by employing Pd-decorated MoS_2 nanocomposites on SiO_2/Si substrates. The integration of Pd-MoS_2 at the nanoscale not only enhances the device's switching behavior but also addresses the issue of leakage current caused by cross-talk in RRAM arrays. Furthermore, the Pd nanoparticle embedding technology reduces switching dispersion and aids in the formation of CFs within the electric field. This advancement has the potential to enable efficient operation in high-density memory cells without the need for additional selector devices.

3. Experimental Details

3.1. Fabrication Process

The fabrication of lateral CFs RRAM devices based on Pd-MoS_2 nanocomposites is depicted in Figure 2a. Initially, a series of cleaning steps were conducted using acetone, isopropyl alcohol, and deionized water to eliminate organic solvents from the p-type silicon substrate (size: 10 mm × 10 mm). After drying with N_2 gas, a 300 nm SiO_2 layer was generated on the p-type substrate through dry oxidation. For the synthesis of the overall MoS_2 switching channel layer, the CVD method was employed by introducing MoO_3 powder (18 mg) and S powder (120 mg) into the furnace equipment. During the growth of MoS_2, the argon (Ar) gas flow rate, central heating zone temperature, and upstream S zone temperature were set at 25 SCCM, 750 °C, and 180 °C, respectively. Figure 2b illustrates the nanostructures of monolayer MoS_2 (≈0.72 nm) and multilayer MoS_2 (≈1.44 nm). Subsequently, the monolayer and multilayer MoS_2 films were synthesized on the SiO_2 without the need for photolithography. Figure 2c shows the deposition rate of the DC sputter. Following the pattering of a Pd mask (size: 9000 μm × 2500 μm), 8 nm of Pd nanoparticles were embedded with the MoS_2 nanosheets to form the switching channel layer. In this process, optimizing the Pd decoration and MoS_2 synthesis is critical. If the Pd deposition thickness is 1 nm, the Pd molecules at the MoS_2 interface may not be well defined, potentially leading to low Pd nanoparticle coverage density [29]. If the Pd thickness exceeds 10 nm, the Pd nanoparticles tend to form a continuous Pd electrode sheet [30]. Pd, titanium (Ti), and gold (Au) were manufactured using 99.99% pure targets. The DC sputter deposition conditions were held constant, with Ar gas flow rate, DC power, chamber working pressure, and substrate temperature set at 30 SCCM, 100 W, 1.4×10^{-3} Torr, and a temperature range from 0 to 60 °C, respectively. To apply the top electrode (TE) and bottom electrode (BE) through two-terminal electrode mask pattering (size: 7000 μm × 2000 μm), the Ti/Au electrodes were deposited with thicknesses of 10 nm/40 nm and an electrode area of 14,000,000 μm^2, completing the fabrication of the RRAM device.

3.2. Raman Spectroscopy

Raman data spectroscopy precisely analyzes the exact number of layers, structural properties, and energy of the vibration modes, which provide important insights into nanomaterials [31]. In Raman data measurements, Figure 3a,b focus on the crucial peaks associated with two vibrational modes (E_{2g} and A_{1g}) of MoS_2. The E_{2g} peak of MoS_2 is significantly influenced by its crystalline structure, particle size, and thickness during growth. Additionally, the A_{1g} peak vibration is related to the crystalline structure and

thickness of MoS_2, serving as an indicator of material quality. Figure 3c describes the Raman spectrum—an important indicator for understanding the physical properties and structure of monolayer and multilayer MoS_2 on the SiO_2/Si substrate. For monolayer MoS_2, the E_{2g} and A_{1g} peaks were observed at 382 cm^{-1} and 402 cm^{-1}, respectively. In contrast, for multilayer MoS_2, these peaks appeared at 380 cm^{-1} and 407 cm^{-1}, respectively. The E_{2g} peak (in-plane vibrational mode) involves parallel vibrations of Mo and S atoms within MoS_2. Additionally, the A_{1g} peak (out-of-plane vibrational mode) encompasses the vertical vibrations of S atoms [32]. The distance between the two peaks acts as an indicator, which directly represents the number of layers of MoS_2. It was confirmed that the distance between the peaks increases due to high-intensity vibrations as the number of layers increases.

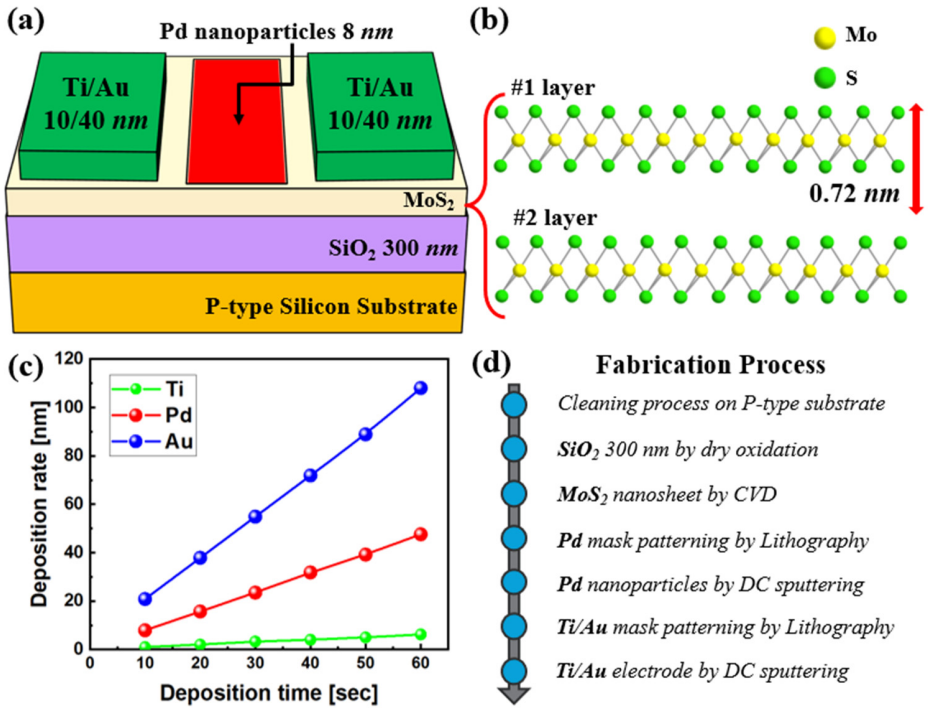

Figure 2. (**a**) The schematic diagram of the lateral-CF-based RRAM device with the Pd nanoparticles/MoS_2 nanosheet switching layer between the Ti/Au top electrode and Ti/Au bottom electrode; (**b**) The structure of monolayer MoS_2 (0.72 nm) or multilayer MoS_2 (1.44 nm) lattice layer; (**c**) Deposition rates of various metals (Ti, Pd, and Au) via DC sputtering; (**d**) The process flow chart illustrating the fabrication of the proposed RRAM architecture.

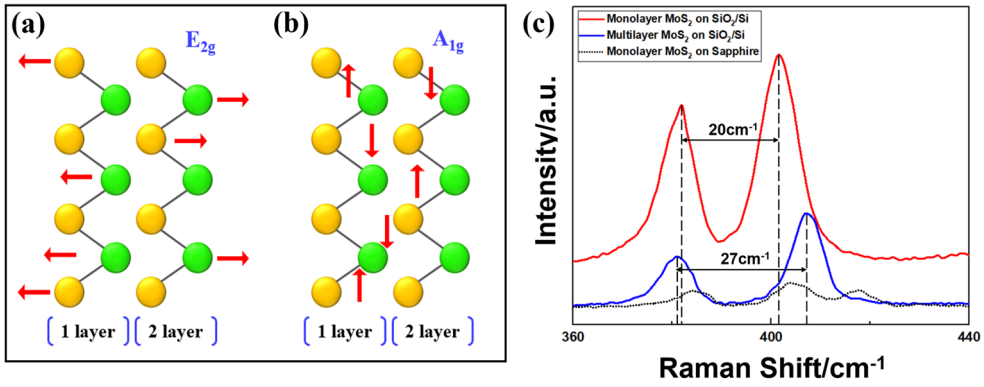

Figure 3. (**a**) E_{2g} band in-plane vibration of MoS_2; (**b**) A_{1g} band out-of-plane vibration of MoS_2; (**c**) Raman spectrum of monolayer MoS_2 and multilayer MoS_2 on the SiO_2/Si. Two vibrational modes (E_{2g} and A_{1g}) of MoS_2.

3.3. Photoluminescence Mapping

Photoluminescence (PL) spectroscopy is utilized to determine the material's electronic states, structural characteristics, and bandgap based on the energy of emitted photons. As illustrated in Figure 4a, PL signals were observed at room temperature using a 532 nm laser. For monolayer MoS_2 samples, it can be observed that the PL intensity exhibits a lower peak compared to multilayer MoS_2. Through PL mapping, MoS_2 synthesized via CVD techniques exhibits high-quality crystalline growth. Planck's constant (6.62×10^{-34} J·s), the speed of light (2.99×10^{8} m/s), Boltzmann's constant (1.38×10^{-23} J/eV), and wavelength are denoted as h, c, k, and λ, respectively, and Equation (1) is used to calculate the energy of emitted photons.

$$E = \frac{h \times c}{k \times \lambda} = \frac{1240}{\lambda}(eV) \quad (1)$$

Figure 4a shows that the PL peak of monolayer MoS_2 nanosheets appears at 660 nm, while that of multilayer MoS_2 nanosheets is located at 995 nm. Applying the conversion relationship between wavelength and photon energy, Figure 4b reveals that the bandgap of monolayer MoS_2 is extracted as 1.87 eV, while that of multilayer MoS_2 is observed to be 1.24 eV. Consequently, this aligns with the bandgap range typically known through research [33]. The intensity of the PL peak represents the efficiency of the light emission process occurring in MoS_2 [32].

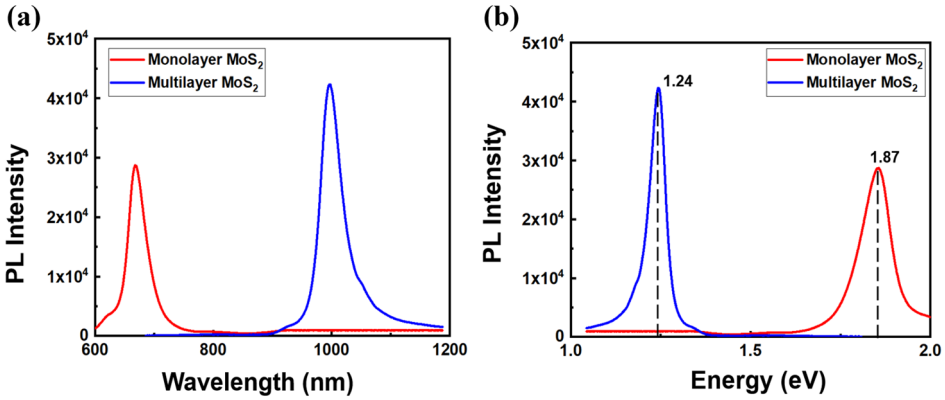

Figure 4. The scanning PL spectrum of both monolayer MoS_2 and multilayer MoS_2; (**a**) Wavelength; (**b**) Energy bandgap of the emitted photon.

4. Results and Discussion

The RS operation model in RRAM devices has typically been described using three main theoretical mechanisms. RS behaviors are influenced by factors such as the deposition thickness, length and width of the switching channel layer, device stack materials, the measurement environment, and RS operation parameters. Generally, thermal–chemical reactions, electrochemical metallization (ECM), and valence change mechanisms (VCM) are employed to explain RS behaviors. In STDP mechanism-based RRAM devices using MXs materials, the ECM model is recognized for forming conductive bridges through the movement of metal ions within the channel layer. In contrast, the VCM model regulates CFs by creating and recombining oxygen vacancies (V_o) induced by an electric field. In the initial state of VCM, an initial high-resistance state (HRS) is established with low concentrations of V_o within the MXs. Subsequently, when a forming voltage is applied to the TE, breakdown occurs within the MXs switching layer, leading to the generation of V_o and the formation of CFs through which the current flows between the electrodes. This phenomenon is commonly referred to as electroforming, characterized by the simultaneous increase in the electric field and temperature, resulting in positive feedback, which generates numerous V_o at once, causing a rapid change in the resistance state. MXs-based RRAM devices can modulate resistance by repeating the SET and RESET processes after the initial formation. Following the formation process, the application of voltage combines oxygen

ions with the filaments, thereby increasing resistance (HRS), which is a key aspect of the RESET process. The RESET process exhibits a more gradual resistance modulation compared to the formation process, as it involves the breaking of CFs, primarily occurring around the interfacial layers. Consequently, in the SET process, which reduces resistance to achieve a low-resistance state (LRS), the CFs reconnect to an even greater extent than during the formation stage. To summarize, by adjusting the voltage applied to the TE, MXs-based RRAM devices can achieve multiple distinct resistance states (HRS, LRS), along with gradual resistance modulation, reflecting variations in synaptic weights in neural network models. Recently, new conceptual models have been proposed to control the current paths by generating ions or vacancies using various switching channel materials, nanomaterials, and nanocomposites in RRAM cells [34,35]. In addition, CFs can be formed in the switching channel layer through nanoparticle-embedded effects and the physical and electrical molecular bonding layer.

4.1. Resistive Switching Mechanisms

The RS mechanism for Pd coated multilayer MoS_2 RRAM device is illustrated in Figure 5. An electrical RS operation (electronic migration by TE and electronic migration by Pd) has been conceived to form the S vacancy (V_s) filaments in the current paths [36]. Figure 5a shows the initial HRS with low concentrations of V_s distributed in the switching layer. When a forward voltage bias is applied to the TE, the switching layer collapses, and negatively charged S ions are accumulated under the TE. Through the SET process, the TiS_x layer is formed by reacting with Ti, as shown in Figure 5b [37]. Additionally, the S ions, which are far from the TE, form V_s filaments due to an electrical field caught in Pd nanoparticles. When a conductive filament connects the TE and BE, the RRAM cells cause an LRS. The migration of S ions in the active channel layer occurs as follows. The S ions, which are far from TE, are not subject to the electronic TE effect. However, S ions are formed via the electric field effect of Pd nanoparticles [38]. When the TE and BE are connected via the lateral CFs, the RRAM devices cause the LRS. Additionally, TE and Pd electronic migration was observed effectively in the formation of lateral CFs at the switching channel interface rather than in the channel. When a negative voltage bias is applied to the TE, the S ions migrate into the MoS_2 layer. As a result, the TiS_x layer decreases in size, and the CFs rupture, causing a transition to an HRS (RESET process).

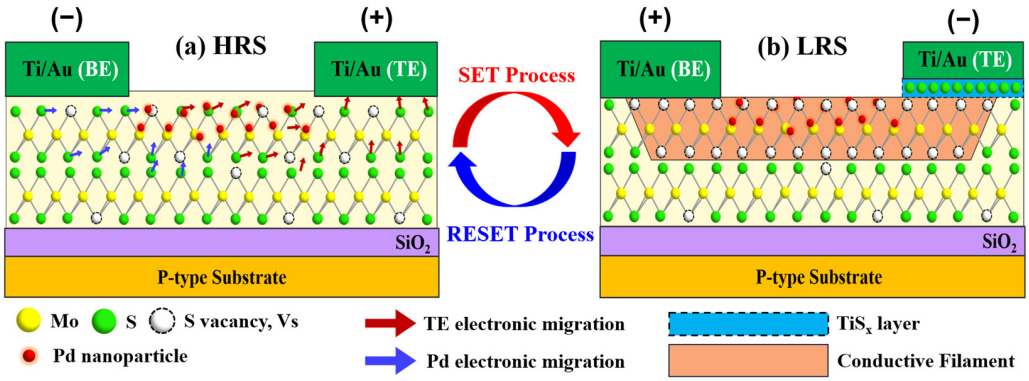

Figure 5. Resistive switching (RS) behavior in the Pd nanoparticle coating multilayer MoS_2 RRAM device is depicted. A schematic representation of the mechanisms for the lateral conductive filaments (CFs)-based RRAM device is shown: (**a**) High-resistance state (HRS, initial state); (**b**) Low-resistance state (LRS, after the SET process). The red and blue arrows indicate the direction of S-ion migration (electronic migration by TE and electronic migration by Pd).

4.2. I–V Measurement

The fabricated Pd-MoS_2 nanocomposite RRAM devices were measured at constant temperature and humidity with a vacuum probe station and semiconductor parameter analyzer (HP4156A). Bias was applied to the TE (size: 7000 μm × 2000 μm) with the

BE (size: 7000 µm × 2000 µm) grounded throughout the measurement process. The compliance current (CC) was set at a value of 20 µA to suppress the overcurrent through the device. Figure 6a illustrates the measured current–voltage (I–V) characteristics of the RRAM device, consisting of an ideal switching layer with multilayer MoS_2 (approximately two layers) and Pd nanoparticles (approximately 8 nm). Additionally, the parameters of the proposed RRAM include the total area (size: 1 cm^2), the lateral CFs-formed switching channel area (size: 7000 µm × 4000 µm), and the MoS_2/Ti contact interface width (channel width: 7000 µm). The normalized I–V curve was extracted by considering the channel width, which activated the formation of CFs in RRAM. Asymmetrical bipolar switching behavior was observed due to the Schottky barrier at the interface of multilayer MoS_2 and the electrode. The Schottky contact at the MoS_2/Ti interface prevented reverse current and allowed forward current to flow. In both the forward and reverse LRS, the rectifying current ratio (>6 × 10) was assessed by comparing the forward current ($I_{forward}$) of 0.612 µA at a forward voltage of +2 V with the reverse current ($I_{reverse}$) of 0.012 µA at a reverse voltage of −2 V. The selector-integrated RRAM controlled leakage current and exhibited self-rectifying operation. The RRAM with the Pd-nanoparticles embedded MoS_2 channel structure demonstrated bipolar switching, with continuous SET and RESET sweeps and stable RS behavior (V_{SET} = +4.75 V, V_{RESET} = −4.1 V), as shown in Figure 6b. When extracting the SET and RESET currents, the I_{SET} and I_{RESET} were found to be less than 1 µA, indicating excellent memory performance, such as low-power operation, high memory window on/off ratio (≈10^3), and nanoscale device fabrication. Furthermore, it appears that the issue of leakage current due to cross-talk in the RRAM array cells was addressed, and high-density memory array stacking was feasible. Table 1 summarizes the comparison of the device stack structure, nanocomposites based MoS_2, on/off ratio, and other parameters for the MoS_2 switching layer RRAM.

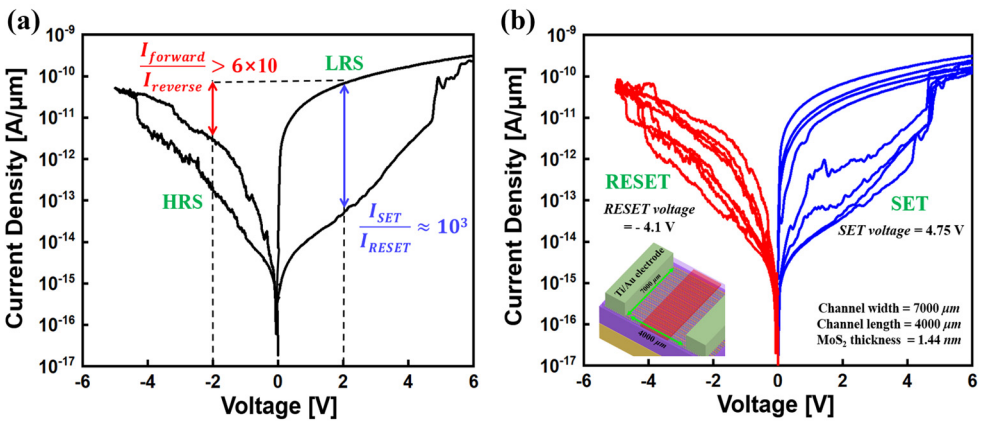

Figure 6. I–V characteristics of Au/Ti/Pd-MoS_2/Ti/Au RRAM. (**a**) Self-rectifying RS operation. A rectifying current ratio was observed at $I_{forward}$ (@ V = +2 V) and $I_{reverse}$ (@ V = −2 V). A memory window (≈10^3) was extracted; (**b**) I–V characteristics of Pd-MoS_2 RRAM for repeated voltage (−6 V to 6 V) sweeps. The switching channel width (7000 µm), switching channel length (4000 µm), and MoS_2 thickness (1.44 nm) are depicted in the RRAM diagram.

Table 1. Summary of the performance parameters of the RRAM device with the type of TE and BE, MoS_2-based switching layer, memory window, and rectifying current ratio.

TE and BE	Switching Layer	On/Off Ratio	Rectifying Ratio	Ref.
ITO and ITO	HfO_x/Pd-MoS_2	≈10^2	-	[3]
Au and Au	MoS_2	≈10^5	-	[28–31]
Au/Ti and Au/Ti	MoS_2	≈10^1	-	[36]
Ti and Pt	MoS_2	≈10^2	-	[37]
Ag and Ag	MoS_2/MoO_x	≈10^6	-	[39]
Au and TiN	HfO_x/MoS_2/TiO_x	≈10^6	-	[40]
Au/Ti and Ti/Au	Pd-MoS_2	≈10^3	>6 × 10	This work

5. Conclusions

This research work demonstrated an independent horizontal switching layer RRAM based on Pd-nanoparticle-decorated multilayer MoS_2. Through the optimization of Pd nanoparticle (approximately 8 nm) deposition via DC sputtering and MoS_2 nanosheet (approximately 1.44 nm) synthesis via CVD, we achieved the electrical migration of V_s and the formation of TiS_x in the switching channel layer. The lateral-CF-based RRAM device reduced the switching dispersion and enhanced the local electric field through the Pd nanoparticle doping method. The MoS_2/Ti contact formed sufficient Schottky barrier effects to exhibit non-linear I–V switching characteristics. The Pd-MoS_2 RRAM, which self-integrated without the need for a selector device, achieved a high memory window (approximately 10^3) and an asymmetric LRS with a rectifying current ratio (>6 × 10). Therefore, it is important to optimize the Pd nanoparticle deposition density, doping time, deposition thickness, and process conditions (temperature, humidity), in addition to analyzing transition metal activation. Furthermore, it is essential to assess the effects of the reduced length and width of the RRAM device's switching channel layer on the on/off current, operating voltage, and switching characteristics. Nanocomposite-based RRAM devices should address the leakage current due to cross-talk in nanoscale cell fabrication and high-density three demension stack arrays. Ultimately, the application of the 2D TMDs nanomaterial memristor platform presents a direction for emerging memory devices and intelligent memristor fields.

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Data Availability Statement: The data presented in this study are available in this article.

Conflicts of Interest: The authors declare no conflict of interest.

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