

Article

Switching Capacitor Filter with Multiple Functions, Adjustable Bandwidth in the Range of 5 Hz–10 kHz

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Abstract: This article proposes a second-order switch-capacitor filter that integrates low-pass, high-pass, band-pass, band-stop, and all-pass, and achieves flexible bandwidth adjustment of the filter through clock rate and capacitance ratio. The final filter design consists of two completely independent second-order switch-capacitor filter channels, and a 4-order Butterworth low-pass filter is designed through two-stage cascades. The two completely independent second-order switch-capacitor filters are integrated on a single chip and manufactured using the Huahong BCD350GE high-voltage 24 V process. The measurement results indicate that the proposed switch-capacitor filter achieves various functional filtering characteristics and achieves a bandwidth of 5 Hz to 10 kHz. The chip area is $5.1 \times 3.1 \text{ mm}^2$, powered by a dual power supply of $\pm 5 \text{ V}$, and the power consumption is 80 mW.

Keywords: switch-capacitor; second-order filter; rate; bandwidth; dual power



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1. Introduction

In wireless communication systems, filters are essential to obtain accurate signals. The multiple standardization of today's communication protocols makes the filter operating frequency band no longer monolithic, and considering compatibility, filters are required to achieve the filtering of harmful signals in different frequency ranges, so the bandwidth of the filter needs to be adjustable [1,2]. Currently, continuous-time analog filters often use an active resistor–capacitor structure, which is mainly composed of operational amplifiers, resistors R , and capacitors C , and can be applied to higher frequencies [3,4]. But in modern integrated circuit processes, the absolute values of resistors and capacitors are not precise enough, and there is a large absolute tolerance value, which limits the processing of high-precision analog signals. However, a switch-capacitor is used to simulate and replace the resistor so that the ratio of the capacitance is directly related to the accuracy of the signal, where the relative error between two capacitors can be minimized in a standard CMOS process [5]. Moreover, considering the area of the silicon wafer, a small capacitor can be simulated and replace a large resistance resistor, which can save a lot of area. Therefore, the analog filter implemented in the form of switch-capacitor can achieve the advantages of low power consumption, high accuracy, and small area [6–8]. At the same time, switch-capacitor filters also offer programmability options, making it possible to achieve modular and flexible architectures [9]. References [10–13] describe the design of switch-capacitor filters, but only the filtering characteristics of a certain function are designed separately, the range of applications is limited, and the bandwidth is not adjustable. References [14–16] describe the design with an adjustable bandwidth, but the range of adjustment is limited. In this paper, a second-order switch-capacitor filter based on the relationship between the transfer function characteristics of each function filter is designed by using switch-capacitor

technology, which integrates low-pass, high-pass, band-pass, band-stop, and all-pass. The programmable capacitance ratio method can flexibly adjust the bandwidth over a wide range and achieve different quality factor Q values. The second-order filter can be cascaded to form a higher-order filter.

The rest of this article is organized as follows: In Section 2, a second-order filter structure that integrates low-pass, high-pass, band-pass, band-stop, and all-pass is constructed based on the transfer functions of each power filter. Section 3 provides a specific design for the internal circuit and achieves adjustable bandwidth and Q value design. Section 4 completes the design of the fourth-order Butterworth low-pass filter by cascading the designed second-order filter. Section 5 completes the chip testing results. Sections 6 and 7 provide discussions and conclusions, respectively.

2. Circuit Structure

Starting from the theory of standard response of second-order filters, we study the response of second-order filters. It is not only important for the design of second-order filters, but also a fundamental requirement for designing high-order filters. Among all filtering function functions, the second-order filter response can be written as follows:

$$H(s) = \frac{N(s)}{(s/\omega_0)^2 + 2\zeta(s/\omega_0) + 1} \quad (1)$$

In the equation, $N(s)$ determines the functional characteristics of the filter, which is a polynomial of order 2 or less, ω_0 is the undamped natural frequency, and ζ is the damping coefficient. From the denominator of the above equation, it can be seen that this transfer function has two poles related to ζ :

$$p_{1,2} = \left(-\zeta \pm \sqrt{\zeta^2 - 1} \right) \omega_0 \quad (2)$$

When $\zeta > 1$, the poles are two negative real poles, and the natural response of the system consists of two decaying exponential terms. The system is stable and is referred to as overdamping. When $0 < \zeta < 1$, a pair of conjugate negative poles will be generated, and the natural response of the system consists of a decaying sine term. The system is stable and is called underdamped. When $\zeta = 0$, the poles appear on the imaginary axis, and the natural response of the system consists of a constant amplitude with a frequency of ω_0 sine term. When $\zeta < 0$, a pole appears in the right half plane, and the natural response of the system reveals that the system is unstable. Therefore, in filter design, we must ensure that $\zeta > 0$ to ensure the stability of the filter system.

The transfer functions of the second-order low-pass, band-pass, high-pass, band-stop, and all-pass filters in the s -domain are as follows:

low-pass:

$$H_{lp}(s) = \frac{H_0}{\frac{s^2}{\omega_0^2} + \frac{1}{Q} \frac{s}{\omega_0} + 1} \quad (3)$$

band-pass:

$$H_{bp}(s) = \frac{H_0 \frac{s}{\omega_0} \frac{1}{Q}}{\frac{s^2}{\omega_0^2} + \frac{1}{Q} \frac{s}{\omega_0} + 1} \quad (4)$$

high-pass:

$$H_{hp}(s) = \frac{H_0 \frac{s^2}{\omega_0^2}}{\frac{s^2}{\omega_0^2} + \frac{1}{Q} \frac{s}{\omega_0} + 1} \quad (5)$$

band-stop:

$$H_{np}(s) = \frac{H_0 \left(\frac{s^2}{\omega_0^2} + \frac{\omega_z^2}{\omega_0^2} \right)}{\frac{s^2}{\omega_0^2} + \frac{1}{Q} \frac{s}{\omega_0} + 1} \tag{6}$$

all-pass:

$$H_{ap}(s) = \frac{H_0 \left(\frac{s^2}{\omega_0^2} - \frac{1}{Q} \frac{s}{\omega_0} + 1 \right)}{\frac{s^2}{\omega_0^2} + \frac{1}{Q} \frac{s}{\omega_0} + 1} \tag{7}$$

where H_0 is the DC gain, ω_0 is the cutoff frequency (the center frequency of the band-pass and the band-stop filter), also known as the -3 dB frequency, Q is the quality factor of the filter, and ω_z is a zero introduced by the band-stop filter. According to the relationship of ω_z and ω_0 , band-stop filters can be divided into three types: standard band-stop, low-pass band-stop, and high-pass band-stop. If the zero frequency is the same as the pole frequency, it is a standard band-stop. If the zero frequency is greater than the pole frequency, it is a low-pass band-stop. If the zero frequency is less than the pole frequency, it is a high-pass band-stop.

From the above Formulas (3)–(7), it can be seen that their denominator contains the 2nd term of the complex frequency s , and an integrator circuit unit can generate the 1st term of the complex frequency s , as well as the 1st term circuit of s containing the value of Q . Therefore, the filter must contain two integrator circuits and arithmetic operation circuits. And the integrator circuits need to be connected in series to form the 2nd term of s . From the molecular point of view, the simplest is the low-pass filter, the DC gain is extracted beyond the fractional equation, and the molecular term is only 1. From the comparison of Equations (3) and (4), $H_{bp} = H_{lp} \times \frac{s}{\omega_0} \frac{1}{Q}$, it can be seen that the transfer function of the integrator circuit is $\frac{\omega_0}{s}$, which is the inverse function of the above equation, so the low-pass can be realized by the band-pass output and then through the integrator circuit. And the input signal and $\frac{1}{Q}$ of the band-pass signals attenuated are summed up, then standard band-stop filter can be realized, as shown in Figure 1.

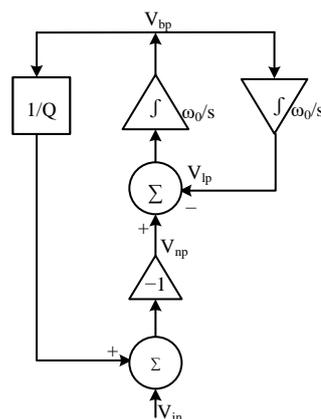


Figure 1. Structure of second-order filters (low-pass, band-pass, and standard band-stop).

The corresponding s -domain transfer function is:

low-pass:

$$\frac{Vlp}{Vi} = - \frac{1}{\frac{s^2}{\omega_0^2} + \frac{1}{Q} \frac{s}{\omega_0} + 1} \tag{8}$$

band-pass:

$$\frac{V_{bp}}{V_i} = -\frac{\frac{s}{\omega_0}}{\frac{s^2}{\omega_0^2} + \frac{1}{Q} \frac{s}{\omega_0} + 1} \tag{9}$$

band-stop (standard type):

$$\frac{V_{np}}{V_i} = -\frac{\frac{s^2}{\omega_0^2} + 1}{\frac{s^2}{\omega_0^2} + \frac{1}{Q} \frac{s}{\omega_0} + 1} \tag{10}$$

According to Formulas (5)–(7), it can be seen that the high-pass band-stop, high-pass, and all-pass filtered outputs can also be obtained through arithmetic operations on the low-pass and band-pass outputs, and their structures are shown in Figures 2a, 2b and 2c, respectively.

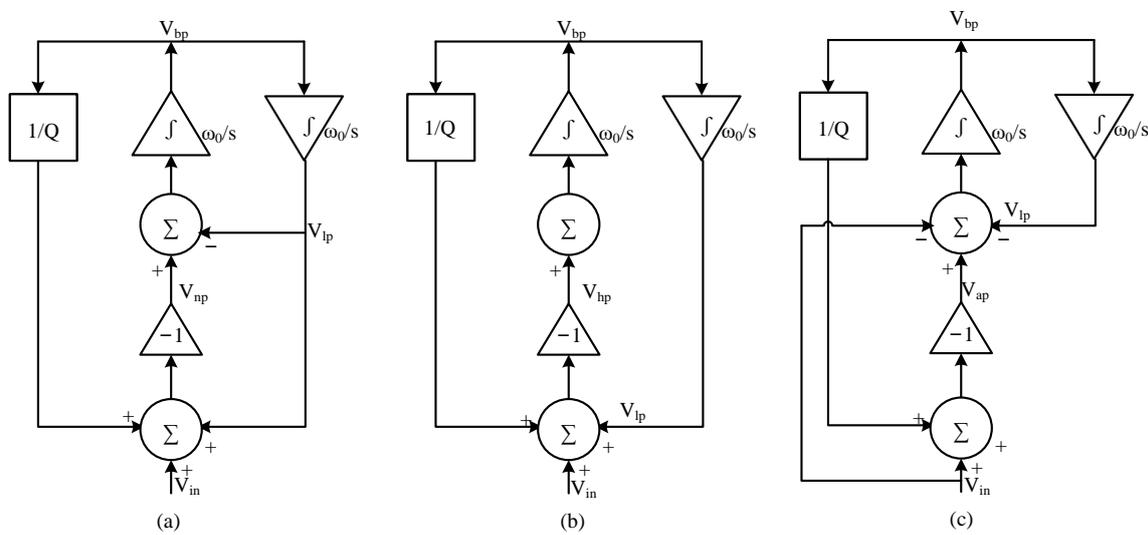


Figure 2. Structure of second-order filters: (a) high-pass band-stop, (b) high-pass, (c) all-pass.

In Figure 2a, its corresponding s-domain transfer function is:

low-pass:

$$\frac{V_{lp}}{V_i} = -\frac{\frac{1}{2}}{\frac{s^2}{2\omega_0^2} + \frac{1}{Q} \frac{s}{\sqrt{2}\omega_0} + 1} \tag{11}$$

band-pass:

$$\frac{V_{bp}}{V_i} = -\frac{\frac{1}{2} \frac{s}{\omega_0}}{\frac{s^2}{2\omega_0^2} + \frac{1}{Q} \frac{s}{\sqrt{2}\omega_0} + 1} \tag{12}$$

band-stop (high-pass type):

$$\frac{V_{np}}{V_i} = \frac{\frac{1}{2}(\frac{s^2}{\omega_0^2} + 1)}{\frac{s^2}{2\omega_0^2} + \frac{1}{Q} \frac{s}{\sqrt{2}\omega_0} + 1} \tag{13}$$

In Figure 2b, its corresponding s-domain transfer function is:

low-pass:

$$\frac{V_{lp}}{V_i} = -\frac{1}{\frac{s^2}{\omega_0^2} + \frac{1}{Q} \frac{s}{\omega_0} + 1} \tag{14}$$

band-pass:

$$\frac{V_{bp}}{V_i} = -\frac{\frac{s}{\omega_0}}{\frac{s^2}{\omega_0^2} + \frac{1}{Q} \frac{s}{\omega_0} + 1} \tag{15}$$

high-pass:

$$\frac{V_{hp}}{V_i} = \frac{\frac{s^2}{\omega_0^2}}{\frac{s^2}{\omega_0^2} + \frac{1}{Q} \frac{s}{\omega_0} + 1} \tag{16}$$

In Figure 2c, its corresponding s-domain transfer function is:

low-pass:

$$\frac{V_{lp}}{V_i} = -\frac{2}{\frac{s^2}{\omega_0^2} + \frac{1}{Q} \frac{s}{\omega_0} + 1} \tag{17}$$

band-pass:

$$\frac{V_{bp}}{V_i} = -\frac{2 \frac{s}{\omega_0}}{\frac{s^2}{\omega_0^2} + \frac{1}{Q} \frac{s}{\omega_0} + 1} \tag{18}$$

all-pass:

$$\frac{V_{ap}}{V_i} = -\frac{\frac{s^2}{\omega_0^2} - \frac{1}{Q} \frac{s}{\omega_0} + 1}{\frac{s^2}{\omega_0^2} + \frac{1}{Q} \frac{s}{\omega_0} + 1} \tag{19}$$

In order to save area, this article adopts the method of introducing taps at different positions in the same filter loop to achieve low-pass, high-pass, band-pass, band-stop, and all-pass filtering functions. The overall architecture is shown in Figure 3, where the module mode select is controlled by the two bit control words M0 and M1 to control the conduction states of switches S1, S2, and S3. The corresponding relationships are shown in Table 1, and the four operating modes, mode 1, mode 2, mode 3, and mode 4, correspond to the four filtering structures mentioned above. Compared to mode 1, mode 2 achieves the same functionality, but the Q value in mode 2 is $\sqrt{2}$ that in mode 1, which improves the quality factor and has a wider range of adaptation. The dashed boxes in Figure 3 represent the bandwidth and quality factor Q adjustment sections, respectively.

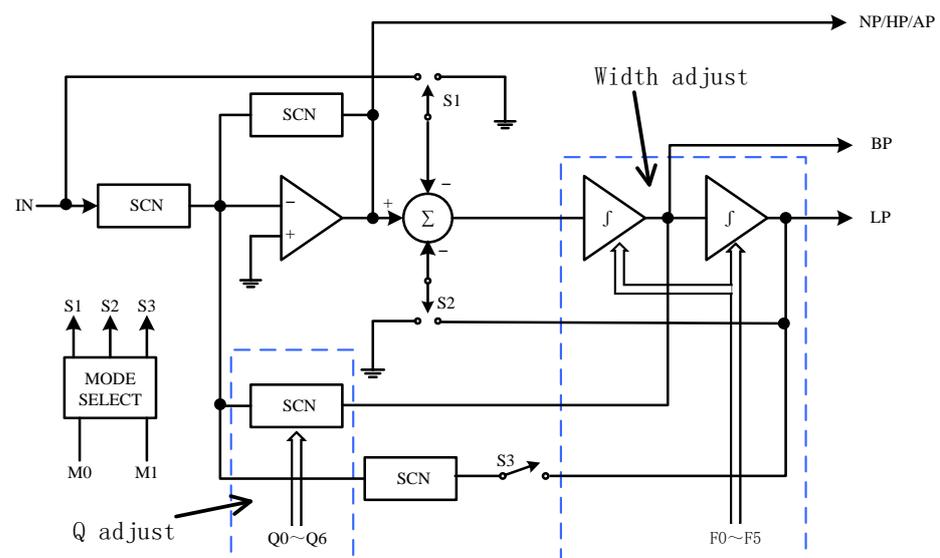


Figure 3. Overall structure of second-order filter.

Table 1. Working mode selection.

M1, M0	S3, S2, S1	Mode	Functions
00	000	mode 1	low-pass, band-pass, band-stop (standard)
01	100	mode 2	low-pass, band-pass, band-stop (high pass)
10	110	mode 3	low-pass, band-pass, high-pass
11	001	mode 4	low-pass, band-pass, all-pass

In order to achieve the fast simulation speed of AC characteristics and easy observation of impact response in transient simulation, the overall architecture adopts active RC mode for the switch-capacitor module SCN and integrator module, and then replaces resistors with capacitors. In the circuit, all devices adopt an ideal model without parasitic parameters, and the operational amplifier gain is set to 100 dB without bandwidth limitation. The corresponding simulation results under the four operating modes are shown in Figure 4. From the simulation results, it can be seen that this structure can fully achieve low-pass, high-pass, band-pass, band-stop, and all-pass filter functions.

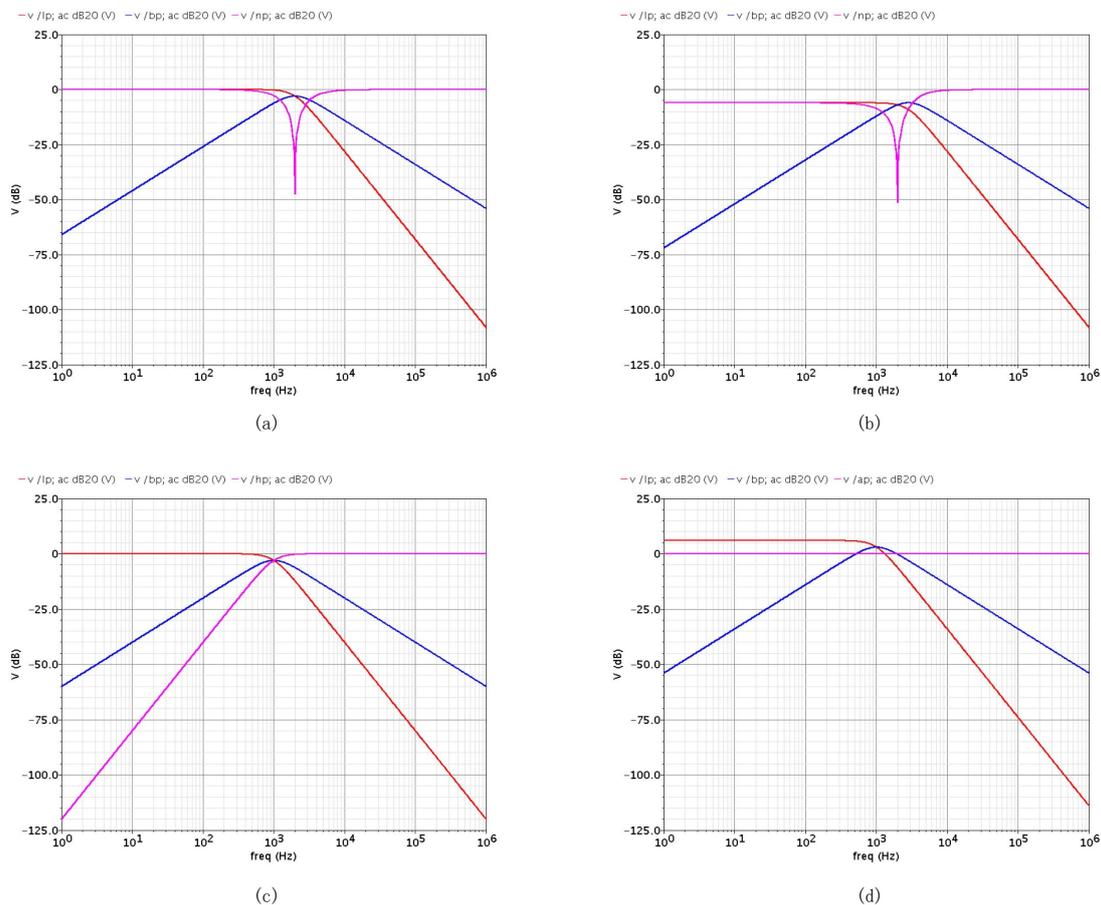


Figure 4. Simulation results: (a) working mode 1, (b) working mode 2, (c) working mode 3, (d) working mode 4.

3. Circuit Design

3.1. Switching Capacitance of Analog Resistors

Figure 5 shows the most common parallel switch-capacitor structure, which consists of two independent voltage sources V1 and V2, two controlled switches S1 and S2, and capacitor C [17]. This structure is simple and flexible in application, but there are various parasitic capacitors in the capacitors manufactured by CMOS technology. Among them, the

parasitic capacitance C_{tp} between the top plate and ground and the parasitic capacitance C_{bp} between the bottom plate and ground are the most difficult to handle, which can significantly affect the sampling accuracy and circuit performance [18–20]. In order to reduce this impact, a new structure has been designed based on the above structure, which is insensitive to parasitic capacitance. The circuit structure is shown in Figure 6, and two sets of controlled switches S3 and S4 have been added. Then, four sets of controlled switches are composed of two non-overlapping clocks ϕ_1 and ϕ_2 controls, with a clock frequency of f_{clk} .

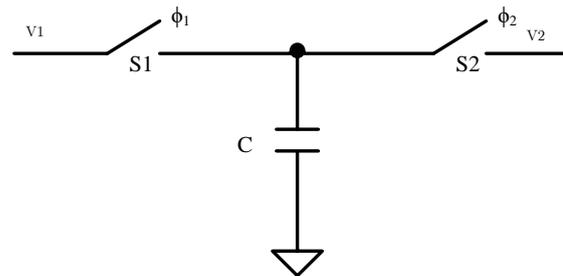


Figure 5. Structure of parallel switch-capacitors.

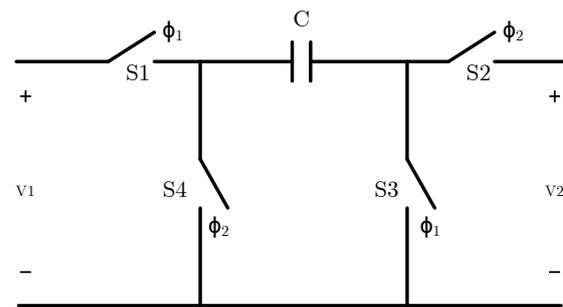


Figure 6. Switch-capacitor structure insensitive to parasitic capacitance.

At that time, the clock ϕ_1 is at a high level, switches S1 and S3 are on, S2 and S4 are off, and C is charged to V1. At that time, the clock ϕ_2 is at a high level, switches S2 and S4 are on, S1 and S3 are off, and C is discharged to V2. This results in an average current of:

$$\bar{I} = \frac{\Delta q}{T} = \frac{C(V1 - V2)}{T} \tag{20}$$

According to Ohm’s theorem, the equivalent resistance between V1 and V2 is:

$$R_{eq} = \frac{V1 - V2}{\bar{I}} = \frac{1}{Cf_{clk}} \tag{21}$$

If the clock frequency f_{clk} is 200 kHz, simulating a large resistor with a resistance value of 10 MΩ requires a capacitance value of 0.5 pF and consumes only 1% of the area of the silicon formed resistor made by the standard CMOS process [21]. In addition, filters implemented using switch-capacitor technology have higher accuracy than traditional RC structure filters, where the time constant is:

$$\tau = RC_F \tag{22}$$

Therefore, the error of the time constant comes from the error of the capacitance and resistance values during the chip manufacturing process. As the manufacturing process is separate, the error generated by the capacitance and resistance during the chip manufac-

turing process can be calculated separately. Below, we will calculate the error of the time constant caused by the resistance and capacitance separately as follows:

$$\frac{d\tau}{\tau} = \frac{d(RC_F)}{(RC_F)} = \frac{dR}{R} + \frac{dC_F}{C_F} \tag{23}$$

Under existing process conditions, the error in the capacitance and resistance values brought about during the chip casting process can be controlled below 10%. However, for the overall filter circuit, there may be a 20% error in the process production process, which is unbearable for many application systems. When using switch-capacitor simulation resistance technology, the time constant τ can be expressed as:

$$\tau = RC_F = \frac{C_F}{C_I f_{clk}} \tag{24}$$

Therefore, its error can be calculated as:

$$\frac{d\tau}{\tau} = \frac{d\left(\frac{T}{C_I} C_F\right)}{\left(\frac{T}{C_I} C_F\right)} = \frac{dT}{T} + \frac{dC_F}{C_F} - \frac{dC_I}{C_I} \approx \frac{d\left(\frac{C_F}{C_I}\right)}{\left(\frac{C_F}{C_I}\right)} \tag{25}$$

From the above equation, it can be seen that the precision of the time constant τ depends on the clock cycle and the matching degree of the two capacitors. In the existing process environment, the error of the crystal oscillator clock can be controlled within 0.001%, then $\frac{dT}{T} = 0$. Hence, compared to traditional active filters, the error of the time constant of switch-capacitor filters is only affected by the ratio of the two capacitors [22–24]. Under existing process conditions, the relative error caused by manufacturing two capacitors with precise ratios is very small, not exceeding 0.05%. Switching capacitor technology greatly optimizes the accuracy of the filter.

3.2. Switch-Capacitor Integrator

The switch-capacitor integrator adopts a switch-capacitor structure that is not sensitive to parasitic capacitance [25,26], as shown in Figure 7. In order to facilitate the analysis of the impact of parasitic capacitance, parasitic capacitance has been added to the figure. The clock timing diagram of two non-overlapping phases is shown in Figure 8.

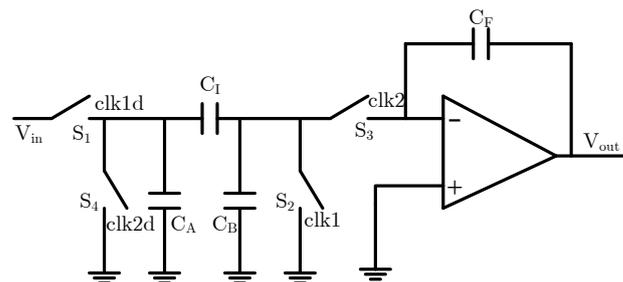


Figure 7. Switch-capacitor integrator with parasitics.

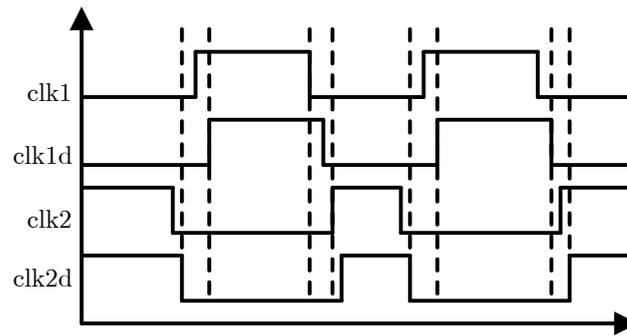


Figure 8. Two-phase non-interleaved clock timing diagram.

In Figure 7, C_A and C_B are the parasitic capacitances of the sampling capacitor C_I at the upper and lower plates A and B, respectively. The clock signals clk1 , clk2 , and their respective delay signals clk1d and clk2d control different switches. The two phases are as follows:

- (1) Sampling phase. From the timing diagram, it can be seen that the arrival of clk1 causes the S2 switch to close first, causing a short circuit at both ends of the parasitic capacitor C_B . The charge on it is cleared, and then S1 closes. The input signal V_{in} charges the C_I until clk1 flips to 0. S2 first opens, and point B is suspended. The charge stored at point B will not lose or change, and then switch S1 opens. The injection effect caused by switch S1 will not cause any change in the integral charge.
- (2) Integration stage. From the timing diagram, it can also be seen that the switch S3 controlled by clk2 is first closed. Due to the virtual short circuit of the ideal operational amplifier (i.e., the closed-loop feedback of the operational amplifier), the parasitic capacitance C_B is shorted at both ends, and the charge only exists at the left end of C_I . When S4 is closed, C_A is shorted, the virtual short circuit of the operational amplifier causes the C_I to be shorted as well. The charge at the A end is discharged to the ground, and the charge at the B end is fully forced to the integrating capacitor C_F , thus this realizes integration operation. In the final stage, S3 is disconnected first, so that the injection effect caused by the disconnection of the previous stage S4 does not change the integration result [27].

3.3. Switch Circuit

During the operation of MOS switches, there are three mechanisms that generate corresponding errors, namely, channel charge injection, clock feedthrough, and switch thermal noise. They will generate gain errors, DC offset, and nonlinear errors to varying degrees. Below, we will discuss these error factors separately and then complete the design of the switch circuit based on the analysis.

3.3.1. Switch Error

When the MOS switch is on, V_{in} charges the sampling capacitor to make $V_{in} = V_{out}$, and after charging is completed, there is still an inversion layer charge in the channel. After the switch is disconnected, this part of the charge will be randomly injected into the source and drain stages. Taking NMOS as an example, as shown in Figure 9, this will make the charge on the sampling capacitor C_H not equal to $V_{in}C_H$. The amount of charge in the channel is:

$$Q_{ch} = WLC_{ox}(V_{DD} - V_{in} - V_{TH}) \quad (26)$$

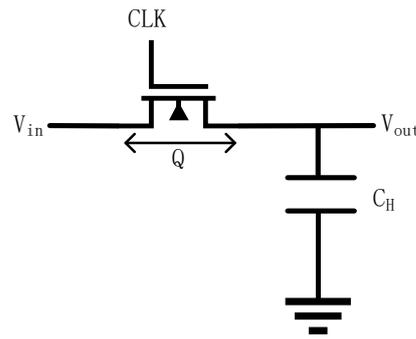


Figure 9. Channel injection effect.

If channel charges are uniformly injected into the source and drain electrodes, a bias voltage difference of ΔV is generated on the sampling capacitor C_H :

$$\Delta V = \frac{WLC_{ox}(V_{DD} - V_{in} - V_{TH})}{2C_H} \tag{27}$$

This voltage error will cause a negative step in the voltage drop across the sampling capacitor C_H . Similarly, if the switch is PMOS, the output voltage drop will have a positive step. The steps of these two voltage drops are exactly opposite, so the design of the switching circuit utilizes this to improve the consequences of channel charge injection effect.

Due to the difficulty in determining the distribution of channel charge Q_{ch} between the source and drain terminals, considering the worst-case condition where all channel charges are injected into the sampling capacitor C_H , the final result of V_{out} is:

$$V_{out} = V_{in} - \frac{WLC_{ox}(V_{DD} - V_{in} - V_{TH})}{C_H} = V_{in} \left(1 + \frac{WLC_{ox}}{C_H} \right) - \frac{WLC_{ox}}{C_H} (V_{DD} - V_{TH}) \tag{28}$$

The above equation indicates that the channel charge injection effect can bring both gain error and DC offset [28]. According to the above formula, we can reduce the deviation of the output voltage by reducing the size of the MOS transistor switch or increasing the sampling capacitor C_H . However, both of these methods will slow down the circuit speed and cause greater performance damage in high-frequency operating environments. Therefore, we cannot use this method to reduce the channel charge injection effect.

The second error caused by the switch is clock feedthrough. Due to the presence of gate source and gate drain capacitors in MOS switches, when the clock flips, these two capacitors will also transfer the charges stored on them to the sampling capacitor, resulting in sampling error, as shown in Figure 10.

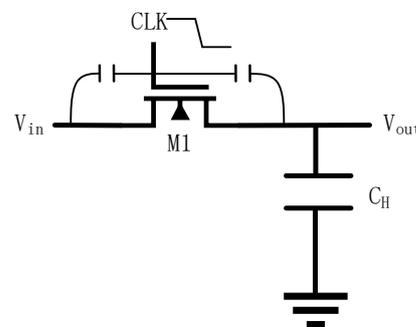


Figure 10. Clock feedthrough effect.

The error caused by clock feedthrough can be expressed as:

$$\Delta V = V_{CK} \frac{WC_{OV}}{WC_{OV} + C_H} \tag{29}$$

Among them, C_{OV} is the unit overlap area capacitance at the gate source interface or the gate drain interface, and V_{CK} is the clock pulse voltage. From the above equation, it can be seen that reducing the width of MOS switches can weaken the impact of clock feedthrough effect, but this also reduces the switching speed.

The third error caused by a switch is the thermal noise of the switch. As long as there is a resistance in the circuit, thermal noise will be generated, and the switch has a conducting resistance. During the sampling and integration stages, thermal noise can have an impact, which can affect the output voltage. However, the magnitude of the noise is not related to the switch conduction resistance value, but rather to the position of the noise generating module. The closer to the input port, the greater the noise, so the sampling capacitance should be larger. However, this directly affects the area of the chip capacitance.

3.3.2. Switch-Circuit Design

In the above three mechanisms, except for the third type of thermal noise, the other two types of error are directly related to the size of the switch MOS. The smaller the size of the switch MOS, the smaller the error caused. So usually, the length is chosen to be close to the minimum size of the process. To ensure a certain speed, the width is chosen to be several to several tens of times the length. In CMOS switches, due to the opposite channel charges between PMOS and NMOS transistors, this can compensate for most of the errors caused by channel charge injection. At the same time, the conduction switches of PMOS and NMOS transistors complement each other, and the clock feedthrough effect can also be mutually suppressed. If PMOS and NMOS choose the same size, the errors caused by channel charge injection and clock feedthrough can completely cancel each other in the first-order approximation. That is to say, CMOS switch transistors can provide higher accuracy than single MOS transistors. Meanwhile, due to the fact that CMOS switches connect two single MOS switches in parallel, the conduction resistance of CMOS switches is smaller than that of single MOS switches, and its conduction resistance should also be small as the input signal changes. Therefore, the switch circuit adopts a transmission gate switch, and its circuit structure is shown in Figure 11.

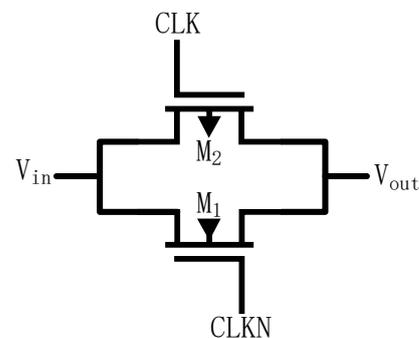


Figure 11. Transmission gate switch.

According to the derivation in Section 3.3.1, NMOS and PMOS transistors will generate two steps with opposite polarity directions. To eliminate the steps, the parameters of NMOS and PMOS transistors in the transmission gate must meet the following equation:

$$W_1 L_1 C_{ox} (V_{CK} - V_{in} - V_{THN}) = W_2 L_2 C_{ox} (V_{in} - |V_{THP}|) \quad (30)$$

By optimizing and adjusting the size of NMOS and PMOS transistors, the steps brought by switch sampling are minimized. Figure 12 shows the steps brought by the NMOS transistor switch, Figure 13 shows the steps brought by the PMOS transistor switch, and Figure 14 shows the steps brought by the transmission gate switch.

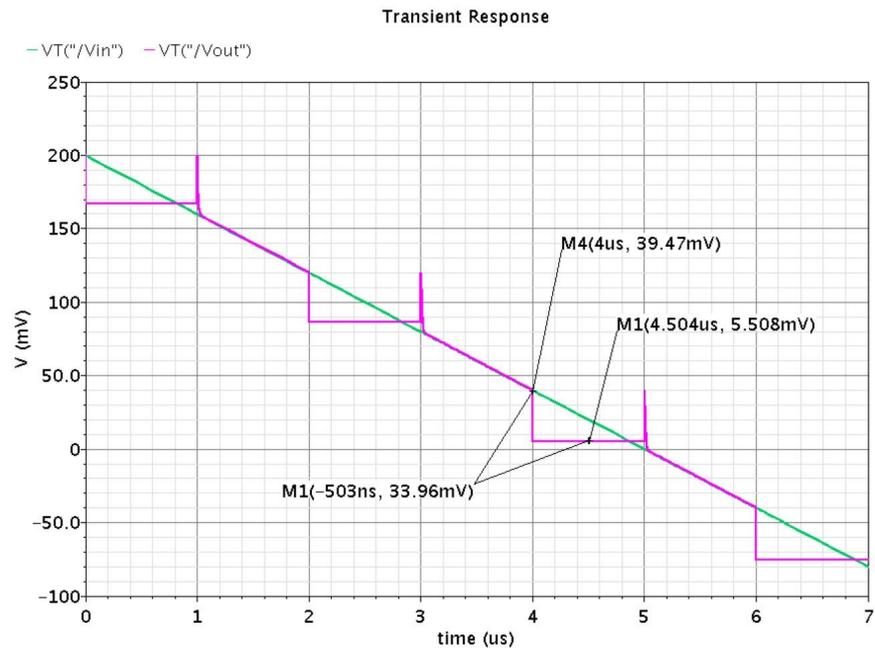


Figure 12. Steps brought by NMOS transistor switches.

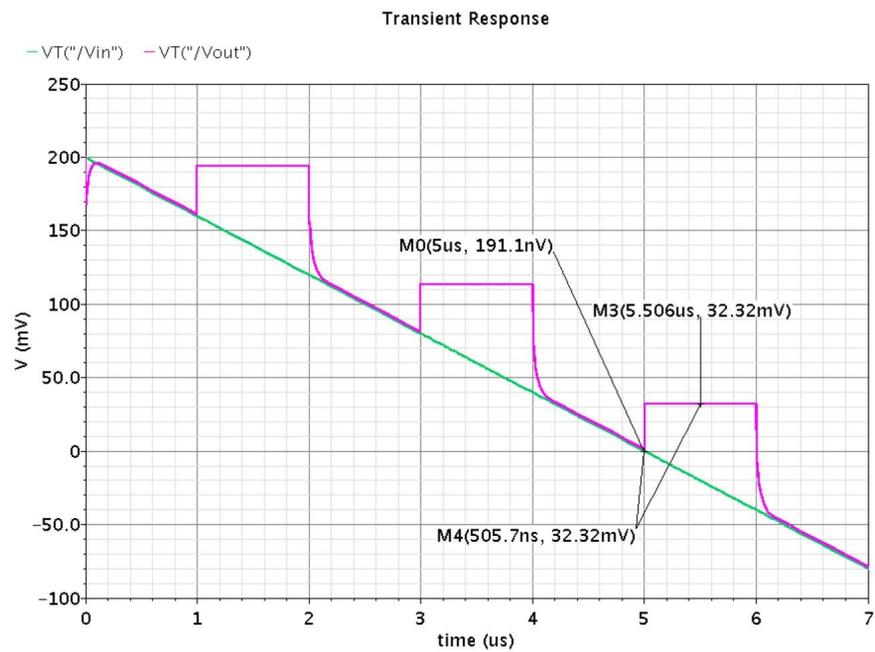


Figure 13. Steps brought by PMOS transistor switches.

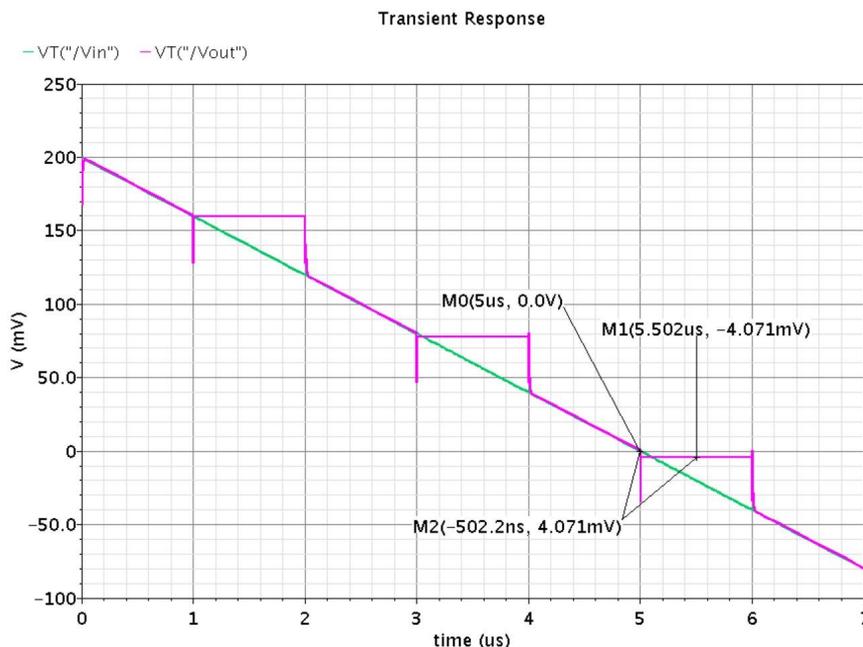


Figure 14. Steps brought by the transmission gate switch.

From the above figure, it can be seen that the negative step size brought by the NMOS transistor switch is 33.96 mV, the positive step size brought by the PMOS transistor switch is 32.32 mV, and the step size brought by the complementary use of the transfer gate switch is 4.07 mV, greatly reducing the impact of the switch channel charge injection effect on the overall circuit.

3.4. Operational Amplifier

In previous system architectures and simulations, operational amplifiers were considered an ideal component. In practical situations, operational amplifiers are not ideal. Thus, it is necessary for us to analyze the impact of some non-ideal characteristics of operational amplifiers on switch-capacitor filters [29] in order to help us obtain reasonable design indicators for operational amplifiers and guide design.

3.4.1. The Impact of Limited DC Gain

The most basic unit of a cascaded switch-capacitor filter is a switch-capacitor integrator. Figure 7 shows a parasitic capacitor insensitive inverse integrator. The limited DC gain of the operational amplifier is A_0 , and the most direct impact to the integrator is that the potential at the inverting input end of the operational amplifier is no longer zero, but $-V_{out}/A_0$, which is related to the output signal.

Considering $V_X = -V_{out}/A_0$, the calculated transfer function is:

$$H(e^{j\omega T}) = [1 + m(\omega)]e^{j\theta(\omega)} \cdot H_0(e^{j\omega T}) \tag{31}$$

Among them, $H_0(e^{j\omega T})$ is the integrator transfer function for ideal operational amplifiers, $m(\omega)$ and $\theta(\omega)$ represent the amplitude error and phase error, respectively. We assume that $m(\omega) \ll 1$, $\theta(\omega) \ll 1$, $\omega T \ll 1$, then near the cutoff frequency there are:

$$m(\omega) \approx -\frac{1}{A_0} \left(1 + \frac{C_I}{2C_F} \right) \approx -\frac{1}{A_0} \tag{32}$$

$$\theta(\omega) \approx \frac{1}{A_0} \frac{C_I/C_F}{\omega T} \approx \frac{1}{A_0} \tag{33}$$

Among them, the amplitude error $m(\omega)$ can be directly equivalent to the ratio error of capacitance C_I and C_F . For an integrating circuit with an operational amplifier gain $A_0 = 1000$, the amplitude error is 0.1%, which is on the same order of magnitude as the capacitance mismatch, so the amplitude error can be ignored. However, phase error is not the case, as it can affect the pole position of the integrator, thereby affecting the pole distribution of the filter. Phase error will affect the center frequency of the filter ω_0 and quality factor Q . When the operational amplifier gain $A_0 = 1000$, the impact of phase error on the center frequency can be ignored, while the impact on the quality factor Q is not the same. The quality factor Q when considering the finite gain of the operational amplifier is approximately related to the quality factor Q_0 when considering the ideal operational amplifier, as follows:

$$\frac{1}{Q} = \frac{1}{Q_0} + \frac{2}{A_0} \quad (34)$$

For filters with higher Q values, this impact cannot be ignored. Assuming $Q_0 = 20$ and $A_0 = 1000$, we can calculate $Q = 19.2$, which is a relatively large error. We may be able to increase the DC gain of the operational amplifier a bit. When $A_0 = 10,000$, $Q = 19.92$ can be calculated, which is a relatively satisfactory result. Therefore, in our subsequent design, designing the DC gain of the operational amplifier to be above 80 dB is a reasonable indicator.

3.4.2. The Impact of Limited Unit Gain Bandwidth

We still analyze the impact of limited unit gain bandwidth from the perspective of integrators. Firstly, similar to limited DC gain, a limited unit gain bandwidth can bring amplitude error $m(\omega)$ and phase error $\theta(\omega)$ to the transfer function of the integrator. Here, we directly cite the conclusions of the literature, and in the worst-case scenario:

$$|m(\omega)| \approx |\theta(\omega)| \approx \omega T \exp\left(-\frac{\omega_{GB} T}{2}\right) = \omega T \exp\left(-\frac{\pi f_{GB}}{f_c}\right) \quad (35)$$

Among them, ω is the angular frequency of the signal, f_{GB} is the unit gain bandwidth of the operational amplifier, and f_c is the clock frequency. When $f_{GB} \geq 5f_c$, the error is already much less than one-thousandth. From this perspective, $f_{GB} \geq 5f_c$ is sufficient.

Another more important impact of limited unit gain bandwidth is speed, which directly affects the linear establishment speed of small signals. For a single pole operational amplifier, considering the finite unit gain bandwidth, its open-loop transfer function is:

$$H(s) = \frac{-A_0}{1 + 1/\omega_1} \quad (36)$$

ω_1 is the main pole of the operational amplifier. After being connected into a closed loop, the step response of the output voltage is established in exponential form:

$$V_{out} = 1 - \exp\left(-\frac{t}{\tau}\right) \quad (37)$$

The time constant τ directly affects the establishment speed, and the expression is:

$$\tau = \frac{1}{\beta\omega_{GB}} = \frac{1}{2\pi\beta f_{GB}} \quad (38)$$

Among $\beta = C_F/(C_I + C_F)$ is the feedback coefficient (in switched-capacitor filters, the integral capacitor C_F is often much larger than the switching capacitor C_I , and the feedback coefficient is close to 1). In our design, β has a minimum of approximately 0.8. For a 0.1% small signal establishment accuracy, the required establishment time t_{set} is approximately

7τ . We hope that t_{set} cannot exceed half of the clock cycle T ; perhaps $t_{set} = T/3$ is a good choice, which is $7\tau = T/3$. Bringing it into Equation (38) and selecting $\beta = 0.8$ can obtain:

$$T = 21\tau = \frac{21}{0.8 * 2\pi * f_{GB}} \quad (39)$$

It can be concluded that:

$$f_{GB} = \frac{21}{0.8 * 2\pi * T} \approx 4.2f_c \quad (40)$$

Therefore, considering both accuracy and speed, the unit gain bandwidth of the operational amplifier needs to meet $f_{GB} \geq 5f_c$. However, due to the presence of parasitic capacitance, the feedback coefficient of the integrator β becomes less than 0.8, the unit gain bandwidth of the operational amplifier also needs to be correspondingly increased to meet the requirements of establishment speed. These are relative to single pole operational amplifiers, and in practice we may use two-stage operational amplifiers, namely, dual pole operational amplifiers. For bipolar operational amplifiers, due to the signal passing through two RC delays, the step response speed will be slower compared to single pole operational amplifiers. This requires the operational amplifier to have a higher unit gain bandwidth. However, a higher unit gain bandwidth means a wider white noise spectrum and higher white noise energy. We know that noise folding is inevitable in switch-capacitor circuits. Thus, a higher unit gain bandwidth will result in higher white noise energy being generated within the passband. This is not what we hope for. Therefore, considering all factors, we choose $5f_c \leq f_{GB} \leq 10f_c$.

3.4.3. Operational Amplifier Circuit Design

For the analysis of the above operational amplifier, we adopt a two-stage operational amplifier, whose structure is shown in Figure 15. It consists of a two-stage amplifier and a phase compensation circuit. The first stage amplifier consists of M1, M2, M3, M4, and M5, which convert the differential mode input voltage into a differential mode current. This differential mode current acts on the current mirror load composed of M3 and M4 to restore the differential mode voltage. The second stage amplifier is composed of M6 and M7, with M6 as the input and amplifier tube of the second stage amplifier and M7 as the load of the current source. C is the compensation circuit. Figure 16 shows the amplitude frequency phase frequency characteristic curve of the amplifier. The low-frequency gain of the amplifier is 93 dB, the unit gain bandwidth is 6.3 MHz, and the phase margin is 64° .

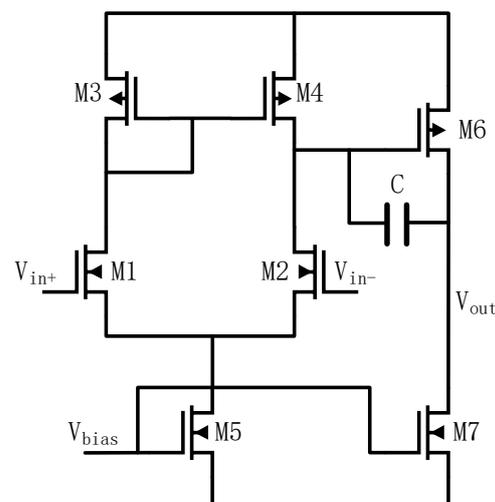


Figure 15. Operational amplifier structure.

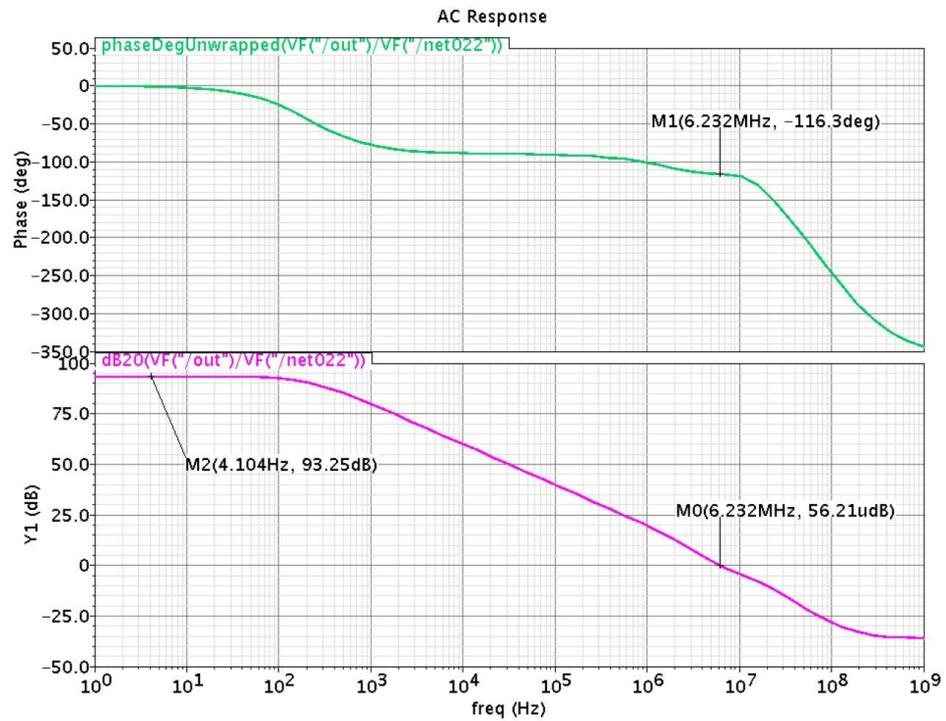


Figure 16. Operational amplifier Bode diagram.

3.5. Clock Circuit

The design of the switch-capacitor integrator adopts a structure that is insensitive to capacitors, so its clock requirements are very important. The design introduces two-phase non-interleaved clocks, and in order to eliminate the uncertainty of the input clock duty cycle, the input clock signal is processed in 2-division frequency with a duty cycle of 50%. The schematic structure of clock generation is shown in Figure 17.

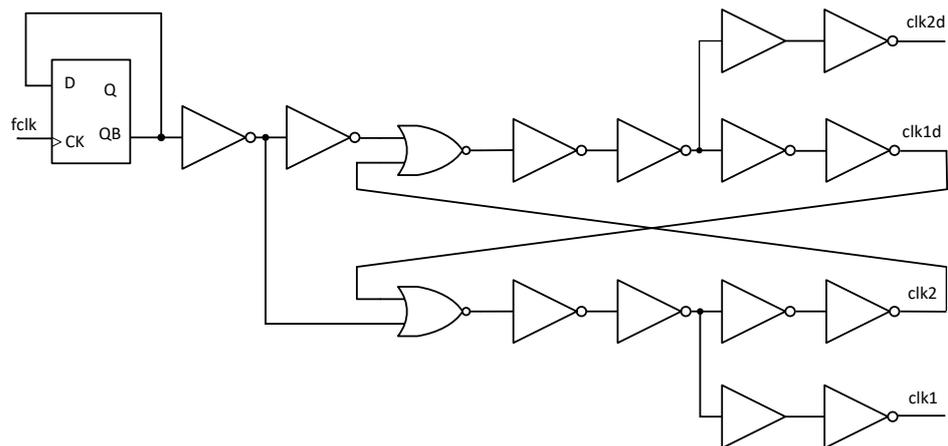


Figure 17. Clock circuit.

This structure starts with a D flip-flop for division by 2, followed immediately by inverters, NOR gates, and AND gate to accomplish a two-phase non-interleaved clock output. The series inverters constitute a delay circuit, and the more inverters in series, the longer the time the pulses do not overlap. When designing the size of the inverter, the driving problem needs to be considered. In order to improve the driving ability, the size of the series inverter link should be gradually increased, especially for the inverter at the output position.

3.6. Adjustable Bandwidth Design

The combination of switch and capacitor realizes the simulation of resistance; the principle of operation is essentially to simulate the process of resistance “carrying” charges. Due to the clock signal being divided by 2, the equivalent impedance of the switch-capacitor is:

$$R_{eq} = \frac{1}{C_I \times \frac{1}{2}f_{clk}} \tag{41}$$

The pole formula of the integrator circuit is:

$$\omega_0 = \frac{1}{R_{eq} \times C_F} \tag{42}$$

Bringing Equation (41) into Equation (42) yields

$$f_0 = \frac{\omega_0}{2\pi} = \frac{C_I \times f_{clk}}{4\pi \times C_F} \tag{43}$$

where C_I is the sampling capacitance of the integrator and C_F is the holding capacitance of the integrator. According to the above Equation (43), it can be seen that bandwidth can be adjusted by changing the ratio of clock frequency to capacitance without changing the original structure of the circuit [30]. The C_F value in this article adopts programmable output, and its structure is shown in Figure 18. The six switches connected to the output end of the operational amplifier use complementary CMOS transmission gates due to signal passage. The six switches connected to the ground wire only require a single NMOS transistor. The switch group is jointly controlled by control positions $F5 \sim F0$ and their reverse positions $\bar{F5} \sim \bar{F0}$. In order to obtain accurate ratio relationships and layout, $1/8C_I$ is set as the minimum unit capacitance C_{unit} , and the C_F value can be programmed as an integer multiple of the fixed unit capacitance, with a range of $64C_{unit}$ to $127C_{unit}$. Therefore, the calculation formula for frequency and control words is as follows, where N is an integer from 0 to 63.

In mode 1, mode 3, and mode 4 operating states:

$$\frac{f_{clk}}{f_0} = (64 + N) * \frac{\pi}{2} \tag{44}$$

In mode 2 operating states:

$$\frac{f_{clk}}{f_0} = \frac{1}{\sqrt{2}} * (64 + N) * \frac{\pi}{2} \tag{45}$$

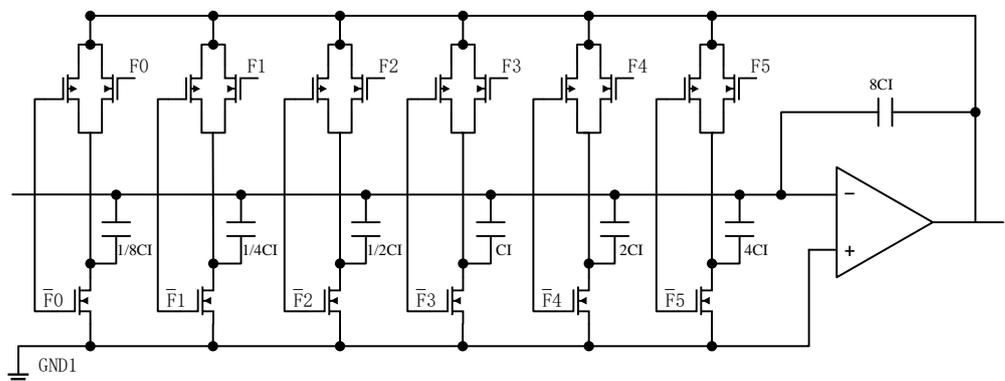


Figure 18. Switching integral capacitor.

Set f_{clk} to 200 kHz and Q to 1. Under operating mode 1, change C_F to simulate the low-pass, band-pass, and band-stop outputs of the second-order switch-capacitor filter as shown in Figure 19. Red represents $N = 0$, green represents $N = 32$, and blue represents $N = 63$.

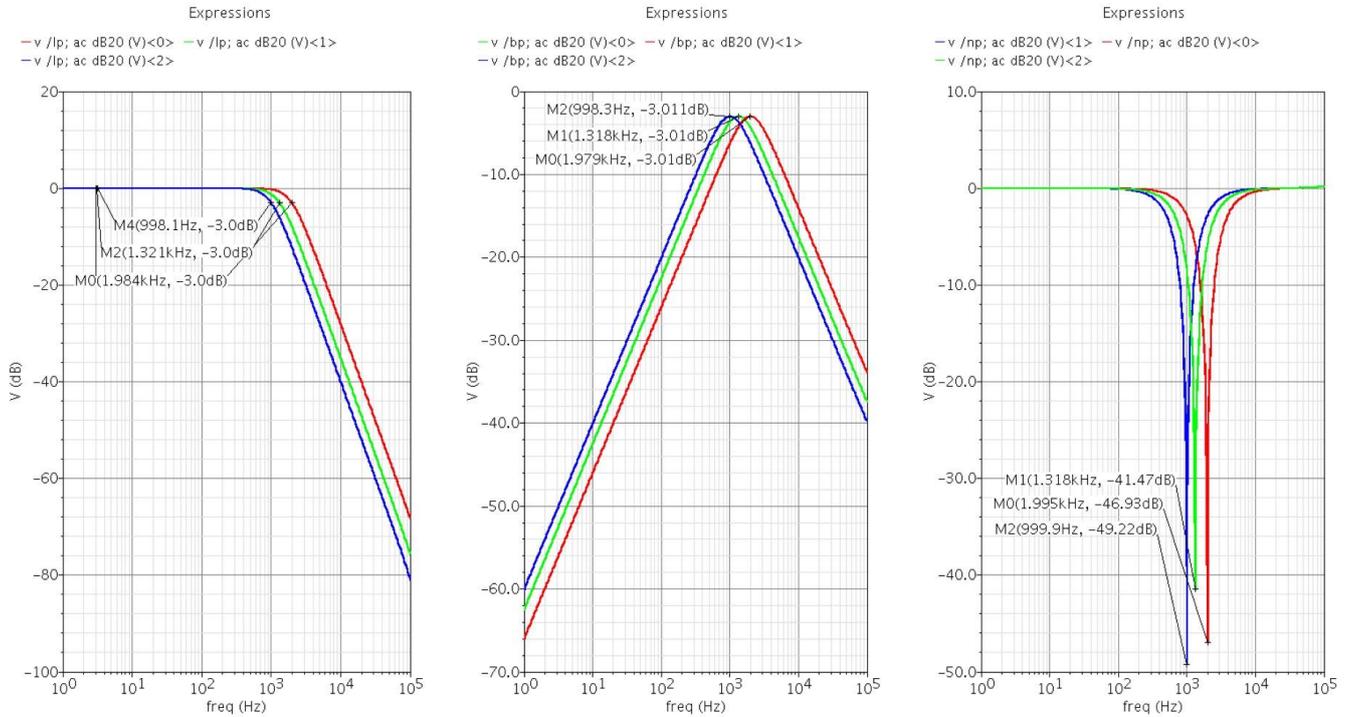


Figure 19. Bandwidth adjustment simulation.

3.7. Q-Adjustable Design

In order to make the designed filter more adaptable, the Q value is also adjustable. The Q value affects the attenuation speed of the filter transition band. The larger the Q , the faster the attenuation, the steeper the amplitude frequency curve, and the faster the phase change. The Q -value adjustable method is the same as the bandwidth adjustment method, and it is also obtained through different capacitance ratios. The structure of the adjustable capacitance part is shown in Figure 20, where the switches controlled by Q_6 to Q_0 adopt the same structure as in Figure 18, and 128 levels of Q -value adjustable are achieved through 7-bit control bits. In order to save area, C_1 in the figure is set to $32C_{unit}$. The relationship between Q value and control word is as follows, where N is $0 \sim 127$ (where switches $Q_6 \sim Q_0$ are low level and the switch is conductive).

In mode 1, mode 3, and mode 4 operating states:

$$Q = \frac{64}{128 - N} \tag{46}$$

In mode 2 operating states:

$$Q = \sqrt{2} * \frac{64}{128 - N} \tag{47}$$

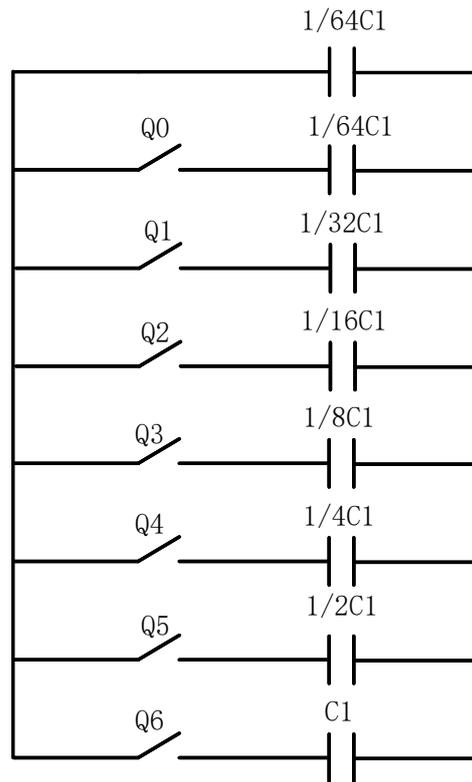


Figure 20. Q-value adjustable capacitor structure.

Set $f_{clk} = 200$ kHz, $f_0 = 2$ kHz, and adjust the Q value under working mode 1. The band-stop output is shown in Figure 21. Red represents $N = 0$ ($Q = 0.5$), green represents $N = 64$ ($Q = 1$), blue represents $N = 96$ ($Q = 2$), and black represents $N = 124$ ($Q = 16$).

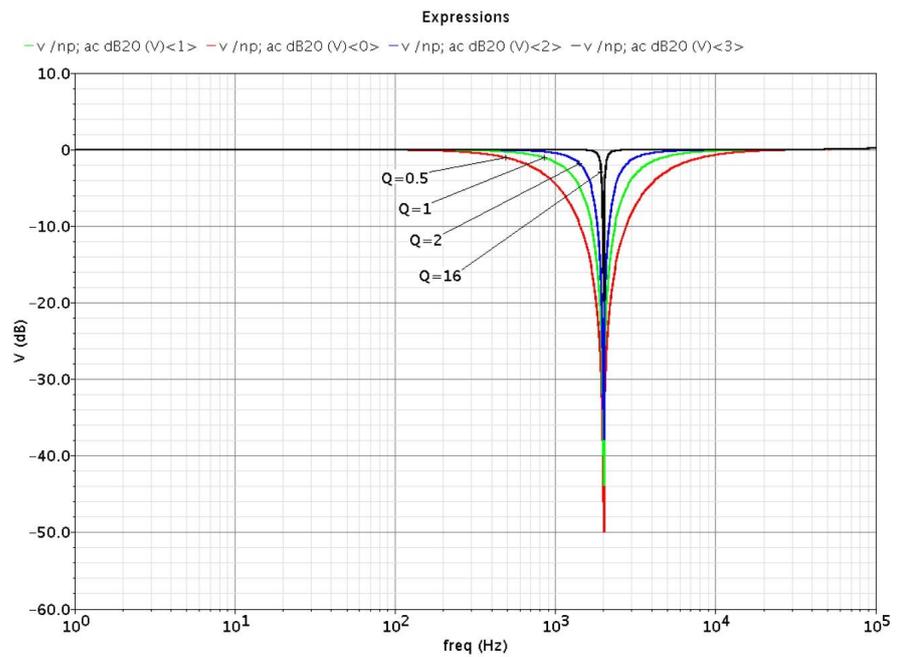


Figure 21. Q-value adjustment simulation.

4. Fourth-Order Butterworth Low-Pass Filter

Based on the above second-order filter characteristics, a fourth-order Butterworth low-pass filter is designed by cascading dual second-order filters, and its structure is shown in Figure 22. The input signal is input from the IN port of Filter A, with the low-pass output LP of Filter A as the input of Filter B, and the low-pass output LP of Filter B as the output of a fourth-order low-pass filter. The digital module is the digital interface part, which realizes the selection of working modes and the assignment of C_F and quality factor Q . The digital interface part is composed of address lines A3 to A0, data lines D1 and D0, and write enable control bit \bar{W} . When the write enable bit is at a low level, data are written to the register corresponding to the address line, and when the write enable bit is high, the value in the register remains unchanged. The correspondence between register functions and address lines is shown in the Table 2.

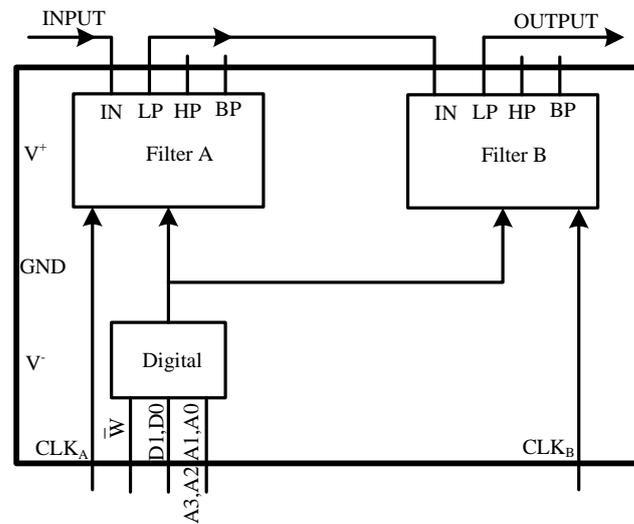


Figure 22. Fourth-order Butterworth low-pass filter.

Table 2. Correspondence between Registers and Address Lines.

D0, D1	A3, A2, A1, A0	LOCATION
M0A, M1A	0000	0
F0A, F1A	0001	1
F2A, F3A	0010	2
F4A, F5A	0011	3
Q0A, Q1A	0100	4
Q2A, Q3A	0101	5
Q4, Q5A	0110	6
Q6A, X	0111	7
M0B, M1B	1000	8
F0B, F1B	1001	9
F2B, F3B	1010	10
F4B, F5B	1011	11
Q0B, Q1B	1100	12
Q2B, Q3B	1101	13
Q4B, Q5B	1110	14
Q6B, X	1111	15

The configuration of the filter is as follows: the clock signal frequency f_{clk} is 200 kHz, the operating mode is mode 1, and the cutoff frequency f_0 is 2 kHz. Then the ratio of capacitance is determined in the two-stage filter according to Formula (43). Using the Filter

Solutions software, we obtain the transfer function $H(S)$ of the filter, as well as the transfer functions $H_A(S)$ and $H_B(S)$ for each stage:

$$H(S) = H_A(S) \cdot H_B(S) \tag{48}$$

$$H_A(S) = \frac{1.579e^8}{S^2 + 2.323e^4S + 1.579e^8}, Q_1 = 0.542 \tag{49}$$

$$H_B(S) = \frac{1.579e^8}{S^2 + 9.61e^3S + 1.579e^8}, Q_2 = 1.306 \tag{50}$$

The internal circuit structures of Filter A and Filter B are the same. Figure 23 shows the internal circuit of Filter A. Based on the requirements of f_0 , Q_1 , and Q_2 , the component values and register configurations of each level of filter are determined, as shown in Tables 3 and 4.

The selection of unit capacitance C_{unit} is a compromise considering speed, layout area, matching degree, and noise. From the perspective of circuit speed and layout area, the smaller the unit capacitance, the better. However, if the capacitance per unit area is too small, it will have a negative impact on matching and noise. We know that the mismatch between capacitors (without considering layout factors) is inversely proportional to the capacitance area. In order to achieve sufficient matching, the side length of a unit capacitor is designed to be above 20 μm . The KT/C noise is directly related to the capacitance value. During the switching capacitor charging process, a total root mean square noise voltage of $\sqrt{KT/C}$ is generated on the capacitor charging resistor, where the component distributed within the cutoff frequency is $\sqrt{KT/MC}$, and M is the oversampling rate. Taking into account the above performance parameters, the side length of C_{unit} is selected as 30 μm . C_2 and C_3 are adjustable capacitors that adjust the Q value and bandwidth respectively. They can be obtained from Equations (51) and (52).

$$Q = \frac{C_1}{C_2} \tag{51}$$

$$\frac{f_{clk}}{f_0} = \frac{C_3}{C_0} \times 4\pi \tag{52}$$

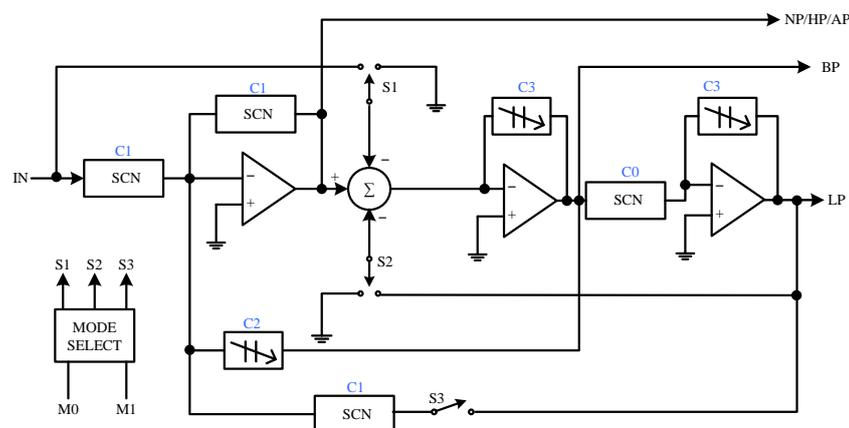


Figure 23. Internal circuit structure of filter A.

Table 3. Circuit parameter values.

Filter	Parameter	Value ($C_{unit} = 380.1 \text{ fF}$)
Filter A	C0	$8 \times C_{unit}$
	C1	$32 \times C_{unit}$
	C2	$59 \times C_{unit}$
	C3	$64 \times C_{unit}$
Filter B	C0	$8 \times C_{unit}$
	C1	$32 \times C_{unit}$
	C2	$24.5 \times C_{unit}$
	C3	$64 \times C_{unit}$

Table 4. Register configuration.

Filter	Register	D1, D0	A3, A2, A1, A0
Filter A	M1, M0	00	0000
	F1, F0	00	0001
	F3, F2	00	0010
	F5, F4	00	0011
	Q1, Q0	10	0100
	Q3, Q2	10	0101
	Q5, Q4	00	0110
	X, Q6	00	0111
Filter B	M1, M0	00	1000
	F1, F0	00	1001
	F3, F2	00	1010
	F5, F4	00	1011
	Q1, Q0	11	1100
	Q3, Q2	11	1101
	Q5, Q4	00	1110
	X, Q6	01	1111

The fourth-order low-pass filter operates in mode 1, with an input frequency of 2 kHz sine wave and an amplitude of 2 V. Transient simulation is completed at a clock frequency of 200 kHz, and the simulation results are shown in Figure 24.

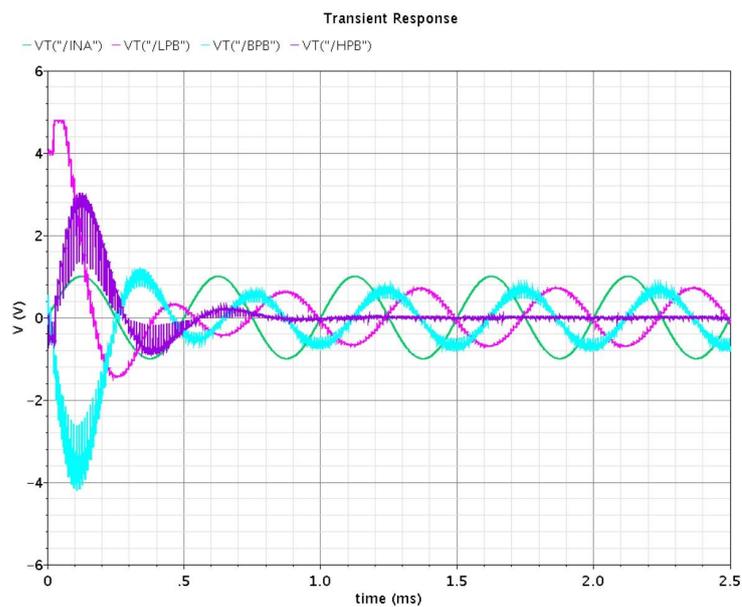


Figure 24. Transient simulation results.

5. Test Results

Based on the Huahong BCD350GE 1P4M layout process, the layout design of a two-stage second-order switch-capacitor filter is completed. As shown in Figure 25, the layout area of this circuit is $5.1 \times 3.1 \text{ mm}^2$.

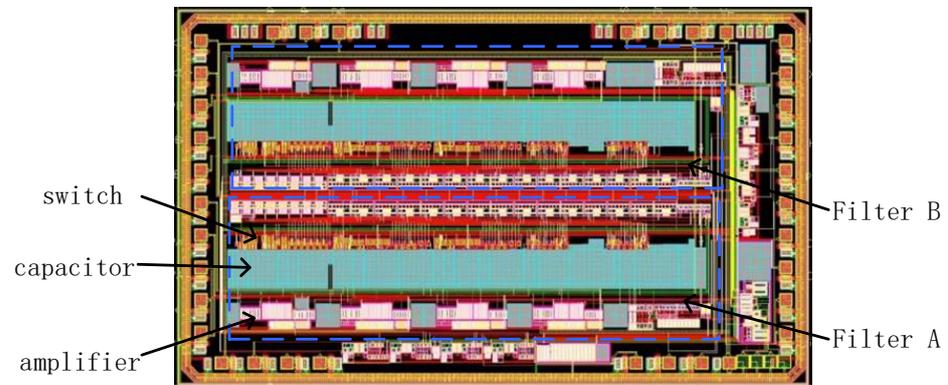


Figure 25. Layout design.

The photos of the testing environment and printed circuit board (PCB) are shown in Figure 26. The power supply provides +5 V power to the PCB board, and the signal generator generates input signals. An oscilloscope is used to observe the waveform of the filter output point. The chip adopts a dual power supply of $\pm 5 \text{ V}$, with a power consumption of approximately 80 mW. The traversal of working frequency, center frequency, and quality factor are completed based on different configuration data. The test results are shown in Table 5, and the bandwidth can be adjusted from 5 Hz to 10 kHz.

The structure of filters A and B in the chip is identical. Filter A is tested under four different operating modes, and the input and output waveforms are shown in Figure 27a–d. The clock frequency is 200 kHz, and the input signal is 2 kHz. Through configuration, $f_0 = 2 \text{ kHz}$ and $Q = 1$ are achieved. According to the test results, the output characteristics fully cover low-pass, high-pass, band-pass, band-stop, and all-pass filtering functions.

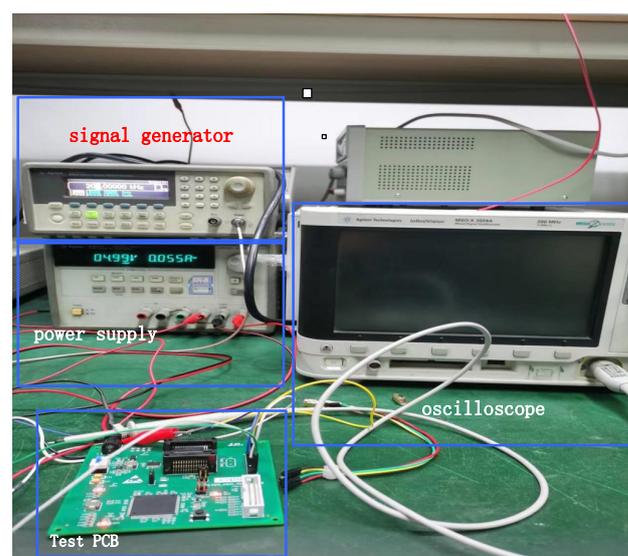
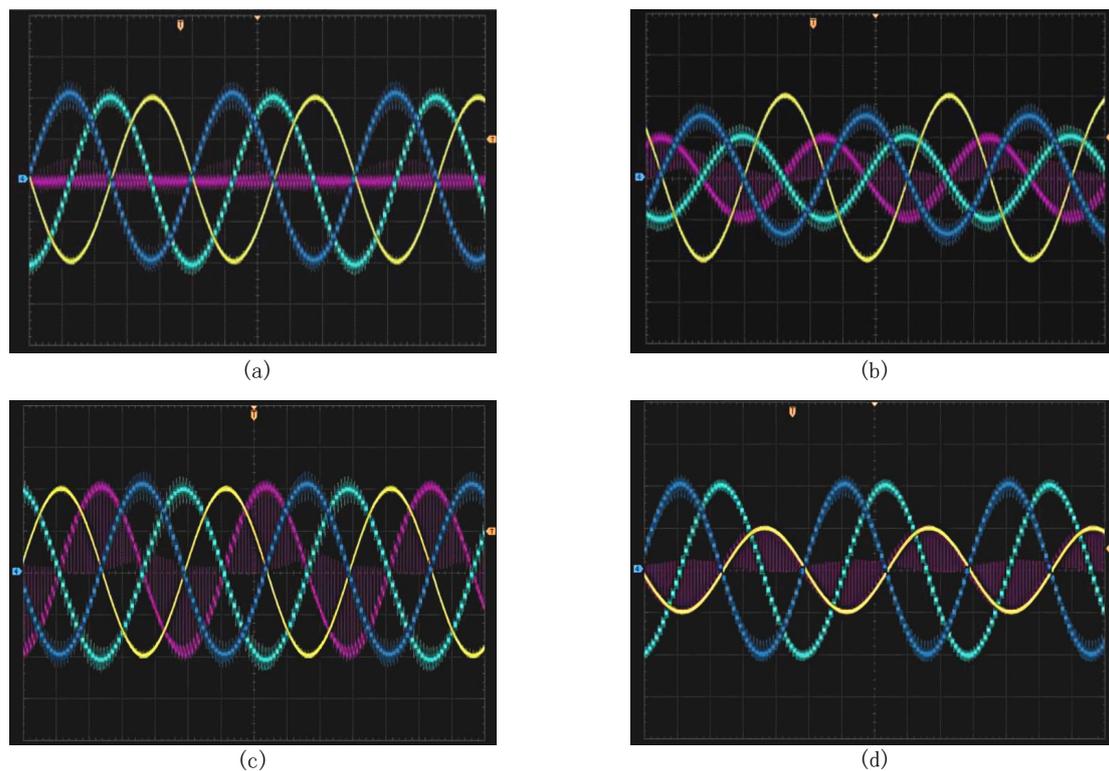


Figure 26. Test environment and the PCB.

Table 5. Bandwidth adjustability test.

Q	Mode	Fclk	f0
1	1	500 Hz–500 kHz	5 Hz–5 kHz
1.41	2	500 Hz–500 kHz	5 Hz–6 kHz
1	3	500 Hz–500 kHz	5 Hz–5 kHz
1	4	500 Hz–500 kHz	5 Hz–5 kHz
64	1	1 kHz–1000 kHz	10 Hz–10 kHz
90.5	2	5 kHz–500 kHz	50 Hz–10 kHz
64	3	500 Hz–500 kHz	5 Hz–5 kHz
64	4	500 Hz–1000 kHz	5 Hz–10 kHz

**Figure 27.** Transient test results in 4 modes: (a) mode 1, (b) mode 2, (c) mode 3, (d) mode 4.

6. Discussion

The test results show that our second-order switch-capacitor filter is powerful and can cover all functional filtering characteristics, including low-pass, high-pass, band-pass, band-stop, and all-pass functional filtering. In addition, it also has other advantages. On the chip, 64 level center frequency and 128 level Q value can be independently programmed and adjusted without affecting each other. When switching frequency points, different frequency points can be achieved without the need for many external devices, making adjustment flexible. It has a wide range of applications, with two independent second-order switch-capacitor filters on the chip that can be used separately or cascaded into a fourth-order filter. It can also use a weighted structure of chip and chip cascading to achieve higher-order filters. For example, in railway transportation systems, the track frequency shift automatic blocking system achieves an automatic blocking function through frequency shift signals, such as the UM71 standard uplink carrier frequency center frequencies of 2000 Hz and 2600 Hz, respectively, and the center frequencies of the downlink carrier frequency are 1700 Hz and 2300 Hz, respectively. Before detecting frequency shift signals, preprocessing of the signal is necessary. Usually, there are several methods to achieve switching between multiple frequency points in the low frequency range. The first method

is to use a multi-stage frequency selection circuit in series. Due to the discreteness of device parameters, this method requires that all frequency selection circuits have a small deviation in the center frequency, making it difficult to change the multi-stage center frequency uniformly. The second method uses multiple analog switches, operational amplifiers, resistors, capacitors, and other discrete components to form an active filter for frequency selection. However, the circuit uses a large number of components, making parameter adjustment very difficult. Our universal filter has a dual second-order universal switch-capacitor active filter that is easy to program and can switch between different frequency points without the need for many external devices. It can be used as a signal filtering unit in the front end of railway frequency shift signal detection instruments. Currently, the chip has completed board level testing, and the next step will be system-level testing in the railway system.

Table 6 summarizes the performance comparison results between this article and other references, indicating that the switch-capacitor filter designed in this article has strong functionality. Foreign countries have always had an advantage in the field of high-precision, low-power, and low-offset switch-capacitor filters. In recent years, domestic research has mainly focused on high-order switch-capacitor filters, N-path switch-capacitor filters, and Gm-C filters, while there is relatively little research on universal filters. We have designed a second-order universal switch-capacitor filter, hoping to complete some work to fill the gap. However, we believe that we still need to optimize the switch-capacitor filter chip from the following aspects: (1) Power consumption. From the test results, using a ± 5 V power supply voltage, the power consumption is 80 mW, which is higher than traditional continuous time filters. We need to further optimize the power consumption based on the characteristics of the process, cost, etc. (2) Optimization of internal circuit structure. As one of the important units, the performance of the operational amplifier directly affects the performance of the switch-capacitor filter. From the design of the operational amplifier structure, the structure is simple, but the bandwidth is small. For CMOS operational amplifiers, the bandwidth will be limited by the characteristic frequency f_T of the MOS transistor, where the characteristic frequency f_T is proportional to the gate length L^2 of the MOS transistor. We adopt the 24 V high-voltage transistor process, where the minimum gate length of NMOS is 3 μm , while the minimum gate length of PMOS is 4 μm , which greatly limits the bandwidth of the amplifier. The next step is to optimize the structure to achieve a high bandwidth operational amplifier.

Table 6. Performance comparison.

Parameter	Reference [3]	Reference [4]	Reference [15]	This Paper
implementation method	active RC	active RC	switched capacitor	switched capacitor
function	low-pass	low-pass	low-pass	low-pass, high-pass, band-pass, band-stop, all-pass
cut-off frequency	1 MHz~32 MHz adjustable	0.3 MHz~10 MHz adjustable	100 Hz~500 Hz adjustable	5 Hz~10 kHz adjustable
filter order	6	8	2	4
technology	TSMC0.18 μm	GSMC0.18 μm	2P2M 1.2 μm N-well MOS process	BCD350GE high voltage 24 V process
supply voltage	1.8 V	1.8 V	-	± 5 V
consumption	20 mW	15.48 mW	-	80 mW

7. Conclusions

In this paper, a bandwidth adjustable filter is designed by using switch-capacitor technology, which integrates low-pass, high-pass, band-pass, band-stop, and all-pass. The

circuit has a simple structure and can independently achieve 64 level bandwidth and 128 level Q value adjustable through programming, without affecting each other. Two second-order switch-capacitor filtering channels with the same structure are integrated into the chip and manufactured using the Huahong BCD350GE high-voltage 24 V process. The measurement results indicate that the proposed switch-capacitor filter can achieve multifunctional filtering characteristics, including low-pass, high-pass, band-pass, band-stop, and all-pass. Meanwhile, it can achieve a bandwidth of 5 Hz to 10 kHz. The chip area is $5.1 \times 3.1 \text{ mm}^2$, powered by a dual power supply of $\pm 5 \text{ V}$, and the power consumption is 80 mW. The chip can be used alone and can also be cascaded to achieve high-order filtering.

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References

1. Yang, C.L.; Zhang, Y.; Yang, X.Q.; Qi, C. Development of a General Module for Programmable Switched Capacitor Low Pass Filter. *Electron Technol. Appl.* **2022**, *48*, 136–139.
2. Yan, X.H.; Mu, W.J. Design of a stacked miniaturized 5G FR2 frequency band filter. *Commun. Technol.* **2021**, *54*, 1768–1773.
3. Gao, B.; Zhang, Z.Y.; Ye, X.Y. Programmable Active RC Filter with On Chip Autotuning. *Semicond. Integr. Circuit* **2017**, *42*, 184–189.
4. Xie, M.; Ren, X.; Ma, C.; Zhang, R.; Lai, Z. A Low Power Channel Selection Filter for Multifrequency and Multimode Receiver. *Microelectronics* **2012**, *42*, 534–538.
5. Allen, P.E.; Holberg, D.R. switched capacitor circuit. In *CMOS Analog Integrated Circuit Design*; Feng, J., Li, Z.Q., Eds.; Publishing House of Electronics Industry: Beijing, China, 2003; pp. 402–407.
6. Huang, J.F.; Wen, J.Y.; Lin, Y.J. Chip design of a 10-MHz switched capacitor low-pass filter for wireless application. In Proceedings of the 2014 Sixth International Conference on Wireless Communications and Signal Processing (WCSP), Hefei, China, 23–25 October 2014; pp. 1–5.
7. Lulec, S.Z.; Johns, D.A.; Liscidini, A. A 150- μW 3rd-order butterworth passive-switched-capacitor filter with 92 dB SFDR. In Proceedings of the IEEE Symposium on VLSI Circuits Digest of Technical, Kyoto, Japan, 5–8 June 2017; pp. 142–143.
8. Singh, N.; Bansod, P.P. Switched-capacitor filter design for ECG application using 180 nm CMOS technology. In Proceedings of the 2017 International Conference on Recent Innovations in Signal Processing and Embedded Systems (RISE), Bhopal, India, 27–29 October 2017; pp. 439–443.
9. Kaya, K.; Ozanoglu, K.; Kahya, Y.P.; Dundar, G. Programmable Switched-Capacitor Filter Design Tool for Biomedical Signal Acquisition. In Proceedings of the 2023 19th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), Funchal, Portugal, 3–5 July 2023; pp. 1–4.
10. Chang, J.; Liu, S.B. Design of Switched Capacitor Low Pass Filter. *Design of Switched Capacitor Low Pass Filter. Electron. Des. Eng.* **2012**, *20*, 171–173.
11. Du, D.H.; Xiong, F.; Lin, Y.S. A 4-order Switched Capacitor Low Pass Filter with High Linearity and Low Power Consumption. *Semicond. Technol.* **2010**, *35*, 1222–1225.
12. Fan, T.; Peng, J.; Zhang, Z. Design and Simulation Method of Bandpass Switched Capacitor Filter. *Microelectron. Comput.* **2009**, *26*, 90–92.
13. Xiao, Y.P.; Hu, X. Design and Simulation of High Order Elliptic Filters. *Electron. Meas.* **2007**, *30*, 147–150.
14. Hu, P.F.; Xie, L.; Jin, X.L. Design of Bandwidth Adjustable High Order Switched Capacitor Filter. *Microelectronics* **2015**, *45*, 357–361.

15. Xiang, B.; Nin, X.W.; Mo, B.X.; Lv, Z.J. Design of a Bandwidth Adjustable Low Pass Switched Capacitor Filter. *Microelectronics* **2003**, *6*, 541–544.
16. Sun, S.Q.; Lin, J.; Wang, Y.J. Design and Implementation of a Low Frequency Bandpass Filter with Adjustable Center Frequency. *J. Electron. Meas. Instrum.* **2006**, *20*, 59–63.
17. Sansen, W.M.C. *Analog Design Essentials*; Springer: Berlin/Heidelberg, Germany, 2007; pp. 335–336.
18. Yan, J.M. Bandwidth Adjustable 14th Order Switched Capacitor Bandpass Filter. Master's Dissertation, Harbin Institute of Technology, Harbin, China, 2017.
19. Wang, J. Optimization Design of a Configurable Switched Capacitor Filter. Master's Dissertation, Harbin Institute of Technology, Harbin, China, 2022.
20. Mirchandani, N.; Shrivastava, A. High Stability Gain Structure and Filter Realization with less than 50 ppm/°C Temperature Variation with Ultra-low Power Consumption using Switched-capacitor and Sub-threshold Biasing. In Proceedings of the 2018 IEEE International Symposium on Circuits and Systems (ISCAS), Florence, Italy, 27–30 May 2018; pp. 1–5.
21. Sheng, J.G.; Chen, Z.L.; Shi, B.X. 1 V CMOS switched-capacitor filter. *J. Circuits Syst.* **2005**, *10*, 28–30.
22. Xing, Q.F. Design and Application Research of Switched Capacitor Filter. *Comput. Knowl. Technol.* **2011**, *7*, 1669–1679.
23. Wu, A.D. Design of Switched Capacitor Elliptical Low Pass Filter. *J. Zhejiang Univ. Foreign Lang.* **2013**, *4*, 101–104.
24. Xia, X.R. Research and Implementation of Programmable Switched Capacitor Filter System. Master Dissertation, Hunan University, Hunan, China, 2009.
25. Marzuki, A. *CMOS Analog and Mixed-Signal Circuit Design*; Taylor & Francis Group: Leiden, The Netherlands, 2020.
26. Wang, D. Design of Eighth Order Low Pass Elliptic Switched Capacitor Filter. Master's Dissertation, Harbin Institute of Technology, Harbin, China, 2021.
27. Razavi, B. *Analog CMOS Integrated Circuit Design*; Chen, G.C., Cheng, J., Zhang R.Z., Translators; Xi'an Jiaotong University Press: Xi'an, China, 2018.
28. Al-Badawy, K.A.; Soliman, E.A.; Mahmoud, S.A. Design of switched capacitor biquad filter with quality factor tunability. In Proceedings of the 2009 International Conference on Microelectronics—ICM, Marrakech, Morocco, 19–22 December 2009; pp. 30–33.
29. Martin, K.; Sedra, A. Effects of the Op-Amp Finite Gain and Bandwidth on the Performance of Switched-Capacitor Filters. *IEEE Trans. Circuits Syst.* **1981**, *28*, 822–829. [[CrossRef](#)]
30. Hasan, M.N.; Saeedi, S.; Gu, Q.J.; Sigmarsson, H.H.; Liu, X. Design Methodology of N-Path Filters With Adjustable Frequency Bandwidth and Filter Shape. *IEEE Trans. Microw. Theory Tech.* **2018**, *66*, 2775–2790. [[CrossRef](#)]

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