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Demonstration of a Frequency Doubler Using a Tunnel Field-Effect Transistor with Dual Pocket Doping

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Abstract: In this study, a frequency doubler that consists of a tunnel field-effect transistor (TFET) with dual pocket doping is proposed, and its operation is verified using technology computer-aided design (TCAD) simulations. The frequency-doubling operation is important to having symmetrical current characteristics, which eliminate odd harmonics and the need for extra filter circuitry. The proposed TFET has intrinsically bidirectional and controllable currents that can be implemented by pocket doping, which is located at the junction between the source/drain (S/D) and the channel region, to modify tunneling probabilities. The source-to-channel (I_{SC}) and channel-to-drain currents (I_{CD}) can be independently changed by managing each pocket doping concentration on the source and drain sides ($N_{S,POC}$ and $N_{D,POC}$). After that, the current matching process was investigated through $N_{S,POC}$ and $N_{D,POC}$ splits, respectively. However, it was found that the optimized doping condition achieved at the device level (namely, a transistor evaluation) is not suitable for a frequency doubler operation because the voltage drop generated by a load resistor in the frequency doubler circuit configuration causes the currents to be unbalanced between I_{SC} and I_{CD}. Therefore, after symmetrical current matching was performed by optimizing $N_{S,POC}$ and $N_{D,POC}$ at the circuit level, it was clearly seen that the output frequency was doubled in comparison to the input sinusoidal signal. In addition, the effects of the S/D and pocket doping variations that can occur during process integration were investigated to determine how much frequency multiplications are affected, and these variations have the immunity of S/D doping and pocket doping length changes. Furthermore, the impact of device scaling with gate length (L_G) variations was evaluated. Based on these findings, the proposed frequency doubler is anticipated to offer benefits for circuit design and low-power applications compared to the conventional one.

Keywords: tunnel field-effect transistor; frequency doubler; ambipolar current; band-to-band tunneling; pocket doping technique

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1. Introduction

In wireless communication systems, a frequency doubler, which is composed of nonlinear devices such as a Schottky device and transistors, is essential to make a stable radio frequency (RF) source with a reliable low-frequency crystal oscillator [1–4]. However, these nonlinear elements generate unwanted odd harmonics beyond the intended frequency, requiring the use of additional filtering to prevent signal distortion [5–7]. As a result, circuit configurations can become complex. Therefore, a single transistor-based frequency doubler, which utilizes bidirectional current characteristics, has been extensively researched with two-dimensional transition metal dichalcogenides (TDMC), graphene, carbon nanotube (CNT) devices, and tunneling field-effect transistors (TFETs). Due to their ambipolar device characteristics, which can fundamentally eliminate the odd harmonic components in the output signal, there is no requirement for additional filter circuitry [8–12]. For TDMC materials, MoS_2 and WSe_2 are representative n-type and ambipolar semiconductors, which

indicate higher mobility values of 200–500 cm^2 V^{-1} s^{-1} with good switching characteristics (on- and off-current ratio of 10^8). However, to make the circuit with those devices, a higher operating voltage is required compared to the conventional complementary MOS (CMOS) device. In addition, graphene- and CNT-based frequency doublers have high power dissipations by poor leakage current control due to their small energy bandgap.

Recently, a new concept for a frequency doubler has been proposed using a single ferroelectric FET (FeFET) with a doped hafnium oxide layer (HfO_2) [13]. The operation principle of this device is that the current can be modulated by biasing to the gate due to the polarization effect caused by dipole changes in the ferroelectric layer like the conventional FeFET. Then, to realize the ambipolar characteristics, this proposed device used a gate-induced drain leakage (GIDL) current with a drain voltage (V_D) control. Hence, to make the symmetrical current characteristics, the change in threshold voltage and currents, depending on the polarization up and down, is firstly required, and then the GIDL current generated between the gate and drain overlap region has to be optimized by controlling the V_D. For these methodologies, it is inevitable to increase the leakage power because a high V_D should be applied to make a higher GIDL current during the frequency-doubling operation, meaning that this scheme is not effective for circuit designs in terms of low-power applications.

Therefore, we proposed a new frequency doubler based on a single TFET transistor. Inherently, it is well known that TFETs have low leakage currents and steep subthreshold slopes (*SS*s), making them a good candidate for low-power applications [14–22]. This TFET differs from the metal-oxide-semiconductor field-effect transistor (MOSFET) in that it uses band-to-band tunneling (BTBT) as the carrier injection mechanism, eliminating the SS limitation (>60 mV/dec) associated with thermionic emission in MOSFETs at room temperature. In the case of an n-type TFET, its structure includes a p-type source, intrinsic channel, and n-type drain region, making it compatible with a conventional MOSFET process integration where the modification is limited to the source dopant type. Although TFETs have lower leakage current and lower temperature sensitivity compared to MOSFETs, they face a trade-off that manifests itself in a lower on-current due to increased tunneling resistance, resulting from a smaller tunneling region.

Furthermore, without any process changes, they have ambipolar current characteristics because of two types of tunneling components: a source-to-channel tunneling current (I_{SC}) at $V_G > 0$ and a channel-to-drain tunneling current (I_{CD}) at $V_G < 0$, for n-type device operations. In the conventional TFETs, it has been reported that only the source-to-channel tunneling contributes to the on-current related to the switching characteristics, while the channel-to-drain tunneling is considered to be suppressed as a leakage current. In contrast, the proposed frequency doubler utilizes both source-to-channel and channel-to-drain tunneling components to generate an output signal with doubled frequency. However, I_{SC} and I_{CD} are not exactly the same because of the gap in the tunneling resistance. Therefore, dual pocket doping technologies, which are applied at the interfaces between the channel and source/drain regions, are adapted to control I_{SC} and I_{CD}, independently, leading to symmetric current matching. Those electrical characteristics are verified with a technology computer-aided design (TCAD) device and circuit simulations with well-calibrated model parameters.

2. Device Parameters and Models

Figure 1 shows the proposed TFET structure with the dual pocket doping technologies (n-type operation). These pocket doping regions are to introduce additional dopants, either n-type (energy band down) or p-type (energy band up), into a specific region of the device, changing tunneling probabilities. In order to investigate the electrical characteristics, a gate length (L_G) of 50 nm, interfacial layer thickness (T_{ox}) of 0.7 nm, high-κ thickness (T_{HK}) of 1.5 nm, and body thickness (T_B) of 10 nm were chosen. Additionally, the doping concentrations of the source (1×10^{20} cm^{-3}), channel (5×10^{17} cm^{-3}), and drain (1×10^{20} cm^{-3}) were employed, respectively. To implement symmetrical current characteristics, the n^-

pocket doping is added between the p^+ source and channel regions to control I_{SC} while the p^- pocket doping is applied between the channel and n^+ drain region for changing I_{CD}. Each pocket doping length is defined as 9 nm and the concentration is varied to perform current matching for frequency doubling. All device simulations were carried out using commercial TCAD tools of Synopsys Sentaurus^{TM} [23].

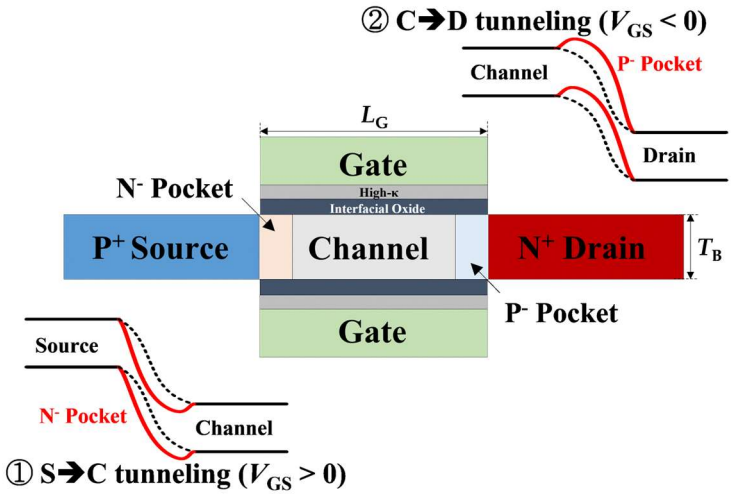

Figure 1. Schematic of an n-type operation tunneling field-effect transistor (TFET) with dual pocket doping regions to independently control tunneling currents, source-to-channel tunneling (I_{SC}), and channel-to-drain tunneling current (I_{CD}). The black dotted line indicates the process condition without pocket doping and the red solid line shows the process condition with docket doping.

In order to accurately calculate tunneling currents, a planar TFET was fabricated on a (100) p-type silicon-on-insulator (SOI) wafer. The gate stack underwent a precise dry oxidation process at 800 °C for 30 s, resulting in the formation of a 3 nm SiO_2 gate dielectric. The subsequent step involved depositing n^+-doped polycrystalline silicon as a gate electrode through a Low-Pressure Chemical Vapor Deposition (LPCVD) process. Following gate patterning, the source and drain regions were achieved through a careful ion-implantation process. Notably, source and drain implantations were executed separately, employing BF_2 with a dose of 8×10^{14} cm^{-2}, a 7° tilt, and an energy of 10 keV for both the source and drain. The subsequent activation of dopants was achieved through a Rapid Thermal Process (RTP) conducted at 900 °C for 5 s. To predict the band-to-band tunneling (BTBT) generation rate (G) per unit volume in the uniform electric field, Kane's model is used, and the fitted parameters are as follows [19]:

$$G = A\left(\frac{F}{F_0}\right)^P exp\left(-\frac{B}{F}\right)$$

where F_0 = 1 V/m, P = 2.5, A_{ind} = 4.0×10^{14} $cm^{-3} \cdot s^{-1}$, and B_{ind} = 9.9×10^6 $V \cdot cm^{-1}$ were used to reflect the indirect tunneling components. Figure 2 shows that the simulated transfer curves (linear and log scale) are well-matched to the measured data of the fabricated TFET after the calibration process. Additionally, the OldSlotboom model was used to consider the effects of heavy doping on bandgap narrowing in the source/drain (S/D) regions. Also, Fermi statistics and the Shockley–Read–Hall recombination model were applied. The performance evaluations were conducted at a V_D of 1.0 V.

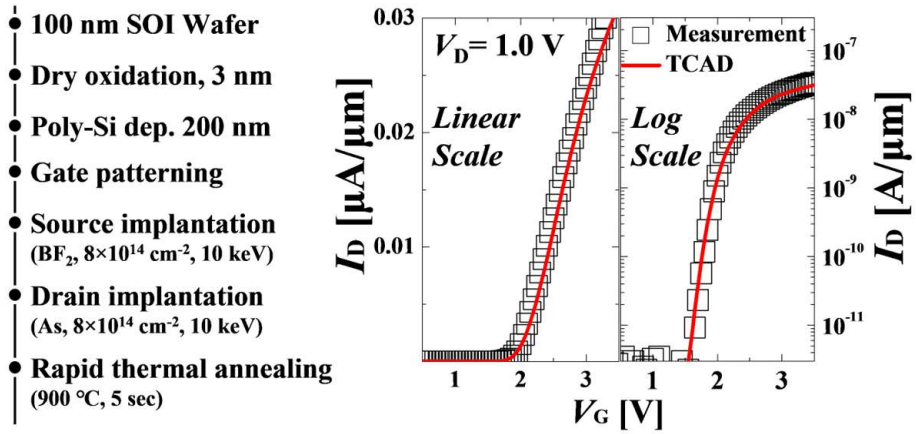

Figure 2. Process sequence of the fabricated planar TFET on a silicon-on-insulator (SOI) wafer and the calibrated drain current (I_D)-gate voltage (V_G) characteristics with measured results and TCAD device simulations.

3. Result and Discussions

3.1. Dual Pocket Doping Effects

The effects of the dual pocket doping on the source and drain sides were investigated to achieve symmetrical current matching. First, Figure 3a shows the drain current (I_D)-gate voltage (V_G) characteristics of the proposed TFET with varying n^- pocket doping concentrations on the source side ($N_{S,POC}$), while the pocket doping was not applied on the drain side. As $N_{S,POC}$ was varied from 5.0×10^{17} cm^{-3} to 1.5×10^{19} cm^{-3}, it was clearly observed that the threshold voltage for I_{SC} ($V_{TH,SC}$) becomes shifted by modulating tunneling resistances, resulting in gradual I_{SC} changes. However, I_{CD} hardly changed regardless of $N_{S,POC}$. To understand this phenomenon induced by $N_{S,POC}$, the energy band diagrams were illustrated in the channel direction at V_D = 1.0 V and V_G = 0.5 V with $N_{S,POC} = 5.0 \times 10^{17}$ cm^{-3} and 1.5×10^{19} cm^{-3} as shown in Figure 3c. Then, it was understood that the tunneling width becomes thinner on the source side by increasing $N_{S,POC}$, and there is no electrical effect on the drain side, which means that I_{CD} is little changed. Next, the p^- pocket doping concentration on the drain side ($N_{D,POC}$) was examined for I_{CD} modulation, excluding the pocket doping on the source side. Figure 3b indicates the I_D-V_G characteristics with V_D = 1.0 V and changing $N_{D,POC}$ from 5.0×10^{17} cm^{-3} to 1.5×10^{19} cm^{-3}. As $N_{D,POC}$ went up, the threshold voltage for I_{CD} ($V_{TH,CD}$) decreased and I_{CD} increased. Compared to the $N_{S,POC}$ variation, it showed completely opposite characteristics. Then, the energy band diagrams were also checked with respect to different $N_{D,POC}$ values (Figure 3d). It was confirmed that only the drain side was locally changed with higher $N_{D,POC}$, whereas little change on the source side was observed. As a result, this pocket doping technique can achieve the required I_{SC} and I_{CD} values independently, making it suitable for implementing current matching for frequency doublers.

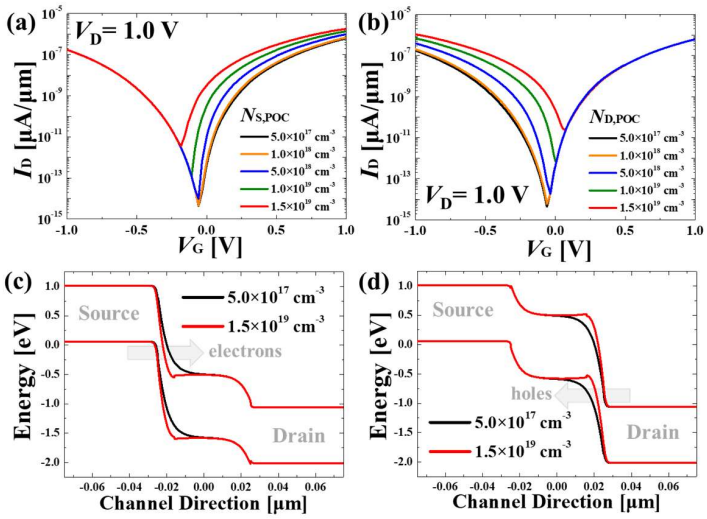

Figure 3. I_D-V_G characteristics with various pocket doping concentrations (**a**) on the source side and (**b**) on the drain side. Energy band diagrams at 5 nm underneath the interfacial oxide (**c**) for n^- pocket doping concentrations on the source side were ($N_{S,POC}$) = 5.0 × 10^{17} cm^{-3} and 1.5 × 10^{19} cm^{-3} at drain voltage (V_D) = 1.0 V and V_G = 0.5 V, and (**d**) for p^-, the pocket doping concentrations on the drain side were ($N_{D,POC}$) = 5.0 × 10^{17} cm^{-3} and 1.5 × 10^{19} cm^{-3} at V_D = 1.0 V and V_G = −0.5 V.

3.2. Current Matching at the Device Level

Based on dual pocket doping technology, the I_{SC} and I_{CD} values in the TFET device were separately optimized under the $N_{S,POC}$ and $N_{D,POC}$ conditions. Figure 4a denoted the $V_{TH,SC}$ and $V_{TH,CD}$ extracted at I_D = 1.0 nA/μm, and Figure 4b showed the I_{SC} and I_{CD} values at V_G = 1.0 V and −1.0 V with V_D = 1.0 V, depending on $N_{S,POC}$ and $N_{D,POC}$. It was obvious that both V_{TH} and I_D can be independently controlled. To conduct device level-based current matching optimization, we set the I_D of 1.0 μA/μm and then selected $N_{S,POC}$ and $N_{D,POC}$ values of 5.0 × 10^{18} cm^{-3} and 1.4 × 10^{19} cm^{-3}, respectively. Then, to rigorously understand the feasibility of a single TFET for performing frequency doubling, the comprehensive mixed-mode circuit level simulations with physical models were conducted with R_L = 300 kΩ and C = 5 × 10^{-14} F as a load resistor and DC block capacitor as shown in Figure 5. The operation principle of frequency doubling is as follows. Once the sinusoidal input signal (V_{IN}) was applied for a half cycle (0 V → V_{DD} → 0 V), I_{SC} flowed through the TFET and then V_N was changed from V_{DD} to V_{DD} − $I_{SC}R_L$ and to V_{DD}, leading to one cycle. Subsequently, for a half-cycle V_{IN} (0 V → $-V_{DD}$ → 0 V), the current flow transitioned from I_{SC} to I_{CD} upon reaching the minimum conduction point. Thus, I_{CD} flowed through the TFET and V_N changed from V_{DD} to V_{DD} − $I_{CD}R_L$ and to V_{DD}, resulting in one cycle. Finally, the output signal (V_{OUT}) was obtained from V_N through a DC block capacitor, and its frequency was doubled compared to V_{IN}.

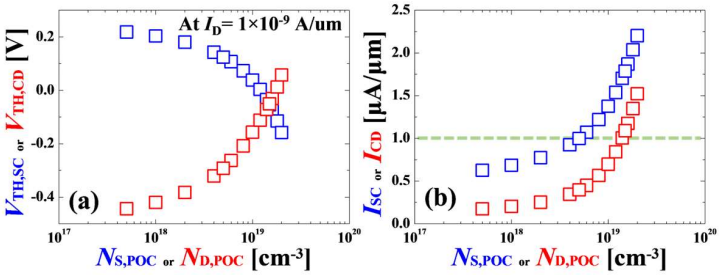

Figure 4. (**a**) The threshold voltage values for I_{SC} ($V_{TH,SC}$) and I_{CD} ($V_{TH,CD}$) were extracted at I_D = 1 × 10^{-9} A/μm using a constant current method, depending on $N_{S,POC}$ and $N_{D,POC}$. (**b**) The summarized I_{SC} (blue) and I_{CD} (red) values were extracted at V_G = 1.0 V and −1.0 V, depending on $N_{S,POC}$ and $N_{D,POC}$.

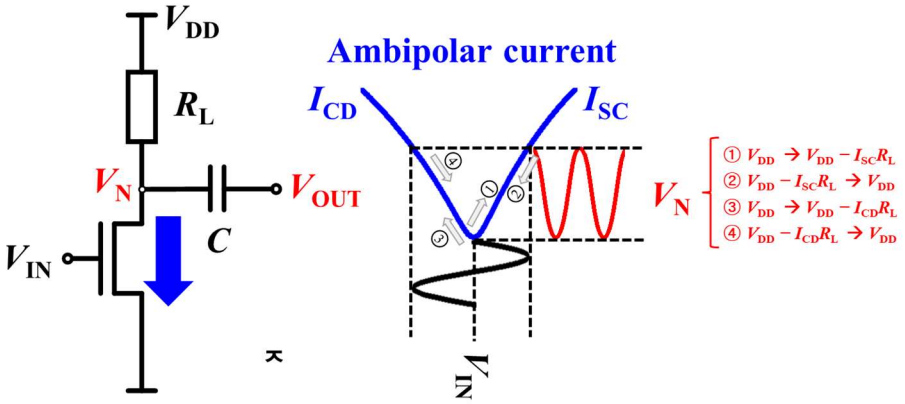

Figure 5. Mixed-mode circuit simulation configuration for the frequency doubler operation with a single proposed device (V_{DD} = 1.0 V, R_L = 300 kΩ, $C = 5 \times 10^{-14}$ F).

To evaluate the frequency doubler operation, the symmetrical I_D-V_G characteristics of the proposed device with the optimized condition were checked as shown in Figure 6a. Based on the mixed-mode circuit simulation, Figure 6b plotted the transient characteristics of I_D according to V_{IN}. However, it was confirmed that the I_{SC} and I_{CD} were unexpectedly different, even though the current matching process was performed in terms of the device level. Particularly, I_{CD} is smaller than I_{SC}. It was found that this phenomenon is caused by the frequency doubler circuit configuration because the V_D of the proposed device was changed by $V_{DD} - I_D R_L$, and it directly affected source-to-channel and channel-to-drain tunneling probabilities.

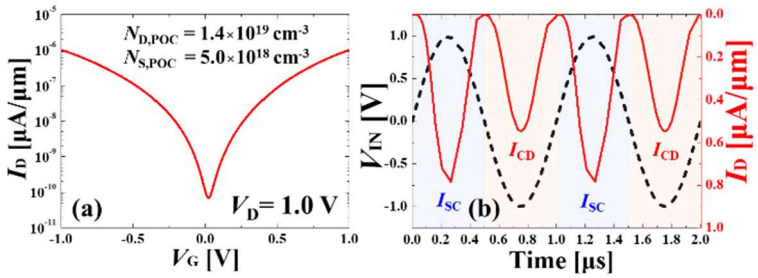

Figure 6. (**a**) Symmetrical I_D-V_G characteristics with $N_{S,POC} = 5.0 \times 10^{18}$ cm^{-3} and $N_{D,POC} = 1.4 \times 10^{19}$ cm^{-3} at the device level. (**b**) Transient characteristics of V_{IN} and I_D with optimized pocket doping concentrations.

To better understand this current mismatching based on the optimized $N_{S,POC}$ and $N_{D,POC}$ conditions, the I_D-V_G characteristics were investigated with different R_L values at the circuit configuration as shown in Figure 7a. As a reference, the optimized I_D-V_G characteristics at the device level, perfectly matched the I_{SC} and I_{CD} values, were used. Then, when R_L was increased from 50 kΩ to 500 kΩ at the circuit level, it was found that the I_{CD} was continuously reduced for a V_G value higher than −0.5 V, while I_{SC} was changed relatively less. The details of the extracted I_{SC} and I_{CD} are indicated in Figure 7b. It can be clearly seen that I_{CD} variations are much greater than I_{SC} with increasing R_L. To find out the origin of this difference in variation, the energy band diagrams were examined in the channel direction with R_L = 50 kΩ and 500 kΩ. To check I_{SC} variation, once V_D = 1.0 V and V_G = 1.0 V were applied, the electrons in the valence band of the source started to pass through a thinned tunneling barrier between the source and channel regions as shown in Figure 7c. Since the source was directly connected to the ground, the potential energy was fixed irrespective of R_L. Whereas the potential energy of the drain was affected by the voltage drop ($I_{SC}R_L$). Thus, as R_L was increased from 50 kΩ to 500 kΩ, V_D was decreased, reducing the potential difference between the source and drain. Nevertheless, the tunneling barrier near the valence band edge of the source region was changed little, allowing I_{SC}

to be slightly reduced. In the case of the I_{CD} variation, V_D = 1.0 V and V_G = −1.0 V were biased to cause the holes to flow by tunneling from the drain to channel regions as shown in Figure 7d. When R_L was changed from 50 kΩ to 500 kΩ, it was clearly seen that the potential energy of the drain was decreased by a higher voltage drop ($I_{CD}R_L$). In contrast to I_{SC}, the tunneling barrier near the conduction band edge of the drain region was significantly modulated, allowing I_{CD} to be remarkably reduced. Hence, the current matching, not the device-based optimization, should be required in the frequency doubler circuit configuration.

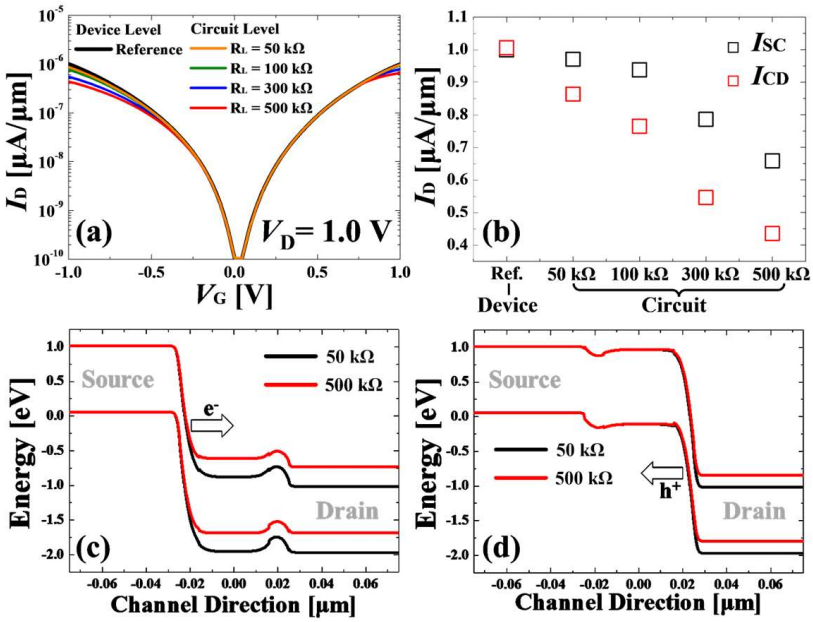

Figure 7. For optimized pocket doping condition ($N_{S,POC}$ = 5.0 × 10^{18} cm^{-3} and $N_{D,POC}$ = 1.4 × 10^{19} cm^{-3}), (**a**) I_D-V_G characteristics, and (**b**) summarized I_{SC} and I_{CD} values with various R_L values at the circuit level compared to the device level. Energy band diagrams with R_L = 50 kΩ and 500 kΩ (**c**) at V_D = 1.0 V and V_G = 1.0 V for I_{SC} (**d**) at V_D = 1.0 V and V_G = −1.0 V for I_{CD}.

3.3. Frequency Doubler Operation

Figure 8a shows the I_{SC} and I_{CD} values with respect to each pocket doping concentration in terms of the device and circuit levels. The circuit level currents were extracted from the frequency doubler circuits with R_L = 300 kΩ and C = 5 × 10^{-14} F. Here, $N_{S,POC}$ and $N_{D,POC}$ values of 1.0 × 10^{18} cm^{-3} and 1.6 × 10^{19} cm^{-3}, respectively, were chosen to achieve current matching at the circuit level, and then the symmetric I_D-V_G characteristics were verified with the optimized doping condition as shown in Figure 8b. It was clearly seen that the I_{CD} values at the device level are larger than those at the circuit level under the same process condition due to an $I_{CD}R_L$ voltage drop. To check the frequency-doubling operation, the transient characteristics of I_D were investigated according to V_{IN} with a peak voltage of 1 V and a frequency of 1 MHz (Figure 8c). The changes in I_{SC} and I_{CD} are almost identical, making similar voltage drops. Subsequently, the output signals through a DC block capacitor were confirmed with doubled frequency compared with that of the input signal while maintaining its amplitude as shown in Figure 8d. Then, the operating frequency range of the proposed frequency doubler was evaluated. As the input frequency increases from 10 kHz to 10 MHz, it was confirmed that the output signal has a doubled frequency without signal distortions compared with the input frequency (Figure 8e,f).

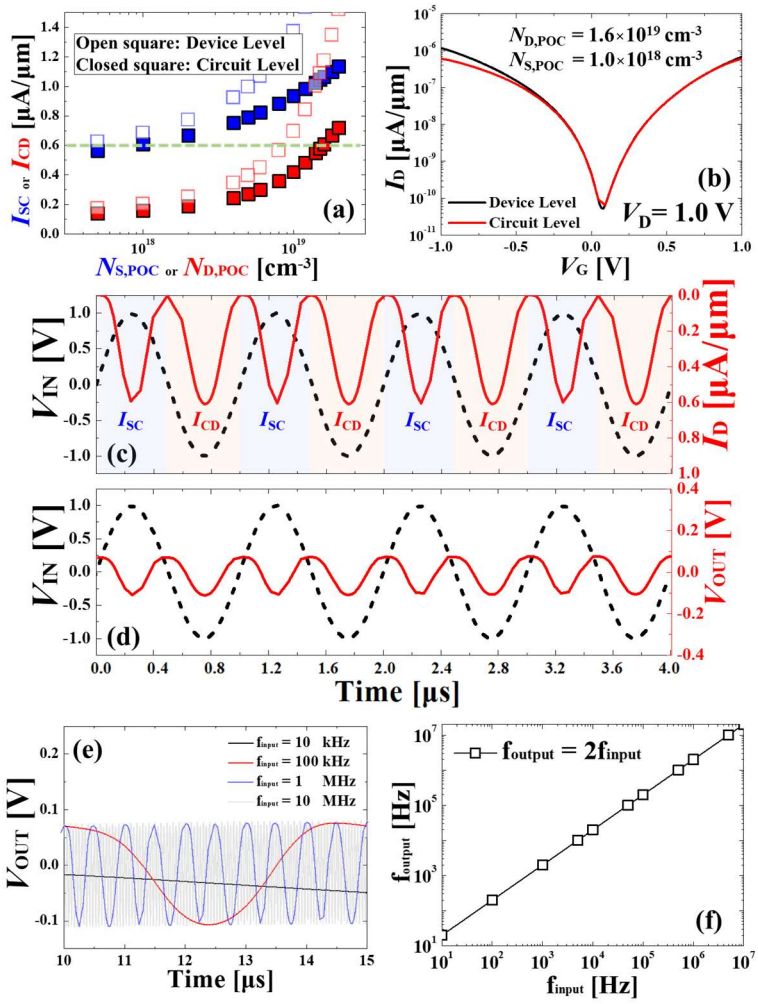

Figure 8. (**a**) The summarized I_{SC} (blue) and I_{CD} (red) values depend on $N_{S,POC}$ and $N_{D,POC}$ at the device and circuit levels. (**b**) Symmetrical I_D-V_G characteristics with $N_{S,POC}$ = 1.0 × 10^{18} cm^{-3} and $N_{D,POC}$ = 1.6 × 10^{19} cm^{-3} at the circuit level. Transient characteristics of (**c**) I_D and (**d**) V_{OUT} regarding V_{IN} with a peak voltage of 1 V and a frequency of 1 MHz. (**e**) V_{OUT} characteristics and (**f**) the frequency response according to V_{IN} with different input frequencies from 10 kHz to 10 MHz.

In terms of device scalability, the performance of the frequency doubler was estimated with respect to L_G based on the optimized process condition. Since each pocket doping length was defined as 9 nm in the channel region, here, the minimum L_G was limited to 20 nm. Therefore, as L_G decreased from 50 nm to 20 nm, it was observed that both I_{SC} and I_{CD} were little changed as shown in Figure 9a. After that, the transient characteristics of V_{OUT} were investigated depending on L_G (Figure 9b). It was clearly seen that the frequency-doubling operations are maintained without the amplitude reduction in the output signal regardless of L_G, implying that the proposed frequency doubler has the merit of exhibiting little performance degradation for device scaling, which means it is strongly immune to short channel effects (SCEs). Additionally, in order to evaluate the effects of tunneling current degradation, which directly affects the output signal, the influences of S/D doping concentration (N_{SD}) variations, induced during process integrations, were investigated. Figure 9c indicates the transfer characteristics with N_{SD} variations from 5 × 10^{19} cm^{-3} to 5 × 10^{20} cm^{-3}, which can be varied by ion implantation and an annealing process. As the N_{SD} became lower, the switching characteristics were degraded, leading to a reduction in I_D by increasing the tunneling resistances. On the other hand, it was clearly seen that as N_{SD} increases, I_D increases due to the decreases in the tunneling barrier at the junction. Even

though the magnitude of I_D slightly fluctuated, it was found that the frequency doubling was properly operated as shown in Figure 9d.

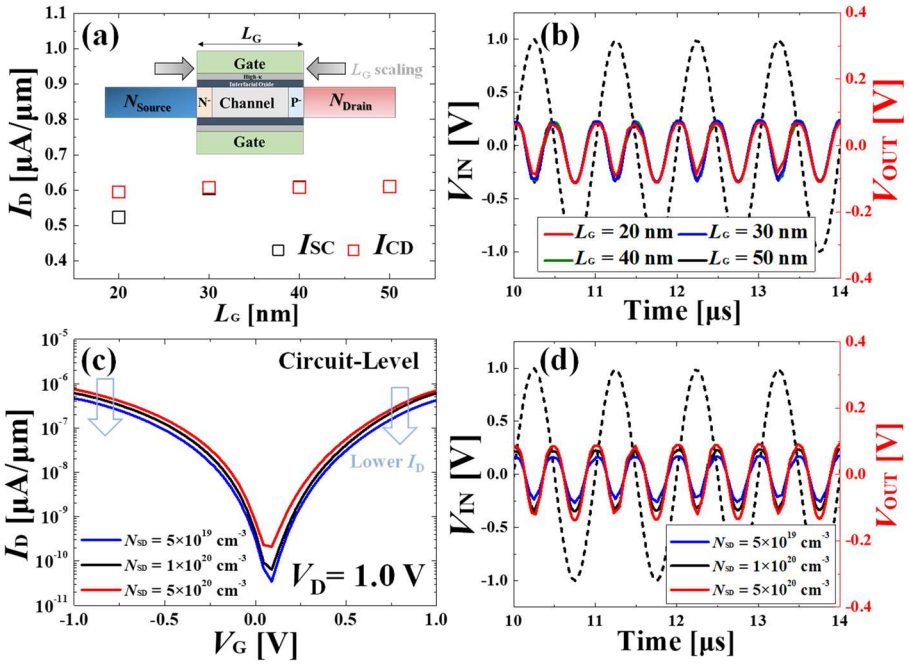

Figure 9. (**a**) The summarized I_{SC} and I_{CD} values depend on L_G values from 20 nm to 50 nm, with the optimized process condition at the circuit level simulations. (**b**) Transient characteristics of V_{IN} and V_{OUT} with different L_G. For the process variations, (**c**) the transfer and (**d**) transient characteristics with changing S/D doping concentrations (N_{SD}) from 5×10^{19} cm^{-3} to 5×10^{20} cm^{-3}.

In addition, although pocket doping technology is widely used as a method to control the tunneling barrier for performance optimization, if a heavy doping concentration or diffused doping region is applied to a specific region to modulate the on-current and threshold voltage, tunneling components could occur regardless of the gate bias, resulting in performance variations. Thus, the effects of pocket doping diffusion, which can be induced during process integration, were investigated to verify the validity of the frequency doubler performance. Then, each pocket doping length on the source and drain sides ($L_{S,POC}$ and $L_{D,POC}$) was split from 6 nm to 12 nm (Figure 10a). The I_{SC} and I_{CD} values, regarding $L_{S,POC}$ and $L_{D,POC}$, were summarized in Figure 10b. As the pocket doping length was increased, both currents increased marginally. In particular, it was observed that the I_{CD} variations appear slightly higher than the I_{SC} variations. It was due to the doping concentration difference ($N_{D,POC} > N_{S,POC}$) determined by the current matching optimization. However, these current variations were not as large as the changes caused by $N_{S,POC}$ and $N_{D,POC}$, which induced large V_{TH} and I_D shifts. To check how much $L_{S,POC}$ and $L_{D,POC}$ variations can affect the frequency doubler operation, the transient characteristics were evaluated. As can be seen in Figure 10c,d, it was found that $L_{S,POC}$ and $L_{D,POC}$ changes did not have a major impact on the frequency-doubling operation due to small current variations, implying that the proposed scheme has immunity against the pocket doping diffusion.

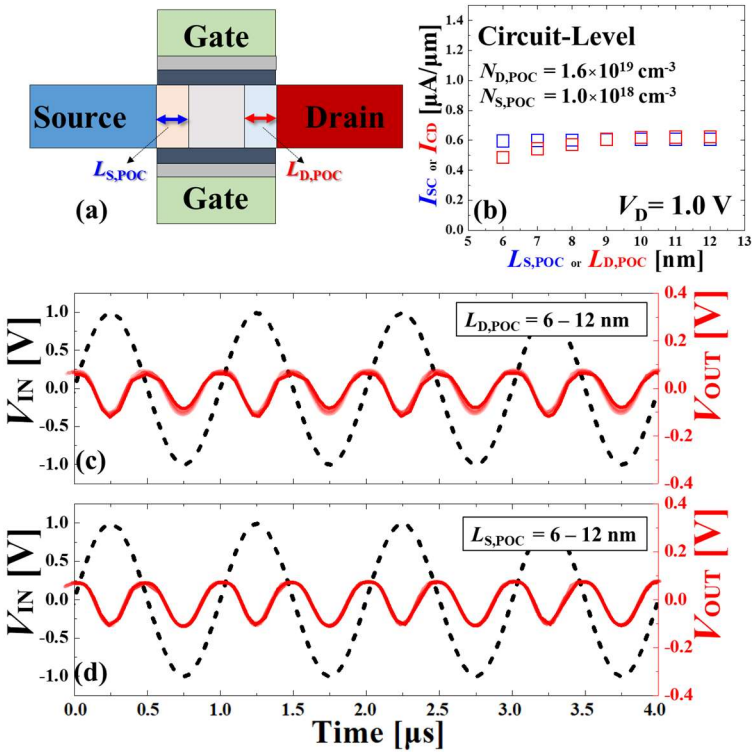

Figure 10. (**a**) Schematic of pocket doping length splitting for considering dual pocket doping diffusion. (**b**) The summarized I_{SC} (blue) and I_{CD} (red) values, depending on $L_{S,POC}$ and $L_{D,POC}$ at the circuit level simulations. Transient characteristics of V_{OUT} with changing (**c**) $L_{S,POC}$ and (**d**) $L_{D,POC}$.

4. Conclusions

In this work, a TFET with dual pocket doping was introduced to double an input frequency, and its functionality and performances were verified using a commercial TCAD device and circuit simulations with the calibrated BTBT physical models. Achieving frequency doubling is essential to having symmetrical current characteristics because it eliminates the odd harmonics and the need for additional filter circuitry. The proposed device can have ambipolar current behavior as an intrinsic property of TFETs and can independently control the I_{SC} and I_{CD} by $N_{S,POC}$ and $N_{D,POC}$ changes, which modulate the tunneling barrier, respectively. The changes of the tunneling resistance on the source- and drain side were confirmed by the analysis of the energy band diagrams as well as transfer characteristics. However, although the optimized process condition, by controlling various $N_{S,POC}$ and $N_{D,POC}$ for symmetrical current matching, was found at the device level, it was unexpectedly confirmed that current mismatching occurred by V_D reduction ($V_D = V_{DD} - I_D R_D$) in the frequency doubler circuit. To find out the optimized $N_{S,POC}$ and $N_{D,POC}$ values for symmetrical current matching, the circuit level should be considered. After that, the input frequency can be doubled using mixed-mode circuit simulations. From these results, it is a very meaningful result for not only the proposed one but also other devices with different channel materials and structures using the same frequency doubler circuit configuration. Moreover, it is expected that the proposed frequency doubler will be utilized for low-power applications because it has the potential to be advantageous for the circuit design due to its simple circuitry with a single tunneling device as compared to conventional frequency doublers.

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