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9.9 µW, 140 dB DR, and 93.27 dB SNDR, Double Sampling ΔΣ Modulator Using High Swing Inverter-Based Amplifier for Digital Hearing Aids

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Abstract: In this paper, an ultra-low-power second-order, single-bit discrete-time (DT) double sampling ΔΣ modulator was proposed for hearing aid applications. In portable biomedical devices that are permanently used such as hearing aids, short battery lifetime and power dissipation are considerable issues. In a typical delta–sigma modulator, the most power-consuming parts are the operational transconductance amplifiers (OTAs), and their elimination without loss of efficiency is now challenging. This proposed modulator includes an ultra-low-power self-biased inverter-based amplifier with swing enhancement instead of power-hungry OTAs. Low voltage amplifier design reduces output swing voltage, affecting delta–sigma modulator efficiency and decreasing the signal-to-noise and distortion ratio (SNDR) and dynamic range (DR) values. In this article, the proposed amplifier's source and tail transistors were biased in the sub-threshold region, increasing the output swing voltage significantly and leading to desired properties for a hearing aid modulator. The proposed amplifier peak-to-peak swing voltage was approximately 1.01 V at a 1 V power supply. In addition, the proposed modulator design used a standard 180 nm CMOS technology, which obtained 140 dB DR and 93.27 dB SNDR for a 10 kHz signal bandwidth with an oversampling ratio (OSR) of 128. Finally, the modulator's effective chip area was 0.02 mm^2 and consumed only about 9.9 µW, while the figure of merit (FOM_W) and FOMs achieved 1.31 fJ/step and 183.31, respectively.

Keywords: ultra-low power; self-biased inverter-based amplifier; discrete-time (DT); hearing aids; delta–sigma modulator; inverter-based amplifier; double sampling; subthreshold; high swing amplifier

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1. Introduction

Nowadays, low power dissipation is critical in biomedical systems. The design of these systems, particularly portable ones, is significant due to their battery life (e.g., hearing aids and pacemakers). Many people use hearing aids worldwide since hearing impairment is a severe disability that limits people's social activities and communications [1,2]. There are two types of hearing aids, namely digital and analog. Digital hearing aids are commonly used due to the possibility of digital signal processing, high-quality sound production, and better noise reduction. An essential digital hearing aid block is an analog-to-digital converter (ADC) that receives an audio signal from the hearing aid microphone and converts it to a digital signal; then, further processing is performed using a digital signal processor (DSP). ADC is implemented in various structures such as sigma–delta, pipelines, and successive-approximation register (SAR). The sigma–delta ADC type is a popular converter for hearing aid applications due to its ease of design, low noise generation, off-band noise transmission, and low power consumption. Increasing the modulator order, oversampling ratio (OSR), and quantizer bits improves the ADC resolution but complicates the circuits and consumes more power. Therefore, there is a trade-off between resolution, costs, and power dissipation.

Figure 1 illustrates a typical digital hearing aid on the transmitter and receiver sides. As shown, the digital hearing aid transmitter consists of a microphone, amplifier, delta–sigma modulator, decimation filter, and DSP, while the receiver comprises a speaker. The delta–sigma modulator block of digital hearing aids is the concern of this paper. The operational transconductance amplifiers (OTAs) of the conventional sigma–delta are power-hungry parts in the whole hearing aid circuit. Thus, previous research proposed various methods to decrease the ΔΣ circuits' power dissipation, including opamp-sharing [3], double-sampling [4], and switched-opamp [5]. Another solution is to eliminate the OTAs and replace them with circuits that consume less power. There are many suggestions to replace OTAs with low-power and low-complexity circuits, including passive circuits [6] and inverter-based [7], time-based [8], and comparator-based [9] amplifiers. However, OTA elimination usually reduces the converter's efficiency; therefore, a trade-off between power dissipation and performance must be considered for the ADC design. In 1958, Kilby built the first integrated circuit [1], which was applied in a hearing aid as its first commercial application. In 1982, CUNY in New York developed the first all-digital hearing aid [1]. This hearing aid was made up of a minicomputer and a digital processor array and had a large size so that it was necessary for one person to carry its equipment. The improved digital hearing aid became commercially available in 1990 with features such as adaptive noise cancellation, voice recognition, and automatic gain control. Today, invisible hearing aids are the standard for design. However, only one out of five people still use hearing aids due to the lack of acceptance by people, the device's efficiency, social acceptance, and cost. The hearing range of a healthy person is in the dynamic range (DR) of about 130 dB. This DR in conventional modulators increases power consumption. Hence, a high DR with low power consumption is the main challenge in hearing aids [1,10].

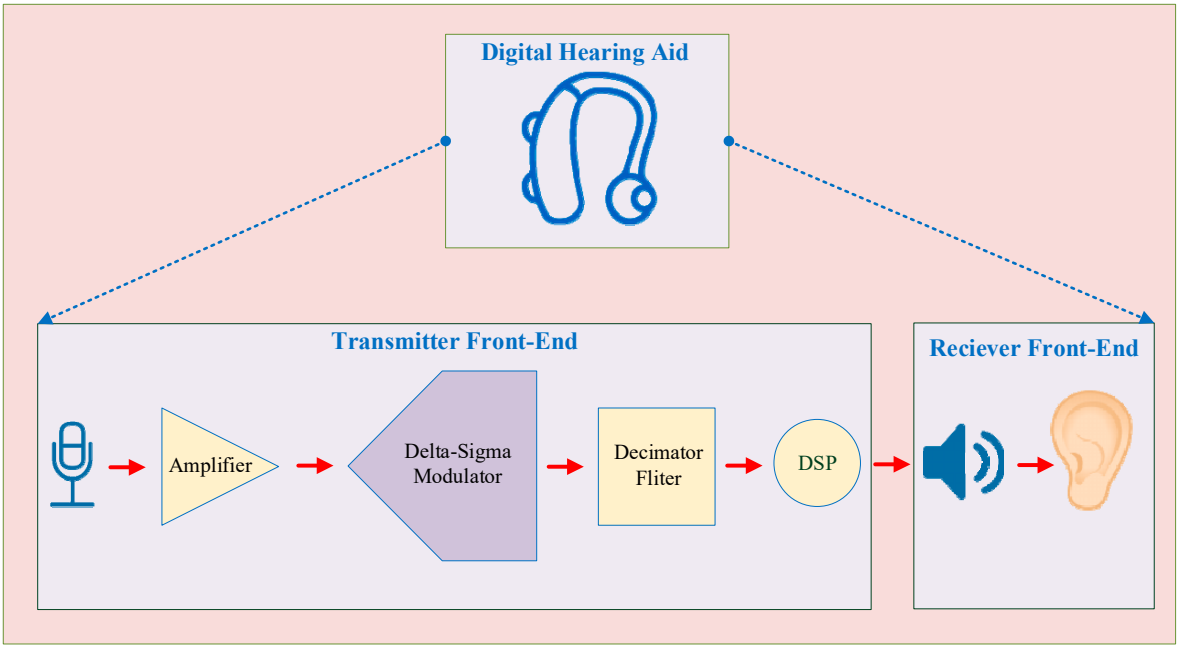

Figure 1. Block diagram of digital hearing aids.

On the other hand, it is noteworthy that the amplification and discrimination of speech from noise or signal-to-noise ratio (SNR) enhancements are significant in hearing aid design. In addition, the American National Standards Institute for hearing aids recommends that the total harmonic distortion (THD) must be at the 5–10% level, which is −20 to −26 dB. However, a −20 dB distortion is audible and objectionable in many cases, while a −40 dB distortion is undetectable. Other important hearing aid properties are high resolution, small size, comfortable design, and ease of use [1]. The challenge of this specification is that if the power consumption is reduced, the SNDR and DR are also reduced because the

threshold voltage of the transistors does not change by reducing the supply voltage, and as a result, the swing of the OTA output in the modulator stages is diminished, and then, the efficiency of the modulator is reduced.

This paper proposed an ultra-low-power self-biased inverter-based amplifier with a swing enhancement used in the DT sigma–delta modulator for a hearing aid application. Some effective transistors in the output voltage swing of the proposed amplifier are biased in the subthreshold region. In the subthreshold region, the transistors' overdrive voltage is decreased and near 0 V, so the output swing is improved. It means that the power consumption is reduced, and the proposed amplifier consumes about 1.93 μW.

The proposed differential modulator was also designed with 1 V, while the peak-to-peak swing voltage is about 1.01 V. A double sampling method was employed to improve the modulator efficiency. According to the specifications required for the hearing aid, the modulator was considered a single-bit, single-loop, cascade of integrators with feedback summation (CIFB) structure that works at a sampling frequency of 2.56 MHz and an input signal bandwidth of 10 kHz. It also consumes about 9.9 μW with a signal-to-noise and distortion ratio (SNDR) of 93.27 dB. The 15.2-bit modulator has a dynamic range of 140 dB and a THD of −41.61 dB. The modulator implementation improved performance and the figure of merit (FOM) value relative to previous research. Pre-layout, post-layout, and post-layout with pad analysis revealed that the proposed modulator is suitable for a high-resolution digital hearing aid. The remaining sections of this paper are organized as follows:

Section 2 describes the proposed modulator system-level design. Section 3 consists of the circuit implementation of the proposed ultra-low-power self-biased inverter-based amplifier, its circuit analysis, and other parts of the modulator circuit. The modulator simulation results are given in Section 4. The simulation results are discussed in Section 5. Section 6 presents the conclusions.

2. System-Level Design of the Proposed ΔΣ Modulator

There are many considerations to choosing an appropriate hearing aid delta–sigma modulator, including OSR, order, topology, single- or multi-loop structure, and the number of quantizer bits. As discussed earlier, low power consumption and high efficiency in hearing aid modulator design are significant. This work used a CIFB single-loop topology because of it has low distortion, high performance, low complexity, a small area, and only one feedback digital-to-analog converter (DAC). Furthermore, a one-bit quantizer was applied due to its inherent linearity and the fact that additional circuits such as dynamic element matching or data weighted averaging are not necessary [1,11]. Figure 2 displays the system level of the proposed second-order, double sampling, single-loop CIFB structure, and single-bit modulator with an OSR of 128.

By using the double sampling method, C1 is divided into two equal coefficients (C1A and C1B), and it seems that the sampling rate is doubled, while in reality, the sampling frequency has not changed, and the sampling process performs in two (instead of one) clock phases [10]. In addition, half of the sampling capacitor is activated in each clock phase. When clock 1 is in a high state, capacitor CS1A is charged with the input signal voltage, while the charge stored in capacitor CS1B is transferred to capacitor CI1, and the output of the integrator represents a change. Similarly, when clock 2 is in a high state, CS1B samples the input signal, and the charge stored on the CS1A capacitor is transferred to the integrator capacitor CI1; therefore, the integrator output demonstrates a change.

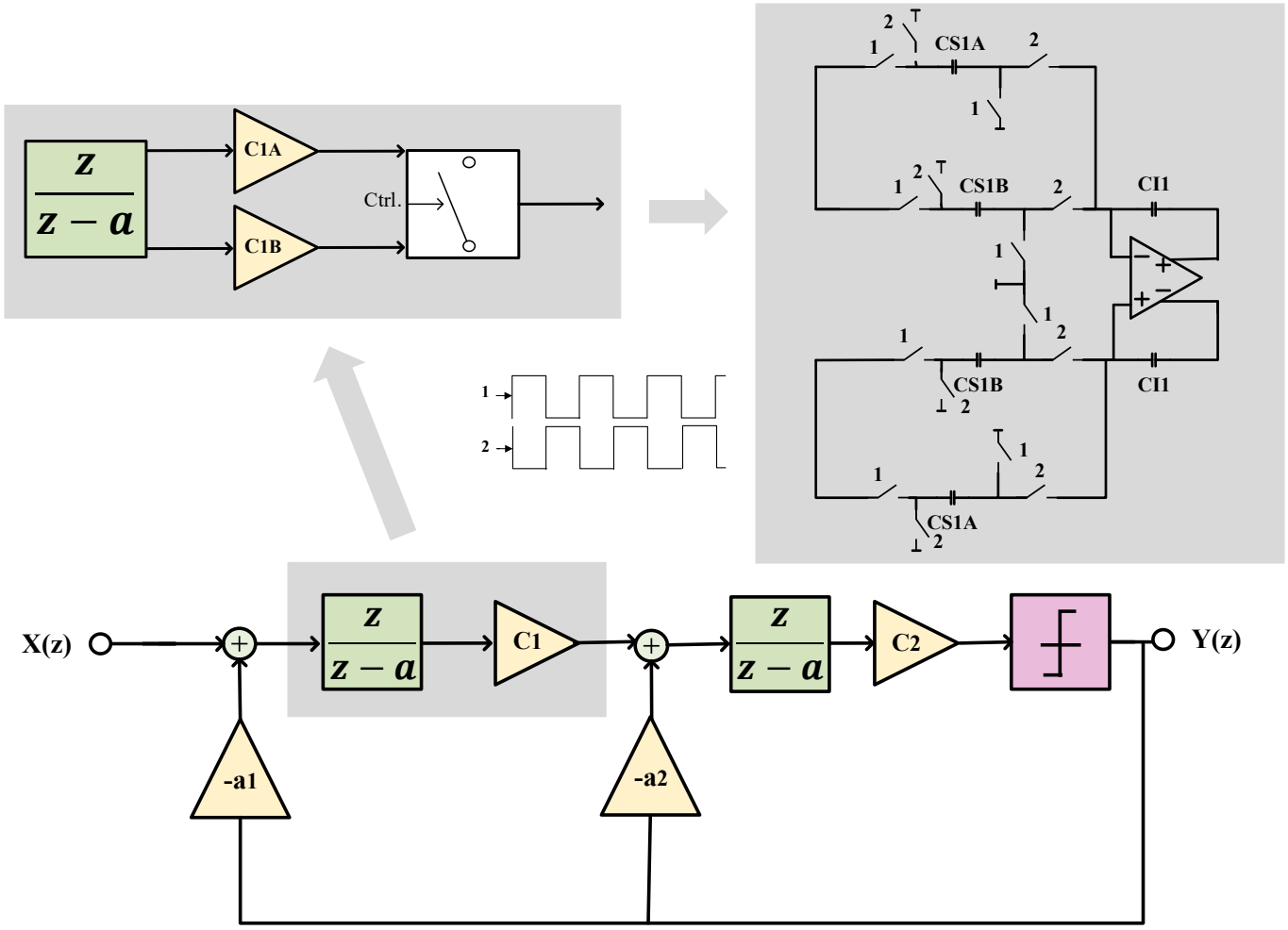

Figure 2. System level of the proposed double sampling CIFB modulator.

The proposed modulator is inherently stable because it uses a second-order modulator with a single-bit DAC. 'α' is related to the modulator filter's amplifier direct current (DC) gain and ideally equals 1. However, in reality, it is less than one and is obtained from Equation (1) as follows:

$$\alpha = \frac{Gain\ (DC) - 1}{Gain\ (DC)} \tag{1}$$

Assuming that feedback coefficients a_1 and a_2 equal 1, signal transfer function (NTF) and signal transfer function (STF) are obtained as follows:

$$NTF = \frac{\left(1 - Z^{-1}\right)^2}{1 + (c_2 * q - 2) * Z^{-1} + (1 + c_1 * c_2 * g - c_2 * g) * Z^{-2}} \tag{2}$$

$$STF = \frac{c_1 * c_2 * q * Z^{-2}}{1 + (c_2 * q - 2) * Z^{-1} + (1 + c_1 * c_2 * g - c_2 * g) * Z^{-2}} \tag{3}$$

where q is a quantizer gain. The coefficients must be chosen so that STF and NTF are equal to

$$STF = Z^{-2} \tag{4}$$

$$NTF = \left(1 - Z^{-1}\right)^2 \tag{5}$$

The proposed modulator coefficients are presented in Table 1. The system design power spectral density (PSD) analysis of the proposed modulator for the different filters' amplifier DC gain (α) is depicted in Figure 3. As a result, the efficiency and the precision of the modulator increases whenever α gets closer to 1. One of the critical parameters for reducing the performance in the sigma–delta modulator is the amplifier DC gain; since, in non-ideal conditions, the 'α' value is less than 1. According to Figure 3, the modulator's precision varies from 13.38 to 15.96 bits by increasing the 'α' value.

Table 1. The systematically designed delta–sigma modulator coefficients.

Coefficient	Value
$a_{1,2}$	1
C_1	0.4
C2	0.8

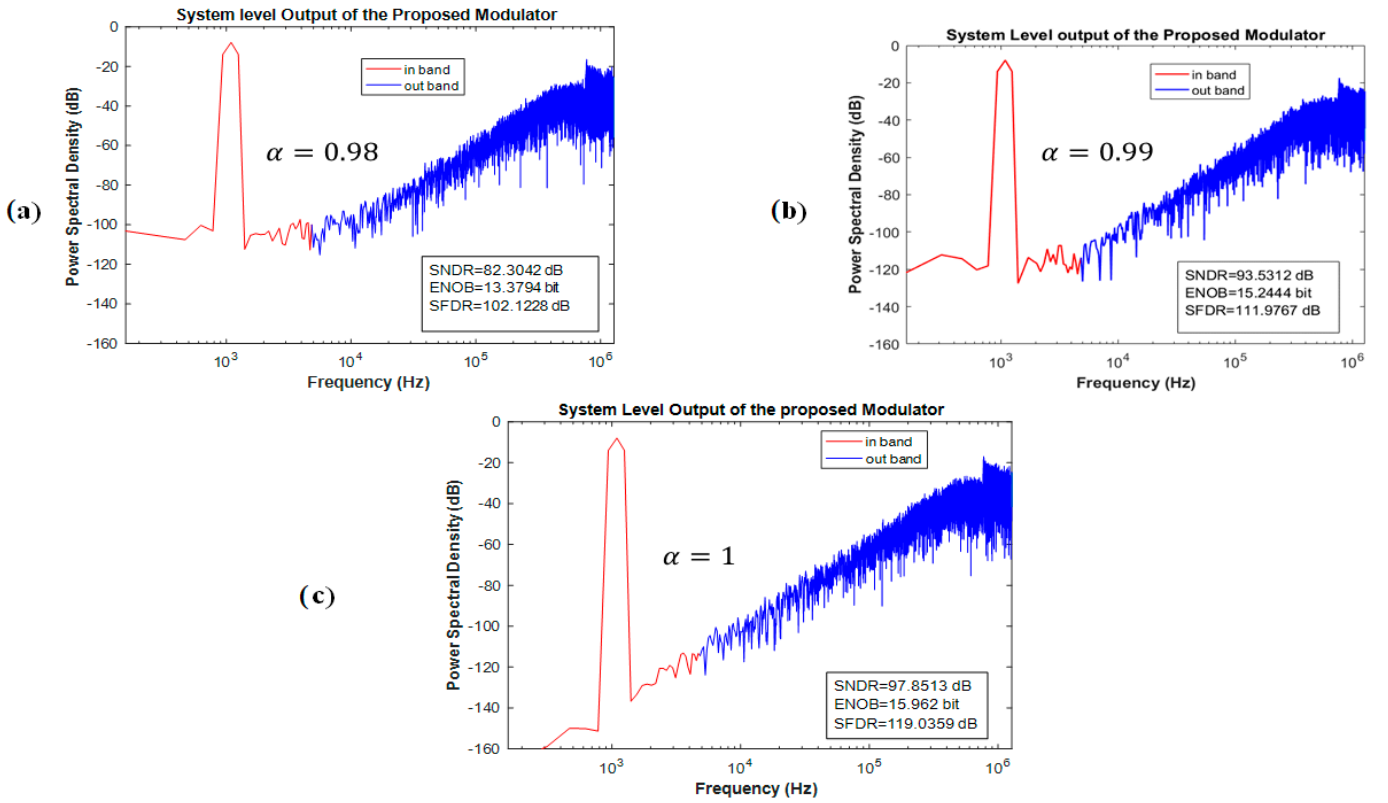

Figure 3. System level output of the proposed modulator for different filters' amplifier DC gain: (**a**) α = 0.98 and (**b**) α = 0.99 and (**c**) α = 1.

3. Circuit Implementation of the Proposed ΔΣ Modulator

A typical DT sigma–delta modulator includes loop filters, a quantizer, and DAC. The filter used in this modulator is low pass and is implemented with switched-capacitor circuits. The quantizers can be of single- or multi-bit type. A single-bit quantizer is composed of a preamplifier, comparator, and latch. DAC is a feedback path to compare the digital output signal with the input signal and identify charge redistribution [12]. The proposed modulator schematic is illustrated in Figure 4. The sampling and integration capacitors are obtained according to the modulator coefficients (Table 1) and listed in Table 2.

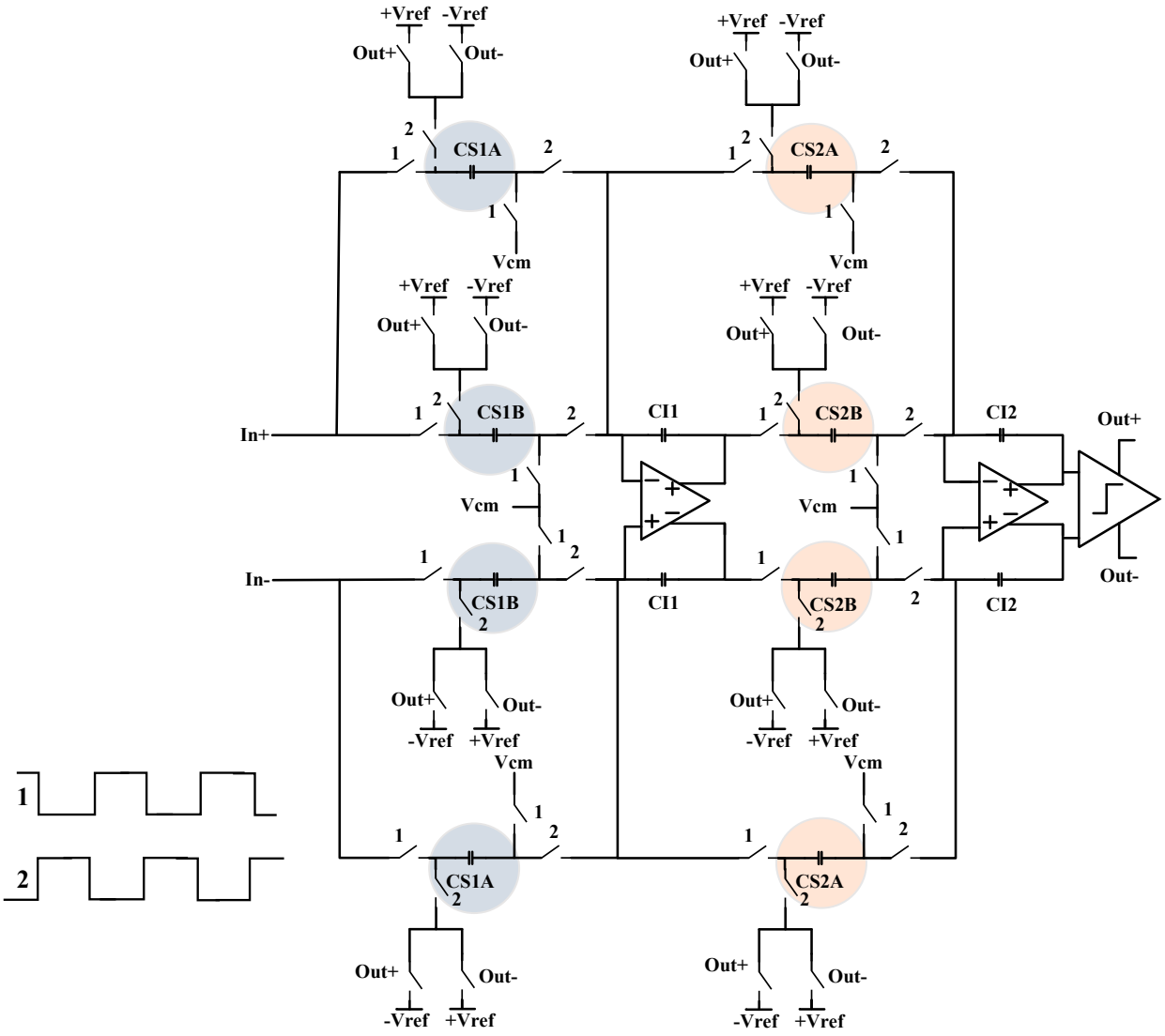

Figure 4. The proposed double sampling sigma–delta modulator for hearing aid applications.

Table 2. Sampling and integrator capacitors of the proposed ΔΣ modulator.

Capacitor	Value
$Cs_{1A,1B}$	0.2 pF
$Cs_{2A,2B}$	0.1 pF
CI_1	1 pF
CI_2	0.25 pF

As shown in Figure 4, there are two branches to perform the sampling process. When clock 1 is high, the CS1A capacitor is charged with the input signal voltage, while the charge stored in the CS1B capacitor is transferred to CI1. Similarly, when clock 2 is high, CS1B samples the input signal, the stored charge on the CS1A capacitor is transferred to the integrator capacitor CI1, and the integrator output represents a change.

3.1. The Proposed Self-Biased Differential Inverter-Based Amplifier with Swing Enhancement

As mentioned previously, the OTAs are the most power-dissipating parts of the sigma–delta modulator. Various methods were proposed to replace the OTAs with low-consumption circuits. One of them uses an inverter-based amplifier [13,14], which has

better efficiency if the amplifier is designed as self-biased and differential [13–16]. A fully differential inverter-based amplifier is shown in Figure 5 [16].

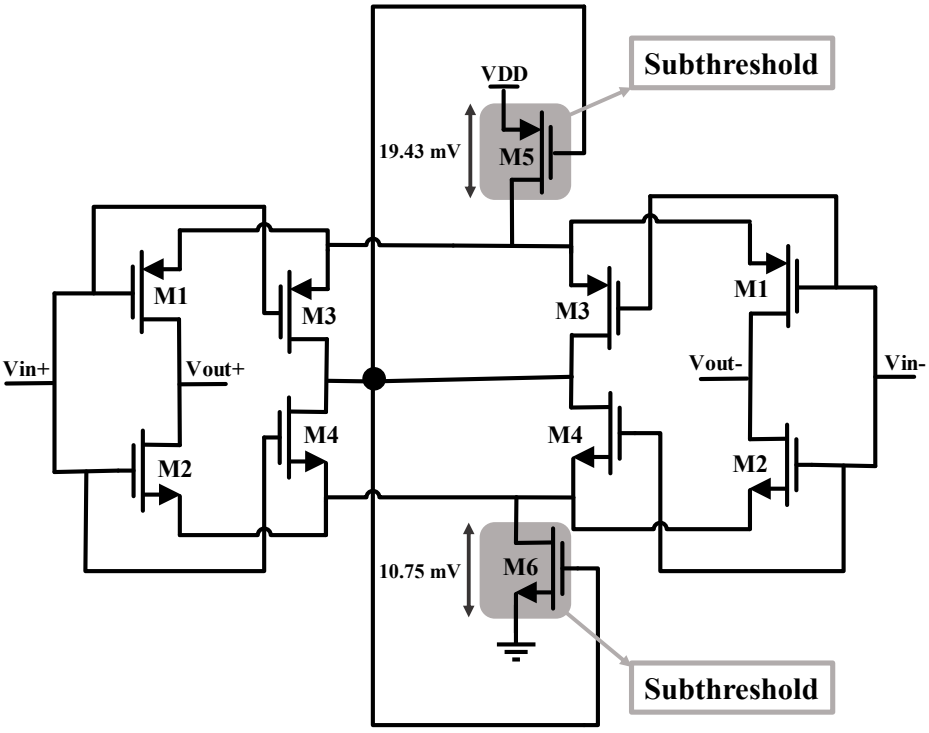

Figure 5. The proposed robust self-biased differential inverter-base amplifier.

This work suggested a high swing, ultra-low-power, self-biased, differential inverter-based amplifier with a voltage gain of 52.46 dB at a 1 V power supply (Figure 5).

In the proposed amplifier circuit, M5 and M6 transistors operate in subthreshold regions, and the remaining amplifier transistors operate in the saturation region. Furthermore, the whole amplifier consumes only 1.93 µW. Moreover, the positive and negative output swing equal 0.51 and 0.51 V, respectively, and the peak-to-peak swing voltage is 1.01 V. Table 3 provides the aspect of the ratio of the amplifier transistors, and the current, voltage, and region of all amplifier transistors of the proposed amplifier are also presented in Table 4.

Table 3. The aspect of the ratio of the proposed amplifier transistors.

Transistor	$M_{1,3}$	$M_{2,4}$	M_5	M_6
$\frac{W}{L}$	$\frac{6\ \mu m}{2\ \mu m}$	$\frac{1\ \mu m}{2\ \mu m}$	$\frac{8\ \mu m}{180\ nm}$	$\frac{2.5\ \mu m}{180\ nm}$

Table 4. The transistors' voltage, current, and region in the proposed inverter-based amplifier.

Parameter \ Transistor	$M_{1,3}$ (pMOS)	$M_{2,4}$ (nMOS)	M_5 (pMOS)	M_6 (nMOS)
I_D	482.79 nA	482.79 nA	1.93 µA	1.93 µA
V_{gs}	−480.57 mV	489.25 mV	−494.42 mV	505.58 mV
V_{th}	−452.54 mV	461.88 mV	−509.88 mV	525.29 mV
V_{ds}	−474.99 mV	494.83 mV	−19.43 mV	10.75 mV
Region	Saturation	Saturation	Subthreshold	Subthreshold

The M5 and M6 gate-source voltages are less than the threshold voltage and are biased in the subthreshold region; therefore, the overdrive voltage of M5 and M6 is extremely low and equals −19.04 and 10.75 mV, respectively. This reduction in overdrive voltage increases the amplifier swing voltage, which significantly affects the efficiency of the sigma–delta modulator. The remaining transistors are in the saturation region, and their current equals 482.79 nA.

3.1.1. Analysis of the Proposed Amplifier

The bode diagram (gain and phase) of the proposed inverter-based amplifier was obtained at 27 °C with standard 180 nm CMOS technology (Figure 6). The voltage gain is 52.46 dB, and the phase margin is 88.86 degrees using 100 fF load capacitors.

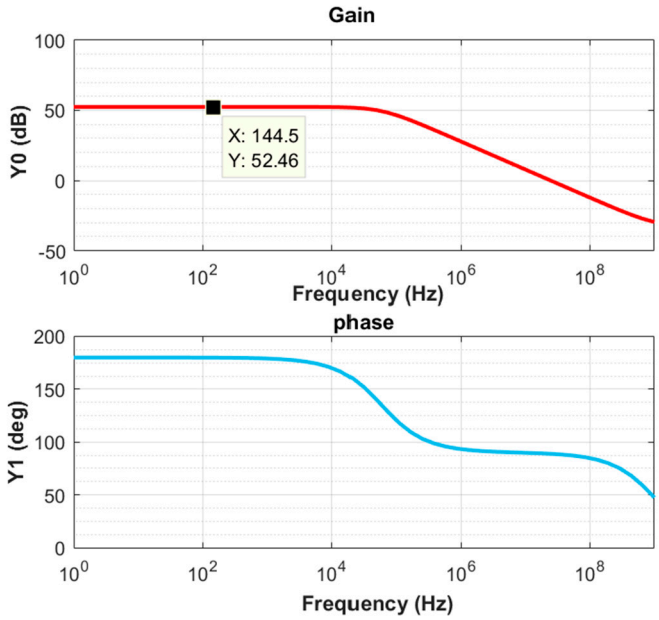

Figure 6. The proposed inverter-based AC gain and phase diagrams.

Common-mode voltage gain (AC) and differential voltage gain (AD) of the proposed amplifier are plotted in Figure 7. AC is lower than 1; therefore, the common mode rejection ratio (CMRR) is greater than AD and equals 64.53 dB, while AD and AC equal 52.46 dB and −12.07 dB, respectively.

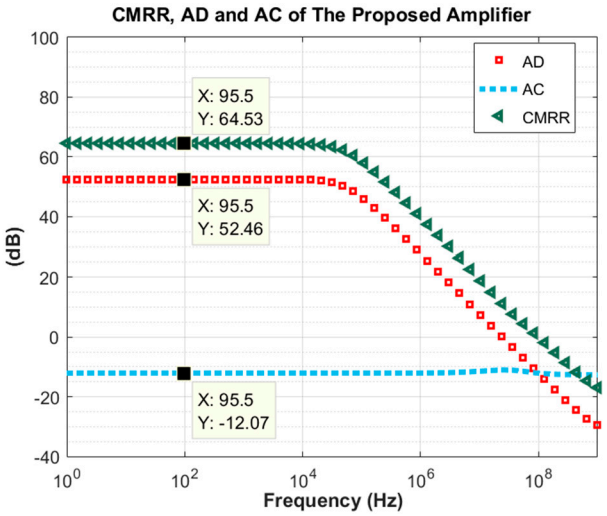

Figure 7. AC, AD, and CMRR vs. frequency analysis of the proposed amplifier.

The proposed amplifier corner analysis was performed at −40, 27, and 85 °C, the results of which are summarized in Table 5.

Table 5. The voltage gain corner analysis of the proposed amplifier.

Corner \ Temp (°C)	−40	27	85
TT	52.37	52.46	51.79
FF	50.4	49.9	48.97
SS	52.04	52.69	52.46
FS	50.82	50.72	49.72
SF	50.96	50.91	49.56

The Monte Carlo analysis with 1000 iterations was also calculated to evaluate the voltage gain stability of the proposed amplifier against various processes and mismatching. Based on the obtained data in Figure 8, the average voltages gain is 50.13, 52.05, and 51.44 dB at 27, −40, and 85 °C, respectively.

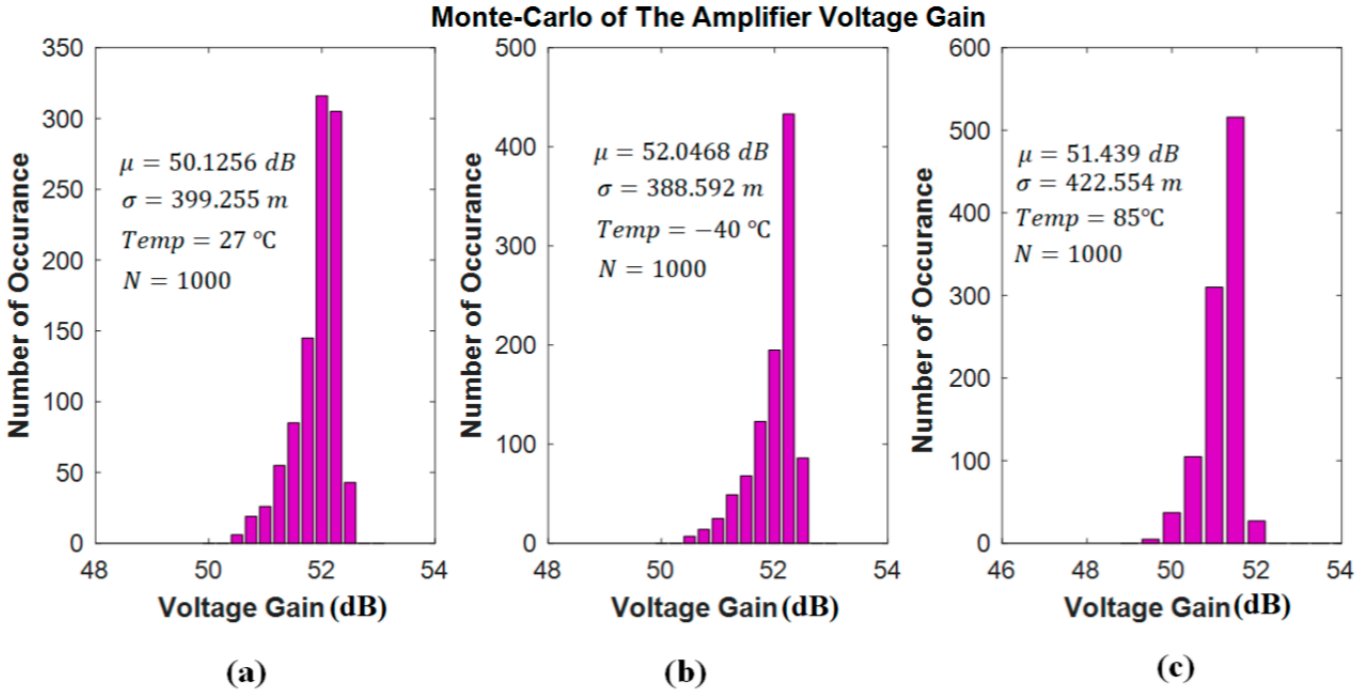

Figure 8. The Monte Carlo analysis of the proposed amplifier's voltage gain for various processes and mismatching at (**a**) 27, (**b**) −40, and (**c**) 85 °C, respectively.

Additionally, the voltage gain varieties versus power supply voltage are displayed in Figure 9. Based on the results, with ±10% changes in power supply, the voltage gain varies between 52.38 and 52.16 dB, while the amplifier gain changes between 53.13 and 51.53 dB when the power supply alters by ±20%.

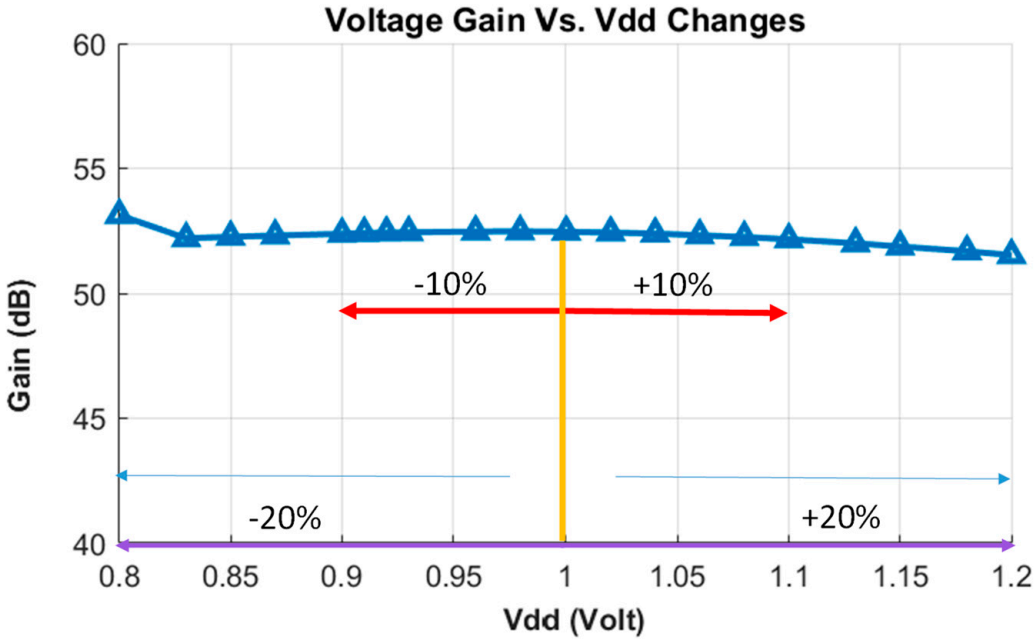

Figure 9. Voltage gain changes in the proposed amplifier due to different power supply voltage ranges.

In addition, the power supply rejection ratio (PSRR) for both rails (positive and negative) is plotted in Figure 10. The PSRR+ and PSRR–equal 54.79 and 52.32 dB, respectively.

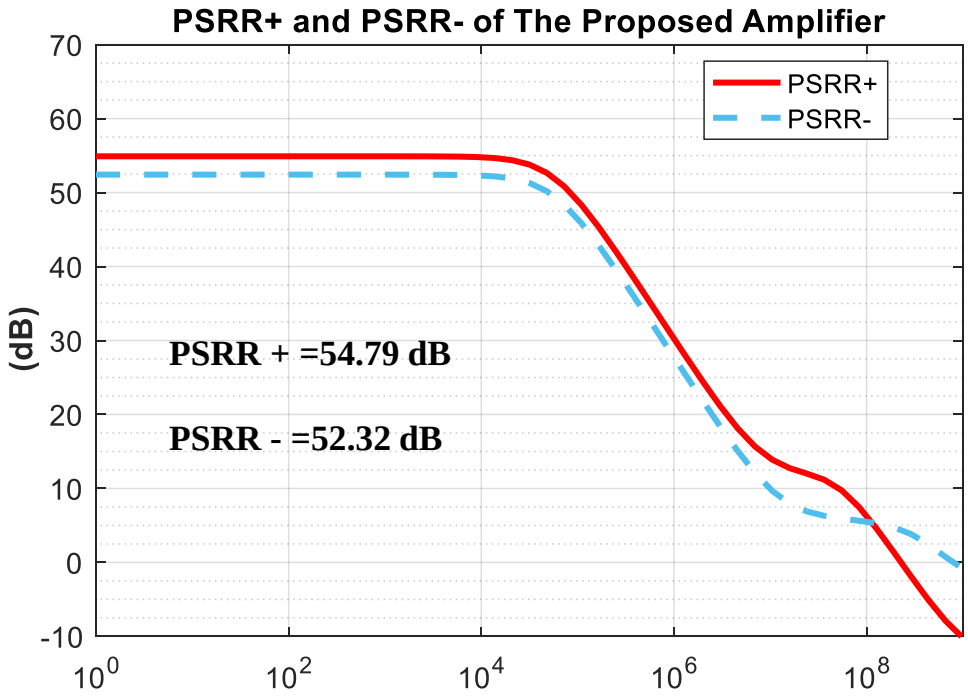

Figure 10. PSRR+ and PSRR- of the proposed inverter-based amplifier.

In Figure 11, the voltage gain changes with different temperatures. In this diagram, the temperature changes from −40 to 85 °C; as a result, the voltage gain varies from 52.37 to 51.79 dB. Therefore, the proposed amplifier has the stability to process temperature, power supply variations, and mismatching.

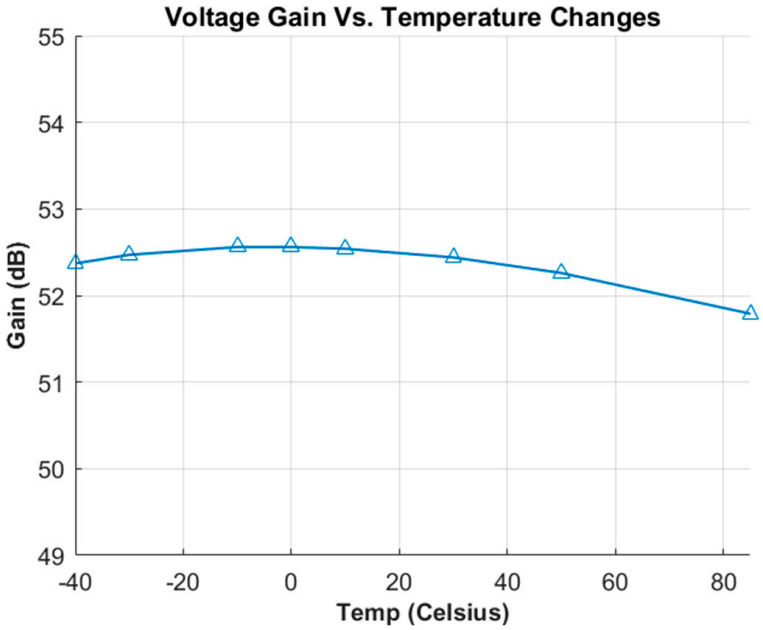

Figure 11. The proposed amplifier's voltage gain changes due to different temperatures.

3.1.2. The Proposed Amplifier's Noise Analysis

Noise reduction is an essential issue in low-power circuit design. Hence, the hearing aid design with low power consumption and low noise is a significant challenge. The equivalent input noise against the frequency analysis of the proposed amplifier is depicted in Figure 12. The root means square of the input noise equals 0.51 µV. In addition, more noise analyzes were performed; SNDR, SFDR, and THD values were obtained as 77.25, 73.35, and −77.25 dB, respectively.

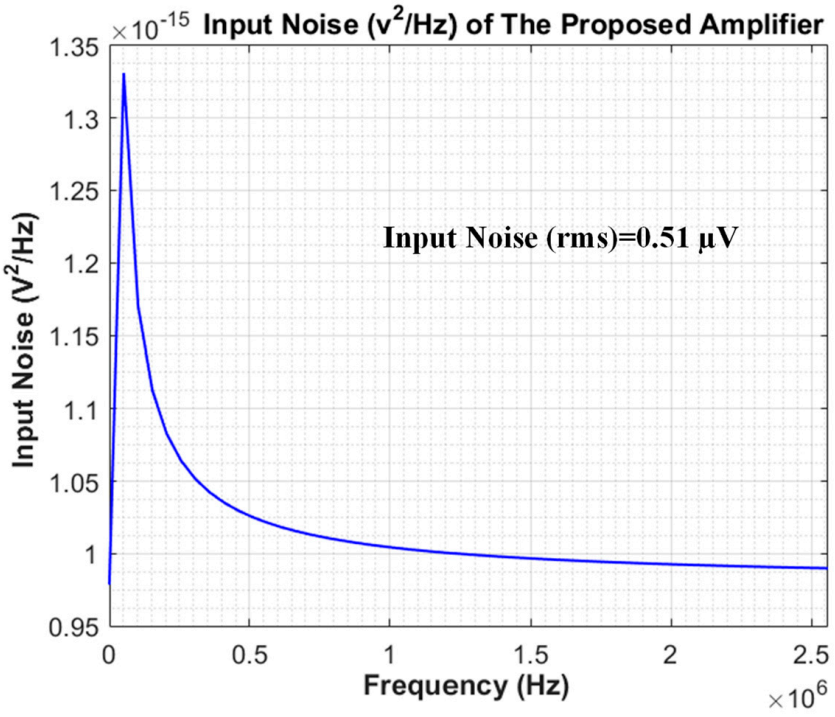

Figure 12. Input noise analysis of the proposed amplifier.

3.1.3. Output Swing Voltage of the Proposed Amplifier

As mentioned above, in this paper, a modulator was presented using a low-power inverter-based amplifier with the improved swing. The high and low output swing voltages of the proposed amplifier's circuit were obtained using Equations (6) and (7), respectively.

$$V_{swing}(Positive) = V_{DD} - |V_{OD}(5)| - |V_{OD}(1)| \quad (6)$$

$$V_{swing}(Negative) = V_{OD}(2) + V_{OD}(6) \quad (7)$$

M_5 and M_6 gate-source voltages are less than the threshold voltage and operate in the sub-threshold region. The positive and negative output swing equal 0.51 and 0.51 V, respectively, and the peak-to-peak swing voltage is 1.01 V. In the sub-threshold region, the overdrive voltage is extremely low, and the drain current of the MOS transistor is obtained from Equation (8) as follows [17,18]:

$$I_{Dsub} = \begin{cases} 2n\mu c_{ox} {V_T}^2 \frac{w}{l} \left(e^{\frac{V_{GS}-V_{th}}{\eta V_T}} \right) \left(1 - e^{-\frac{V_{DS}}{V_T}} \right), \; V_{DS} < 3V_T \\ 2n\mu c_{ox} {V_T}^2 \frac{w}{l} \left(e^{\frac{V_{GS}-V_{th}}{\eta V_T}} \right), \; V_{DS} \geq 3V_T \end{cases} \quad (8)$$

When VDS > 3VT, IDsub is independent of Vds, while IDsub exponentially depends on Vds if VDS > 3VT. According to Table 4, the M_5 and M_6 transistors' overdrive voltages equal −19.43 and 10.75 mV, respectively. Therefore, the output swing increased, leading to an improvement in the efficiency of the proposed modulator. Figure 13 displays the output swing of the amplifier plotted for the input DC voltage of −0.5 V to +0.5 V. Furthermore, the modulator output voltage was plotted for different inputs and shown in Figure 14. In addition, the properties of the proposed modulator are listed in Table 6.

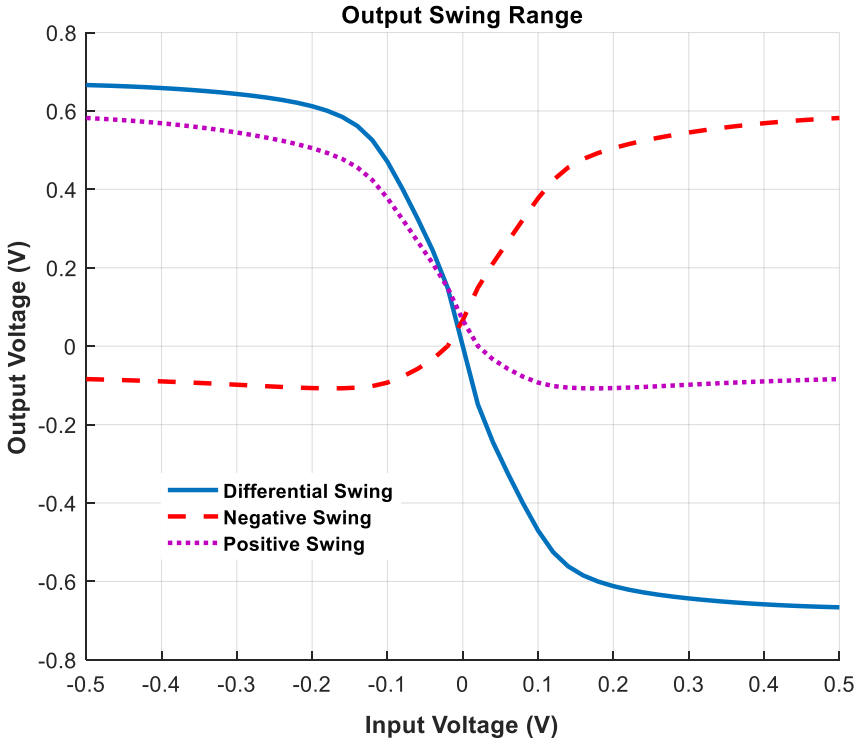

Figure 13. The output swing of the proposed inverter-based amplifier.

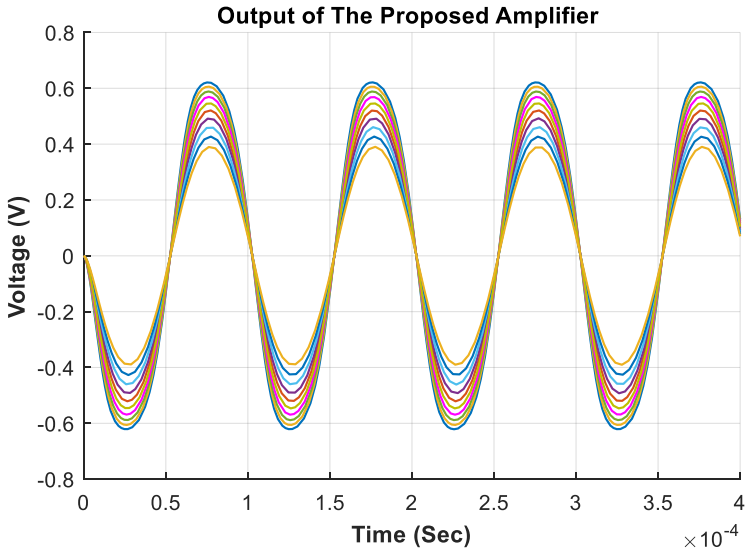

Figure 14. The output voltage of the proposed amplifier for differential input.

Table 6. The specifications of the proposed self-biased inverter-based amplifier.

Parameters	Value
Power Supply (V)	1
Power Consumption (µV)	1.93
Tech (nm)	180
Gain (dB)	52.46
Peak-to-peak Swing Voltage (V)	1.01
Phase Margin (degree)	88.86
Slew Rate + (V/µSec)	104.68
Slew Rate − (V/µSec)	−119.78
PSRR + (dB)	54.79
PSRR − (dB)	52.32
CMRR	64.53
RMS Input Noise (µV)	0.51
SNDR (dB)	77.25
SFDR (dB)	73.35
THD (dB)	−77.25

3.2. Quantizer

As mentioned earlier, a single- or multi-bit quantizer was used in a sigma–delta modulator. The single-bit quantizer is inherently linear, while the multi-bit one is nonlinear, and additional circuits are necessary for linearization. Moreover, using a single-bit quantizer in a high-order modulator (more than second-order) leads to instability. A single-bit quantizer consists of a preamplifier, a comparator, and a latch. A single-bit quantizer was employed in the proposed modulator, and Vref+ and Vref− were considered as 0.8 and 0.2 V, respectively. Figures 15 and 16 illustrate a block diagram of the single-bit quantizer and the quantizer's circuits, respectively.

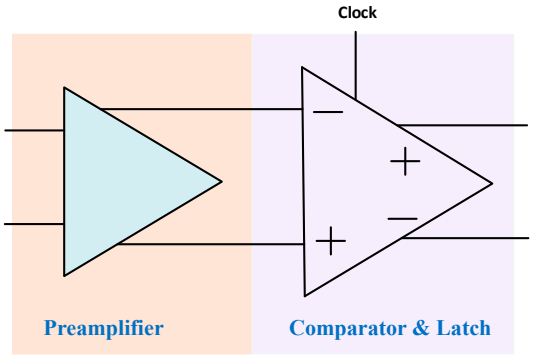

Figure 15. Block diagram of a single-bit quantizer.

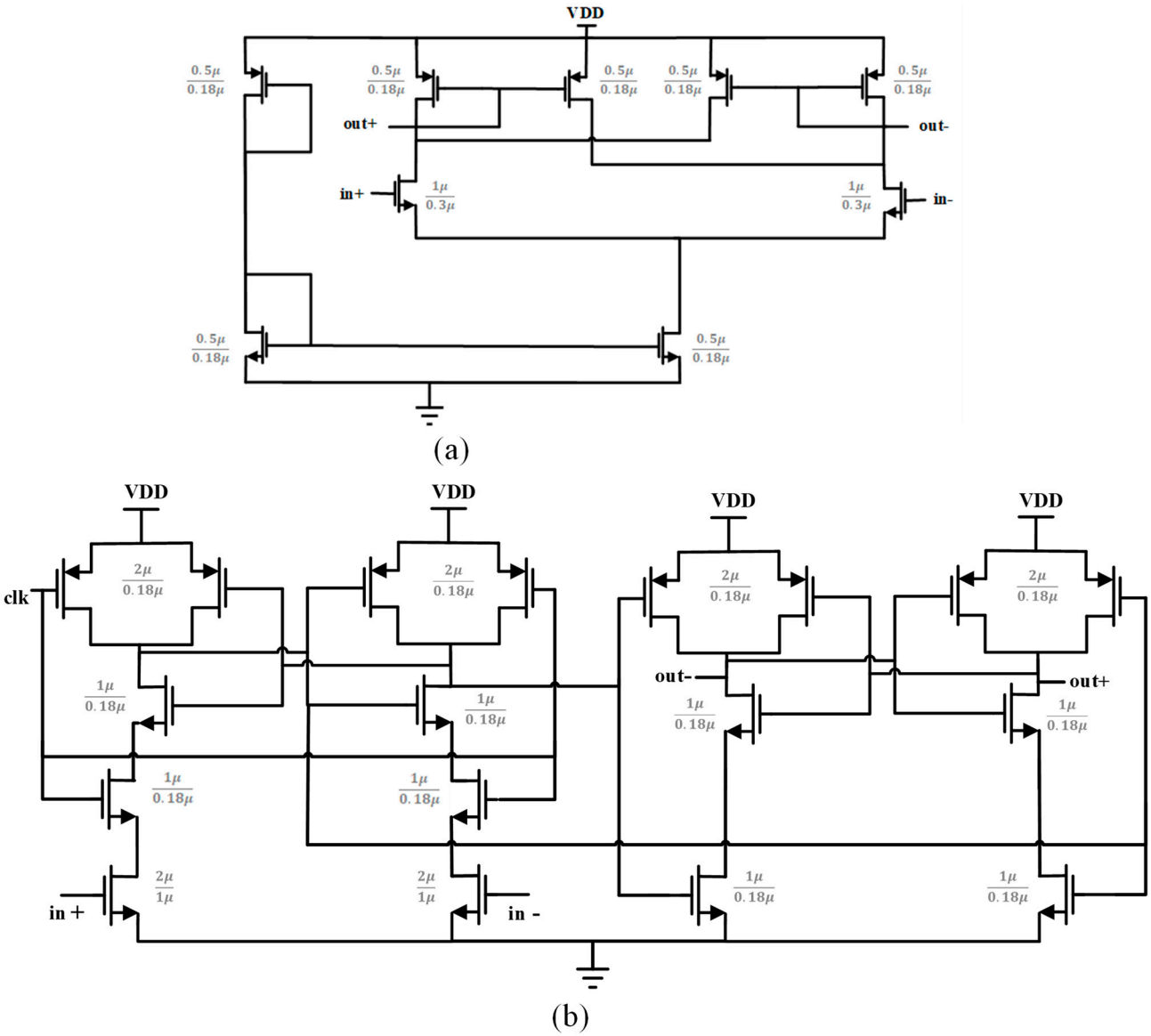

Figure 16. Circuits of the applied single-bit quantizer: (**a**) preamplifier and (**b**) comparator and latch.

3.3. Switches

Transmission gates (TG) were used in the proposed modulator to eliminate charge injection and clock feedthrough effects. The switch circuit is shown in Figure 17. Furthermore, the switches' SNDR, SNR, and THD were obtained from the sinusoidal input (Table 7).

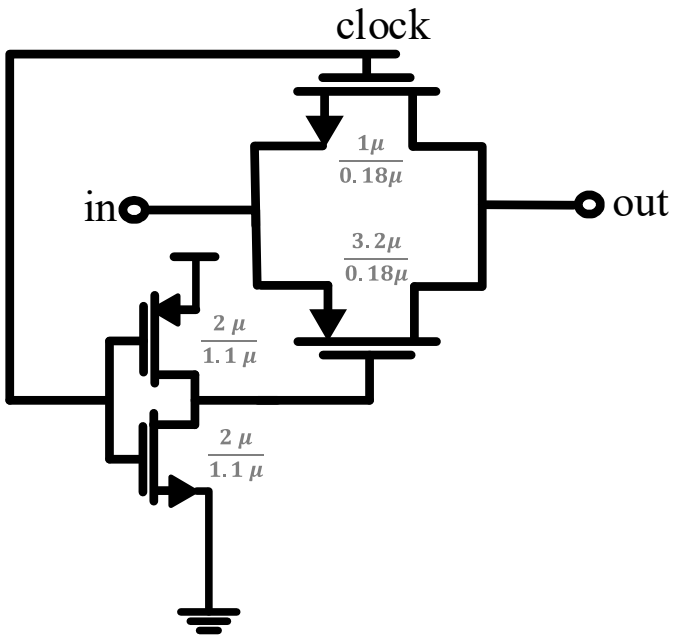

Figure 17. Transmission gate switch circuit.

Table 7. The properties of the proposed modulator TG switch.

SNDR (dB)	SNR (dB)	THD (dB)
71.5	89.5	−42.23

The proposed double sampling second-order, CIFB, single-bit, single-loop modulator was designed for the hearing aid application. The bandwidth frequency and the sampling frequency were 10 kHz and 2.56 MHz, respectively. The simulation results are presented and explained in the next section.

4. Simulation Results

The proposed second-order ΔΣ modulator was simulated using standard 180 nm CMOS technology. The simulation was performed for 16,384 points in a transient CADENCE analysis environment. The input frequency, the sampling frequency, the frequency bandwidth, and the modulator's oversampling ratio were about 1.94 kHz, 2.56 MHz, 10 kHz, and 128, respectively. The two integrator outputs of the proposed modulator are depicted in Figure 18.

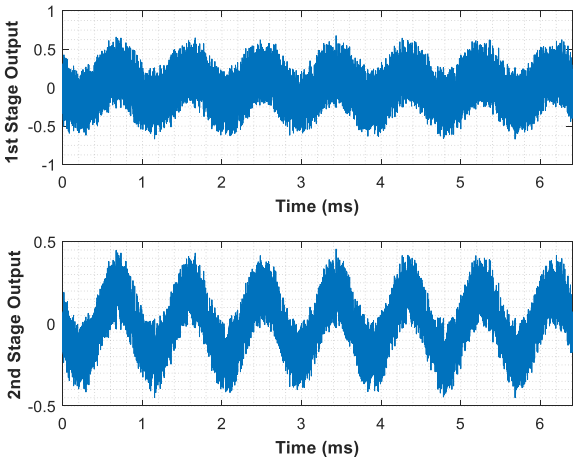

Figure 18. The ΔΣ modulator's two integrator outputs.

Figure 19 illustrates the PSD, spurious free dynamic range (SFDR), and THD of the proposed modulator's pre-layout, post-layout, and post-layout with pad. The pre-layout analysis demonstrates that the modulator achieves an SNDR of 93.27 dB, with 15.2-bit precision, and an SFDR of 99.48 dBc, while the post-layout results represent an SNDR of 85.86 dB, with 13.97-bit precision, and an SFDR of 96.97 dBc. Additionally, the post-layout with pad results reveal an SNDR of 85.92 dB, with 13.98-bit precision, and an SFDR of 103.59 dBc. The DR of the proposed modulator depicted in Figure 20 is equal to 140 dB.

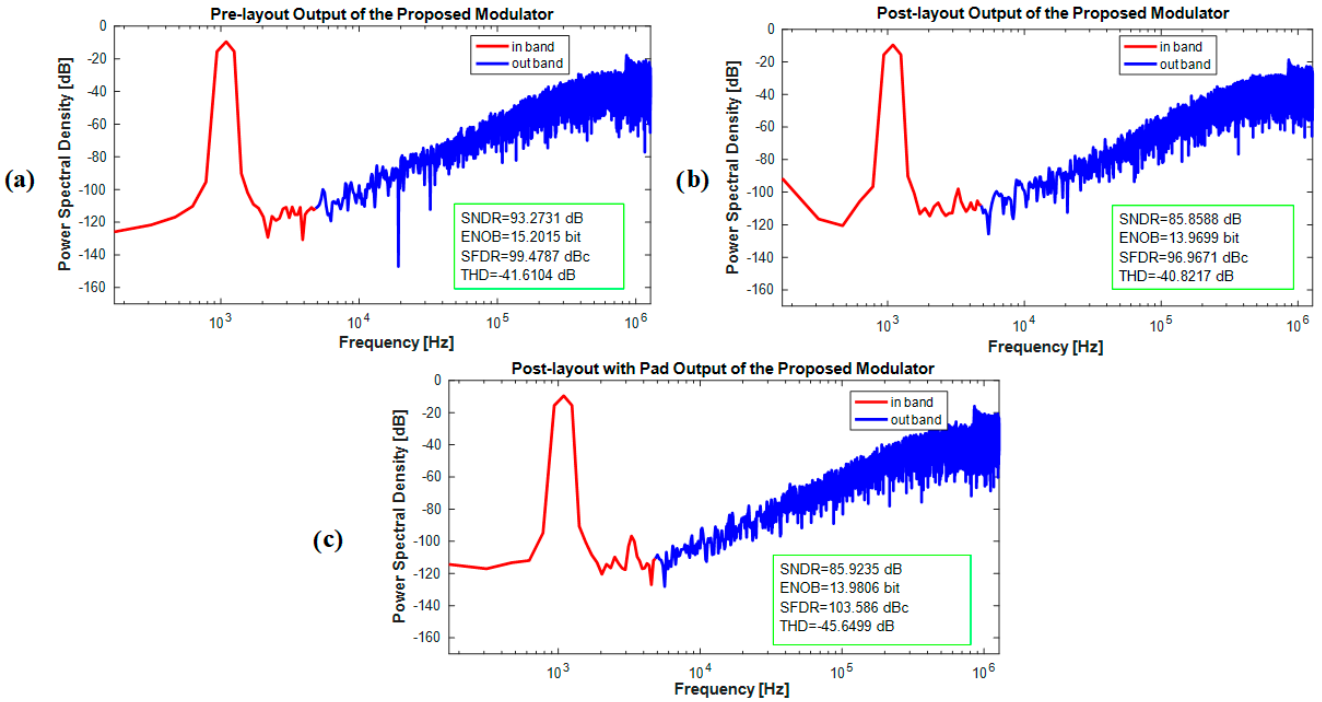

Figure 19. The ΔΣ modulator's PSD, the effective number of bits (ENOB), and THD results: (**a**) pre-layout, (**b**) post-layout, and (**c**) post-layout with pad.

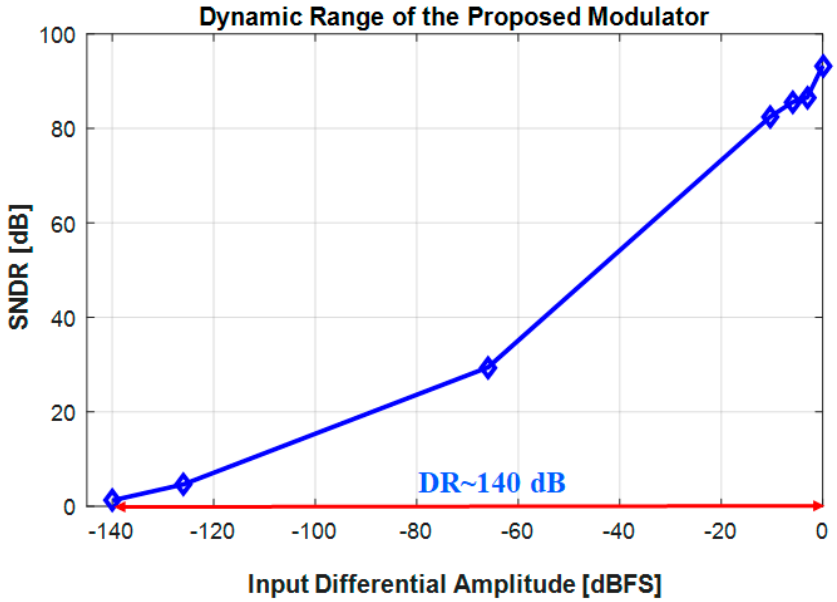

Figure 20. The proposed ΔΣ modulator's dynamic range.

According to the desired specifications for the hearing aid mentioned earlier, the proposed modulator has suitable specifications. The FOM_W, FOM_S, and FOM_{DR} for the proposed modulator were calculated using Equations (9)–(11) as follows [11,19]:

$$FOM_W = \frac{Power\ consumption}{BW * 2 * 2^{\frac{SNDR-1.76}{6.02}}} \tag{9}$$

$$FOM_S = 10 * \log\left(\frac{BW}{Power}\right) + SNDR(dB) \tag{10}$$

$$FOM_{DR} = DR + 10\log\left(\frac{BW}{Power}\right) \tag{11}$$

BW and SNDR represent an input signal bandwidth and an SNDR, respectively. The modulator achieves a FOM_W of 1.31 fJ/step value, while FOM_S and FOM_{DR} are 183.31 and 230.04 dB, respectively. Moreover, the measured power breakdown (Figure 21) demonstrates the main parts of the modulator power consumption separately. The two amplifiers consume a total of 4.48 µW.

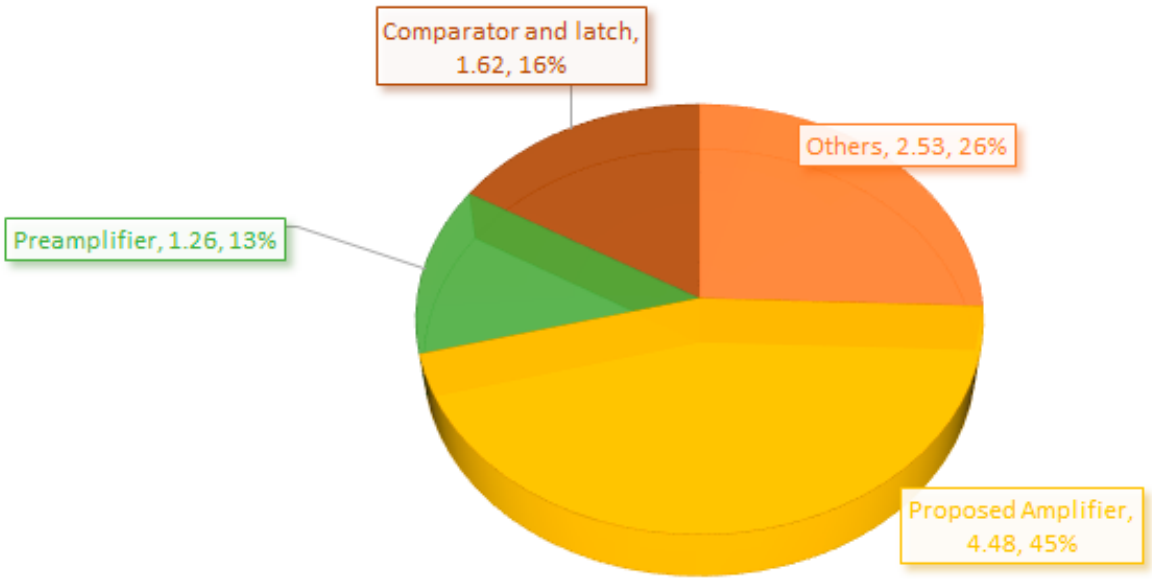

Figure 21. The measured power breakdown (in µW and percent).

Furthermore, Figure 22 depicts the proposed modulator layout. The layout of the designed modular indicates an effective area of 173.41 µm * 100.7 µm $(0.02\ mm^2)$, which is suitable for the hearing aid. The properties of the modulator are summarized in Table 8.

In addition, corner and power supply tests were performed for post-layout validation. A Monte Carlo (Figure 23) analysis with 50 iterations and 16,384 points was performed for the proposed modulator to evaluate SNDR stability against various processes and mismatching. The results of the corner and power supply changes are depicted in Table 9.

The post-layout power supply was swept from 0.7 to 1.8 V and the SNDR of the proposed modulator was calculated (Figure 24). According to the specifications required for the hearing aid, the nominal voltage is 0.9 to 1.1 V. In this range, the SNDR value changes from 82.01 to 88.54 dB and the power consumption is reasonable.

Table 10 presents data on the performance of this activity, and other similar modulators working in the audio bandwidth range. It is clear that the proposed modulator consumes ultra-low power and has valuable features and acceptable FOM compared to the other studies.

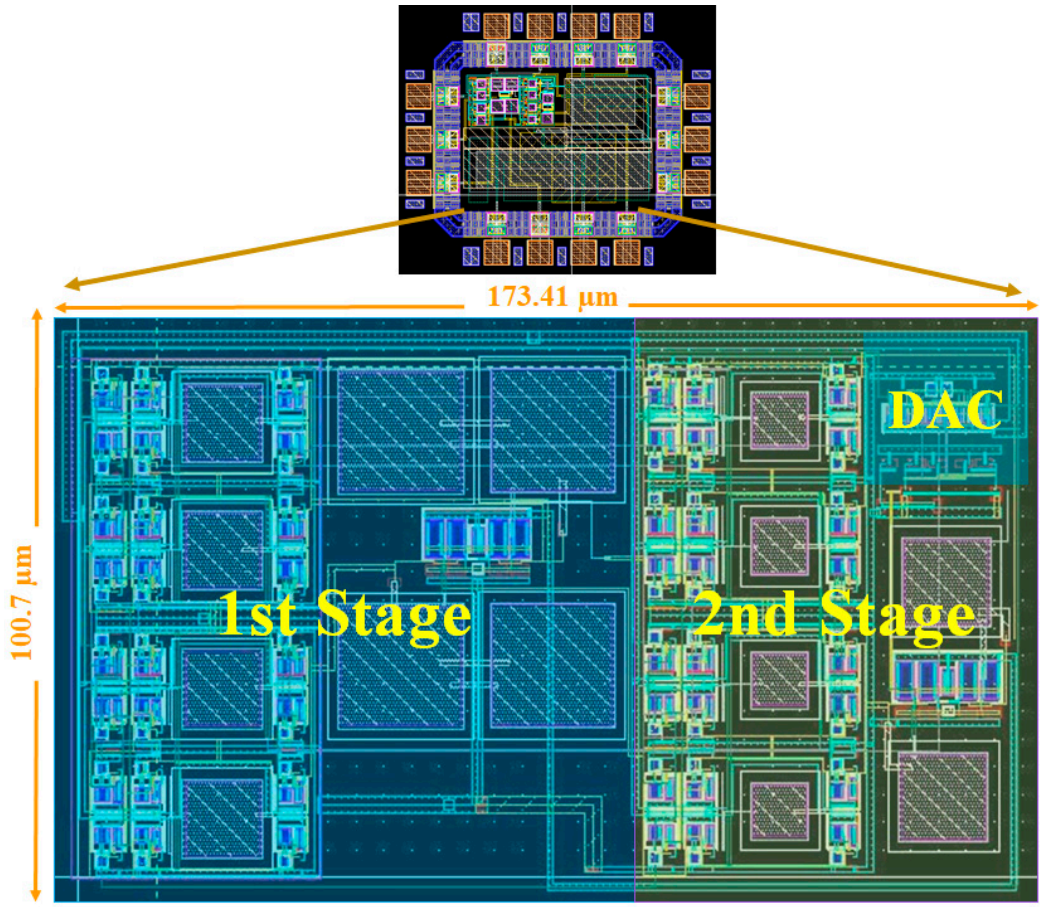

Figure 22. The proposed ΔΣ modulator's layout and floorplan.

Table 8. The proposed modulator's properties.

Modulator Parameters	Value
Power Supply (V)	1
Power Consumption (µV)	9.9
Tech (nm)	180
Peak SNDR (dB)	93.27
DR (dB)	140
Order	2nd order
Structure	Double Sampling CIFB
FOM_s	183.31
FOM_w (fJ/step)	1.31
$FOM_{DR\ (dB)}$	230.04
Area (mm^2)	0.02

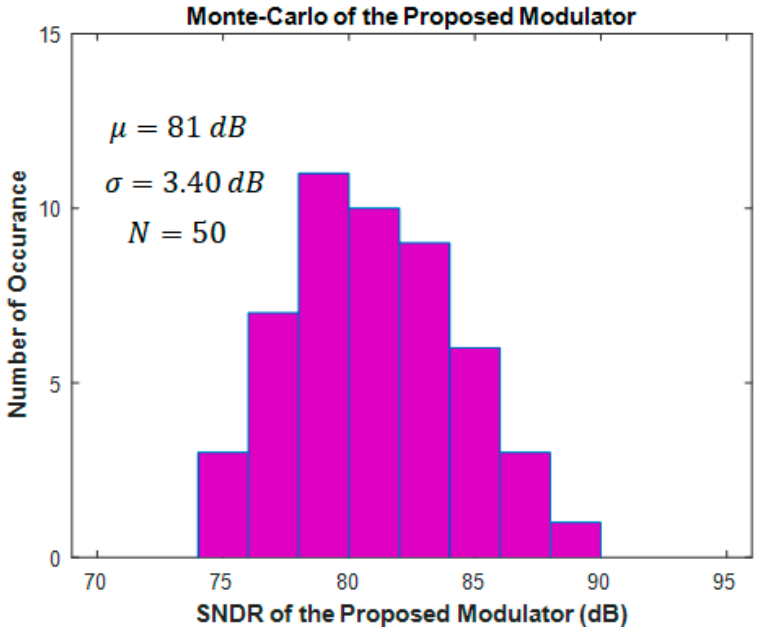

Figure 23. The Monte Carlo analysis of the proposed modulator's SNDR for various processes and mismatching.

Table 9. The post-layout results of the corner and power supply tests.

	Corner	Temp (°C)	SNDR (dB)	SFDR (dB)	THD (dB)	Precision (Bits/Sample)
Post-layout Corner Test	**TT**	27	85.86	96.98	−40.82	13.97
	FF	27	94.75	102.24	−40.88	15.45
	SS	27	69.25	101.68	−39.77	11.21
	SF	27	69.39	84.19	−46.19	11.23
	FS	27	83.98	98.32	−45.48	13.66

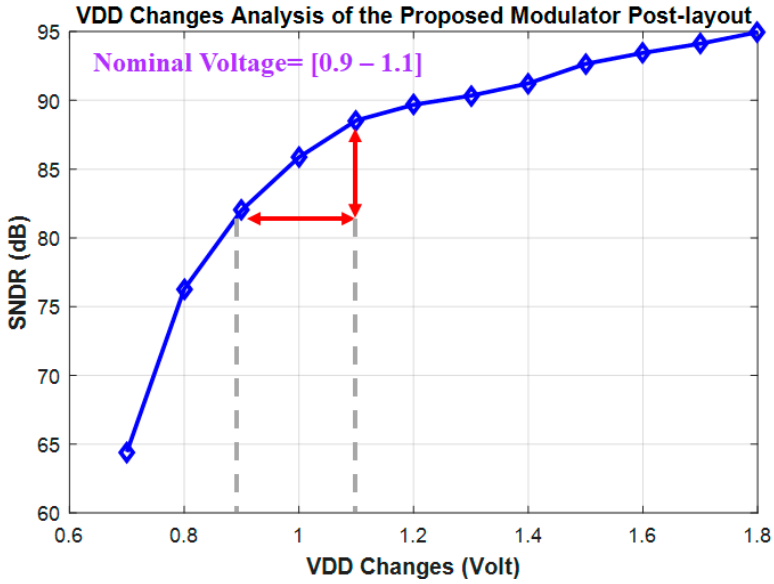

Figure 24. The power supply and nominal voltage analysis of the proposed modulator.

Table 10. The performance comparison of delta–sigma modulators.

Ref.	Vdd [V]	BW [KHz]	OSR	Fs [MHz]	SNDR (dB)	DR (dB)	Pow. (μW)	FOM_S (dB)	FOM_{DR} (dB)	FOM_w (fJ/step)	Tech (nm)	Result	Year
[20]	1.2	20	32	1.28	72.5	91	165	155.5	171.84	92	130	Measure	2012
[21]	1.2	10	128	2.56	87.8	90	148	166	168.3	36	180	Measure	2012
[22]	1.8	10	64	1.28	84.4	88	570	156.84	160.44	210.1	180	Measure	2013
[23]	0.5	20	51.2	2	60.8	70.1	43.4	147.44	156.74	121	65	Measure	2017
[24]	1.2	20	76.8	3.07	101.4	105.7	3500	168.97	173.27	91	130	Measure	2018
[25]	1	25	100	5	94.6	98.5	175	176.15	180	7.97	65	Measure	2018
[26]	0.9	20	128	5.12	86.4	91	103.4	169.27	173.86	150	180	Measure	2018
[11]	0.8	24	64	3.07	89.6	91	49.6	176.6	178	50.6	65	Measure	2019
[10]	1.2	20	64	2.56	81.17	NA	54	166.86	NA	14.44	180	Simulate	2019
[27]	1.8	25	128	3.2	106	NA	3650	169.4	NA	44.75	180	Measure	2020
[28]	1.8	25	256	12.8	106.1	102.3	2200	171.16	172.86	50.23	180	Measure	2021
[29]	1.8	10	16	0.32	74.24	78	36	158.68	162.44	42.75	180	Simulate	2021
[30]	1.8	10,000	8	160	98.4	101	26,300	184.2	186.8	1.93	180	Simulate	2021
[31]	1	19.5	256	10	88.5	91.7	43.5	175	178.2	51.2	180	Measure	2021
[32]	1.8	24	64	3.07	96.2	98	340	174.7	176.49	13.42	180	Measure	2022
[33]	1.8	1.5	341.3	1.024	118.1	126	1600	177.8	185.72	81.17	180	Simulate	2022
[34]	1.1	156.25	8	2.5	83.1	84	70.3	176.57	177.47	1.93	180	Simulate	2022
This work	1	10	128	2.56	93.27	140	9.9	183.31	230.04	1.31	180	Simulate	2023

5. Discussion

This study aims to provide a sigma–delta modulator with ultra-low power consumption and suitable efficiency for hearing aid applications. DR is significant for this application since the modulator will be saturated and create an unpleasant sound for the user if DR is unsuitable. On the other hand, hearing aids are permanently used, and high power consumption leads to rapid battery discharge. Hence, there is a trade-off between the DR value and power consumption. In this design, an inverter-based amplifier with improved output swing was applied in a modulator that increased voltage swing using the multi-region bias method, and the FOMs, FOMw, and FOM_{DR} show the modulator's proper efficiency.

6. Conclusions

The current article presented an ultra-low-power second-order double-sampling DT sigma–delta modulator with a CIFB structure for digital hearing aids. For the circuit implementation of the modulator, the inverter-based amplifier with swing enhancement was proposed and used instead of power-hungry OTAs. Based on the findings (Table 6), the proposed amplifier worked at 1 V and consumed 1.93 μW, while the DC gain and the swing voltage were 52.46 dB and 1.01 V, respectively. Furthermore, the modulator functioned at a sampling frequency of 2.56 MHz and an input signal bandwidth of 10 kHz. It also consumed about 9.9 μW at 1 V with an SNDR of 93.27 dB. The 15.2-bit modulator had a dynamic range of 140 dB and a THD of −41.61 dB. Therefore, the proposed modulator is appropriate to use in hearing aids.

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