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A Charge Sensitive Amplifier in a 28 nm CMOS Technology for Pixel Detectors at Future Particle Colliders

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Abstract: This paper is concerned with the design of a Charge Sensitive Amplifier (CSA) in a 28 nm CMOS technology. The CSA discussed in this work is conceived for High Energy Physics (HEP) experiments at next-generation colliders, where pixel detectors will be read out by specific front-end chips, typically including a CSA exploited for charge-to-voltage conversion of the signal delivered by the sensor. The main analog performance parameters of the CSA, also referred to as the pre-amplifier, are assessed here by means of specific Spectre simulations, which are meant to evaluate the behavior of the analog processor in terms of noise, linearity and capability to compensate for very large detector leakage currents. Noise simulations revealed an equivalent noise charge close to 75 electrons rms for typical operating conditions. Up to 50 nA sensor leakage current can be compensated for thanks to the CSA Keummenacher feedback network. The total current consumption of the CSA is close to 2.2 µA, which, together with a power supply of 0.9 V, translates to a power consumption of 2.0 µW.

Keywords: charge sensitive amplifier; pixel sensors; low-noise electronics

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1. Introduction

High Energy Physics (HEP) experiments at the next-generation colliders call for advanced pixel detectors read out by means of radiation hard front-end chips, typically including a Charge Sensitive Amplifier (CSA), also referred to as pre-amplifier, which converts the charge delivered by the sensor into a voltage signal for further on-chip processing.

The state-of-the-art pixel readout chips in the HEP community are being developed by the CERN RD53 Collaboration [1], and are focused on the planned upgrades (called phase-II upgrades) of the CMS and ATLAS experiments at the Large Hadron Collider (LHC) [2,3]. The RD53 chips are fabricated in a 65 nm CMOS technology and expected to survive a Total Ionizing Dose (TID) of about 1 Grad (SiO_2), accumulated in around 10 years of operation, while being able to deal with particle hit rates of the order of 3 GHz/cm^2. Three different analog front-end designs have been developed in the framework of RD53 [4]. The front-ends are called Synchronous, Linear and Differential, and they feature an overall area (including the CSA, the comparator and other ancillary blocks, such as the charge injection circuit and in-pixel threshold tuning DAC) of 35 × 35 µm^2. The Synchronous and Linear front-ends include a CSA with a Krummenacher feedback network [5] for detector leakage current compensation, while the Differential front-end features a constant current mirror feedback, with a dedicated slow feedback path for sensor leakage compensation. The performance of the RD53 analog front-ends has been compared and reported in [6].

The HEP designers' community is now migrating to the 28 nm node, which is the major commercial successor of the 65 nm one, for the development of IP blocks and, in general, readout circuits for future experiments, including possible post phase-II LHC upgrades [7,8]. Recent studies carried out on single transistors fabricated in the 28 nm technology point to a high degree of radiation tolerance for such a technology node [9,10]. This finding, together with the possibility of pushing more intelligence at the pixel-level,

thanks to denser digital logic integrated in the front-end circuits, makes the 28 nm process an ideal candidate for the development of next-generation pixel readout chips for HEP.

In this work, the design of a charge sensitive amplifier in a commercial 28 nm CMOS technology is discussed. The presented CSA is, together with the front-end described in [11], amongst the first ones designed by the HEP community in the 28 nm process. The main simulation results, mostly concerned with noise performance, stability, and capability to operate with sizable detector leakage currents, are presented.

2. The Charge Sensitive Amplifier

The charge sensitive amplifier presented in this work is based on the so-called Krummenacher architecture, serving the two-fold purpose of compensating for the detector leakage current and restoring the pre-amplifier baseline after signal arrival. The schematic diagram of the CSA is shown in Figure 1.

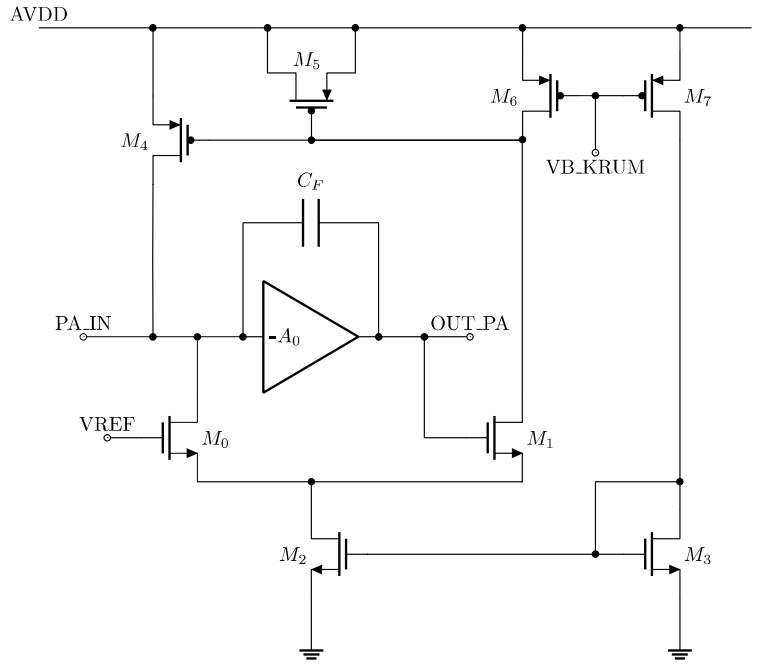

Figure 1. Schematic diagram of charge sensitive amplifier with Krummenacher feedback network.

The pre-amplifier includes a gain stage, whose schematic is shown in Figure 2, and a differential pair (M0 and M1) biased with the tail current generator, implemented by means of M2, draining a current I_K set to 25 nA. The PMOS transistor M6 also implements a current generator, sourcing a current equal to $I_K/2$. Thus, in quiescent conditions, the same current—$I_K/2$—flows in M0 and M1, and the DC level at the output is locked to the voltage *VREF* applied to the gate of M0. Small signal analysis of the circuit leads to the formulation of the following transfer function, featuring two poles p_1 and p_2:

$$H(s) = \frac{V_{out}}{Q_{in}} \approx \frac{2/g_{m1}}{\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right)} \tag{1}$$

where V_{out} is the Laplace transform of the output signal, Q_{in} is the charge delivered by the detector connected to the input pin (*PA_IN*), and g_{m1} is the transconductance of M1 transistor. It can be easily shown that the angular frequencies—p_1 and p_2—of the two poles are given by:

$$p_1 = \frac{g_{m1}/2}{C_F} \tag{2}$$

with C_F being the preamplifier feedback capacitance, and

$$p_2 = A_0 p_0 \frac{C_F}{C_F + C_D} \tag{3}$$

with C_D being the detector capacitance, A_0 and p_0 the DC gain and the angular frequency of the dominant pole of the preamplifier gain stage, respectively. By assuming an angular frequency p_2 much larger than p_1, the time response of the pre-amplifier to a delta-like charge input signal can be shown to be:

$$Vout(t) \approx U(t) \frac{Q_{in}}{C_F} [\exp(-p_1 t) - \exp(-p_2 t)] \tag{4}$$

$U(t)$ being the step function. As p_2 is much larger than p_1 (as in the case of the discussed preamplifier), Equation (4) can, thus, be approximated by means of a step function, with amplitude given by Q_{in}/C_F. Hence, the charge-to-voltage conversion factor provided by the CSA, usually referred to as charge sensitivity G_Q, is given by:

$$G_Q \approx \frac{1}{C_F} \tag{5}$$

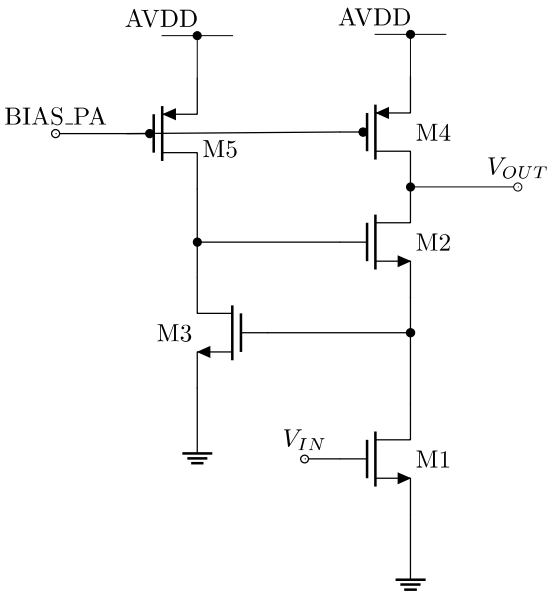

Figure 2. Schematic diagram of preamplifier gain stage.

In the actual design of the preamplifier, C_F has been implemented by means of a Metal–Oxide–Metal (MoM) capacitor of 4 fF. It is worth noticing that Equation (4) holds for small input signals not able to fully unbalance the differential pair M0-M1. On the other hand, for a large input charge, the Krummenacher feedback network gets saturated, and the feedback capacitance—C_F—is linearly discharged by a constant current $I_K/2$. In the presence of a detector leakage current, the feedback path reacts in such a way to adjust the potential at the gate of the M4 PMOS transistor, which, thus, carries the quiescent current—$I_K/2$—plus the DC leakage current itself, preventing the saturation of the CSA.

The schematic diagram of the CSA gain stage is shown is Figure 2. The input signal—V_{IN}—is fed to the gate of M1, whereas the output signal is obtained at the drain of M2 and M4 transistors. The gain stage is biased with a current of 2 μA flowing in the input

branch, and a current close to 200 nA in the branch including M3. The stage implements a regulated cascode architecture, whose low frequency gain—A_0—can be shown to be:

$$A_0 \approx -\frac{g_{m1}}{\frac{g_{ds1}g_{ds2}}{g_{m2}}\frac{g_{ds3}}{g_{m3}} + g_{ds4}} \tag{6}$$

where g_{dsi} and g_{mi} are, respectively, the drain-to-source conductance and the transconductance of transistor Mi.

A figure of merit of paramount importance in the field of front-end electronics for pixel detectors is the so-called Equivalent Noise Charge (ENC), which is defined as the input charge for which the front-end Signal-to-Noise ratio is equal to 1. It is possible to compute the ENC by means of:

$$ENC = \frac{v_{n,out}}{G_Q} \tag{7}$$

where $v_{n,out}$ is the noise root mean square evaluated at the preamplifier output. With reference to Figure 1, it can be shown that:

$$ENC^2 \propto C_D^2 ENC^2 \propto \frac{g_{m4}}{g_{m1}} \tag{8}$$

Hence, the equivalent noise charge is expected to increase by increasing the detector capacitance, as well as for larger detector leakage currents, where the transconductance of the PMOS transistor M4 might become significantly larger than the one of M1.

3. Simulation Results

Figure 3 shows the open-loop gain of the CSA simulated with different models (namely, TT, FS, SF, FF and SS; T = typical, F = fast, and S = slow) at a temperature T = −20 °C (i.e., the typical operating temperature for pixel sensors in current HEP experiments), with a default power supply voltage of 0.9 V.

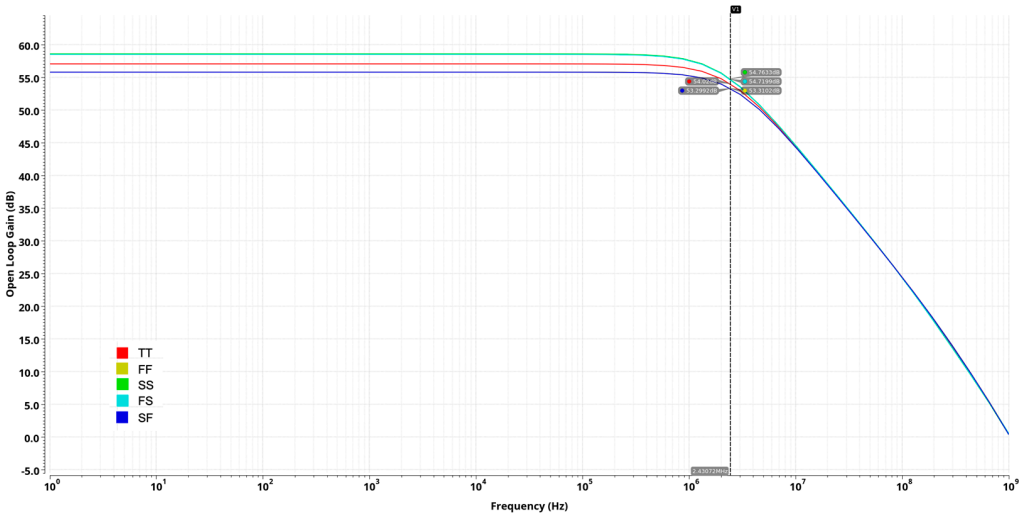

Figure 3. Simulated open-loop gain of charge sensitive amplifier.

The open-loop gain A_0 was found to be close to 57 dB in the TT corner, with a cut-off frequency close to 2.4 MHz. The maximum simulated gain was obtained in the SS corner, being A_0 = 58.6 dB, while the minimum was achieved in the FF corner, with A_0 = 55.8 dB.

The time behavior of the preamplifier is reported, again for different simulation corners, in Figure 4, which shows the CSA output in response to different input charges (namely, 1000, 6000, 10,000, 15,000 and 20,000 electrons). Except for the response obtained for an input charge Q_{in} = 1000 electrons, where the differential pair in the CSA feedback network is not fully unbalanced, it is possible to appreciate the linear return to baseline,

together with an undershoot that was found to be larger for larger input charges. In order to evaluate the linearity of the preamplifier, Figure 5 shows the CSA peak amplitude as a function of the input charge.

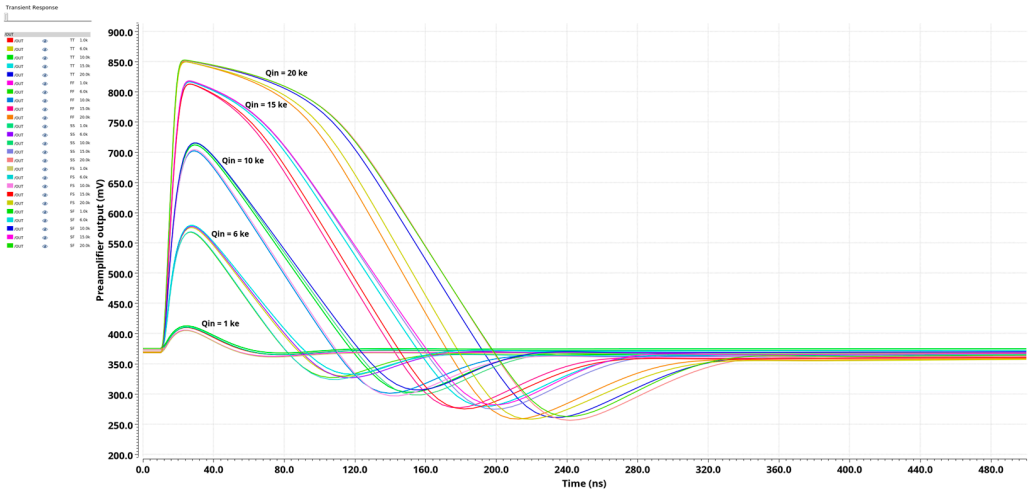

Figure 4. Simulated output of charge sensitive amplifier in response to an input charge ranging from 1000 to 20,000 electrons.

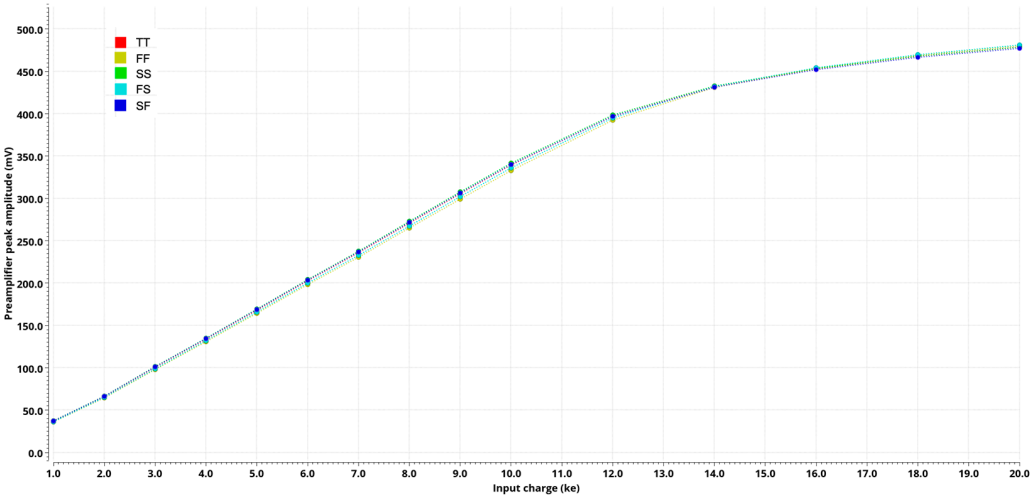

Figure 5. Preamplifier peak amplitude as a function of input charge.

A linear behavior was achieved for input signals up to 10000 electrons, whereas for larger signals the CSA output tends to saturate. However, it is worth noticing here that, for detectors with a thickness of the order of 100–150 µm (as the ones foreseen for the phase-II upgrades of CMS and ATLAS experiments at the LHC [12,13]), the most probable value of the charge delivered by the sensor is close to 6000 electrons. Such a value is reduced to around 4000 electrons for irradiated sensors.

The stability of the CSA was assessed by means of the STB analysis in Spectre by breaking the feedback loop at the preamplifier input. With reference to Figure 1, it is worth noticing that a low frequency pole, not captured through the simplified expression of the transfer function reported in Equation (1), is associated with the node connected to the gate of transistor M4. Such a pole is placed at a very low frequency, proportional to the ratio of the transconductance of M4 and the capacitance provided by the MOS capacitor M5. Stable operation of the CSA is guaranteed by maximizing the M5 capacitance. Figure 6 shows the simulated phase margin, for different corners, as a function of the detector capacitance. The phase margin was found to lie in a range between around 84° and 60°, which was obtained for the maximum simulated detector capacitance of 100 fF.

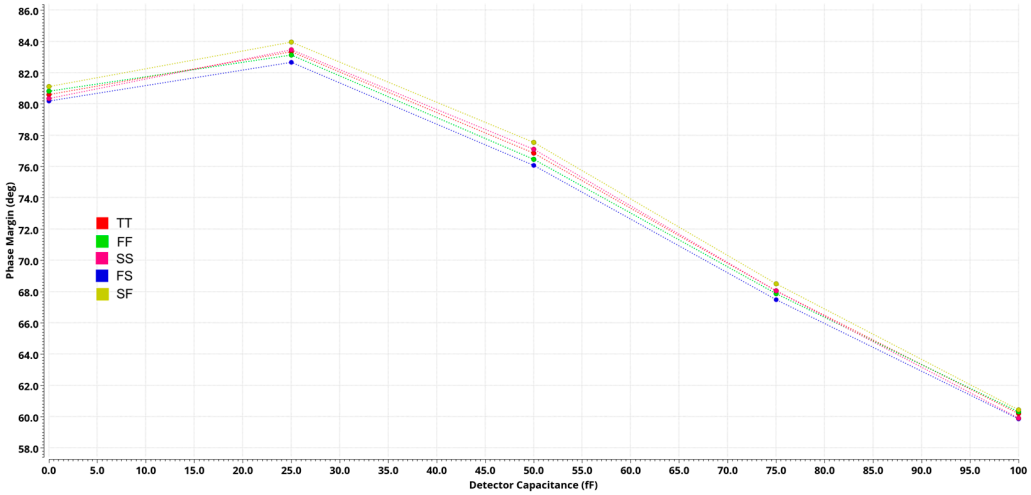

Figure 6. Simulated phase margin as a function of detector capacitance.

Figure 7 shows the equivalent noise charge, as a function of the detector capacitance, for different simulation corners.

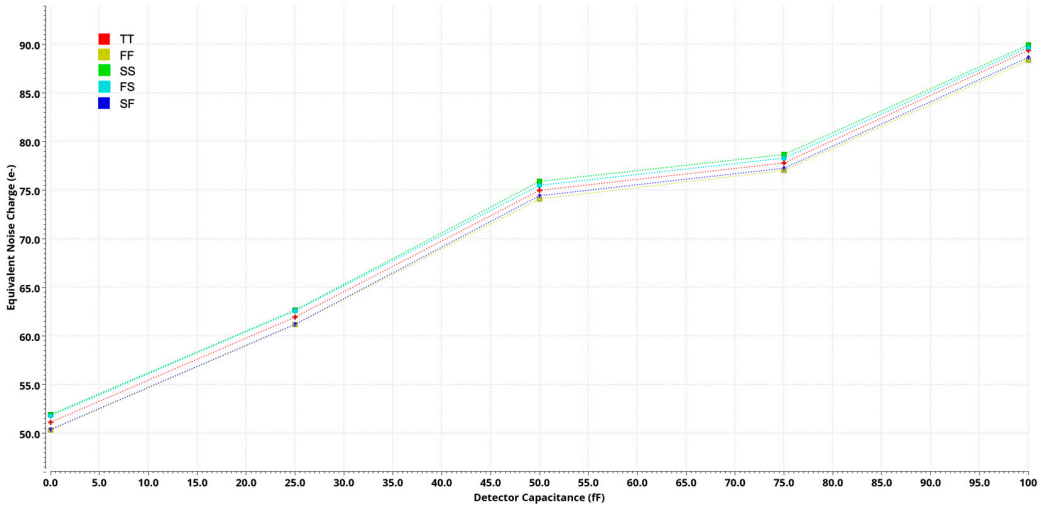

Figure 7. Simulated equivalent noise charge as a function of detector capacitance.

As pointed out in Equation (8), the ENC increases by increasing the detector capacitance—C_D—with a noise level close to 75 electrons rms achieved for C_D = 50 fF, which is the capacitance expected for the sensors to be operated in the phase-II upgrades of the CMS and ATLAS experiments at the LHC. It is worth noticing that the ENC performance of the charge sensitive amplifier discussed in this work is comparable to the performance obtained in the RD53 front-ends [6], leading to a Signal-to-Noise Ratio of 38 dB.

The capability of the CSA to deal with large, radiation-induced detector leakage current is demonstrated in Figure 8, which shows the preamplifier output in response to an input signal of 4000 electrons (as mentioned, this is the most probable value for the charge delivered by an irradiated pixel sensor in the high-luminosity upgrades of CMS and ATLAS).

Both the preamplifier baseline and the peak amplitude were found to be almost insensitive to the detector leakage. This finding is also confirmed in Figure 9, which shows the DC output as a function of the leakage current. A variation close to 0.1% was obtained in simulation for the worst-case detector current—I_L—of 50 nA. From the standpoint of time domain response, Figure 8 points to a slightly faster discharge of the CSA feedback capacitance in the presence of a detector leakage current. From simulation, the discharge

process with I_L = 50 nA is around 4 ns faster compared to the case of a CSA connected to a non-leaky detector.

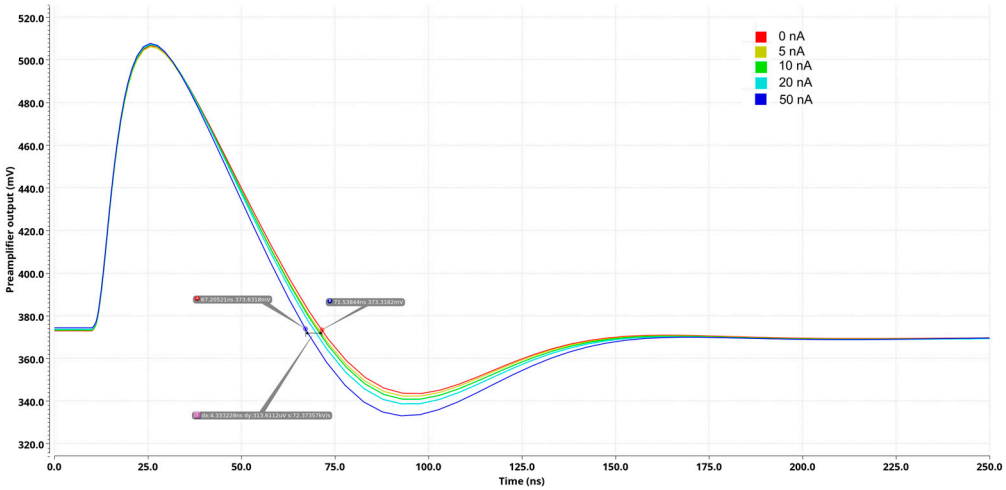

Figure 8. Preamplifier output in response to an input charge of 4000 electrons, with a detector leakage current ranging from 0 (red curve) to 50 nA (blue curve), in TT corner.

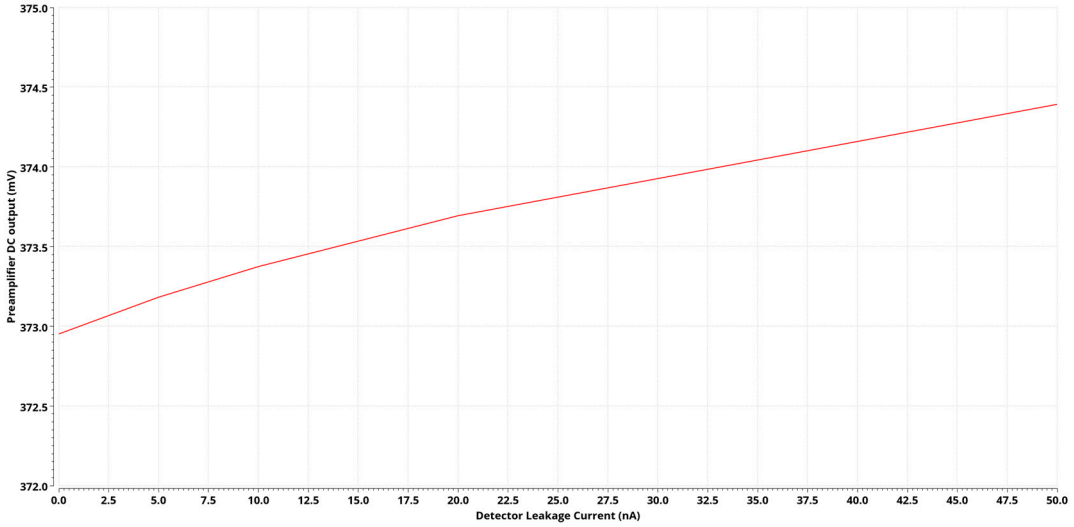

Figure 9. Pre-amplifier DC output as a function of detector leakage current, for the TT corner.

Another key point in the design of the CSA is the uniformity of the DC output from pixel to pixel. Since, in this design, the charge sensitive amplifier is DC coupled to the subsequent stage (i.e., the threshold discriminator), the pixel-to-pixel preamplifier baseline mismatch directly translates to threshold non-uniformity in the readout matrix. To guarantee very low threshold operation, an in-pixel threshold tuning DAC is typically integrated in front-end channels for HEP applications [TDAC].

Figure 10 shows the distribution of the pre-amplifier baseline as obtained from a Monte-Carlo simulation with 500 runs. The standard deviation of the DC output is close to 5.7 mV, which, divided by the nominal charge sensitivity of the channel (35 mV/ke$^-$), translates to a threshold dispersion around 160 electrons rms. It is worth noticing that this value is significantly larger than the simulated ENC; hence, an in-pixel DAC for fine threshold tuning is strictly needed in this design.

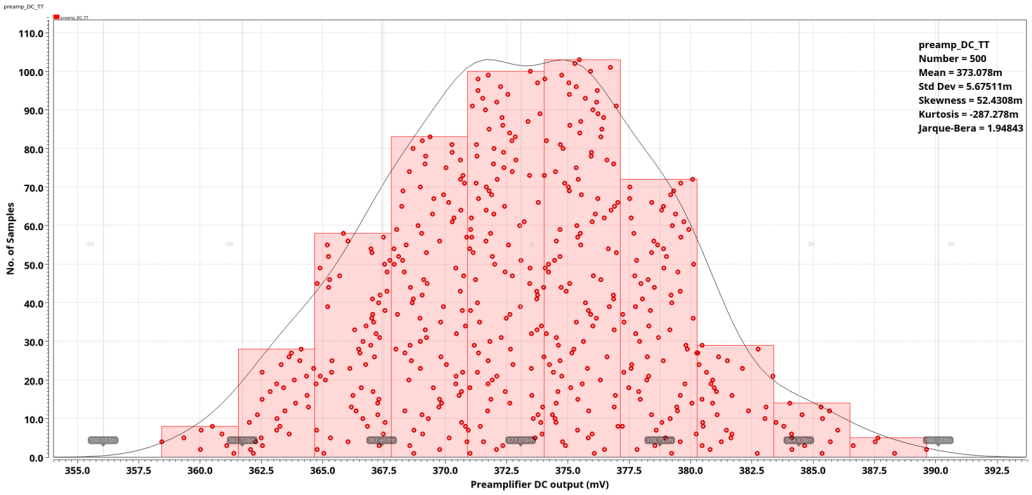

Figure 10. Pre-amplifier DC output as obtained from a Monte-Carlo simulation with 500 runs.

The layout of the charge sensitive amplifier is shown in Figure 11. The size of the analog macro is 6.5 × 21.5 μm^2; for reference, it is worth recalling here that the size of the macro, including the CSA, the comparator stage and other ancillary in-pixel blocks, in the RD53 chips is close to 35 × 35 μm^2.

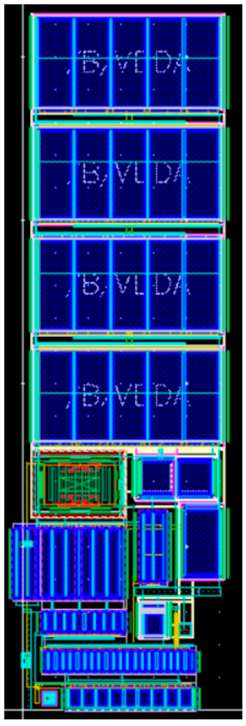

Figure 11. Layout of charge sensitive amplifier. Size of cell is 6.5 × 21.5 μm^2.

4. Conclusions

The design of a charge sensitive amplifier conceived for pixel detector applications and HEP experiments was presented. The CSA was designed in a commercial 28 nm CMOS technology and a number of circuit simulations, mainly concerned with noise, stability and capability of the CSA to compensate for detector leakage currents, were carried out. The preamplifier discussed in this work featured a Krummenacher feedback network topology, which was proved to be able to withstand sensor leakage currents up to 50 nA with a negligible DC shift at the CSA output. Noise simulations revealed an equivalent noise charge of 75 electrons rms for a detector capacitance of 50 fF, comparable to the

noise performance achieved in the pixel front-end chips developed by the CERN RD53 collaboration, which is currently developing the readout ASICs for the planned upgrades to the CMS and ATLAS experiments at the Large Hardon Collider. The overall current consumption of the proposed CSA is close to 2.2 μA, which, together with a power supply voltage of 0.9 V, translates to a power consumption of about 2 μW.

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Conflicts of Interest: The authors declare no conflict of interest.

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