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An Integrated Charge Pump for Phase-Locked Loop Applications in Harsh Environments

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Abstract: Among all the functions that electronics currently perform, clock synthesis has a backbone role. Charge pump phase-locked loops (CP-PLL) are widely used to accomplish clock synthesis thanks to their versatility. One of the most critical parts of CP-PLLs is the charge pump, which greatly influences the system's performance. Even though several high-performance charge pumps have been proposed in the past, with the quick spread of electronics in all the engineering fields, the design of such electronic devices has encountered several additional challenges dictated by external environmental conditions. Examples of these engineering sectors are space, aerospace, industrial, and automotive applications, where the charge pump has to face high environmental temperatures and radiation effects. As a consequence, its design and experimental characterization have to be performed to ensure reliability when operating in harsh conditions. However, to the best of the authors' knowledge, no works in the literature have ever presented a complete charge pump design and characterization in such harsh environments. Therefore, to fill this gap, this paper presents a charge pump for PLL applications specifically designed to reach operating temperatures up to 200 °C and total ionizing dose levels up to 100 Mrad. All design choices have been experimentally verified and are discussed throughout the paper in detail. With the proposed design, we obtained an output current variation of less than 8% at 200 °C and less than 2.5% at 100 Mrad. As opposed to the CPs that can be found in the literature, these results were measured on silicon. The performed measurements confirm that the current variation at 200 °C is better than that of the state-of-the-art CPs operating at lower temperatures, which, moreover, were only simulated.

Keywords: charge pump; phase-frequency detector; total ionizing dose; high-temperature electronics; harsh environments; reliable electronics; integrated circuit design and characterization

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1. Introduction

Electronic components have been used pervasively in many applications, each of them characterized by specific constraints and challenges. Among these challenges, the most extreme ones are mainly related to harsh environmental phenomena, such as high temperatures, which may characterize the application environments, and the presence of radiation. Non-exhaustive examples of applications in which high temperatures undermine electronics' reliability are space, avionics, and aerospace applications, where the temperature can reach values up to 150 °C [1–4], as well as automotive and several industrial sectors, where the maximum temperature may reach 200 °C [5,6]. On the other hand, in space and aerospace environments, radiation can severely undermine electronics' reliability [7–9]. Therefore, the characterization of electronic components designed to operate in harsh environments needs to be performed in very high-temperature conditions, and in the presence of radiation.

Among all the functions that electronics carry out, clock synthesis is required in almost any complex system, spanning telecommunications and microprocessor design. In general, clock synthesis performs a backbone role in any system employing digital electronics.

Several strategies to generate clock signals have been proposed and used in the past. Among them, the phase-locking technique, which is achieved thanks to phase-locked loops or similar circuits, has spread out thanks to its versatility and performance. Particularly, charge pump phase-locked loops (CP-PLLs) have been widely adopted in several fields characterized by harsh environments [10,11].

A critical component that CP-PLLs rely on is the charge pump (CP). Its task is to convert the digital signals generated by a phase-frequency detector (PFD), which depends on the reference and feedback signal of the PLL, into a current to charge or discharge a loop filter, thus generating a voltage to control the oscillator. Therefore, it is easy to recognize that CP greatly influences the whole PLL's performance, and, therefore, that it should be carefully designed and characterized.

Several innovative designs have been proposed in the literature, such as those in [12,13]. Indeed, in [12], a novel CP is presented which implements both static and dynamic current compensation to achieve a low current mismatch. However, neither process–voltage–temperature corner simulations are presented, nor is any consideration given to temperature dependence or radiation hardness, thus limiting the range of applicability of the proposed design. In [13], the proposed CP design showed even better current matching performance, but this result was based on a simulation with temperatures up to only 85 °C, and no electromigration discussion is presented. The same holds true for the works presented in [14,15], where strategies to improve power, area, and noise performance are illustrated, but no techniques were implemented to address temperature or radiation issues. Moreover, none of these state-of-the-art CP designs have been electrically characterized, and, to the best of the authors' knowledge, no work has ever presented a complete thermal characterization up to 200 °C plus total ionizing dose (TID) tests up to 100 Mrad. This radiation value covers the levels of interest for space, transport, and avionics applications.

The works on CPs present in the literature, for instance, those in [16,17], discuss electrical and under-radiation measurements of PLLs or testbench PLLs, rather than measurements of the CP itself. Instead, there are no works focusing on CP design or measurements for such high temperature values. To fill this gap, in this paper, we present the design, prototyping, and complete electrical, thermal (up to 200 °C), and TID (up to 100 Mrad) characterization of a CP. It is worth mentioning that electronics in harsh environments pervaded by radiation also face single event effects (SEE). However, in [18], the authors demonstrated that, in CP-PLL applications, the main source of faults due to SEEs is the oscillator, rather than the CP. Indeed, they presented a PLL with a fully triplicated PFD and a partially triplicated frequency divider, but no SEE-hardening strategies were implemented on the CP or on the oscillator. The main SEE results of the work in [18] highlight that the oscillator and the part of the frequency divider not implementing triplication were the most sensitive blocks, while the CP contribution to the overall cross-section was negligible. Although this result could be counterintuitive given the influence that the CP has on the PLL's performance, it could be explained by considering that the CP usually occupies a much smaller area than the rest of the PLL, thus leading to a negligible contribution to the overall cross-section. This is why the focus of this work is on the cumulative degradation effects induced by temperature and TID in harsh environments, which are independent of the area of the circuits.

In this paper, we also briefly present the design and characterization of a PFD that we used to drive the CP during the tests. Indeed, the CP was tested in conjunction with the PFD to analyze its transient behavior and to analyze the CP behavior in a typical use-case. The design was carried out with the 65 nm TSMC technology Process Design Kit (PDK), and the prototype was fabricated using the same technology.

The remainder of the paper is organized as follows: In Section 2, the schematic and layout design of the CP and the testbench PFD are presented; in Section 3, the chip prototype and the setups for the electrical, thermal, and irradiation measurements are summarized; in Section 4, the electrical measurement results are reported and discussed; in Section 5, the results deriving from the thermal characterization are described in detail, whereas the X-ray

test results are reported in Section 6; and finally, the comparison with the state-of-the-art method is carried out in Section 7 and conclusions are drawn in Section 8.

2. Circuit Description

The block diagram of the designed charge pump is shown in Figure 1. It consists of the following blocks: a mirror (main bias mirror in the figure) that generates the bias currents ($I_{BIASOut1}$, $I_{BIASOut2}$, and $I_{BIASOut3}$) starting from the input current I_{in} for all the other blocks; the output mirrors (Output P Mirror and Output N Mirror) providing the up (I_{UP}) and down (I_{DOWN}) output currents; the circuitry, called bias voltages circuitry in the figure, that generates the bias voltages (V_{BiasP} and V_{BiasN}) for the output mirrors by exploiting the current $I_{BIASOut1}$ generated by the Main Bias Mirror; and finally, the DOWN Current Mirror and the UP Current Mirror that provide the input currents ($I_{BIAS-UP}$ and $I_{BIAS-DOWN}$) to the output mirrors, starting from $I_{BIASOut2}$ and $I_{BIASOut3}$, respectively. Additionally, two switching transistors are used to control the CP's output current based on the output signals (UP_{IN} and $DOWN_{IN}$) of the PFD. A detailed transistor-level schematic of the six blocks is depicted in Figure 2, together with an indication of their sizes. The output mirrors are high-swing cascode mirrors to obtain a high output impedance without sacrificing the output swing. Drain nodes of the switching transistors (MN12 and MP11) are connected to the gates of the main transistors of the output mirrors (MN8, MN9, MP9, and MP10) to let the PFD turn off the corresponding output current. Contrary to classic source- or drain-switching configuration, where switching transistors are connected to either the drain or the source node, in our design, they are connected to the gate of the output mirror. This solution allowed us to reduce the charge injected by the switching transistors into the output node. Moreover, the feed forward of the UP and DOWN signals through the gate–drain capacitance of the switching transistors towards the output node was diminished as well. The bias voltages for the secondary transistors of the output mirrors are provided by the bias voltages circuitry, composed of a pMOSFET simple mirror and a diode-connected nMOSFET. Finally, the input currents to the output mirrors are provided by the up current mirror and the down current mirror, which are separated to avoid crosstalk between the down switch and the up output current, and vice versa.

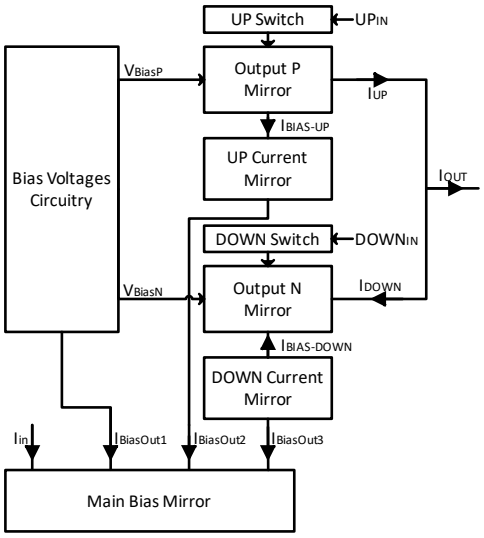


Figure 1. Block diagram of the CP. The arrows indicate the direction of the current flow for currents (I_{in}, $I_{BIASOut1}$, $I_{BIASOut2}$, $I_{BIASOut3}$, $I_{BIAS-DOWN}$, $I_{BIAS-UP}$, I_{DOWN}, and I_{UP}) and the input/output direction for voltages (V_{BiasN}, V_{BiasP}, UP_{IN}, and $DOWN_{IN}$).

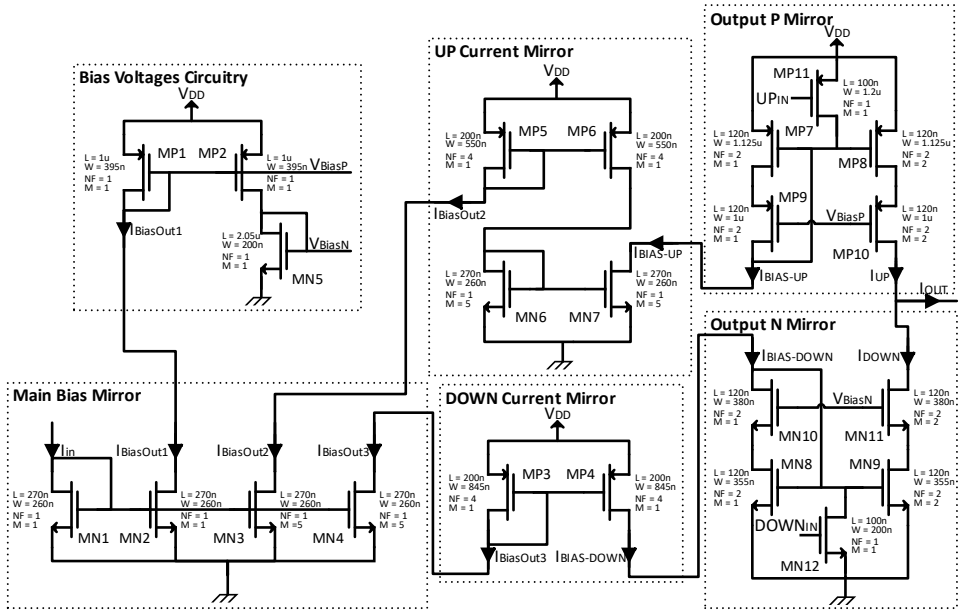


Figure 2. Detailed schematic of the CP.

Apart from the switching transistors and those in the output mirrors, all the other transistors were sized to be at least 200 nm long for two main reasons: firstly, to enhance the impedance seen by their drain and, therefore, enhance the current matching between the masters and the slaves of the mirrors; secondly, to improve the radiation hardness against the TID of both nMOSFET and pMOSFET. Indeed, according to [19,20], the current degradation due to TID in 65 nm CMOS technology decreases as the length of the transistors' channel increases. Below 100 Mrad, which is well above the target TID for several applications, e.g., space, pMOSFETs with lengths of at least 100 nm showed current degradation of less than 10%. The output mirrors, instead, were designed to be 120 nm long, since the output impedance was already improved thanks to the high-swing cascode configuration. The reduction in the gate capacitance obtained thanks to a shorter transistor allowed the CP to turn on and off more quickly. A faster CP, in turn, allowed us to relax the constraints in the design of the PFD, particularly for what concerns the delay of the reset path, as will be clarified later in this section.

To further enhance the robustness against radiation, a wide output swing was targeted for all the mirrors composing the CP. Indeed, the output current of the CP is mostly dictated by the bias current as long as the mirrors of the CP work in strong inversion and in the saturation region. Therefore, if a wide output swing is guaranteed, the CP can more easily compensate for the changes induced by radiation.

Considering these requirements (i.e., channel length above 200 nm and wide output swing), to reach the high-temperature operation which we targeted, we sized the transistors to obtain a target current of 40 µA at the zero-temperature coefficient (ZTC) DC operating point [21,22]. At this point, the decrease in the carrier's mobility and in the threshold voltage with temperature compensated perfectly, leading to a temperature-independent current that depended only on the temperature-independent gate–source voltage. However, several challenges were faced when biasing the transistors in such point: firstly, the ZTC gate-source voltage in the 65 nm CMOS technology was above 650 mV, which made it challenging to force the transistors into strong inversion and into the saturation region with a wide output swing; secondly, the ZTC point depended on the technology corners. Moreover, although, ideally, the ZTC point would be independent of the source–drain voltage (V_{DS}), this is not true in actual designs [23]. The ZTC point was, therefore, an interval rather than a fixed point. Depending on the position of the transistor bias point with respect to the ZTC point (above or below), the current would increase or decrease with the temperature.

While the V_{DS} of the internal mirrors of the CP (i.e., all the mirrors apart from the output mirrors) did not exhibit significant variation through the PVT corners, as it mostly depended on the gate–source voltage (V_{GS}) of the following mirror, the V_{DS} of the output mirrors experienced significant variation since it depended on the output node voltage. Consequently, for the internal mirrors, the ZTC point bias was reached with good approximation, with the current slightly increasing with temperature (i.e., DC bias slightly below the ZTC point). For the output mirrors, instead, this sizing was more challenging. Indeed, given the large V_{DS} variation in the output mirrors, the ZTC point varied over a large range that overlapped with the V_{GS} variation across the PVT corners, thus leading to the opposite behavior in the output current. This depended on the relationship between the VGS and the ZTC point for the combinations of temperature and output voltage.

The complete layout of the CP is shown in Figure 3, in which the different parts composing the CP are highlighted. The placement of the CP's blocks and layout design was focused onto two main objectives:

- First, the reduction in the electromigration effect in the metal wires that can lead to a malfunction of the CP. Indeed, at high temperatures, the electromigration effect is largely enhanced, since it almost doubles every 10°C;
- Second, the establishment of the matching between the mirror transistors of the CP blocks.

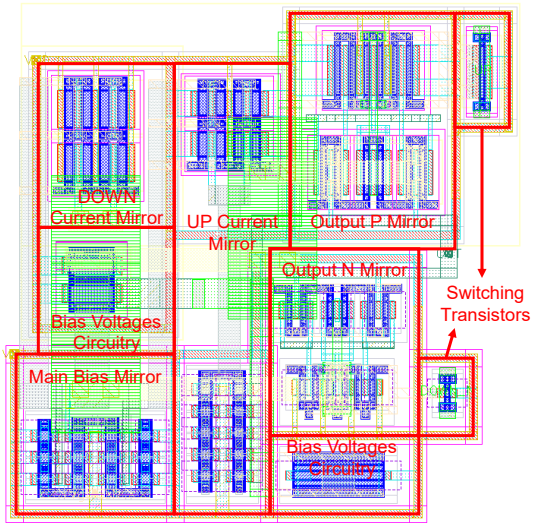


Figure 3. Layout of the proposed charge pump.

To achieve the second objective, the transistors of each block were grouped and placed near each other following an interdigitated common centroid approach when possible. To achieve the first objective, instead, the blocks were placed and routed in order to have the minimum wire length, exploiting as much as possible the higher metal levels, which were thicker. Indeed, short and thick metals suffered less of an electromigration effect.

Following these guidelines, we obtained the layout of Figure 3. In the bottom left corner, there is the bias mirror consisting of 12 identical transistors, as two of the three generated currents were obtained through multiplication by five. The Bias Voltages Circuitry, which include the two pMOSFET over the bias mirror and the nMOSFET in the bottom right corner as indicated by the labels, provide the bias voltages for the output mirrors. The mirrors that generate the currents for the output mirrors can be recognized in the top left corner (DOWN Current Mirror) and in the center (UP Current Mirror), whereas the output mirrors (P and N) are located in the top right corner. They multiplied their input current by two, leading to a total multiplication factor of the whole CP equal to 10. Their layout was designed following a common centroid approach to minimize the matching

error. Finally, on the right edge of the layout, there are the two switching transistors. The total area occupied by the CP was 144 μm^2 (12 $\mu m \times 12$ μm).

From the temperature point of view, the back-end design is one of the most critical phases in CMOS technologies due to the electromigration effect. However, thanks to the compact layout, the metal paths used to locally connect the CP transistors were short (the longest is less than 6 μm long), and the higher metal layers were used whenever possible to exploit their thickness. Moreover, the DC current flowing in the metal wires was limited to 40 μA. Therefore, the electromigration effect experienced for temperatures up to 200 °C was not expected to induce any faults or performance degradation on the CP with the proposed layout.

In Figure 4, the schematic of the PFD is shown. It consists of the classic PFD architecture, in which the propagation delay of the NAND port needed for the reset path was designed to ensure a dead-zone free operation. This is well visible in Figure 5, where the simulated PFD plus CP characteristic is reported with and without the proposed reset path design. As can be seen, the dead-zone without propagation delay optimization was about 0.14 rad, which corresponds to approximately 143 ps. Of course, the elimination of the dead-zone comes at the cost of the insertion of a blind-zone, whose extension should be kept small enough. For example, if we consider a PLL application, too wide a blind-zone could reduce the lock-in range of the PLL, leading to prevention of the locking in the worst case. In the PLL lock state, instead, the blind-zone does not directly affect the performance and, therefore, it is not critical from this point of view. However, it is worth noting that the delay of the reset path of the PFD, which the blind-zone depends on, affects the overall performance of the PLL. Although the schematic in Figure 4 shows a logic gate-based design, the PFD was designed with a transistor-level full custom approach. From the TID viewpoint, the PFD transistors were sized using an approach similar to the CP. However, it is worth noting that the PFD must work at low operating frequencies in typical PLL applications. As a result, a speed degradation due to TID of up to 100 Mrad is usually not critical. The same consideration holds true for the high operating temperatures. Finally, we applied the triple modular redundancy to the PFD design following a transistor-level full-custom approach as well. Indeed, as mentioned in the introduction, the SEE sensitivity of the CP and of a triplicated PFD has been demonstrated to be negligible for typical CP-PLL applications. This way, the effort during the experimental verification could be focused on the TID and temperature characterization.

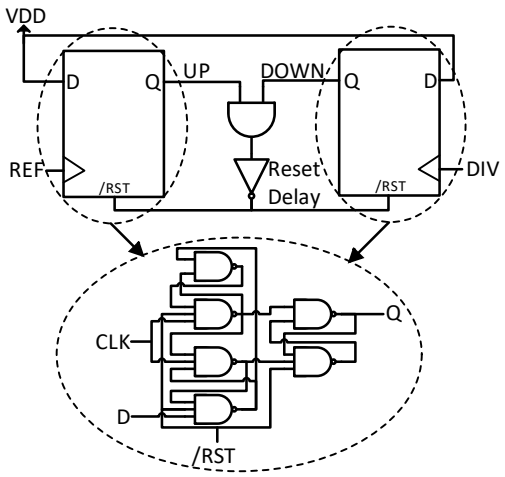


Figure 4. Block scheme of the PFD.

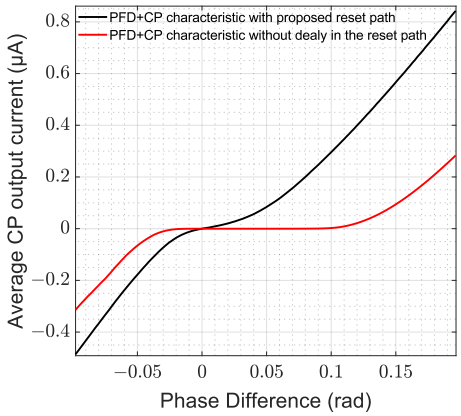


Figure 5. PFD-CP chain characteristic with proposed reset path design (black) and without delay in the reset path (red).

3. Chip Prototype and Measurement Setup

A photograph of the fabricated chip prototype is shown in Figure 6. The PFD and CP were integrated at the bottom of the chip, together with other PLL-related components, and with some additional circuitry to reuse the same PADs for more than one block. As can be noted, the CP was much smaller than the other integrated blocks, while the PFD occupied a large area due to its triplication. Moreover, the CP and PFD were integrated in a complete PLL (at the top), which, however, is not discussed here, as the CP is the focus of this work.

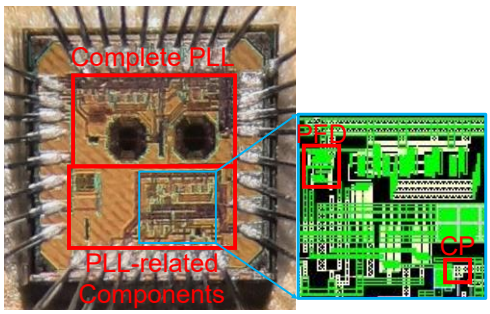


Figure 6. Chip prototype on the left; layout of the bottom-right corner of the chip prototype on the right.

The test chip was designed so that the PFD and CP could be tested as either separate blocks or connected components thanks to three-state input and output buffers, as shown in Figure 7a. A DC signal, labeled SEL in the figure, was exploited to select different configurations: PFD disabled and CP enabled and driven by an external component; or PFD and CP enabled and connected, with the CP controlled by the PFD. Therefore, the first configuration allowed us to test the CP alone, while the second enabled us to test the PFD-CP chain, as well as the PFD alone through the UP and DOWN pins (Figure 7) thanks to the three-state buffers. The DC behavior of the CP was measured by exploiting a digital multimeter, used as an amperemeter. It was connected to a power supply and the output node of the CP, thus allowing for the characterization of the output current for different output voltages.

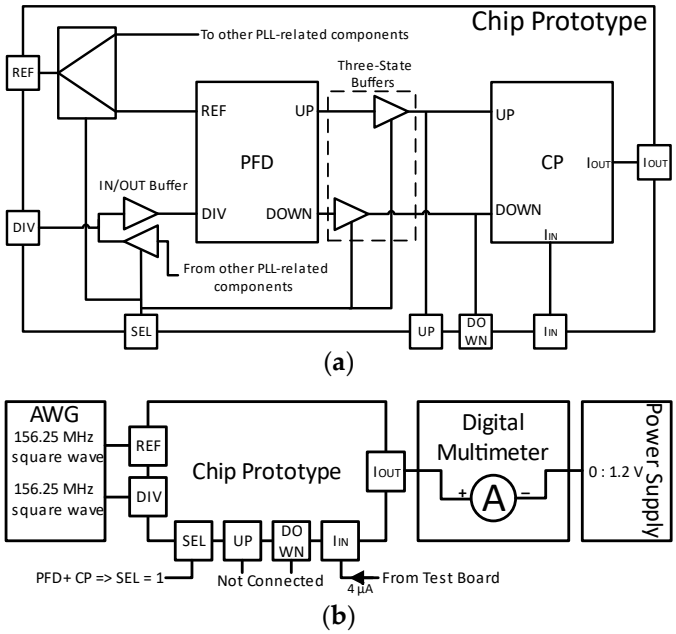


Figure 7. Block diagram of the PFD and CP in the chip prototype (**a**), and test setup for the PFD plus CP cascade (**b**).

The measures were carried out in three different configurations: both the up and down current turned ON, only the up current turned ON, and only the down current turned ON. The PFD, instead, was characterized by utilizing an arbitrary waveform generator and a mixed-signal oscilloscope. Two 156.25 MHz square waves, a standard frequency for ethernet applications, were given as input to the PFD, with their phase differences varying from -2π to 2π. This very wide range was useful for measuring the extension of the blind-zone. Thanks to the mixed-signal oscilloscope, the duty cycles of the outputs of the PFD (UP and DOWN) were measured; afterwards, from the measurement results, the PFD characteristic was derived as in (1), where D_{UP} and D_{DOWN} are the duty cycles of the two output signals. Furthermore, the propagation delay of the reset path was also derived from the measured duty cycles, thereby characterizing the reset time, which is related to the blind-zone. Finally, the PFD and CP were cascaded, and the resulting characteristic of the whole chain was measured with the setup shown in Figure 7b. The stimulus was the same as that for the measurements performed for the PFD alone, whereas the DC component of the output current was measured with the multimeter for different voltages applied on the output node of the CP.

$$PFD_{Char} = D_{UP} - D_{DOWN} \quad (1)$$

All the measurements described so far were also performed at different temperatures to analyze the behavior of the CP when employed in applications characterized by harsh environments. In particular, the die was heated to reach temperatures up to 200 °C. Since the chip prototype was heated locally, the measured performance was not influenced by the instruments or other commercial components used for the test, which worked at room temperature for every measurement performed.

Finally, the chip prototype was irradiated using the X-ray machine of the INFN facilities in Pisa with a dose rate of 57.468 krad/min, and the CP performance variations at various TID levels up to 100 Mrad were measured by exploiting the same test setups and configurations described for the electrical characterization. In this case, the COTS components were protected with a 4 mm thick lead shield to avoid their influence on the measures. The obtained results are reported in the following sections, where they are discussed and analyzed in detail.

4. Electrical Characterization

In Figure 8, the DC characterization of the CP is shown for a nominal output current of 40 µA. Particularly, in Figure 8a, the UP and DOWN currents measured in the first two configurations, as described in the previous section, are reported. As can be seen, the two currents were matched in the 0.3–0.9 V voltage range, where the output impedance is very high. Indeed, this is well observable in Figure 8b, where the measured total output current is plotted. As expected, this current approached 0 in the range of 0.3–0.9 V. From this figure, the output impedance can also be derived as 155 kΩ in the middle of the output voltage range.

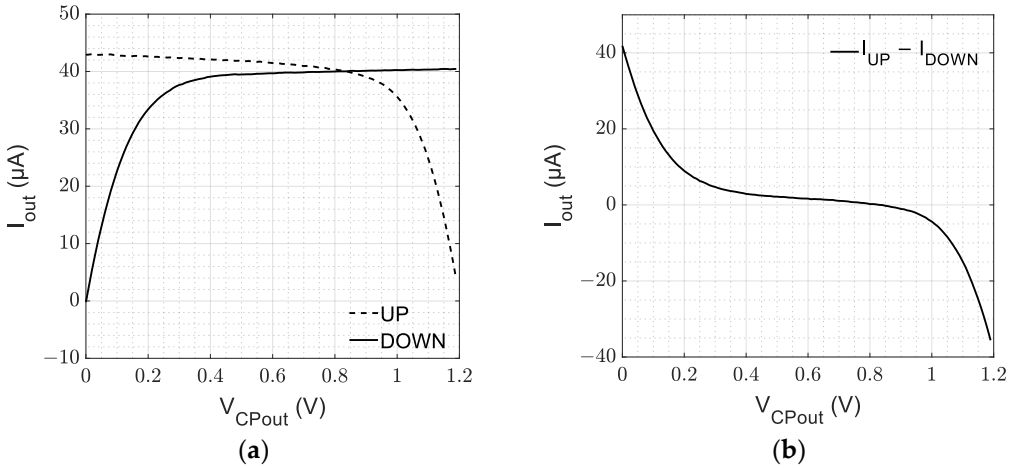


Figure 8. CP electrical DC characterization: (**a**) UP and DOWN currents; (**b**) total output current.

In Figure 9, instead, the derived PFD characteristic is plotted. It was symmetric for positive and negative phase differences, as was expected from the symmetry of the architecture. No dead-zone was present, as can be seen near the zero-phase difference, while, at the edges, the blind-zone is well visible, and it resulted as 0.94 rad, which corresponds to about 950 ps. Because of the blind-zone, phase differences near the $\pm 2\pi$ could not be seen by the PFD, which was in its reset state upon the new edge of the leading signal. Because of this, the edge did not produce any effect, and the following edge of the non-leading signal was seen as the leading one. Consequently, the PFD moved from the reset state into the wrong state, corresponding to a near-zero phase difference. The resulting gain was 0.156, near the ideal one of $1/2\pi$.

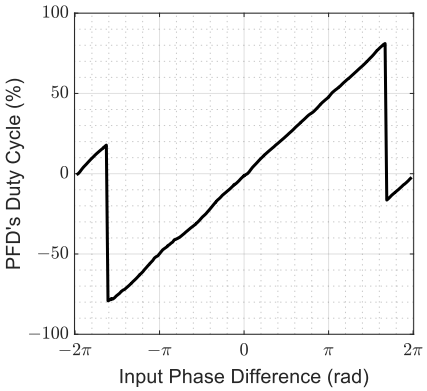


Figure 9. PFD characteristic.

Figure 10a shows the measured, average output current of the PFD and CP together as a function of the phase difference between the PFD input signals, with 0.6 V forced on the output node (solid line). Ideally, the characteristic resulting from the cascade of the PFD

and the CP should be equal to the PFD characteristic multiplied by the UP and DOWN CP currents. This ideal characteristic is also plotted in Figure 10a (dashed line), and was derived from the measured PFD and CP characteristics. As can be seen, there was a slight difference between the ideal and measured results, which was mainly due to the transient behavior of the CP. Indeed, the average current also depended on how the CP behaved when it switched ON and OFF, and on the matching between the UP and DOWN currents during these switching periods.

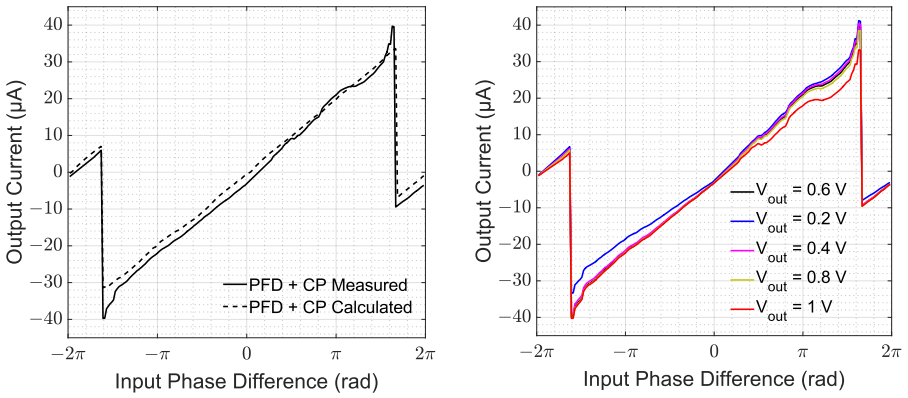
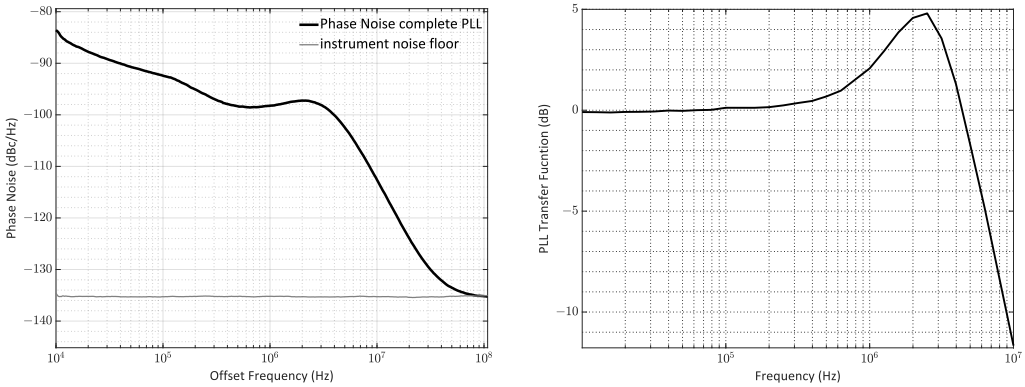


Figure 10. Measurement results of the cascaded PFD and CP: (**a**) measured characteristic with an output node voltage of 0.6 V vs. that calculated from the measures of the CP and PFD taken separately; (**b**) measured characteristic for different output node voltages.

The average total gains resulting from the cascade of the PFD and CP were estimated to be 6.2 μA/rad for negative phase differences, and 7 μA/rad for positive phase differences, when the output node voltage was 0.6 V. Analogously to the PFD behavior depicted in Figure 9, no dead-zone was present, thus confirming that the propagation delay of the reset path of the PFD was long enough to overcome the CP delay, which was kept low by reducing the sizes of the output transistors, as reported in Section 2. Similarly, the blind-zone was also almost the same as that of the PFD alone, and this led to the conclusion that the CP contribution was negligible.

Finally, the results of the same measurement performed for different values of the output node voltage are shown in Figure 10b. As expected, in the high-impedance range of the CP (i.e., 0.3–0.9 V), the influence of the voltage on the CP output current was negligible. Outside of this range, instead, the effect of the non-idealities of the CP became more pronounced. Nevertheless, this did not lead to faulty behavior, but only to performance degradation.

As mentioned in Section 3, the proposed CP and PFD designs were also integrated in a complete PLL at the top of the chip prototype of Figure 6. The measured PLL phase noise of the complete PLL is reported in Figure 11a. It was below −98 dBc/Hz at 1 MHz offset, while the spurs at multiples of the reference frequency due to the CP current mismatch and PFD reset delay were below −48 dBc. Figure 11b, instead, shows the measured phase transfer function. The bandwidth of the PLL was about 5 MHz.



(**a**) (**b**)

Figure 11. (**a**) Phase noise measurement of the complete PLL where the proposed CP and PFD were integrated. The measurement was carried out by exploiting a Rohde and Schwarz FSL18 Spectrum Analyzer (Rohde & Schwarz, Munich, Germany), whose noise floor is reported in the figure. (**b**) Phase transfer function of the complete PLL where the proposed CP and PFD were integrated. The measurements were performed by exploiting a MSO72304DX Tektronix Oscilloscope (Tektronix, Beaverton, OR, USA).

5. Thermal Characterization

Simulations of the CP and PFD for different temperatures from −40 °C to 125 °C showed that the performances of the two devices were more sensitive to high temperatures. Therefore, in this section, the measurement results obtained by exposing the CP and PFD to high temperatures up to 200 °C are reported and discussed. The experimental setup for the measurements was the same as that used for the electrical characterization, apart from an air-based heater focused onto the chip prototype. Thanks to this heater, we could raise the temperature of the chip prototype only, keeping the commercial components of the PCB at around 25 °C, since they were not graded to work above 80 °C. In Figure 12a–d, the DC measurement characterizations of the CP are reported for different temperatures and for different voltages on the output node. In Figure 12a,b, the percentage variations in the UP and DOWN currents are shown. Inside the saturation region of the two output mirrors, the current grew monotonically for both the UP and DOWN branches, as shown by blue, red, black, and magenta lines in Figure 12a,b. Differently, in the triode region, the two currents showed opposite behavior with respect to temperature variations (yellow lines in Figure 12a,b): the UP current tended to decrease, whereas the DOWN current increased, albeit with a lower derivative than the increment in the saturation region. This could have resulted from the position of the ZTC point compared to the actual DC bias point of the output mirrors, the UP and DOWN mirrors, and the main bias mirror. Indeed, the simulations performed during the design and sizing of the CP, described in Section 2, showed that the DC bias point of the main bias mirrors and of the UP and DOWN current mirrors were near, but always below, the ZTC point in every PVT corner. On the other hand, the output mirrors had a ZTC point whose range overlapped with the actual V_{GS} of the main transistors of the output mirrors, and this was determined using the output voltage. This suggests that, in the chip prototype, the currents of all the mirrors but the output mirrors tended to increase. The V_{GS} of the output mirrors, instead, reached above the ZTC point when the output voltage approached the ground or V_{DD} voltage rails (i.e., N and P mirrors in triode region), thus leading to a decrease in the nominal current. Note that, in this scenario, the nominal current refers to the output current with a constant input current to the mirrors. While, for the N output mirror, this was not sufficient to balance the increase in the input current given by the DOWN mirror and the main bias mirror, it was enough for the P output mirror. Nevertheless, as can be derived from the electrical measurements in Figure 8, the operating region of interest was the high-impedance region

in the 0.3 to 0.9 V range. In this voltage interval, both currents increased, leading to a limited increment in the current mismatch.

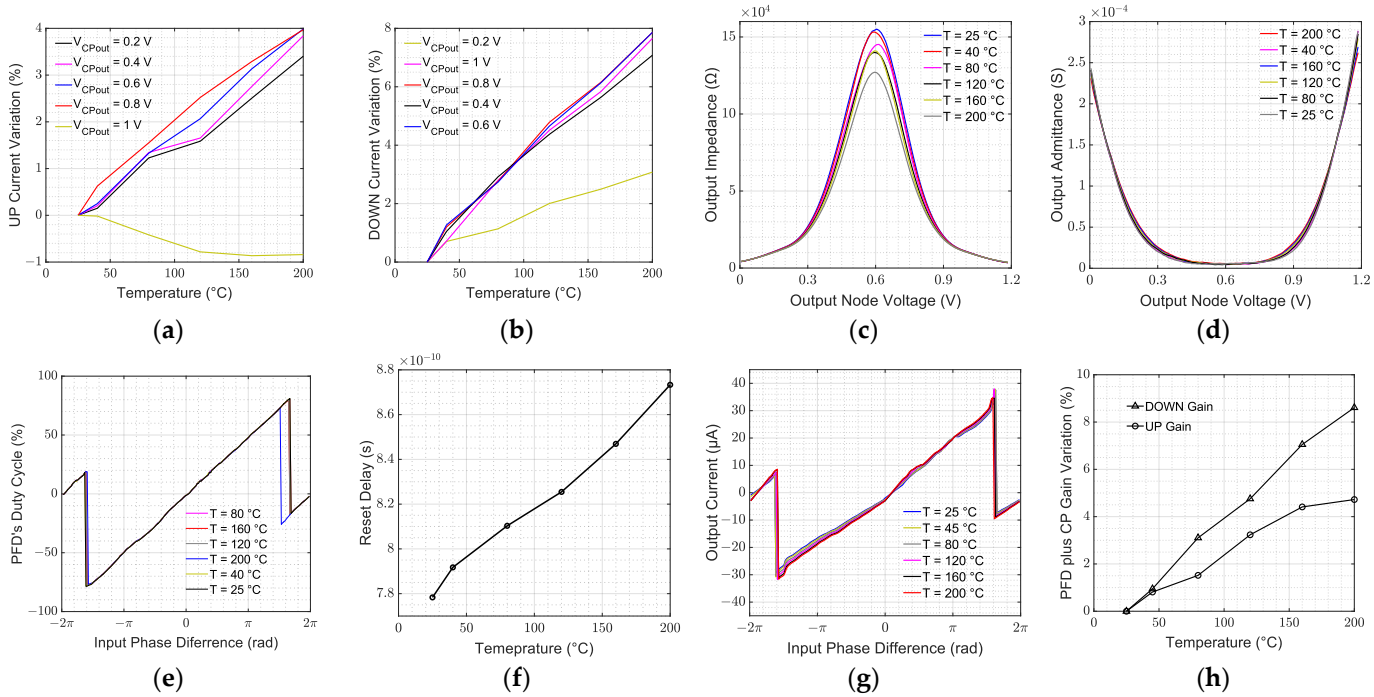


Figure 12. PFD and CP thermal characterization: percentage DC DOWN current variation in (**a**); percentage DC UP current variation in (**b**); CP's output impedance in (**c**); CP's output admittance in (**d**); PFD characteristic in (**e**); propagation delay of the PFD's reset pa path in (**f**); PFD plus CP cascade characteristic in (**g**); PFD plus CP cascade's UP and DWON gain percentage variation in (**h**).

In Figure 12c,d, the output impedances of the CP and its inverse are shown as functions of the output voltage for several temperature values. The output impedance decreased with temperature, thus degrading the CP's current matching in the output range and decreasing the output range as well. The maximum impedance was reached when the output voltage was approximately equal to 0.6 V, i.e., half of the power supply voltage, for all temperatures, and the output range was centered around 0.6 V as well, even though it narrowed down with the temperature.

Concerning the PFD, in Figure 12e, its characteristics at different temperatures are depicted. From the figure, it is evident that the influence of temperature on the PFD was negligible. The only PFD parameter that was slightly affected by temperature was the width of the blind-zone, which increased with it. This is in line with an expected increase in the propagation delay of the reset path due to the decreased mobility of the carrier, which was not compensated by the corresponding decrease in the threshold voltage. Indeed, this result was confirmed by the values of the reset delay for different temperatures, as shown in Figure 12f.

Finally, the effect of temperature on the whole cascade of PFD and CP is evidenced in Figure 12g,h. In particular, Figure 12g shows the characteristic with the output node at 0.6 V, while Figure 12h demonstrates the percentual gain variation in the PFD plus CP cascade at different temperatures with the output node at 0.6 V. As expected from the DC characterization of the CP, the largest variation was seen in the gain for negative phase differences, where the leading current was the DOWN current, while for positive phase differences, the gain variation was less pronounced.

6. TID Characterization

As reported in Section 3, we irradiated the CP up to 100 Mrad, monitoring the UP and DOWN currents during the experiment. The CP UP and DOWN current percentage

variations measured during this experiment are reported in Table 1 for TIDs of 15 Mrad and 100 Mrad. The CP current was measured for output voltages of 0.3 V, 0.6 V, and 0.9 V. The current variation was limited to less than ±2% compared to the current before the experiment, corresponding to less than 1 µA variation. The largest TID effects were seen when the output voltage was 0.3 V, i.e., at the left edge of the output swing of the CP. In these conditions, the nMOSFETs of the output N mirror were in the linear region, whereas the pMOSFETs of the output P mirror worked in the saturation region. However, it is worth mentioning that the variation experienced by the CP current was comparable with the resolution of the instrument used for the measure.

Table 1. CP current variation due to TID.

V_{OUT}	Current Variation @ 15 Mrad		Current Variation @ 100 Mrad	
	UP	**DOWN**	**UP**	**DOWN**
0.3 V	0.09%	−0.46%	1.3%	−1.9%
0.6 V	<0.01%	−0.07%	1%	−0.36%
0.9 V	−1.2%	−0.65%	−0.37%	−1.8%

In Figure 13a,b, the output impedance and output admittance of the CP measured during the X-ray experiments are shown. A drastic reduction in the output impedance was measured at 100 Mrad, while the output range experienced a negligible variation. The reduction in the output impedance of almost 14% was probably due to the increase in the threshold voltage of the transistors MP9, MP10, MN10, and MN11 in Figure 2. Their threshold voltage increase pushed the transistors MP7, MP8, MN8, and MN9 toward the linear region, thus decreasing the impedance seen by their drain. In turn, this led to a decrease in the overall CP impedance. Nevertheless, this effect did not affect the output range, as highlighted in Figure 13b.

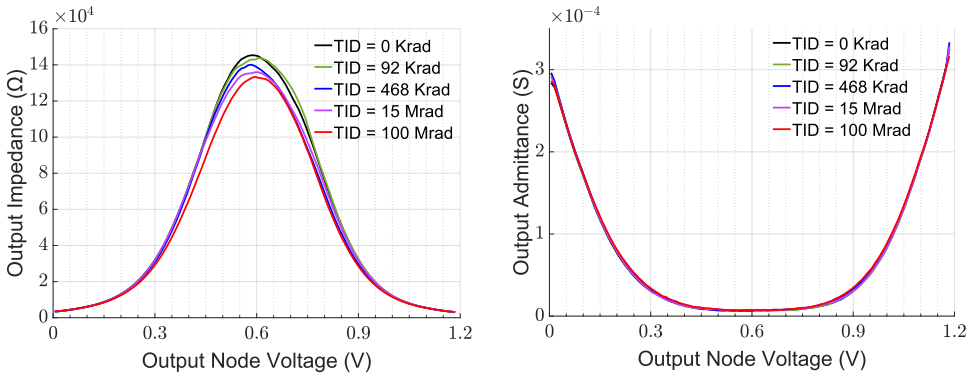


Figure 13. CP TID characterization: output impedance (**a**) and output admittance (**b**) for different TID levels.

7. State-of-the-Art Comparison

In Table 2, the measured CP performance is summarized, together with a comparison with some state-of-the-art CP designs. As already mentioned, none of the state-of-the-art CPs were experimentally verified. In [24], a 180 nm CMOS CP with the same output current as this work was proposed. An operational transconductance rail-to-rail amplifier was added to the CP circuit to improve the current matching between the UP and DOWN current, but this was paid with a very large area overhead. The characterization of the CP in [22] was performed through post-layout simulations showing a very low current mismatch. The output voltage range was almost 50% of the supply voltage, which is similar

to the output voltage range obtained with the design proposed in this work. However, the simulations reported in [24] considered temperatures up to 100 °C only, and no details on the performance results at that temperature were given. The CP proposed in [25] showed even better current matching, with an output range of 50% as well, but no thermal analysis was conducted. In [12], instead, a CP with a wide output range of about 78% of the supply voltage was presented, with worse current matching than [24,25]. However, no thermal simulations were performed. A wide output range was also exhibited by the design in [13], which was obtained with a current matching comparable with [24,25]. In [13], the layout of the proposed CP was also presented, achieving an area occupation of 4346 μm^2. However, the simulations were performed on the schematic view only, up to a temperature of 85 °C, achieving a current percentage variation of 7% with respect to the typical case. Our proposed design, instead, features 8% current variation, but this was achieved at 200 °C. Finally, in [26], a compact CP, which occupied an area of 1564 μm^2, was presented. Not much information on the CP performance was reported, and the schematic simulations were performed up to 100 °C, showing a current variation of 16.5%.

Table 2. Performance summary and comparison with the state of the art.

	This Work	**[24]**	**[25]**	**[12]**	**[13]**	**[26]**
Technology	65 nm	180 nm	55 nm	65 nm	65 nm	130 nm
Power Supply	1.2 V	1.8 V	1.2 V	1.8 V	1 V	1 V
Area (μm^2)	144	220,000	/	/	4346	1564
CP Current (μA)	40	40	400	50	150	63.5
Output Range (V)	0.3–0.9	0.40–1.25	0.3–0.9	0.21–1.62	0.1–0.85	/
Current Mismatch	5%	0.065%	0.025%	0.78%	0.03%	/
Output Impedance	155 kΩ	/	/	/	/	/
Max Temperature (°C)	200	100	/	/	85	100
Output Impedance at max temp	127 kΩ	/	/	/	/	/
Output Range at max temp (V)	0.35–0.85	/	/	/	/	/
Current variation at max temp	8%	/	/	/	7%	16.5%
TID (Mrad)	100	/	/	/	/	/
Output Impedance at max TID	133 kΩ	/	/	/	/	/
Output Range at max TID (V)	0.3–0.9	/	/	/	/	/
Current variation at max TID	<2%	/	/	/	/	/
Type of characterization	measures	post-layout simulation	schematic simulation	schematic simulation	schematic simulation	schematic simulation

Regarding radiation-hard state-of-the-art CPs, instead, the work in [16] is worth mentioning. A source-switching CP was irradiated up to 180 Mrad, but a whole PLL measurement campaign was presented rather than the CP characterization. Therefore, we could not compare our results with those in [16].

The CP proposed in this work, instead, occupied an area of only 144 μm^2, and it was able to reach temperatures up to 200 °C and TID up to 100 Mrad with a current variation limited to 8% for the maximum temperature and 2.5% for the maximum TID level at 25 °C. However, its high robustness was paid in terms of current matching performance, even though the obtained performance was acceptable for most CP-PLL applications [27,28].

8. Conclusions

In this paper, we have presented the detailed design of a CP for PLL applications, achieving an output impedance and a current matching of 155 kΩ and below 5%, respectively.

Moreover, the design of a dead-zone-free PFD has been presented to stimulate and test the CP in a typical use case. In the literature, several novel CPs adopted in PLLs have been proposed, but only very few of them have been directly characterized, since in most cases, the whole PLL characterization has been reported. Moreover, to the best of the authors' knowledge, no thermal or TID characterization of CPs is present in the literature. Differently from previous studies, in this work, we directly characterized the proposed design at different operating temperatures up to 200 °C and under X-rays up to 100 Mrad TID. In such harsh temperature and radiation conditions, the CP proposed in this work showed better performance than state-of-the-art CPs assessed in less harsh environments (i.e., up to only 100 °C and no radiation). Indeed, the simulated current variations for state-of-the-art CPs in [13,26] were up to 7% and 16.5% at 85 and 100 °C, respectively, as opposed to the measured 8% of this work at 200 °C. Moreover, the measurement results of the proposed CP have confirmed its suitability for high-temperature environments by demonstrating that the PFD is almost insensitive to temperature variations. As for the CP, the 4 to 8% current deviation experienced at 25 °C was due to the impossibility of biasing the CP's transistors perfectly in their ZTC points. The analysis of the reasons for the increase or decrease in the output currents has been reported in Section 5 based on reasonable hypotheses.

The CP performance when driven by the PFD has also been presented, verifying the consistency of all the measurements performed. These tests confirm the CP's ability to work in a real use-case application. Finally, the CP behavior when exposed to X-rays for a TID up to 100 Mrad has been presented as well, and the effectiveness of the proposed radiation-hard design has been experimentally demonstrated. Indeed, the maximum current variation experienced during the irradiation was below 2.5%.

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