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A Low-Intensity Pulsed Ultrasound Interface ASIC for Wearable Medical Therapeutic Device Applications

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Abstract: Low-intensity pulsed ultrasound (LIPUS) is a non-invasive medical therapy that has attracted recent research interest due to its therapeutic effects. However, most LIPUS driver systems currently available are large and expensive. We have proposed a LIPUS interface application-specific integrated circuit (ASIC) for use in wearable medical devices to address some of the challenges related to the size and cost of the current technologies. The proposed ASIC is a highly integrated system, incorporating a DCDC module based on a charge pump architecture, a high voltage level shifter, a half-bridge driver, a voltage-controlled oscillator, and a corresponding digital circuit module. Consequently, the functional realization of this ASIC as a LIPUS driver system requires only a few passive components. Experimental tests indicated that the chip is capable of an output of 184.2 mW or 107.2 mW with a power supply of 5 V or 3.7 V, respectively, and its power conversion efficiency is approximately 30%. This power output capacity allows the LIPUS driver system to deliver a spatial average temporal average (SATA) of 29.5 mW/cm^2 or 51.6 mW/cm^2 with a power supply of 3.7 V or 5 V, respectively. The total die area, including pads, is 4 mm^2. The ASIC does not require inductors, improving its magnetic resonance imaging (MRI) compatibility. In summary, the proposed LIPUS interface chip presents a promising solution for the development of MRI-compatible and cost-effective wearable medical therapy devices.

Keywords: wearable devices; charge pump; low-intensity pulsed ultrasound; integrated circuit

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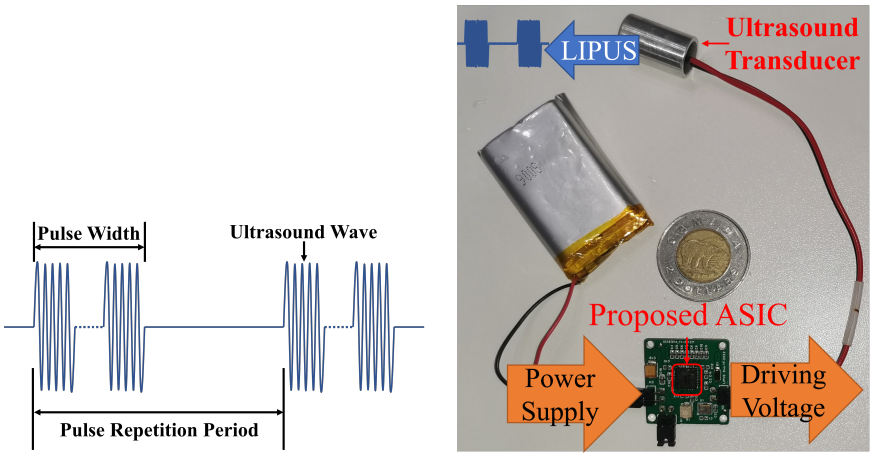
1. Introduction

Ultrasound has been extensively used in medical applications such as diagnosis, therapy, and surgery for almost a century [1,2]. Initially, ultrasound applications were focused on the thermal effect of high-intensity ultrasound to selectively elevate the temperature of specific tissues. However, in recent years, low-intensity ultrasound without thermal effects has received attention and led to various therapeutic applications, such as the healing of fractures [3], cancer therapy [4,5], neuromodulation [6], and peripheral nerve regeneration [7] amongst others.

Low-intensity pulsed ultrasound (LIPUS) is a derivative of low-intensity ultrasound, which delivers ultrasound energy in the form of a pulse wave. An example of a LIPUS wave is displayed in Figure 1a, which illustrates the three parameters of LIPUS: pulse repetition frequency, ultrasound fundamental frequency, and duty cycle. LIPUS is unique in that it can deliver sufficient ultrasound amplitude to the target while maintaining its non-thermal property, as its energy is concentrated in the pulse. LIPUS has been experimentally proven to have therapeutic effects on various tissues, including knee osteoarthritis [8,9], tooth root resorption [10], inflammation inhibition [11], bone fractures [12], and so on. Among the various LIPUS parameters reported in experimental results, the most widely used is a 1.5 MHz ultrasound fundamental frequency, with a pulse width of 200 µs, repeated

at 1 kHz (equivalent to 20% duty cycle), at a spatial average temporal average (SATA) intensity of 30 mW/cm^2. These LIPUS parameters have been applied to fresh fracture healing [12,13], delayed union [14], and nonunion [15], and they have been found to be effective in accelerating fracture healing, which has been approved by U.S. Food and Drug Administration (FDA), as well as supported by The National Institute for Health and Care Excellence (NICE) in the UK. The same set of LIPUS parameters has also been used for intra-oral dental tissue formation and stem cell growth and differentiation [16,17]. Additionally, the Aveo system, a device for orthodontic treatment based on this principle, was approved by Health Canada in 2016.



(**a**) (**b**)

Figure 1. (**a**) Demonstration of a LIPUS wave. (**b**) The proposed highly integrated LIPUS system compared with a Canadian 2 CAD coin.

This project aimed to develop a miniaturized LIPUS interface application-specific integrated circuit (ASIC) chip to create a wearable ultrasonic therapy system. Wearable devices are typically powered with batteries or a portable DC power supply. However, driving an ultrasound transducer requires a voltage higher than the nominal battery voltage or portable DC power supply, necessitating a DC-DC boost voltage converter. Given that the electromechanical conversion efficiency of most ultrasound transducers is around 30% to 35% [18–20], the DC-DC boost voltage converter must be capable of delivering continuous power of 500 mW to support the LIPUS transducer with a 1 cm diameter, a SATA intensity of 30 mW/cm^2, and a duty cycle of 20%. Such power requirements can be easily achieved using inductor-based boost converters, but these inductors are bulky and unsuitable for miniaturized devices. Additionally, inductors are not compatible with the magnetic resonance imaging (MRI) environment, so they are not suitable for MRI-guided ultrasound treatment procedures [21–23]. In this scenario, MRI imaging guides the direction of the ultrasound transducer and provides real-time feedback for the ultrasound stimulation target. This requires the simultaneous operation of both MRI and ultrasound, making the compatibility of ultrasound with MRI crucial. Our ASIC system utilizes a charge pump, also known as a switched-capacitor DC-DC converter, as an alternative solution to address these limitations.

Here, we describe a LIPUS interface chip for a highly integrated ultrasound driver system, which can be applied to portable medical therapeutic devices. The chip was designed and implemented using the AMS 0.35 µm High-Voltage CMOS Process Technology (H35B4D3) with a die area of 4 mm^2. The proposed chip requires only a few passive electronic components to construct the peripheral circuit. With a proper peripheral circuit, the chip is capable of delivering up to 181.5 mW to the ultrasound transducer when powered by a 5 V supply, or 103.3 mW with a 3.7 V power supply, with a power efficiency of 29.7% or 30.8%, respectively. This power output capacity allows the LIPUS system to deliver a SATA of 29.5 mW/cm^2 or 51.6 mW/cm^2 with a power supply of 3.7 V or 5 V, respectively.

The proposed ASIC, its peripheral circuit, and its integration within an ultrasound therapeutic system are displayed in Figure 1b. The remainder of this paper is organized as follows: Section 2 presents the design details of the proposed ASIC, including the system architecture, the charge pump, the high voltage level shifter (HVLS), the half-bridge (HB) driver, and the voltage-controlled oscillator (VCO). Section 3 describes the post-layout simulation results and the test results, which are followed by a discussion subsection. Section 4 summarizes our work.

2. System Architecture and Implementation

The system architecture of the proposed ASIC and its periphery components is illustrated in Figure 2. The system power supply can be either 3.7 V or 5 V, and the power source must be connected simultaneously to the digital power supply DV_{DD}, the analog power supply AV_{DD}, and the power management power supply PV_{DD}. The digital circuit block controls all the digital signals in the system and is primarily responsible for generating proper clock signals for other modules. These clock signals are derived from the off-chip 12 MHz crystal oscillator and the on-chip VCO. The VCO-derived clock signal controls the charge pump, and clock drivers are implemented to enable the clock to drive the large MOSFETs in the charge pump. In this manner, the control voltage V_c can adjust the output of the charge pump V_{pp}, which powers the transducer driver. The transducer driver comprises two high-voltage NMOSs operating as an HB driver. These NMOSs occupy significant areas to achieve low on-resistances, necessitating the need for gate drivers. Additionally, the high-side device Q1 requires an HVLS and external bootstrap circuit consisting of C_{BOOT} and D_{BOOT} to ensure that it remains on when the source voltage rises.

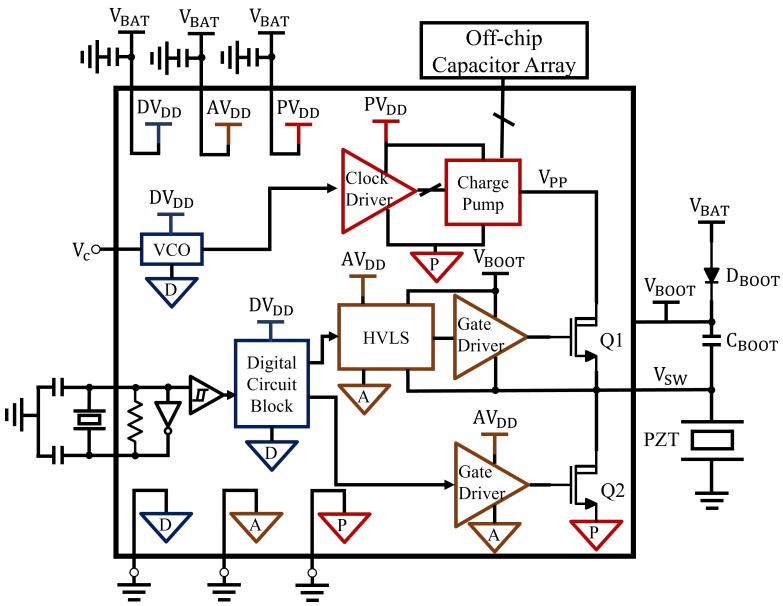


Figure 2. System architecture of the proposed ASIC and its periphery components. The blue boxes are digital modules, the brown boxes are analog modules, and the red boxes are power modules.

2.1. Charge Pump

The proposed LIPUS system requires a DC-DC boost converter to transform the portable power voltage (3.7∼5 V) to a level that can drive the ultrasound transducer. To address concerns around miniaturization and MRI compatibility, a charge pump was selected as the DC-DC boost converter for the proposed system. The design of the four-stage charge pump was based on CP-1 topology, as presented in [24] and shown in Figure 3a. Expanding upon prior research utilizing a fixed-frequency clock, the proposed design incorporates a VCO as a source of adjustable frequency. This feature enables the charge pump to operate at optimal frequencies tailored to different load conditions. HV devices

provided via AMS 0.35 µm High-Voltage CMOS Process Technology (H35B4D3) are utilized in this charge pump topology, allowing the MOSFETs to withstand a higher drain-source voltage. This characteristic enables each stage of the charge pump to boost a higher voltage without breakdown, requiring only four stages to reach the necessary driving voltage (approximately 12∼20 V).

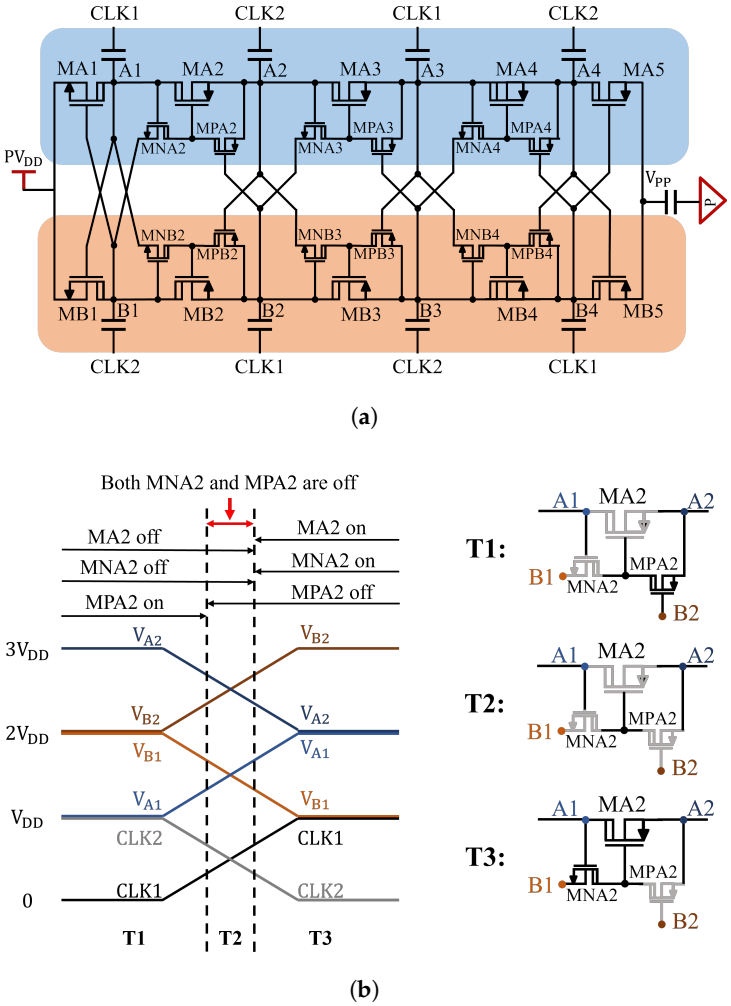


Figure 3. (**a**) Four-stage charge pump in the proposed system (revised from the previous work [24]). (**b**) Switching waveform and the corresponding operation of a representative CTS MA2.

The four-stage charge pump is comprised of two identical branches, each of which works with complementary clocks. Each branch includes charge transfer switches (CTSs) and gate-control transistors. With branch A as an example, MA1, MA2, MA3, MA4, and MA5 act as CTSs to transfer charges to the following stages. MNA2, MPA2, MNA3, MPA3, MNA4, and MPA4 function as gate-control transistors to regulate the opening and closing of their corresponding CTSs. The two out-of-phase clocks, CLK1 and CLK2, oscillate between the voltage power supply PV_{DD} and the ground. During phase 1, when CLK1/CLK2 is high/low, MA2, MA4, MB1, MB3, and MB5 are switched on, while the remaining CTSs are switched off. This results in the transfer of charges from A1 to A2, A3 to A4, PV_{DD} to B1, B2 to B3, and B4 to V_{PP}. During phase 2, when CLK1/CLK2 is low/high, MA1, MA3, MB2, MB4, and MA5 are switched on, while other CTSs are switched off. As a result, charges transfer from PV_{DD} to A1, A2 to A3, B1 to B2, B3 to B4, and A4 to V_{PP}.

The example of MA2 and its gate-control transistors MNA2 and MPA2, as depicted in Figure 3b, is used to provide a detailed explanation of the charge pump's operation. During T1, when CLK1/CLK2 is low/high, MNA2 turns off because $Vgs(MNA2) = V_{A1} - V_{B1} =$

$-V_{DD}$, and MPA2 turns on because $V_{gs}(MPA2) = V_{B2} - V_{A2} = -V_{DD}$. Consequently, the CTS MA2 turns off, as its source A2 is connected to its gate B2 ($V_{gs}(MA2) = 0$). In the clock transition, CLK1 goes higher, while CLK2 goes lower. At the point where $V_{gs}(MPA2) = V_{B2} - V_{A2} > -V_{th}$, MPA2 turns off, marking the start of T2. During T2, all transistors, including MA2, MNA2, and MPA2, turn off. At the end of T2 and the start of T3, MNA2 turns on, as $V_{gs}(MNA2) = V_{A1} - V_{B1} > V_{th}$. Consequently, MA2 turns on, as $V_{gs}(MA2) = V_{B1} - V_{A2} = -V_{DD}$. With this deliberate design, the reverse charge can be avoided since all transistors turn off during T2. Furthermore, the high-voltage MOSFET transistors utilized in this charge pump design can bear a maximum drain-source voltage of $2V_{DD}$. The power supply to the clock driver should remain below 2.5 V or 1.65 V if using standard MOSFETs, which have a lower voltage tolerance of 5 V or 3.3 V. However, by using high-voltage MOSFET transistors, a typical 5 V USB power supply can power the clock driver. Moreover, this design allows each charge pump stage to boost higher voltage, reducing the number of stages required.

2.2. High Voltage Level Shifter

The HVLS is a critical component of the proposed system, as it enables the high-side NMOS of the HB driver to turn on. The primary purpose of the HVLS is to translate logic signals between different voltage domains, with propagation delay and power dissipation being critical parameters. Moreover, the size of the HVLS must be considered, as it affects the chip's cost. Thus, the topology of the HVLS proposed in [25], which utilizes the pulse-triggering approach, was adopted in the proposed system. The overall circuit diagram of the HVLS is depicted in Figure 4, and it comprises an edge detection module, a level shifter, and a latch. The edge detection module generates a pulse to V_{RE} or V_{FE} at the rising or falling edge of the input signal V_{IN_L}, respectively. The level shifter then inverts and lifts the pulse from the low-voltage domain to the high-voltage domain. The resulting notching signal at V_R or V_F changes the latch's state, thus toggling V_{OUT_H} between the high (V_{BOOT}) and low (V_{SW}) levels. In the steady state, all the voltage levels remain stable, and the output is latched.

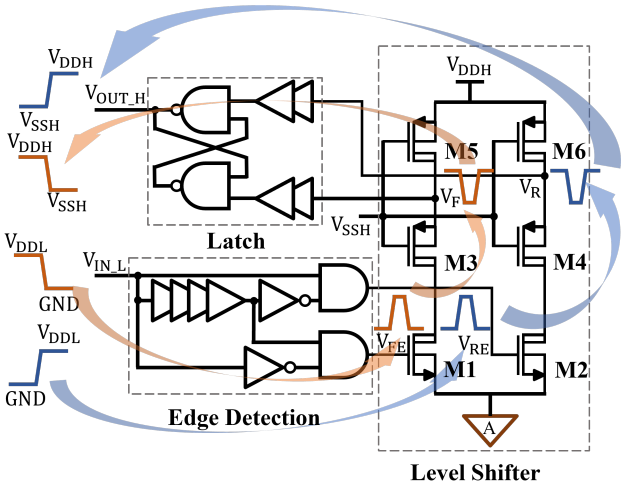


Figure 4. Circuit diagram of the HVLS and its operating principle (revised from the previous work [25]).

2.3. Half-Bridge Driver

The system's output driver utilizes the HB topology, implemented with two NMOS transistors having high drain-source breakdown voltage. An NMOS is used on the high side of the HB because it offers better conducting properties and switch speed than an equivalent PMOS. However, the high-side NMOS requires $V_{GS} = V_G - V_{SW} > V_{th}$ to remain turned on. To meet this requirement, a bootstrap circuit and an HVLS circuit are employed to lift the gate voltage of the high-side NMOS to $V_G = V_{BOOT} = V_{SW} + V_{DD}$.

The on-resistance of the output switches is set to 3.1 ohms, based on a trade-off between the conduction power loss, switching power loss, and occupation area. Their relatively large area (W/L = 10,000 μm/0.5 μm) poses two challenges. First, a large-area NMOS gate has significant parasitic capacitance, requiring a multi-stage gate driver to accelerate turn-on and turn-off. To achieve this, four cascades of inverters are employed, with sizes increasing in a geometric progression. Second, to prevent two NMOS transistors from turning on simultaneously and causing a short circuit between V_{PP} and GND, a dead time generator is used. Its circuit topology and output waveform are shown in Figure 5, which inserts dead time during the turn-on alternation of the two NMOS transistors, allowing both to turn off completely and preventing simultaneous conduction.

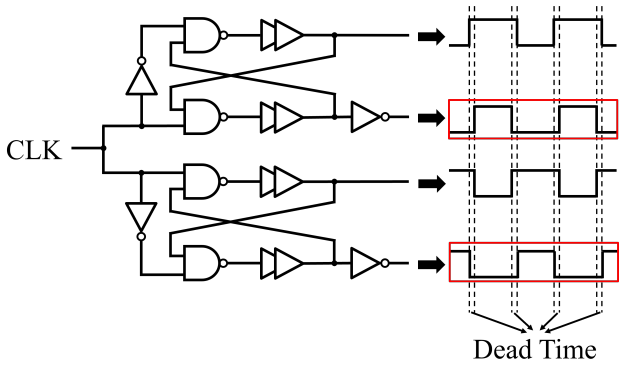


Figure 5. Circuit diagram of the dead time generator and its waveform. The waveforms in the red boxes are used to drive the HB driver.

2.4. Voltage Controlled Oscillator

A three-stage current-starved voltage-controlled ring oscillator (CSVCRO) is used to generate a clock with adjustable frequency for the charge pump module. By allowing the clock frequency to be adjusted, the power output capability of the charge pump can be tailored to the specific requirements of the application. The CSVCRO topology was chosen for its low power consumption, wide frequency range, and high integration capacity [26]. The CSVCRO adjusts the frequency by controlling the current used to charge or discharge the load capacitance, which is achieved by modulating the on-resistances of the pull-down and pull-up transistors. Lower on-resistances allow a larger current to charge or discharge the load capacitance, resulting in a higher frequency, and vice versa.

Figure 6 shows the circuit diagram of the three-stage CSVCRO module, which comprises a complementary control signal generator, a CSVCRO core, and a clock output stage. The complementary control signal generator uses a half-current mirror topology to ensure similar currents through M1 and M2. M4, M8, and M12 limit the pull-up current flow, while M5, M9, and M13 limit the pull-down current flow. In this way, the complementary control signal V_N makes the current limiting capacity of M4, M8, and M12 similar to that of M6, M10, and M14, which are directly controlled via the input control voltage V_P. The three-stage CSVCRO core is composed of M3–M14, which forms three inverters. The current flows of these three inverters are limited by current sources and sinks controlled via V_P and V_N. The output clock signal is buffered via an inverter and then passed to a flip-flop to produce a clock signal with a precise 50% duty cycle and narrow rising and falling edges, making it closer to a square wave. An out-of-phase clock signal $\overline{CLK}$ is generated simultaneously, which is also required for the charge pump module.

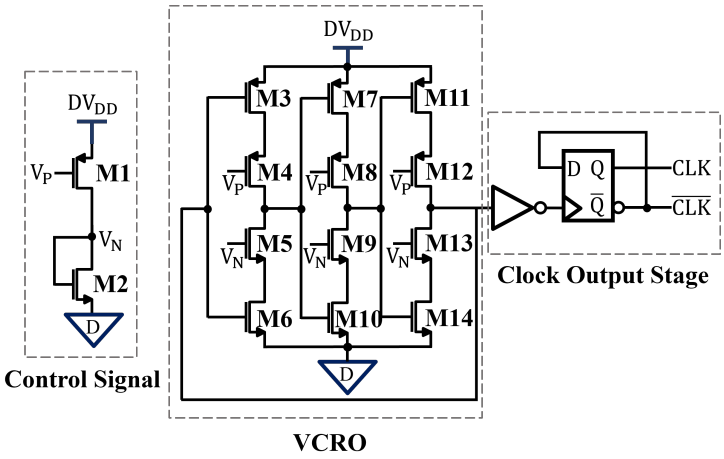


Figure 6. Circuit diagram of the 3-stage current-starved voltage-controlled oscillator.

3. Results and Discussion

Prior to the tape-out, the proposed ASIC was simulated in the AMS 0.35 µm H35B4D3, HIT-kit v4.10, using a Cadence IC 6.1.5 Spectre Circuit Simulator (San Jose, CA, USA). Post-layout simulations were performed with the power supply set to 3.7 V by default. The micrograph of the bare die is shown in Figure 7, and its area is 4 mm^2 including pads. The transistor parameters of the proposed design can be found in Table 1. The post-layout simulated performance of the entire chip, with a transducer load modeled using the Butterworth–Van Dyke model, is presented in Table 2. The capacitance of all capacitors in the array was 4.7 nF, which was chosen after the thorough consideration of several factors, including charge pump output power capacity, efficiency, ripple amplitude, startup speed, and dynamic performance.

Table 1. Transistor parameters.

Transistors in Charge Pump	**Type**	**W/L (µm/µm)**
MA1, MB1	20 V HVNMOS	2200/0.5
MA2-5, MB2-5	20 V HVPMOS	2700/1
MNA2-4, MNB2-4	20 V HVNMOS	300/0.5
MPA2-4, MPB2-4	20 V HVPMOS	1800/1
Transistors in HVLS	**Type**	**W/L (µm/µm)**
M1, M2	50 V HVNMOS	10/0.5
M3, M4	50 V HVPMOS	10/1
M5, M6	5V PMOS	0.5/0.5
Transistors in CSVCRO	**Type**	**W/L (µm/µm)**
M1	5V PMOS	1.2/1
M2	5V NMOS	0.6/1
M3, M7, M11	5V PMOS	6/0.5
M4, M8, M12	5V PMOS	9/0.5
M5, M9, M13	5V NMOS	4.5/0.5
M6, M10, M14	5V NMOS	3/0.5
Transistors in Half Bridge	**Type**	**W/L (µm/µm)**
Q1, Q2	50 V HVNMOS	10,000/0.5

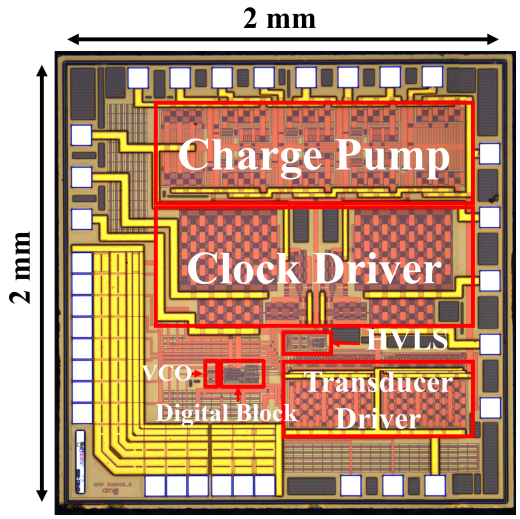


Figure 7. Micrograph of the bare die.

3.1. Simulation Results

To assess the performance of the charge pump under diverse continuous-current delivery conditions, simulations were conducted with various resistive loads (30 Ω, 100 Ω, and 300 Ω) and frequencies (10–60 MHz). The simulation results for the output power, efficiency, ripple voltage, and startup time are presented in Figure 8a,b, where startup time is defined as the time required to reach 90% of the final output voltage. The results indicate that power conversion efficiency decreases with a heavier load. The optimal control frequency varies with the resistive load, necessitating a higher control frequency to achieve maximum output power under heavier loads. Moreover, the control frequency exhibits an influence on the power conversion efficiency, typically reaching its maximum near the frequency associated with peak power. Concurrently, the ripple voltage and the startup time demonstrate a decreasing trend as the control frequency increases. The charge pump typically completes startup in less than 3 µs, with a startup time of approximately 1 µs for 30 Ω and 100 Ω loads. Based on the simulation results, it was observed that a clock frequency range of 10–60 MHz fulfills the power output and speed requirements of the charge pump across common load scenarios. This implies that adjusting the VCO's clock range to cover this frequency span would be beneficial, allowing flexibility to tailor the clock frequency based on specific application demands for output power, efficiency, ripple, and startup time.

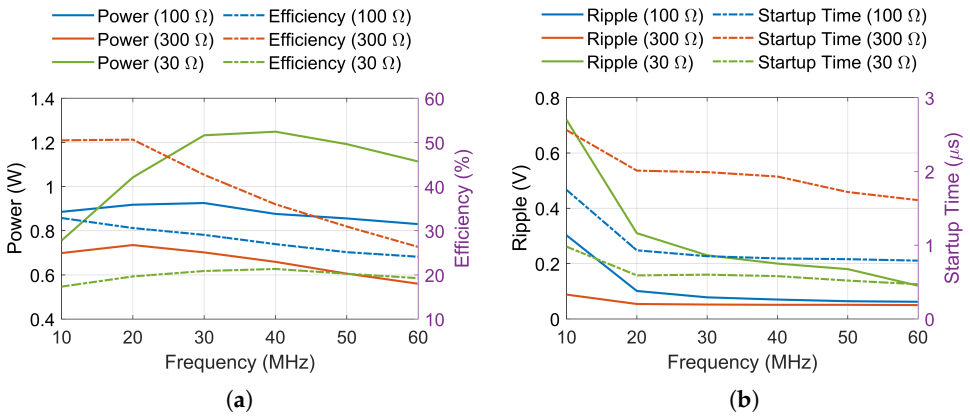


Figure 8. Post-layout simulation result of the charge pump for different loads and different clocks. (**a**) Output power and efficiency. (**b**) Ripple and startup time.

Table 2. Post-layout simulated performance of the proposed ultrasound interface IC chip.

Power	Component	Direction	Power	Efficiency
3.7 V	HB transducer driver	input	89.2	96.97%
		output	86.5	
	DC-DC booster converter	input	242	36.86%
		output	89.2	
	Whole chip	input	244	35.45%
		output	86.5	
5 V	HB transducer driver	input	170.7	96.95%
		output	165.5	
	DC-DC booster converter	input	454.8	37.53%
		output	170.7	
	Whole chip	input	457.7	36.16%
		output	165.5	

3.2. Test Results

To evaluate the performance of the chip, we designed a corresponding peripheral circuit and performed testing. Since the primary objective of our design was to drive the ultrasound transducer, waveform, power input, power output, and ultrasonic power output measurements were used for evaluation. All capacitors in the array of the peripheral circuit were 4.7 nF X5R capacitors. The load used in the testing was a piezoelectric (PZT) transducer manufactured by APC International, Ltd. (Mackeyville, PA, USA), featuring a single resonance frequency of 1.5 MHz and a radiating surface area of 0.95 cm^2. The impedance of the PZT transducer was measured using an MFIA Impedance Analyzer (Zurich Instruments, Zürich, Switzerland), and the results indicated an impedance of $96.2\Omega\angle-25.33^\circ$ at 1.5 MHz. Output waveforms were recorded using a Tektronix TBS 2000 oscilloscope (Tektronix Inc., Beaverton, OR, USA), including the voltage on the load V_{load}, the output voltage of the charge pump V_{PP}, and the current on the load I_{load}. The system was powered using a Keithley 2231A-30-3 precision DC power supply (Keithley Instruments, Cleveland, OH, USA), which provided real-time power dissipation data in the front panel. The current on the load was measured by inserting a series resistor of 0.5 Ω on the ground side of the transducer and measuring the voltage across it. During testing, the controlling voltage was adjusted to the appropriate condition. The ultrasound power output of the transducer was measured utilizing an OHMIC UPM-DT-1000PA ultrasound power meter (OHMIC Instruments, St. Charles, MO, USA). The measurement setup is shown in Figure 9.

Figure 10a,b illustrate the waveforms measured with power supplies of 3.7 V and 5 V, respectively. It was observed that the output voltage of the charge pump (V_{PP}) underwent an immediate drop at the rising edge of the load voltage (V_{load}). This phenomenon was expected, and it was a result of a large transfer of charge from the energy storage capacitor of V_{PP} to the load when switch Q1 was turned on. At other times, the charge pump could restore V_{PP} to its previous level, as only a small number of charges would transfer to the load. The observed ripple in V_{PP} was largely caused by this immediate drop and subsequent restoration process, which is consistent with the simulation results. Furthermore, the implementation of a cross-coupled topology and a relatively high clock frequency in the range of tens of MHz enables the rapid replenishment of the load capacitor's charge, ensuring the maintenance of a certain voltage level. The measured ripple was 2.1 V for a power supply of 3.7 V and 2.9 V for a power supply of 5 V. Furthermore, the impedance mismatch resulted in noticeable ringing in V_{load} and I_{load}, but the single resonant frequency characteristic of the ultrasound transducer made it insensitive to such

distortions. Figure 10c,d presents the waveforms of V_{PP} and V_{load} on a millisecond scale. These figures clearly show the pulsed working mode of the chip with a duty cycle of 20% and a pulse repetition frequency of 1 kHz. During the remaining 80% idle state, the charge pump was turned off to conserve energy. These figures also reveal that V_{PP} fell slowly due to the leakage current during the idle state.

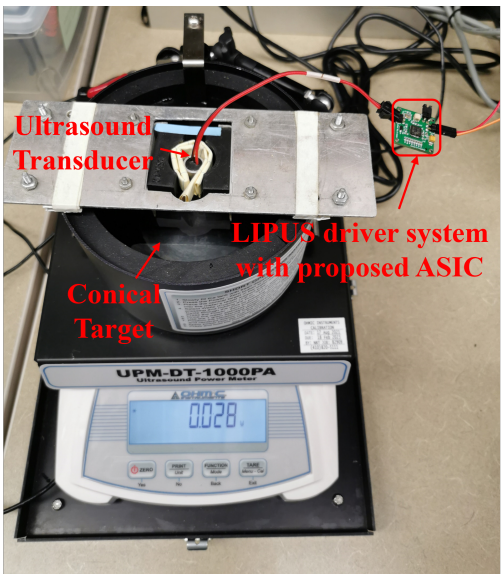


Figure 9. The ultrasound power measurement setup.

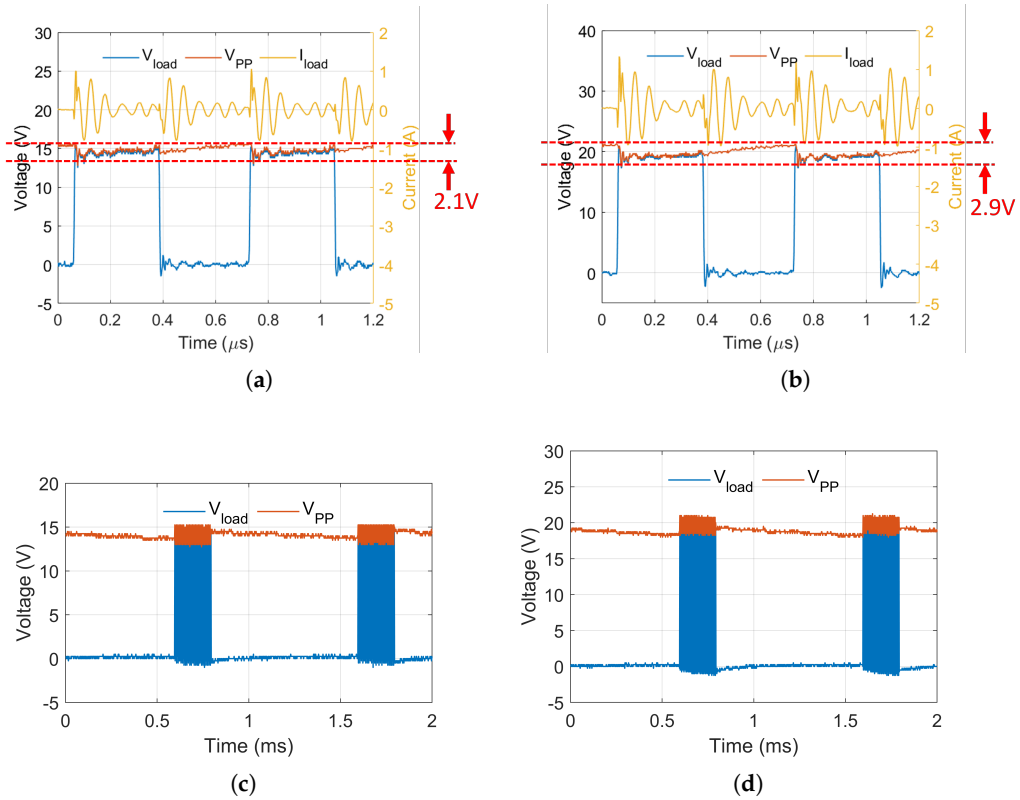


Figure 10. Waveforms on a microsecond scale of the voltage on the load V_{load}, the output voltage of the charge pump V_{PP}, and the current on the load I_{load} with a power supply of (**a**) 3.7 V and (**b**) 5 V. Waveforms on a millisecond scale of V_{load} and V_{PP} with a power supply of (**c**) 3.7 V and (**d**) 5 V.

Table 3 summarizes the power conversion performance of the proposed LIPUS system. The power conversion efficiency was only 30% due to the implementation of the four-stage charge pump. However, even with this relatively low efficiency, the ASIC was still capable of driving the ultrasound transducer to generate 28 mW or 49 mW of power when supplied with 3.7 V or 5 V, respectively. This resulted in an ultrasound power intensity of 29.5 mW/cm^2 or 51.6 mW/cm^2, respectively. Concurrently, lithium batteries and low-dropout (LDO) regulators' configuration was utilized to supply power to the test circuit, generating both 3.7 V and 5.0 V. The output power derived from this battery-powered configuration was closely aligned with those acquired using the DC power supply.

Table 3. Summary of the system performance of the proposed LIPUS chip.

Power supply (V)	3.7	5
Input power of the chip (mW)	347.8	620
Output power to the load (mW)	107.2	184.2
Power conversion efficiency of the chip	30.8%	29.7%
Output ultrasound power (mW)	28	49
Output ultrasound Power intensity (mW/cm^2)	29.5	51.6

3.3. Discussion

The proposed ASIC, when combined with a properly designed peripheral circuit and a customized ultrasound transducer, can deliver an average ultrasound power intensity of 29.5 mW/cm^2 or 51.6 mW/cm^2 (fundamental frequency: 1.5 MHz; pulse repetition frequency: 1 kHz; and duty cycle: 20%) with a power supply of 3.7 V or 5 V, respectively. This range of ultrasonic power intensity and frequency parameters has broad applicability in various therapeutic applications. In addition, the proposed system is suitable for portable and MRI-compatible system development. Acknowledging concerns in the field around MRI-compatibility and off-chip crystal and battery devices and the MRI-compatibility of other modules in the system are focal points for future research.

The total output ultrasound power intensity of 29.5 mW/cm^2 or 51.6 mW/cm^2 incorporates diverse clinical applications into the system, opening up numerous possibilities for utilization. Recent studies have demonstrated the effectiveness of LIPUS with similar frequency settings and average ultrasound power intensities in various therapeutic applications. For example, research has shown that LIPUS with an average ultrasound power intensity of 30 mW/cm^2 can significantly accelerate orthodontic treatment and reduce orthodontically induced tooth root resorption [10,27]. This same parameter setting has also been shown to improve fracture healing and promote osteogenic activity around implants [28,29]. Furthermore, other research groups have validated the efficacy of LIPUS with an average ultrasound power intensity of 50 mW/cm^2 in promoting the proliferation of bone marrow mesenchymal stem cells [30,31].

Table 4 provides a comparison of the performance of the proposed ASIC with the performance of other similar recently published studies [25,32–34] that have employed charge pumps to meet relatively high output power demands (above 5 mW range) in biomedical applications. Another comparable ASIC that utilizes a charge pump for the ultrasound driver system has been described in [35], but the paper does not provide sufficient performance parameters for a comprehensive comparison. Charge pumps are typically designed for μA-level current loads [36]. The design in [33] increased the voltage output range and enhanced conversion efficiency by incorporating a negative voltage charge pump module. Meanwhile, the design in [34] employed Dynamic Output Impedance and Load Energy Recycling methods to boost conversion efficiency. It can be argued that both [33] and [34] enhanced conversion efficiency by modifying the load configuration essentially. Although the systems described in [33,34] exhibit better power conversion efficiency, our proposed work delivers significantly higher output power. In comparison with [25], the implementa-

tion of an adjustable clock frequency in the proposed work allowed the charge pump to operate at its optimal frequency. Consequently, under the same 3.7 V power supply, our proposed work achieved a higher output voltage (15.5 V versus 14 V) and improved energy conversion efficiency (30.8% versus 17%). A notable aspect revealed in the comparison is the utilization of large off-chip pumping capacitors in the proposed system. In high-power designs, which require several hundred milliwatts or even one watt, the use of off-chip capacitors offers enhanced capacitor performance and cost-effectiveness. Additionally, the packaging of capacitors in 01005 packages significantly reduces the surface area required for off-chip components, thereby diminishing the value of on-chip capacitance even further.

Table 4. Comparison with other similar works.

Work	**This Work**	[25]	[32]	[33]	[34]
Technology	0.35 µm HVCMOS	0.18 µm HVCMOS	0.35 µm HVCMOS	0.25 µm BCD	0.18 µm CMOS
V_{in} (V)	5 (3.7)	3.7	3.7	3	3.3
# of stage	4	4	36	4	4
V_{out} (V)	21.5 (15.5)	14	120	9.3	15.4
Frequency	10–60 MHz	20 MHz	10 MHz	N/A	30 MHz
Capacitor	4.7 nF off-chip	132 pF on-chip	N/A	100 pF on-chip	180 pF on-chip
Efficiency	**29.7% (30.8%)**	17%	12.6%	41% @ 49.5 mW	32.3% @ 8.2 mW
Output Power (mW)	**184.2 (107.2)**	72	13.7	49.5	8.2
Die area (mm^2)	2.0 × 2.0	N/A	3.9 × 5.6	2.01 × 1.12	0.7 × 0.8

The ASIC features integration with a digital control block for ultrasound signal generation, requiring only a few passive electronic components to construct an ultrasound driver system. The employed system prototype circuit is merely 2 × 2 cm^2, and it is conceivable that further miniaturization could be attained in practical applications. Moreover, the VCO enables the charge pump to adapt to the optimal output state under varying loads, making the system more versatile. In summary, we have consolidated several essential modules onto a singular ASIC and utilized off-chip capacitors capable of directly generating therapeutic LIPUS intensities with desirable efficiency. A compact, MRI-compatible, and wearable device for LIPUS delivery can be designed based on the proposed ASIC, which is feasible for biomedical applications.

4. Conclusions

This paper introduced a LIPUS interface chip designed for portable medical therapeutic devices, offering a compact, cost-effective, and MRI-compatible solution. The ASIC integrates key components, including a charge pump, a transducer HB driver, VCO, HVLS, and a digital circuit block, implemented using AMS 0.35 µm H35B4D3. Experimental tests indicate a power output of 181.5 mW or 103.3 mW with a 5 V or 3.7 V supply, yielding a power conversion efficiency of approximately 30%. This enables the delivery of a SATA of 29.5 mW/cm^2 or 51.6 mW/cm^2 (fundamental frequency: 1.5 MHz; pulse repetition frequency: 1 kHz; and duty cycle: 20%) with a 3.7 V or 5 V supply, respectively. Notably, the chip's MRI compatibility is enhanced by eliminating the need for inductors. The miniaturized, low-cost, and wearable design positions it as an attractive alternative to bulky and expensive commercial LIPUS devices. In conclusion, the proposed LIPUS interface chip offers a promising solution for portable and cost-effective medical therapeutic devices.

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Abbreviations

The following abbreviations are used in this manuscript:

LIPUS	Low-intensity pulsed ultrasound
SATA	Spatial average temporal average
FDA	Food and Drug Administration
NICE	National Institute for Health and Care Excellence
ASIC	Application-specific integrated circuit
MRI	Magnetic resonance imaging
HVLS	High voltage level shifter
HB	Half-bridge
VCO	Voltage-controlled oscillator
CTS	Charge transfer switch
CSVCRO	Current-starved voltage-controlled ring oscillator

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