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A First-Order Noise-Shaping SAR ADC with PVT-Insensitive Closed-Loop Dynamic Amplifier and Two CDACs

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Abstract: This paper presents a first-order noise-shaping (NS) successive approximation register (SAR) analog-to-digital converter (ADC) with a process, (supply) voltage, and temperature (PVT)-insensitive closed-loop integrator and data-weighted averaging (DWA). The use of a cascode floating inverter amplifier (FIA)-type dynamic amplifier with high gain enables an aggressive noise transfer function while minimizing the power consumption associated with the use of an active filter. In the proposed ADC, the residue is generated by a capacitive digital-to-analog converter (CDAC) employing DWA, which is made possible by employing a second CDAC, which operates after the SAR operation is completed. The proposed ADC is designed with a 28 nm CMOS process with 1 V power supply. The simulation results show that the ADC achieves the SNDR of 71.2 dB and power consumption of 228 μW when operated with a sampling rate of 80 MS/s and oversampling ratio (OSR) of 10. The Schreier figure-of-merit (FoM) is 173.6 dB, and Walden FoM is 9.6 fJ/conversion-step.

Keywords: analog-to-digital converter (ADC); successive approximation register (SAR); noise shaping (NS); process–voltage–temperature (PVT) insensitivity; data-weighted averaging (DWA)

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1. Introduction

Successive approximation register (SAR) analog-to-digital converters (ADCs) are well suited for mobile applications because they consume low electrical power and require low supply voltage due to their digitally friendly nature [1–3]. However, comparator noise and the die area of the digital-to-analog converter (DAC) limit the signal-to-noise-distortion ratio (SNDR) [4]. Delta-sigma (DS) ADCs are used in high-resolution applications [5–9]. DS ADCs designed for high-end audio applications can achieve signal-to-noise-and-distortion ratios (SNDRs) higher than 100 dB, which is translated into an effective number of bits (ENOBs) larger than 16 bits. However, their bandwidth is limited because DS ADCs require large over-sampling ratios (OSRs) for effective quantization noise suppression in the signal band. The OSR is defined as f_S/(2*BW), where f_S represents the sampling (or operating) frequency and BW represents the signal bandwidth. Therefore, if we increase the OSR for a given bandwidth, we need to increase the sampling frequency. The power consumption becomes excessively high when the sampling frequency is raised too much. Therefore, the BW of DS-ADCs with high SNDR has been limited. For example, the audio applications that require a very high SNDR typically use only 20 kHz of bandwidth.

To overcome these disadvantages, noise-shaping (NS) SAR ADCs, which combine the merits of the SAR ADC and the delta-sigma ADC, have been proposed [10–17]. The noise transfer function (NTF) of an NS-SAR ADC can be made sharp by using a closed-loop feedback integrator using an operational trans-conductance amplifier (OTA) [10]. Because the closed-loop gain of an integrator is defined by the ratio of capacitors, the NTF of a NS-SAR ADC with closed-loop integrators employing OTAs is relatively insensitive against process, (supply) voltage, and temperature (PVT) variations. However, an OTA is a

power-hungry block because of the static current consumption. Instead of OTAs, open-loop dynamic amplifiers with low power consumption were proposed for the loop filter [9]. However, the gain of them is sensitive to the PVT variations and clock timing, which eventually affects NTF. To avoid the use of amplifiers altogether, passive noise shaping techniques were employed in [14–17]. Usually, the passive noise shaping relies on the charge transfer between capacitors controlled by switches. The fact that there is no power consumption by active devices is a clear advantage. However, in a passive charge transfer, a complete transfer cannot occur. Therefore, an integrator using this technique is very lossy, and the NTF becomes weak. As a result, NS-SAR ADCs employing passive noise shaping achieved only modest resolution [14–17].

This paper presents a first-order NS-SAR ADC with a closed-loop integrator employing a dynamic amplifier. Because it uses a closed-loop integrator, it is robust against the PVT variations. To achieve a high open-loop gain required for a precise operation of the closed-loop integrator while maintaining a high power-efficiency, a cascode floating inverter amplifier (FIA)-type dynamic amplifier was employed. The proposed ADC employs two capacitive DACs (CDACs), of which one is for the conventional SAR operation and the other is for the noise-shaping. Using two CDACs makes it easier to optimize them individually. The capacitance of the CDAC used for SAR operation, which is called "coarse CDAC" in this work, can be small for low power consumption because the noise and mismatch from the coarse CDAC is shaped by the NTF of the NS-ADC at least partially and do not contribute significantly to SNDR degradation. The noise and mismatch from the residue-generating second CDAC is not shaped by the NTF. Therefore, they should be suppressed directly. To suppress the thermal sampling noise, the second CDAC, which is called "fine CDAC" in this work, was designed to be large. To suppress the nonlinear distortion arising from the mismatch between the capacitors in the fine CDAC, we employed mismatch error shaping, more specifically, data weighted averaging (DWA) technique [18]. It is noted that when a single CDAC is used for both the SAR operation and the residue generation, it is difficult to apply DWA technique because of the time-delay associated with the DWA logic. However, in this work, because we used a separate CDAC for the residue generation, the DWA can be applied bypassing the delay issues.

This paper is an extension of [19]. The rest of this paper is organized as follows. In Section 2, we explain the operation of the proposed NS-SAR ADC. The implementation details of the CDACs, dynamic amplifier, and comparator are presented in Section 3. Section 4 presents the results obtained from SPICE-level simulations, and Section 5 concludes this work.

2. Proposed NS-SAR ADC

Figure 1 shows the signal flow diagram of the proposed NS-SAR ADC. The input of the SAR ADC is the sum of the external analog input, V_{IN}, and the integrated residue voltage, V_{int}. The SAR output, D_{OUT}, is converted by a digital-to-analog converter (DAC) into an analog version. The residue is generated by subtracting this analog, D_{OUT}, from the input signal, and by integrating the residue, the V_{int} is produced. Note that all of this signal processing is performed in the analog domain. The V_{int} is added to the feedforwarded external input signal to form the input signal of the SAR ADC for the next cycle of the ADC operation.

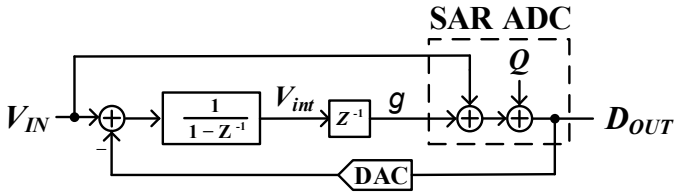

Figure 1. Signal flow diagram of the proposed NS-SAR ADC.

It should be noted that, in this work, the sampling frequency is 80 MHz. With an OSR of 10, this corresponds to an ADC bandwidth of 4 MHz. An 8-bit digital output, D_{OUT}, is produced at the sampling frequency of 80 MHz. However, after the digital decimation filtering of D_{OUT}, the digital signal frequency is lowered to 8 MHz, and the effective resolution is increased to higher than 12 bits. In this structure, the full scale (FS) input voltage range is determined by the reference voltages used by the DAC, which converts the digital output, D_{OUT}, into an analog voltage. It means that, if V_{refp} and V_{refn} are the maximum and the minimum output voltages of the DAC, respectively, the FS input range is between V_{refp} and V_{refn}.

From Figure 1, we can obtain the following first-order NTF of the NS-SAR ADC:

$$\mathrm{NTF}(z) = \frac{1 - z^{-1}}{1 + (g-1)z^{-1}}, \tag{1}$$

where g represents the gain of the residue path, which controls how much the NTF is aggressive. It is noted that, when $g = 1$, the NTF becomes simply $1 - z^{-1}$. In this work, to make the NTF more aggressive, $g = 1.8$ is used. The details are described later in the paper.

Figure 2 shows the simplified schematic of the proposed NS-SAR ADC implementing the signal flow of Figure 1. The diagram is drawn in a single-ended form for convenience, whereas the actual circuit is differential. The small box located at the lower-right corner represents the timing diagram. The NS-SAR ADC consists of an 8-bit SAR ADC, a CDAC for residue generation, and a residue integrator. In the sampling phase, $\varnothing_S$, V_{IN} is sampled on the coarse and the fine CDACs, using bootstrapped switches. In the SAR conversion phase, the SAR ADC converts the signal $V_{IN} + gV_{int}$ into D_{OUT}, where V_{int} is the integrated residue. V_{int} is added to V_{IN} virtually by the two-input-pair comparator. For a SAR conversion, the dynamic latch-type two-input-pair comparator is operated eight times by $\varnothing_{COMP}$, which is produced by an asynchronous SAR logic [20]. After a SAR conversion, $\varnothing_0$ clock becomes high, and a new residue is generated on the fine CDAC by applying the conversion result D_{OUT} after it is processed by the DWA logic. After the settling of the fine CDAC, $\varnothing_1$ becomes high, and the residue stored on the fine CDAC is integrated on C_F and C_L, producing V_{int}. The residue integrator is implemented in a closed-loop form using an FIA. The FIA is reset when $\varnothing_{RST}$ is high. As mentioned in the Introduction, there are two CDACs, a coarse CDAC and a fine CDAC. The coarse CDAC is used in conventional SAR ADC operations, and the fine CDAC is used to generate the residue voltage from the SAR ADC operations.

The NTF of the proposed ADC can be represented by

$$\mathrm{NTF}(z) = \frac{1 - a \cdot z^{-1}}{1 - b \cdot z^{-1}}, \tag{2}$$

where

$$a = \frac{1}{1 + \frac{1}{A}\left(1 + \frac{C_{Fine}}{C_F}\right)}, \tag{3}$$

and

$$b = \frac{1 - g \cdot \frac{C_{Fine}}{C_F}}{1 + \frac{1}{A}\left(1 + \frac{C_{Fine}}{C_F}\right)}, \tag{4}$$

where g is the comparator gain ratio of the CDAC input and the integrated residue input, C_F is the feedback capacitance of the integrator, C_{Fine} is the total capacitance of the fine CDAC seen at its output, and A is the open-loop gain of the amplifier.

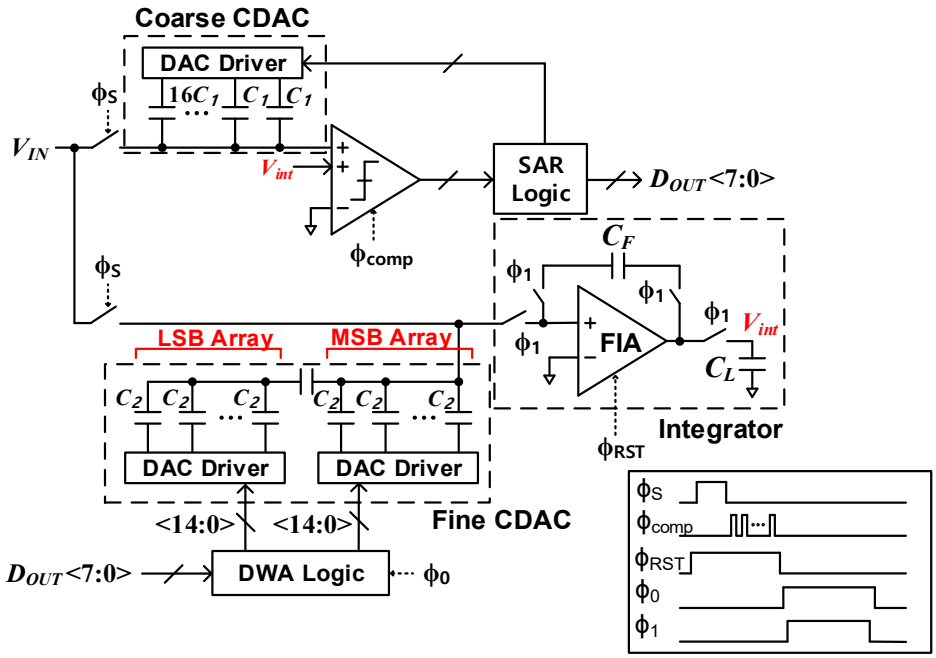

Figure 2. A simplified schematic of the proposed NS-SAR ADC.

Figure 3 shows the plot of NTF for several values of normalized comparator gain ratio defined as $G \equiv g \cdot C_{Fine}/C_F$. The dotted line in Figure 3 represents the bandwidth of the proposed ADC. As G is increased, the NTF becomes more aggressive, and the in-band noise suppression becomes stronger. However, as G becomes larger, the system becomes less stable, as illustrated by the sharp increase in the out-of-band gain at $G = 2$ in Figure 3. If $G > 2$, the ADC becomes unstable.

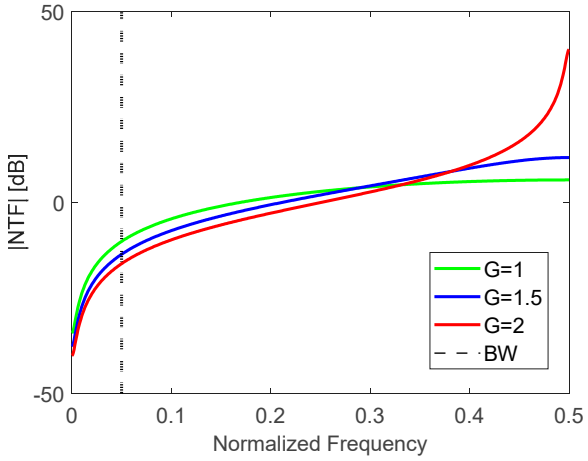

Figure 3. NTF for several values of the normalized comparator gain ratio, G. (A = 100, and V_{IN} = −0.9 dBFS).

Figure 4 shows SNDR as a function of the normalized comparator gain ratio obtained from behavioral simulations using MATLAB. The SNDR reaches the maximum at $G = 2$, and above that, the SNDR drops very rapidly. Therefore, we set G at 1.8 as a trade-off between the noise shaping and the stability.

Figure 5 shows the SNDR as a function of the amplifier gain obtained from behavioral simulations. We can observe that the performance degradation is less than 1 dB only when the open-loop gain is reduced from infinity to 30 v/v. When the gain is reduced further down to 20 v/v, the gain reduction becomes larger than 1.5 dB, which we consider to be too large. To accommodate further gain variations by PVT variation and secure enough

of a margin, we set the nominal gain of the amplifier to 40 v/v, with 30 v/v as the lowest allowable gain. The design of the amplifier is presented in Section 3.2.

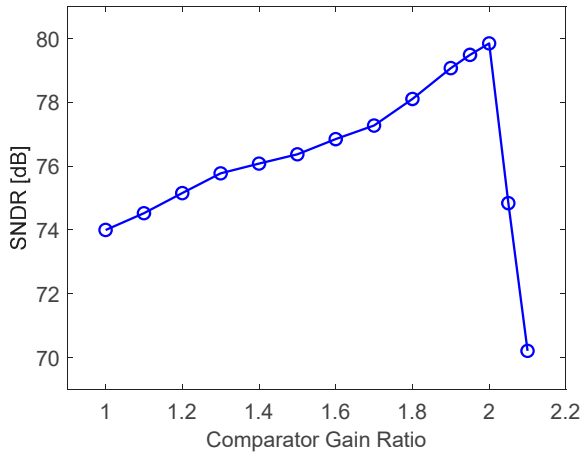

Figure 4. SNDR vs. normalized comparator gain ratio from MATLAB behavioral simulations. (A = 100, V_{IN} = −0.9 dBFS).

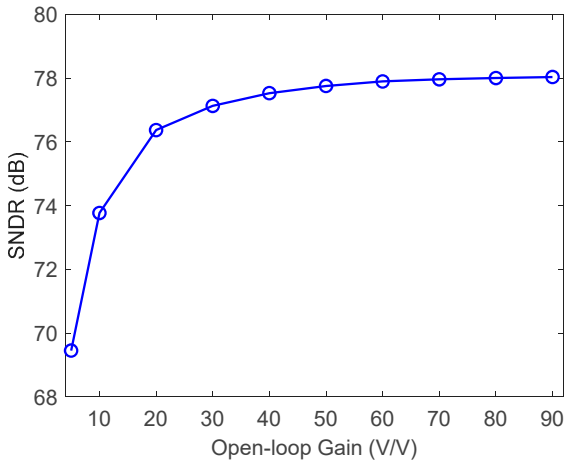

Figure 5. SNDR vs. open-loop gain from MATLAB behavioral simulations. (V_{IN}= −0.9 dBFS).

In Figure 2, the 8-bit SAR output is split into two 4-bit binary signals before being applied to the fine CDAC. Each of the 4-bit signals is converted into 15-bit thermometer-code signals and applied to the MSB or LSB array of the fine CDAC. The mismatch between capacitors making up the arrays introduces nonlinear distortion at the ADC output, which might require the application of a mismatch error shaping (MES) scheme. Therefore, we performed behavioral simulations using MATLAB to investigate this.

Figure 6 shows the SNDR variations against the mismatch rates obtained from the behavioral simulations. The normal distribution was used for the distribution of the capacitance of the unit capacitors. The green squares and yellow triangles represent the SNDR degradation caused by the mismatch when no MES scheme was applied. The green squares represent the case when the mismatch is present in coarse CDAC only and the fine CDAC does not have any mismatch. The yellow triangles represent the case when the fine CDAC has mismatch and the coarse CDAC does not. We can see that the effect of the fine CDAC mismatch on SNDR is much larger than that of the coarse CDAC mismatch. For example, when the coarse CDAC mismatch is 1%, the SNDR reduction is close to zero. However, when the fine CDAC mismatch is 1%, the SNDR is reduced to about 60 dB. Therefore, we focused on the mismatch in the fine CDAC below. The blue and red symbols represent the cases where the MES was applied to the fine CDAC, which was assumed to have mismatch. The coarse CDAC was assumed to be mismatch-free. We used DWA as

our MES scheme. The red symbols represent the case where DWA was applied to both the 4-bit MSB and 4-bit LSB arrays, and the blue symbols represent the case where DWA was applied to the 4-bit MSB array only. It is noted that when DWA was applied to both MSB and LSB arrays, they were applied separately to limit the complexity of the DWA logic. We can observe that even when DWA is applied to the MSB array only, we could obtain almost the same SNDR performance as that obtained when DWA is applied to both arrays. Therefore, we applied DWA to the MSB array only to save power consumption and die area.

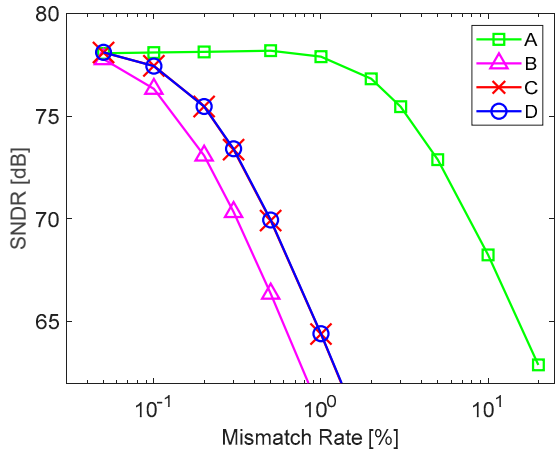

Figure 6. SNDR vs. Mismatch rate with and without DWA obtained from MATLAB behavioral simulations. Average of 100 iterations. $N_{fft} = 2^{15}$, and $V_{IN} = -0.9$ dBFS. A and B, DWA not applied; C, DWA applied to 4-bit MSB and 4-bit LSB separately; D, DWA applied to 4-bit MSB only. A, mismatch is present in coarse CDAC only. B, C, and D, mismatch is present in fine CDAC only.

Figure 7 shows the FFT spectra from MATLAB behavioral simulations with and without DWA applied. The simulations used a sinusoidal input with -0.9 dBFS of amplitude. The mismatch rate (standard deviation) of the fine CDAC was 0.5%. The red curve represents the spectrum from the simulations without DWA, and we can observe large harmonic distortions from the mismatch between capacitors. The blue curve represents the spectrum from simulations without DWA. We can see that the magnitude of harmonic distortions is reduced, and consequently, the SNDR of the ADC is improved.

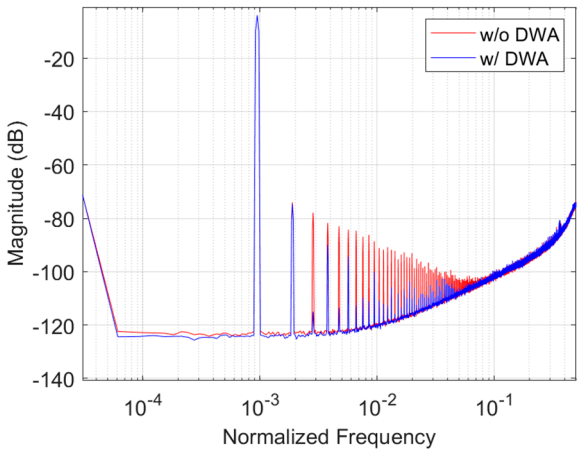

Figure 7. FFT spectra of the proposed NS-SAR ADC output with and without DWA obtained from MATLAB behavioral simulations. Average of 100 iterations. $N_{fft} = 2^{15}$, $\sigma_C = 0.5\%$, and $V_{IN} = -0.9$ dBFS.

Next, we determine the size of the unit capacitors making up the CDACs. It is well known that if we increase the size of the capacitors, we can reduce the kT/C noise

and enhance SNR at the expense of increased CDAC switching power consumption [21]. Therefore, we should make a good compromise when determining the size of the capacitors. When the thermal noise of the CDACs is included, D_{OUT} can be represented by

$$D_{OUT}(z) = V_{IN}(z) + g\frac{z^{-1}}{F(z)}V_{n,f} + \frac{1-z^{-1}}{F(z)}V_{n,c} + \mathrm{NTF}(z)Q(z), \quad (5)$$

where $F(z) = 1 + (g-1)z^{-1}$; and $V_{n,f}$ and $V_{n,c}$ are the thermal noise sampled on the fine and the coarse CDAC, respectively. Equation (5) shows that the noise of the coarse CDAC is shaped, but that of the fine CDAC is not. The in-band noise (IBN) generated by the CDACs can be represented by

$$\mathrm{IBN}_{Fine} \cong \frac{kT}{C_{Fine}} \cdot \frac{1}{OSR}, \quad (6)$$

and

$$\mathrm{IBN}_{Coarse} \cong \frac{kT}{C_{Coarse}} \cdot \frac{\pi^2}{3g^2} \cdot \frac{1}{OSR^3}, \quad (7)$$

where C_{Coarse} is the total capacitance of the coarse CDAC. From Equations (6) and (7), we can observe that C_{Fine} should be about hundred times larger than C_{Coarse} for the same noise contribution at the output of the ADC with an OSR of 10.

To confirm this, we performed behavioral simulations. Figure 8 shows the SNDR variation versus CDAC capacitance obtained from the simulations. The blue circles and the red squares represent SNDR vs. the total capacitance of the coarse CDAC and the fine CDAC, respectively. In the simulations changing the capacitance of the coarse CDAC, the capacitance of the fine CDAC was set very large, and vice versa. We can observe that the proposed ADC has a similar SNDR when the capacitance of the coarse CDAC is about one hundred times smaller than the fine CDAC. It means that, if the total capacitances of the fine and the coarse CDACs are identical, then the overall thermal noise of the proposed ADC is dominated by that of the fine CDAC. Therefore, to minimize the total switching power for a given SNDR requirement, the capacitance of the coarse CDAC should be much smaller than that of the fine CDAC. We set the total capacitance of the fine CDAC to be 960 fF to limit the SNDR degradation by the thermal noise on the fine CDAC to be less than 1 dB.

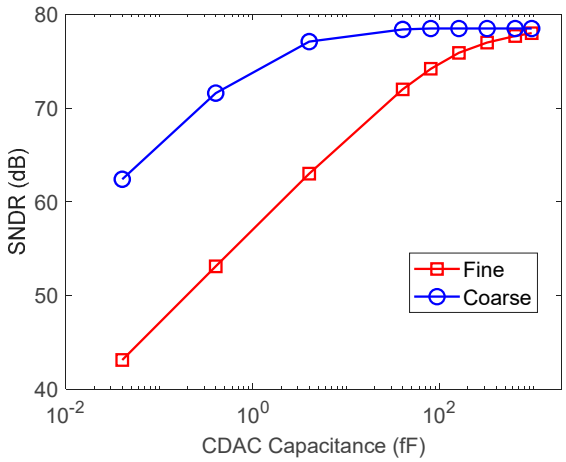

Figure 8. SNDR versus CDAC total capacitance.

A similar guideline leads to 10 fF of the total capacitance of the coarse CDAC. However, this requires a very small unit capacitance. Even after using various techniques (presented in Section 3.1) to increase the unit capacitance, 10 fF of total capacitance would lead to about 0.15 fF of unit capacitance. Although we can design very small custom capacitors, one with this small capacitance is very much susceptible to small manufacturing errors, and the

mismatch rate cannot be guaranteed. Furthermore, it is vulnerable to parasitic capacitance from the nearby wirings too. Figure 6 shows that if the mismatch error of the coarse CDAC is 5% (standard deviation), the SNDR is reduced by about 5 dB to 73 dB. Therefore, it is desired that the mismatch is smaller by several percentage points. Considering these issues, we decided to use a PDK-provided 4.3 fF capacitor as the unit capacitor for the coarse CDAC. This leads to a total capacitance of 284 fF, which is much larger than 10 fF, and it inevitably leads to an increased switching power consumption. The details of the fine and the coarse CDAC configuration are presented in Section 3.1.

It is noted that, because a fine CDAC switching is performed after an SAR conversion is completed, the switching power consumption of the fine CDAC can be significantly reduced. This alleviates the power consumption issue that comes with the large capacitance of the fine CDAC. Furthermore, the simultaneous switching of all the capacitors in the fine CDAC makes the employment of DWA for MES feasible.

3. Circuit Implementation

3.1. CDACs

For the CDACs, we used a structure similar to that used in [22], which combines the split-array CDAC switching method of [2] and the top-plate sampling of [3]. The coarse CDAC capacitors are binary scaled. The single-ended schematic of the 7-bit coarse CDAC is shown in Figure 9a. It is noted that a 7-bit CDAC is sufficient for an 8-bit SAR ADC when the top-plate sampling of [3] is used. It is also noted that the reference voltage for (LSB + 1) is $V_{refp}/4$, and for the (LSB + 2)-th bit switching, only one of two CDAC arrays in the differential structure switches to effectively reduce the reference voltage to $V_{refp}/2$. These allow us to use unit capacitance ($=$ C_1) for LSB + 1, LSB + 2, and LSB + 3. So, the total capacitance of the 7-bit coarse CDAC is $66C_1$.

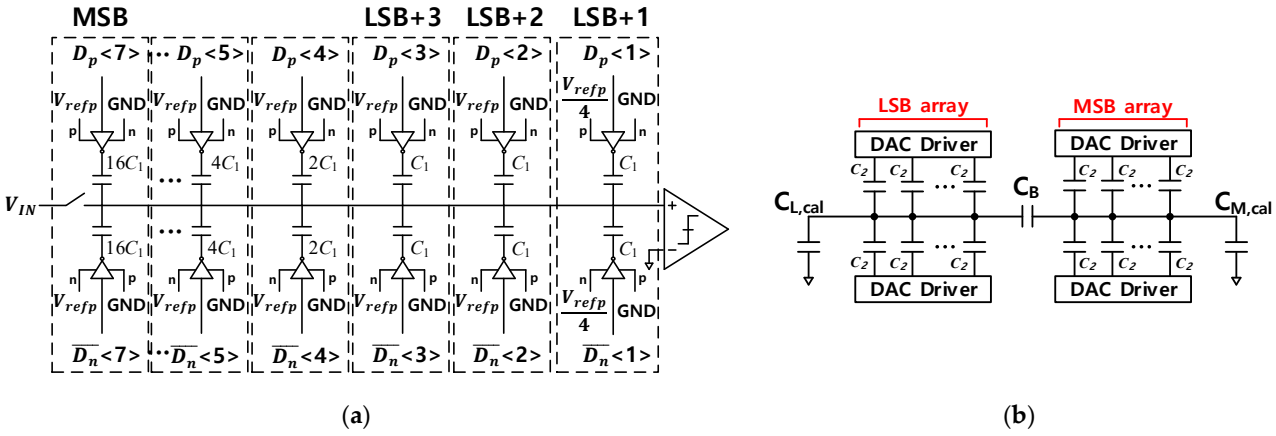

Figure 9. Schematic of the (**a**) coarse CDAC and (**b**) fine CDAC.

Figure 9b shows the schematic of the fine CDAC, which consists of two 15-bit thermometer-coded sub-arrays connected by a bridge capacitor, C_B. The capacitors of the fine CDAC have identical weights ($=$ C_2) to enable the use of DWA. The total capacitance of the fine CDAC seen at the output of the CDAC is $32C_2$. We use tunable capacitor arrays to compensate for the capacitor mismatches. $C_{L,cal}$ compensates for the mismatch of the bridge capacitor, and $C_{M,cal}$ compensates for the gain mismatch between the coarse CDAC and the fine CDAC.

3.2. Cascode Dynamic Amplifier

For a dynamic amplifier, the floating inverter amplifier (FIA) has become very popular [23–26]. However, it is difficult to produce the required gain of 40 v/v with the original structure of [23]. In [24], a two-stage cascaded FIA dynamic amplifier achieved a higher gain. However, the use of a multi-stage amplifier in a feedback structure raises the stability

issues inevitably. Recently, an FIA with cascode structure was introduced [25,26]. Because the cascode FIA can obtain a high gain without suffering from the stability issues, we use a cascode FIA to make the design simple and robust.

Figure 10 shows the schematic of the cascode FIA. When ϕ_{RST} is high, we reset the amplifier by connecting the input and the output terminals to V_{CM} = 0.5 V. We also charge the reservoir capacitor, C_R (=2 pF), to V_{DD}. After ϕ_{RST} becomes low, ϕ_1 becomes high, and the amplification starts. In the amplification stage, C_R is connected to the inverter structure and functions as a power supply. $M_{1(2)p}$ and $M_{1(2)n}$ are input transistors, and $M_{3(4)p}$ and $M_{3(4)n}$ are cascode transistors, which boost the gain of the FIA. The gates of the cascode devices are connected to V_{CM} to avoid using additional bias voltages. This is possible because the output swing of the amplifier is very small. Because we use an 8-bit SAR ADC as a quantizer, the residue voltage, which is used as the input of the FIA, is only a few tens of millivolts. As a result, the differential output voltage of FIA is limited to about 100 mV. Therefore, even when V_{CM} = 0.5 V is used as the bias voltage for the cascode transistors, the gate–drain voltage of the cascode transistors is limited to below 50 mV, and the cascode transistors are not forced to go into the triode region.

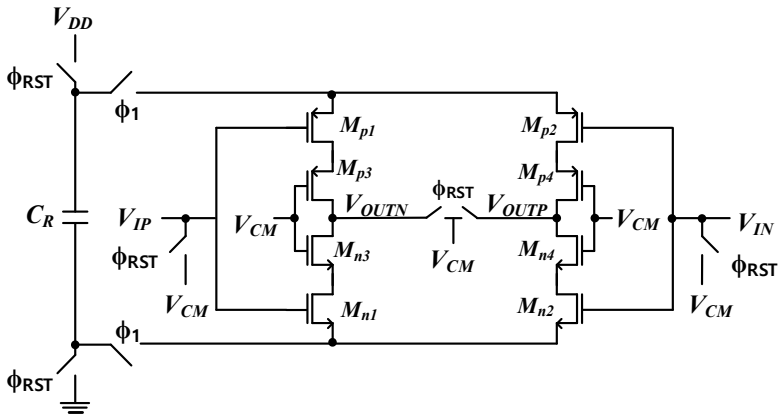

Figure 10. Schematic of the cascode FIA.

In Section 2, we determined that the open-loop gain of the amplifier should be larger than 30 v/v for a proper operation of the residue integrator. To verify that the designed amplifier has a large enough gain in the presence of device mismatches and process variation, we performed Monte Carlo simulations. Figure 11 shows the distribution of the open-loop gain obtained from the Monte Carlo simulations. The mean value of the gain is about 40 v/v, and the gain is almost always larger than 30 v/v, which is sufficient for the accurate closed-loop integration.

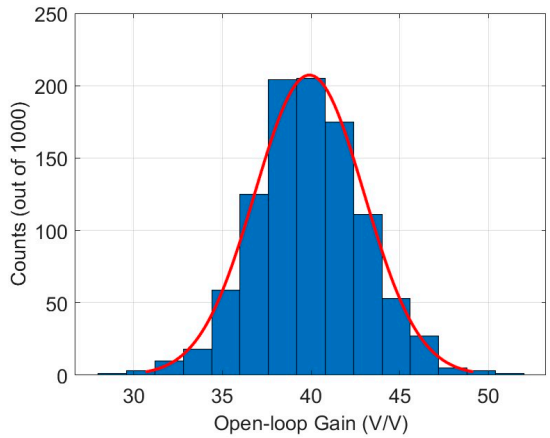

Figure 11. Simulated open-loop gain against process variations from Monte Carlo simulations (1000 runs).

3.3. Comparator

Figure 12 shows the schematic of the comparator with two input pairs designed in a StrongArm latch structure [17]. Of the two input pairs, V_{IP1} and V_{IN1} are connected to the output of the coarse CDAC, and V_{IP2} and V_{IN2} are connected to the output of the residue integrator. The widths of the input transistors for V_{IP2} and V_{IN2} are larger than those for V_{IP1} and V_{IN1} by a factor of g, which is the comparator gain ratio. We used $g = 1.8$, as mentioned in Section 2. The input-referred noise of the comparator determined by transient noise simulations using Spectre was 0.9 mV. It is noted that the input-referred noise of the comparator is shaped by the NTF of the NS-ADC and mostly removed from the signal band. Therefore, the noise performance of the ADC is not strict.

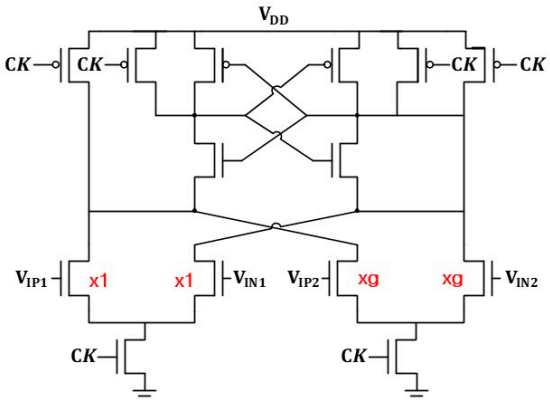

Figure 12. Schematic of the 2-input StrongArm latch comparator.

4. Results

The proposed NS-SAR ADC was implemented in a 28 nm CMOS process. It operates at the sampling rate of 80 MS/s, with a 1 V power supply. Figure 13 shows the output spectra of the NS-SAR ADC. The spectra were obtained by applying discrete Fourier transform (DFT) to the digital output of the ADC obtained from transient simulations using Spectre. The red and the blue lines represent the spectrum with and without noise, respectively. For a comparison, Figure 13 also shows the output spectrum of a simple SAR ADC without noise shaping. The SAR ADC is identical to that in the proposed NS-SAR ADC. The simulations including noise were performed using "transient noise simulation" of Spectre, using noise models provided in the process design kit (PDK). The noise bandwidth ($f_{max,noise}$) of 20 GHz was used, which was confirmed to be high enough after iterations with various noise bandwidths. The black dotted line represents the bandwidth of the proposed NS-SAR ADC.

In Figure 13, we can clearly observe the noise-shaping effect in the spectra from NS-SAR ADC. Whereas the noise from the simple SAR ADC is flat across the whole frequency band, the noise from NS-SAR ADC is clearly shaped by the first-order NTF. By integrating the noise in the bandwidth of the ADC, we can calculate SNDR. When the noise is included in the simulation, the SNDR of the NS-SAR ADC is reduced by 6.6 dB, which means that the thermal noise is about 3.5 times larger than the quantization noise in the signal band. This is a result of the low-power design approach, where the thermal noise dominates over the quantization noise.

Figure 14 shows the SNDR versus input amplitude from Spectre simulations. The maximum SNDR was 76.5 dB when the noise was not included in the simulations (blue circles). The red circles represent the SNDR from simulations including the noise. The ADC achieves a maximum SNDR of 71.2 dB.

Figure 15 shows the SNDR versus input frequency obtained from transient noise simulations. The SNDR performance hardly changes when the input frequency changes within the bandwidth of 4 MHz. The difference between the maximum and the minimum values of SNDR is only about 1.5 dB.

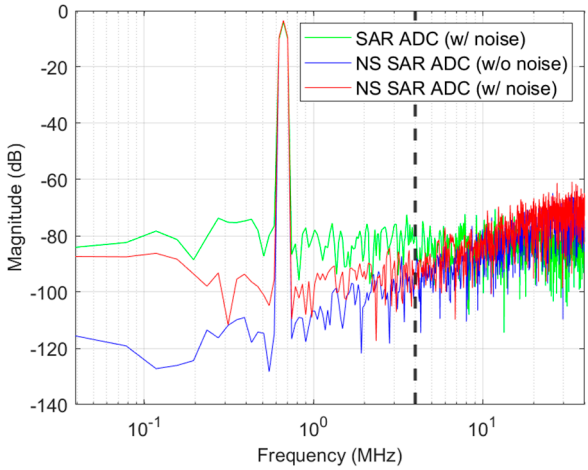

Figure 13. Output spectra obtained from Spectre transient simulations. Blue, NS-SAR ADC without noise; red, NS-SAR ADC with noise; green, SAR ADC with noise. Dashed line represents the signal bandwidth. (N_{fft} = 2048, V_{IN} = −0.3 dBFS, f_{sig} = 664 kHz, Hann windowing.)

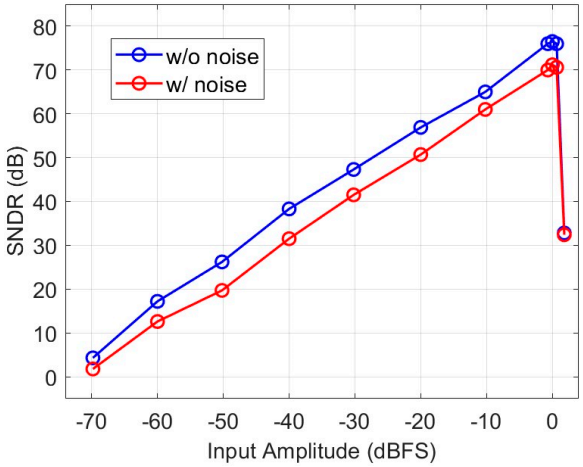

Figure 14. SNDR of the proposed ADC from Spectre transient simulations with and without noise.

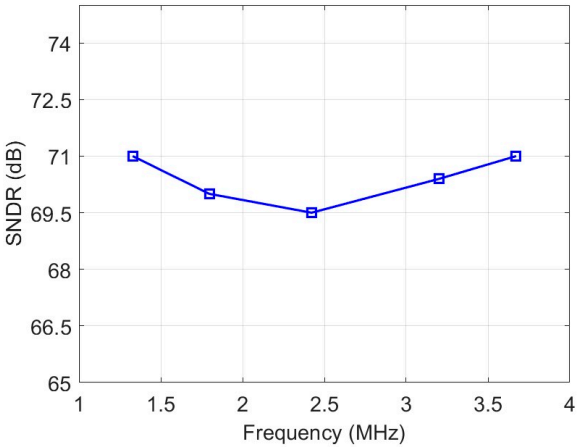

Figure 15. SNDR variation vs. input frequency obtained from Spectre transient noise simulations.

Figure 16 shows the SNDR variation from temperature and power supply variations. Simulations were repeated while changing the process corner conditions. Three corner conditions were simulated. In the legends, “tt”, “ff”, and “ss” represent corners. The first letter represents the nmos performance, and the second letter represents the pmos perfor-

mance. Moreover, "t", "f", and "s" represent "typical", "fast", and "slow", respectively. Figure 16a shows the SNDR variations obtained while changing the temperature. The *y*-axis represents the SNDR variation referenced to that at 30 °C. Figure 16b shows the SNDR variations versus the power supply voltage variation. We observe that the SNDR variation is only about 1 dB under the three corner conditions at all temperature and supply voltage changes.

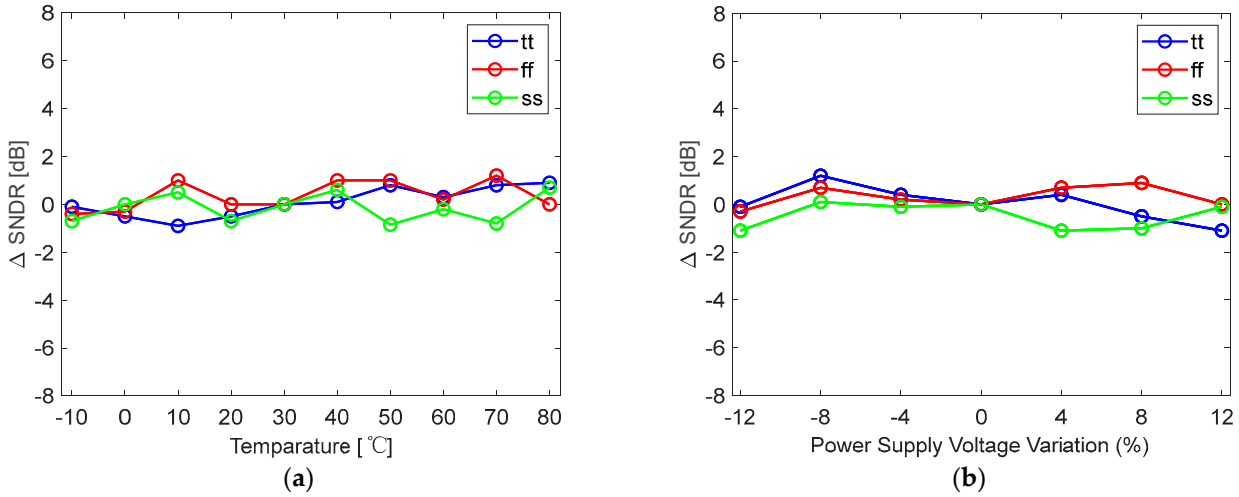

Figure 16. SNDR variation vs. (**a**) temperature and (**b**) power supply variations from Spectre transient noise simulations.

Table 1 represents the power consumption breakdown of the implemented ADC. Operating at the sampling rate of 80 MS/s with a 1-V supply, the proposed ADC consumes 228 µW, of which 50 µW, 43 µW, and 19 µW are consumed by the DWA logic, the CDACs, and the integrator, respectively.

Table 1. Power consumption.

Sub-Block	Power Consumption
Integrator	19 µW
DWA logic	50 µW
CDACs	43 µW
Comparator	18 µW
SAR logic	18 µW
Others	80 µW
Total	**228 µW**

Table 2 summarizes the performance of this work and compares it with existing NS-SAR ADCs. Compared to other works, this work has similar or better performance, realizing a Walden figure-of-merit (FoM) of 9.6 fJ/conv.-step and a Schreier FoM of 173.6 dB. The best two FoMs were obtained by [11,24], which used second-order noise shaping. We can also observe that the bandwidths of these two works are much smaller than those of others.

The silicon area of the proposed NS-SAR ADC is expected to be dominated by the noise-shaping part of the ADC. Our estimate indicates that about 30% of the area will be occupied by the core SAR ADC, including a coarse ADC, a comparator, a SAR logic, and a clock generator. The fine CDAC is expected to occupy about 55% of the total area. However, it should be noted that using two separate CDACs does not increase the chip area of the proposed NS-SAR ADC significantly. If a single CDAC is used for the SAR ADC operation and the residue generation operation, then the CDAC should have the large size of the fine CDAC in this work to satisfy the thermal noise and the mismatch requirement.

Table 2. Performance summary and comparison with prior works.

	[10]	[11]	[15]	[24]	This Work
Process (nm)	65	40	14	40	**28**
Power Consumption (μW)	806	84	1250	107	**228**
fs (MS/s)	90	10	320	10	**80**
OSR	4	8	4	8	**10**
NS order	1	2	1	2	**1**
BW (MHz)	11	0.625	40	0.625	**4**
SNDR (dB)	62	79	66.6	83.8	**71.2**
FoMw (fs/conv·step)	35.8	9	8.9 1	6.8	**9.6**
FoMs (dB)	163.3	178	171.7	181.5	**173.6**

5. Conclusions

This paper presented a first-order NS-SAR ADC equipped with a closed-loop integrator employing a dynamic amplifier. Thanks to the use of the closed-loop integrator, a sharp NTF could be obtained, resulting in a high SNDR. Typically, closed-loop integrators are more robust against PVT variations. However, they require amplifiers with high gains. In this work, a cascode floating inverter dynamic amplifier was employed to obtain a high gain and a low power consumption simultaneously. In this work, in addition to the CDAC used for the SAR operation itself, one more CDAC was used to generate the residue used in the noise shaping. The use of the second CDAC enabled the use of MES and improved the power efficiency. The performance of the NS-ADC proposed in this work was comparable to that of other state-of-the-art NS-ADCs. The Schreier FoM of 173.6 dB is among the best reported. Compared to other NS-ADC, the proposed design used first-order noise shaping, whereas the NS-ADCs with the best FoM employed second-order noise shaping. In the future work, we desire to improve on this. In conclusion, we designed a highly energy-efficient, robust, and high-performance NS-SAR ADC.

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