

Article

## Analysis and Design of a Higher Current ZVS-PWM Converter for Industrial Applications

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**Abstract:** A new auxiliary circuit that can be implemented in DC-DC and AC-DC ZVS-PWM converters is proposed in the paper. The circuit is for ZVS-PWM converters used in applications where high-frequency operation is needed and the load current is higher than that of typical ZVS-PWM converters. In the paper, the operation of a new ZVS-PWM converter is described, its steady-state operation is analyzed, and a procedure for its design is derived and then demonstrated. The feasibility of the new converter is confirmed by experimental results obtained from a prototype.

**Keywords:** DC-DC converter; zero voltage switching; boost converter; pulse width modulation

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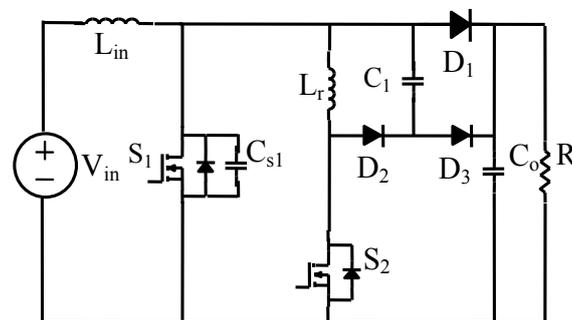
### 1. Introduction

Many techniques that use an active auxiliary circuit to help the main switch of a single-switch pulse-width modulated (PWM) converter turn on with zero-voltage switching (ZVS) have been proposed [1–27]. These techniques reduce switching losses in the main power switch, reduce reverse-recovery losses in the main power diode, and reduce EMI in the converter. The auxiliary circuit is typically placed parallel to the main switch (Figure 1), and is activated just before the main converter switch is to be turned on.

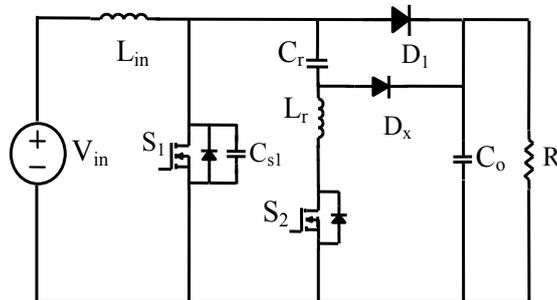
The circuit gradually diverts current away from the main power diode to eliminate diode reverse

recovery current after it is activated. It then discharges the capacitance across the main switch so that the switch can be turned on with ZVS. Finally, the circuit is deactivated from the main power circuit shortly after the main switch is turned on, so that the converter operates as a conventional PWM converter for the remainder of the switching cycle. The auxiliary circuit components have lower ratings than those in the main power circuit, as the circuit is active for only a small portion of the switching cycle. This allows a device that can turn on with fewer switching losses than the main switch to be used as the auxiliary switch.

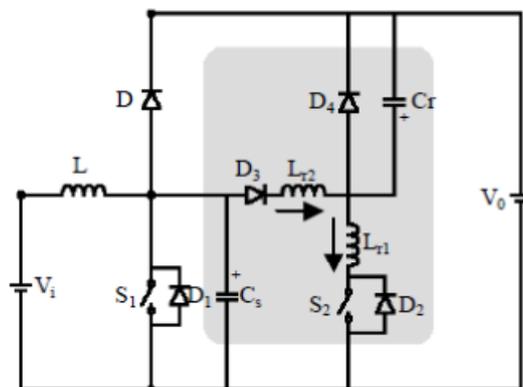
**Figure 1.** Zero-voltage switching (ZVS)-pulse-width modulated (PWM) boost converters with auxiliary circuits. (a) Non-resonant auxiliary circuit [1]; (b) Resonant auxiliary circuit [11]; (c) Dual auxiliary circuit [16].



(a)



(b)



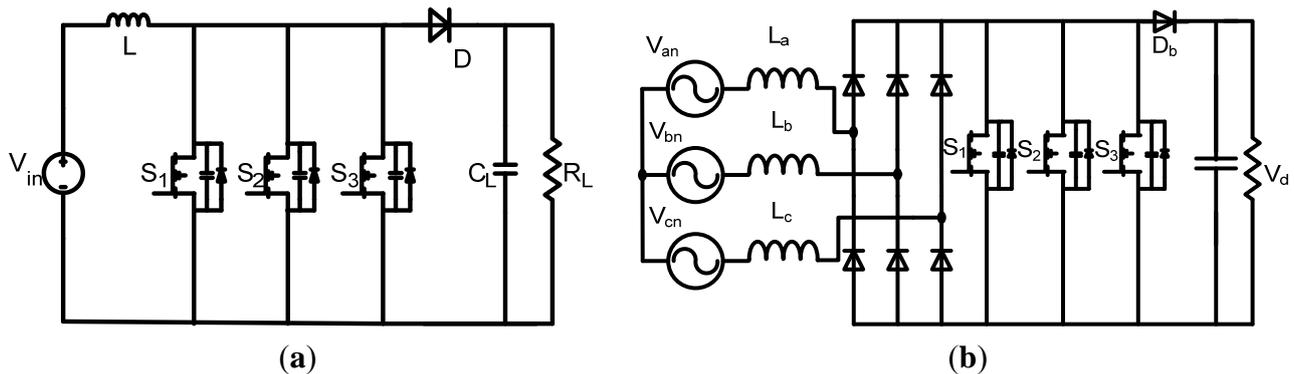
(c)

Previously proposed ZVS-PWM converters, however, have at least one of the following drawbacks:

- The auxiliary switch is turned off while it is conducting current, which generates switching losses and EMI that offset the benefits of the auxiliary circuit [1,5,7,10,13,14,22,23].
- The auxiliary circuit causes the main switch or boost diode to operate with higher peak current stress and more circulating current, which increases conduction losses and results in the need for a higher current-rated device for the main switch [2,3,6,8,11,12,15,21–23].
- The auxiliary circuit components have high peak voltage stresses (at least twice the output voltage) and/or current stresses [2,3,6,8,12].
- Energy from the output, which contributes to circulating current and losses, must be placed into the auxiliary circuit to trigger a resonant process [16,17].

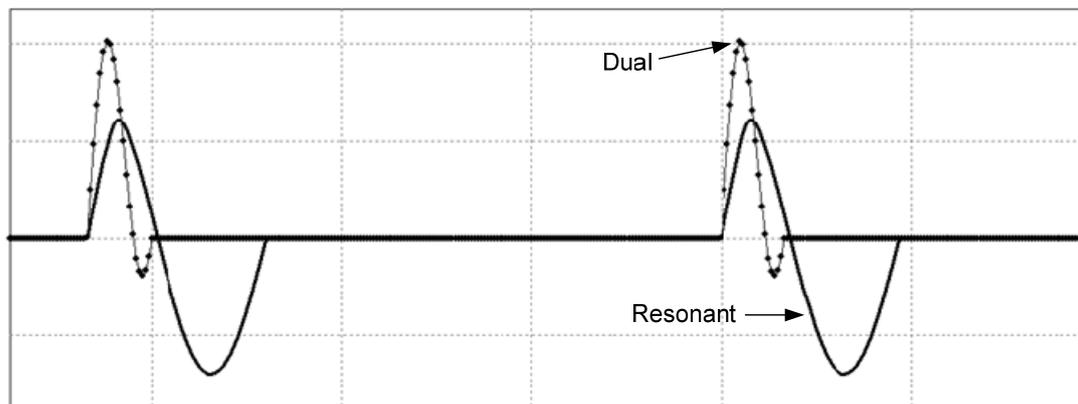
It is standard practice in industry to implement a PWM converter with several MOSFETs in parallel to reduce the on-state resistance of the main power switch and thus its conduction losses. Examples of such an implementation are shown in Figure 2a,b for a DC-DC PWM boost converter and a three-phase AC-DC converter respectively. Although using a single IGBT as the boost switch may be cheaper, IGBTs cannot operate with switching frequencies as high as those that MOSFETs can so that the size of the magnetic and filtering components (and thus the converter size) cannot be made as small. Small converter size is necessary for industrial applications such as telecom power converters that are part of power systems that are placed in cabinets where space is a major issue. An auxiliary circuit can be used to reduce switching losses in a paralleled MOSFET converter that operates with higher power and current, but the above-mentioned drawbacks become worse than what they are for lower power converters.

**Figure 2.** Converters with paralleled MOSFETs. (a) DC-DC boost converter; (b) Three-phase boost rectifier.



For example, the turn-off losses of the auxiliary switch in a converter with a non-resonant auxiliary circuit (*i.e.*, Figure 1a) are considerable. If resonant (Figure 1b and dual Figure 1c) approaches are used to ensure the soft turn-off of the auxiliary switch, then other problems arise, as can be seen from the auxiliary inductor waveforms shown in Figure 3. The negative part of the waveform for the Figure 1b circulates in the main switches and increases their peak stresses and conduction losses. The current waveform for the Figure 1c converter ( $I_{Lr1}$ ) has an extremely high peak, at least double the input current, which makes it difficult to find an appropriate device for the auxiliary switch to carry this current.

**Figure 3.** Typical auxiliary inductor current waveforms for ZVS-PWM boost converters operating with input voltage  $V_{in} = 100$  V, output voltage  $V_o = 400$  V, output power  $P_o = 2$  kW, and switching frequency  $f_{sw} = 100$  kHz. Scale:  $I = 20$  A/div., Time:  $t = 5$   $\mu$ s/div.

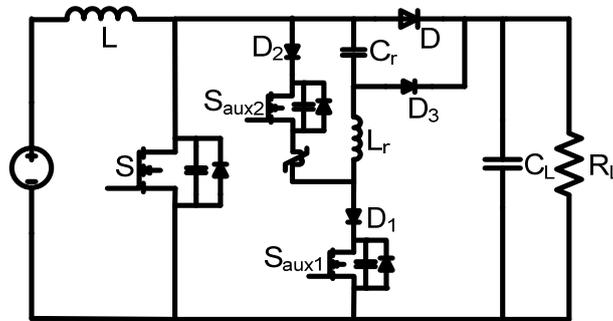


A new auxiliary circuit for ZVS-PWM converters that are implemented with paralleled MOSFETs for higher current applications is proposed in the paper. The circuit is shown in Figure 4. Although almost all previously proposed auxiliary circuits contain only a single active switch because of cost (it is difficult to justify a two-switch circuit in a converter with a single MOSFET as the power switch), the proposed auxiliary circuit can be justified on the following grounds:

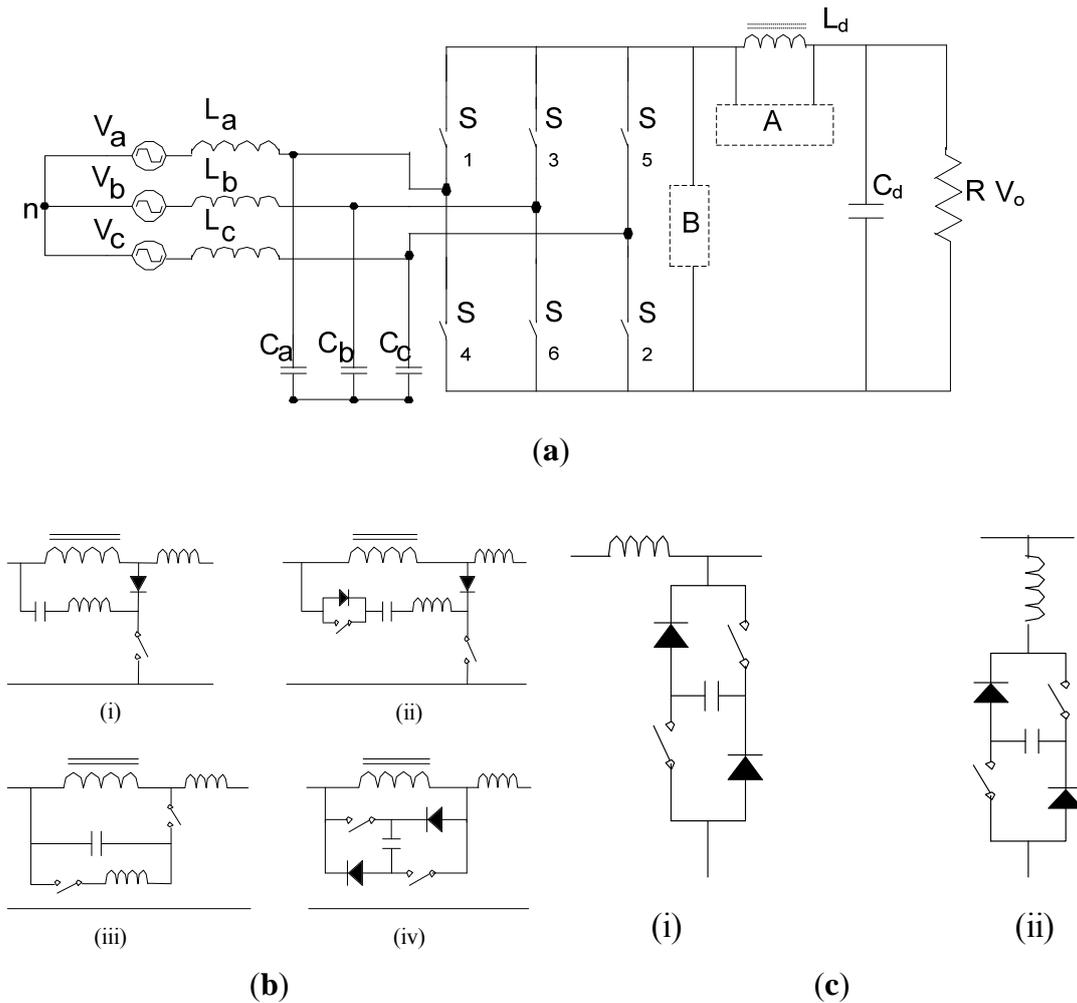
- Its performance is superior to all other single-switch auxiliary circuits for higher current applications because its switches can be turned off softly and it can operate with greater flexibility than single-switch resonant and dual auxiliary circuits. Resonant and dual auxiliary circuits have issues related to the timing of the operation of the auxiliary switch relative to that of the main power switch(es) as the time window of opportunity to turn the auxiliary switch softly varies considerably from light load to heavy load. In other words, ZVS-PWM converters with single-switch auxiliary circuits like the ones shown in Figure 1 are not suitable for higher current applications and should not be used for these applications.
- Cost is less of an issue and performance is the key criterion in applications where multiple MOSFETs are used. If the cost of multiple MOSFETs to improve performance can be justified for the power switch, then it can be justified in the auxiliary circuit.
- Two-switch auxiliary circuits for ZCS-PWM IGBT converters are commonly used in high current applications and there is a vast literature about them [19]. Most multi-switch auxiliary circuits for ZCS-PWM converters that have been proposed have been for three-phase buck-type rectifiers and three-phase current source inverters. In the case of a three-phase rectifier, as shown in Figure 5a, the auxiliary circuit can be placed either across the dc link inductor (Position A) or across the output of the bridge (Position B). Several multi-switch auxiliary circuits are shown in Figure 5b,c. Given that multi-switch auxiliary circuits are widely used in higher power ZCS-PWM applications to improve performance, the use of such circuits in higher

power ZVS-PWM applications where paralleled MOSFETs are used can be justified for the same reason.

**Figure 4.** Proposed DC-DC boost converter.



**Figure 5.** (a) Three-phase six-switch rectifier. (b) Various auxiliary circuit schemes for position A. (c) Various auxiliary circuit schemes for position B.



In the paper, the operation of the new converter is described, its steady-state operation is analyzed, and a procedure for its design is derived and then demonstrated with an example. The feasibility of the new converter is confirmed by experimental results obtained from a prototype converter.

## 2. Modes of Operation

The proposed converter in Figure 4 has an auxiliary circuit that consists of two switches,  $S_{aux1}$  and  $S_{aux2}$ , three diodes, and a resonant tank made of capacitor  $C_r$  and inductor  $L_r$ . The basic operating principles of the proposed circuit are as follows: Auxiliary switch  $S_{aux1}$  is turned on just before the main power switch  $S$  is to be turned on, thus diverting current away from the main power diode  $D$ . Once current has been completely diverted away from  $D$ , the output capacitances of the switch begin to discharge and the voltage across it eventually falls to zero. The main power switch can be turned on with ZVS as soon as the capacitance is fully discharged. Due to the  $C_r$ - $L_r$  resonant tank, the current in the auxiliary circuit naturally falls to zero, thus allowing  $S_{aux1}$  to turn off with ZCS.

Sometime during the switching cycle, while the main power switch is conducting the input current, auxiliary switch  $S_{aux2}$  is turned on. This action results in the voltage across  $C_r$  flipping polarity so that it is negative instead of positive. When the main power switch is turned off, the input current completely discharges  $C_r$  so that there is no voltage across it when the auxiliary circuit is reactivated sometime during the next switching cycle. Equivalent circuit diagrams of the modes of operation that the converter goes through during a switching cycle are shown in Figure 6, and typical converter waveforms are shown in Figure 7. To save on space, switches  $S_1$ ,  $S_2$ , and  $S_3$  are shown in Figure 6 as a single switch,  $S_{123}$ .

**Figure 6.** Modes of operation. (a) Model 0; (b) Model 1; (c) Model 2; (d) Model 3; (e) Model4; (f) Model 5; (g) Model 6; (h) Model 7; (i) Model 8; (j) Model 9.

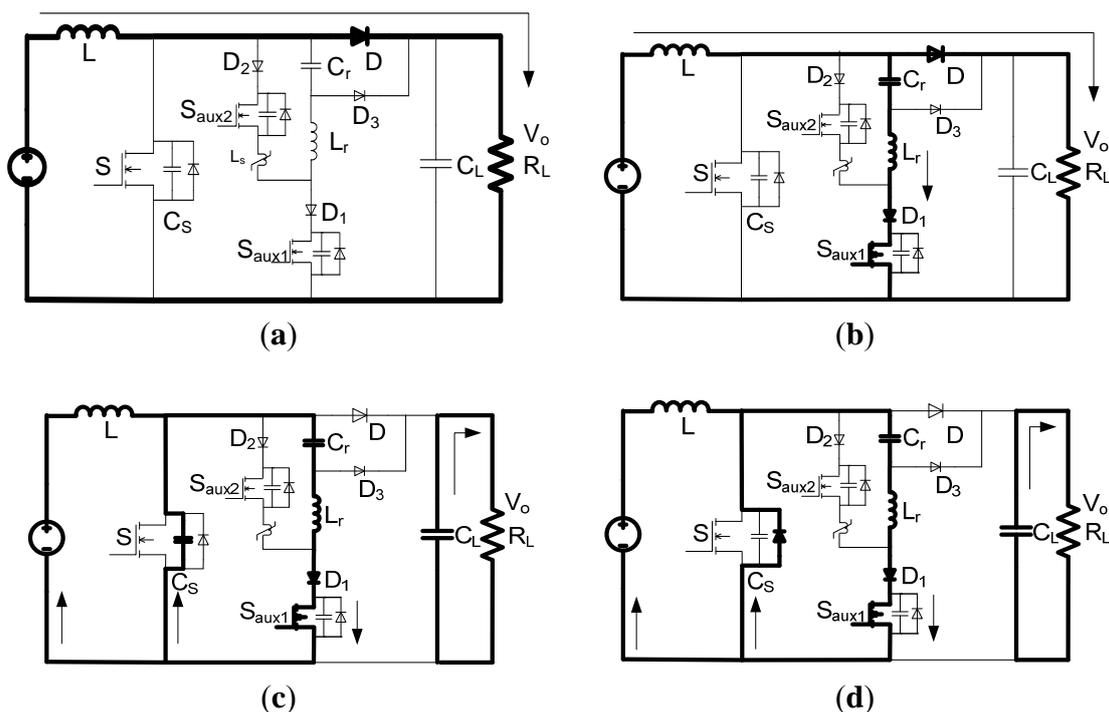


Figure 6. Cont.

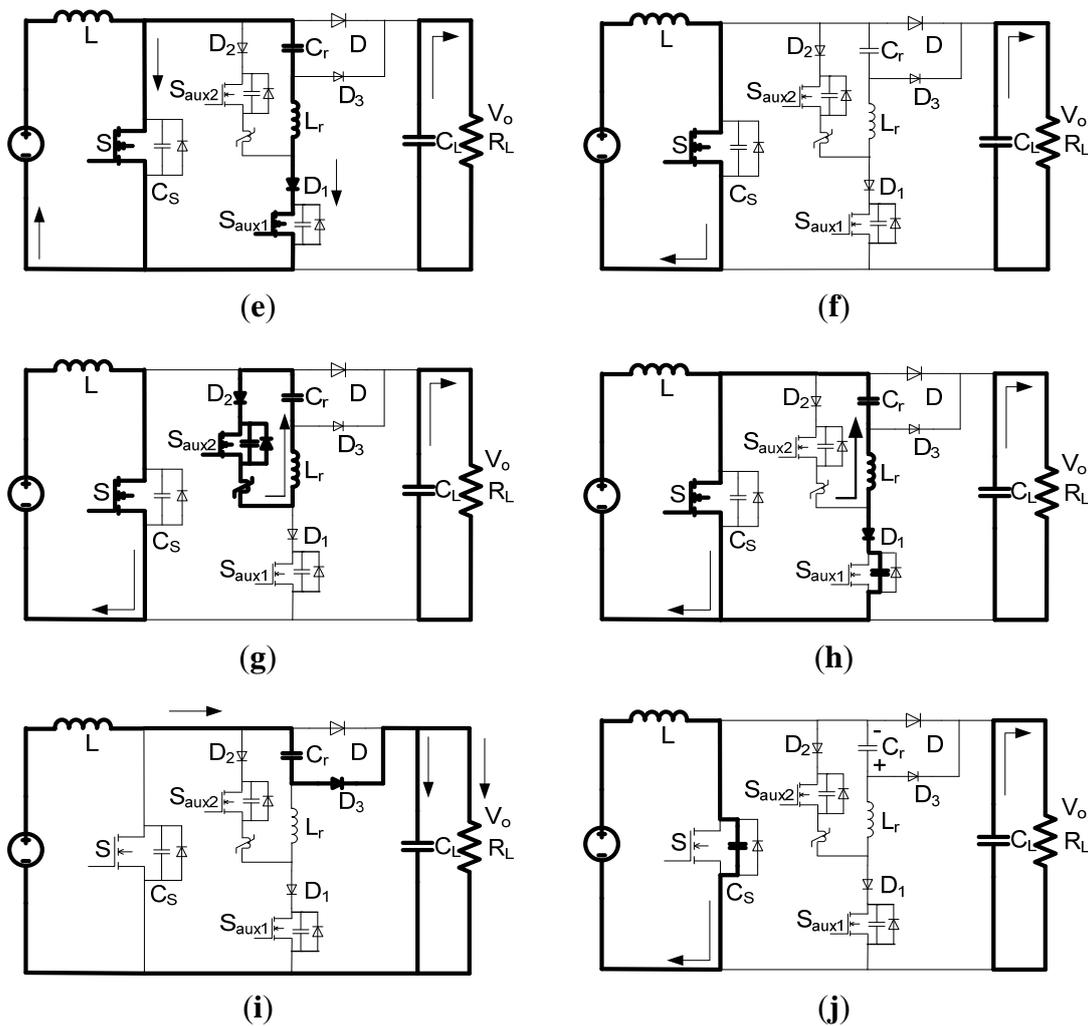
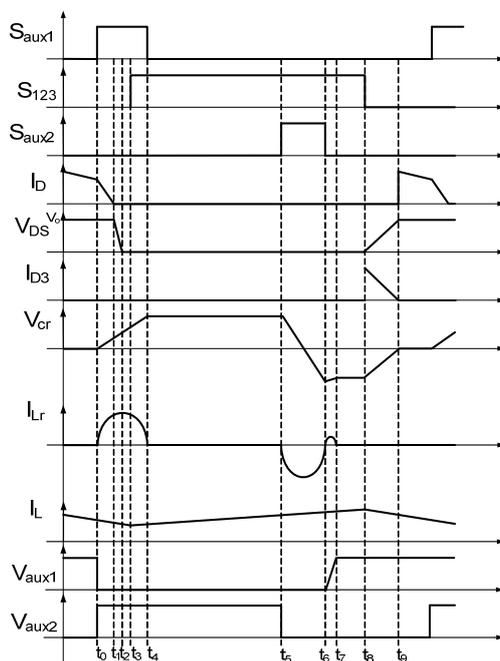


Figure 7. Typical waveforms.



The converter’s modes of operation are as follows:

*Mode 0* ( $t < t_0$ ): All converter switches are off during this mode and current is flowing through the main power diode D.

*Mode 1* ( $t_0 < t < t_1$ ): At  $t = t_0$ , switch  $S_{aux1}$  is turned on and current begins to be transferred away from diode D to the auxiliary circuit. This current transfer is gradual due to the presence of inductor  $L_r$  in the auxiliary circuit, so that charge is removed at a sufficiently slow rate to allow diode D to recover; this helps minimize reverse recovery current. The equations that represent the auxiliary circuit inductor current  $I_{Lr}$  and the auxiliary circuit capacitor voltage  $V_{Cr}$  in this mode are:

$$I_{Lr}(t) = \frac{V_o}{Z_1} \sin(\omega_1(t - t_0)) \tag{1}$$

$$V_{Cr}(t) = V_o - V_o \cos(\omega_1(t - t_0)) \tag{2}$$

where

$$Z_1 = \sqrt{\frac{L_r}{C_r}} \tag{3}$$

$$\omega_1 = \frac{1}{\sqrt{L_r C_r}} \tag{4}$$

and the initial values of  $I_{Lr}$  and  $V_{Cr}$  at the beginning of this mode are zero.

It should be noted that current can flow through the output capacitor of  $S_{aux2}$  after  $S_{aux1}$  is turned on. In order to minimize a sudden increase in current through this capacitor that can cause voltage spikes to appear, a saturable reactor or “spike-killer” inductor ( $L_s$ ) should be placed in series with  $S_{aux2}$ .

*Mode 2* ( $t_1 < t < t_2$ ): At  $t = t_1$ , current stops flowing through the main power diode D and the net capacitance across  $S_{123}$  begins to be discharged through  $L_r$  and  $C_r$ . The current in the auxiliary circuit is the sum of the input current and the current due to the discharging of the capacitances across  $S_{123}$ . The equations that describe the auxiliary circuit inductor current  $I_{Lr}$ , the voltage across  $S_{123}$ ,  $V_{Cs}$ , and the auxiliary circuit capacitor voltage  $V_{Cr}$  in this mode are:

$$I_{Lr}(t) = \frac{V_1}{Z_2} \sin(\omega_2(t - t_1)) + I_1 \cos(\omega_2(t - t_1)) - I_1 + I_{Lr}(t_1) \tag{5}$$

$$V_{Cs}(t) = \frac{C}{C_s} [V_1 \cos(\omega_2(t - t_1)) - V_1 + V_o + I_1 Z_2 \sin(\omega_2(t - t_1))] + \frac{I_{Lm}}{C_r + C_s} (t - t_1) \tag{6}$$

$$V_{Cr}(t) = -\frac{C}{C_s} [V_1 \cos(\omega_2(t - t_1)) + V_{Cr}(t_1) - I_1 Z_2 \sin(\omega_2(t - t_1)) - V_1] + \frac{I_{Lm}}{C_r + C_s} (t - t_1) \tag{7}$$

where

$$I_1 = I_{Lr}(t_1) - \frac{C}{C_s} I_{Lm} \tag{8}$$

$$V_1 = V_o - V_{Cr}(t_1) \tag{9}$$

$$C = \frac{C_r C_s}{C_s + C_r} \tag{10}$$

$$Z_2 = \sqrt{\frac{L_r}{C}} \tag{11}$$

$$\omega_2 = \sqrt{\frac{1}{L_r C}} \tag{12}$$

During this mode, the auxiliary circuit inductor current  $I_{Lr}$ , reaches its peak when  $V_{Cs} - V_{Cr} = 0$  and it is equal to the peak current of  $S_{aux1}$  so that

$$I_{Lr,P} = \frac{\sqrt{V_1^2 + (I_1 Z_2)^2}}{Z_2} + \frac{C}{C_s} I_{Lm} \tag{13}$$

*Mode 3* ( $t_2 < t < t_3$ ): At  $t = t_2$ , the capacitance across the main power switches is completely discharged and current begins to flow through the body diodes of the devices; this allows the switches to be turned on with ZVS. The equations that describe the auxiliary circuit inductor current  $I_{Lr}$  and the auxiliary circuit capacitor voltage  $V_{Cr}$  in this mode are:

$$I_{Lr}(t) = I_2 \cos(\omega_1(t - t_2)) - \frac{V_2}{Z_1} \sin(\omega_1(t - t_2)) \tag{14}$$

$$V_{Cr}(t) = I_2 Z_1 \sin(\omega_1(t - t_2)) + V_2 \cos(\omega_1(t - t_2)) \tag{15}$$

where

$$I_2 = \sqrt{\frac{L_r I_{Lr,P}^2 - C_r V_2^2}{L_r}} \tag{16}$$

$$V_2 = \frac{I_{Lm}}{C_r} (t_2 - t_1) + \frac{C_s}{C_r} V_o + V_{Cr}(t_1) \tag{17}$$

*Mode 4* ( $t_3 < t < t_4$ ): At  $t = t_3$ , the current that was flowing in the body diodes of the main power switches in the previous mode reverses direction and begins to flow through the switches. The modal equations of this mode are the same as those of the previous mode except that the direction of the current through the main power switches is different.

*Mode 5* ( $t_4 < t < t_5$ ): Current stops flowing in the auxiliary circuit at  $t = t_4$  due to the resonant interaction between  $L_r$  and  $C_r$ . Switch  $S_{aux1}$  can be turned off softly with zero-current switching (ZCS) sometime soon afterwards. The converter then operates like a standard PWM boost converter. The voltage across  $C_r$  remains fixed until  $S_{aux2}$  is turned on later in the switching cycle.

*Mode 6* ( $t_5 < t < t_6$ ): At  $t = t_5$ , auxiliary switch  $S_{aux2}$  is turned on, sometime before the main power switches are turned off. As a result, capacitor  $C_r$  begins to discharge through  $L_r$ ,  $S_{aux2}$  and  $D_2$ , and the

voltage that was across it at the start of the mode changes polarity. At the end of this mode, the current in  $C_r$  and  $L_r$  is zero so that  $S_{aux2}$  can be turned off with ZCS. The equations that define this mode are:

$$V_{Cr}(t) = V_{Cr}(t_5) \cos(\omega_3(t - t_5)) \tag{18}$$

$$I_{Lr}(t) = I_{Lr,p} \sin(\omega_3(t - t_5)) \tag{19}$$

*Mode 7* ( $t_6 < t < t_7$ ): The output capacitance of  $S_{aux1}$  needs to be charged after this switch has been turned off so that current continues to flow through  $L_r$  and  $C_r$ . The length of this mode is negligible compared to the length of the other modes given that the output capacitance of  $S_{aux1}$  is much smaller than  $C_r$ , but the voltage across  $C_r$  can be changed during this mode. The voltage across  $S_{aux1}$  during this mode can be expressed as

$$V_{Aux1}(t) = Z_2 \cos(\omega_4(t - t_6)) + Z_3 \tag{20}$$

where

$$Z_2 = -\frac{V(t_6)}{\omega_4^2 C_1 L_r} \tag{21}$$

$$Z_3 = -Z_2 \tag{22}$$

$$\omega_4 = \frac{1}{\sqrt{C_1 L_r}} \tag{23}$$

$$C_1 = \frac{C_r C_{aux1}}{C_r + C_{aux1}} \tag{24}$$

It should be mentioned that if the output capacitance of  $S_{aux1}$  is charged to less than the output voltage  $V_o$  during this mode, then it would be charged up to  $V_o$  during Mode 9 when the main power switches turn off.

*Mode 8* ( $t_7 < t < t_8$ ): During this mode, the main power switches are still on and current in the input inductor rises.

*Mode 9* ( $t_8 < t < t_9$ ): At  $t = t_8$ , the main power switches are all turned off. The voltage of the net capacitance across the main power switches is

$$V_S(t) = V_o - V_{Cr}(t) \tag{25}$$

As a result, the auxiliary circuit capacitor  $C_r$  begins to be discharged as the net capacitance across the main switches continues to be charged; the energy stored in  $C_r$  is transferred to the output during this mode. The mode ends at  $t = t_9$  and the converter enters Mode 0, where it remains until  $S_{aux1}$  is turned on.

### 3. Steady-State Characteristics

The modal equations that are derived in the previous section of the paper can be used to generate steady-state characteristic curves that can be used to see the effect of certain key parameters on the operation of the auxiliary circuit. These key parameters include the values of auxiliary circuit components  $L_r$  and  $C_r$  and the net capacitance across the main power switches,  $C_s$ . Examples of such graphs are shown in Figure 8. Each graph has been generated by keeping certain parameters constant,

then varying other parameters to see the effect of doing so.

**Figure 8.** Characteristic curves. (a) Graph of characteristic curves of  $V_{cr}$  vs.  $L_r$  for different values of  $C_s$  with  $C_r = 50$  nF; (b) Graph of characteristic curves of  $I_{Lr}$  vs.  $L_r$  for different values of  $C_s$  with  $C_r = 50$  nF; (c) Graph of characteristic curves of  $I_{Lr}$  vs.  $L_r$  for different values of  $C_s$  with  $C_r = 50$  nF; (d) Graph of characteristic curves of  $V_{aux1}$  vs.  $L_r$  for different values of  $C_r$  with  $C_s = 2$  nF.

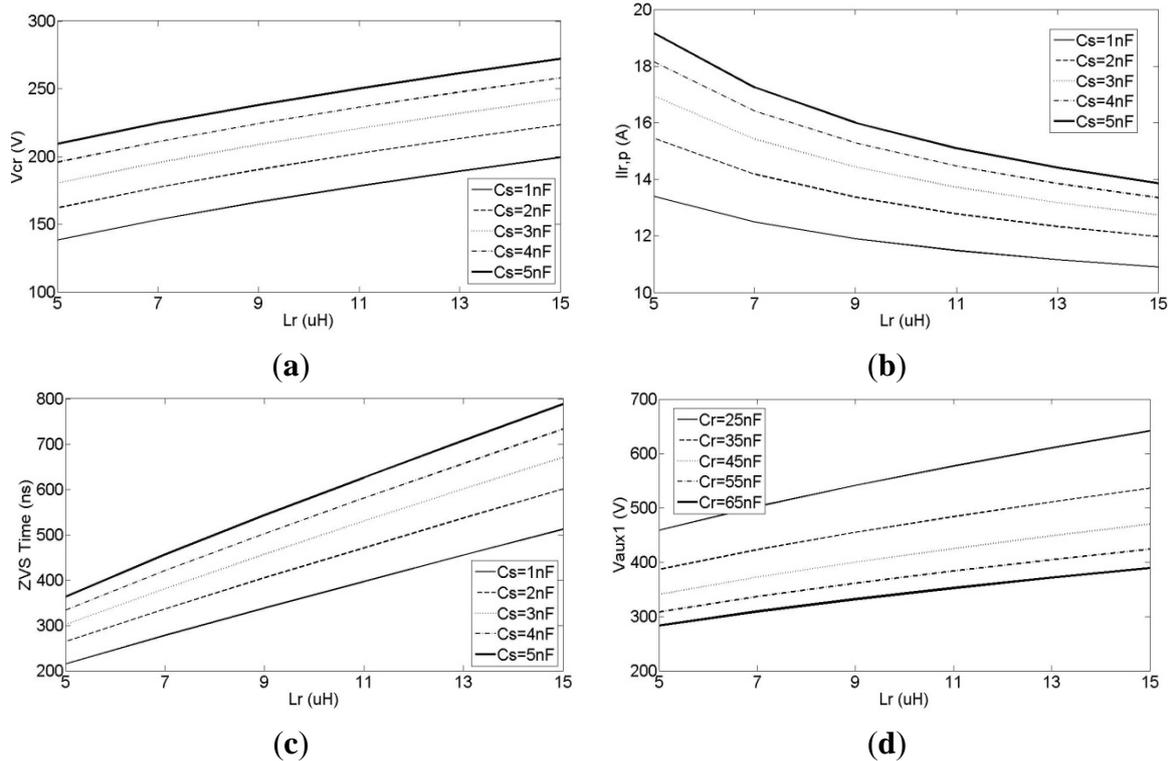


Figure 8a is a graph of  $V_{cr}$  vs.  $L_r$  for different values of  $C_s$  with  $C_r = 50$  nF. This graph shows that  $V_{cr}$  increases as either  $C_s$  or  $L_r$  is increased. The first characteristic can be explained by noting that increasing  $C_s$  increases the amount of energy that is discharged into the auxiliary circuit and is stored in  $C_r$  after the main power diode stops conducting. More energy in  $C_r$  results in higher values of  $V_{cr}$ . On the other hand, according to (4) and (12), higher values of  $L_r$  increase the time duration between  $t_0$  and  $t_2$ ; therefore, more energy is transferred to  $C_r$ , which leads to higher values of  $V_{cr}$ .

Figure 8b is a graph of characteristic curves of  $I_{Lr}$  vs.  $L_r$  for different values of  $C_s$  with  $C_r = 50$  nF. This graph shows that when  $C_s$  increases, more energy is stored in  $C_r$ , which results in higher peak values for  $I_{Lr}$ . Moreover, when  $L_r$  increases, it extends the resonant cycle and reduces the peak value of  $I_{Lr}$ . The average value of the resonant current is related to  $C_s$  and load current and is independent of length of the resonant cycle and the peak of the resonant current.

Figure 8c shows a graph of characteristic curves of ZVS time values vs.  $L_r$  for different values of  $C_s$  with  $C_r = 50$  nF. These time values are when the net capacitance across the main power switches is completely discharged after  $S_{aux1}$  is turned on and is measured from the turn-on instant of this switch. The graph shows that the ZVS times increase as  $L_r$  or  $C_r$  increases. Increasing  $L_r$  increases the time needed for current to be transferred away from the main power diode and it also increases the resonant

cycle of the auxiliary circuit. On the other hand, by increasing  $C_S$ , the amount of stored energy in this capacitor increases and, therefore, it takes more time for it to be discharged.

Figure 8d shows a graph of characteristic curves of  $V_{aux1}$  vs.  $L_r$  for different values of  $C_r$  when  $C_S = 2$  nF. It can be seen that increasing  $L_r$  increases the maximum voltage across  $S_{aux1}$ . Before  $D_1$  goes off after Mode 7 and  $V_{aux1}$  becomes constant,  $V_{aux1}$  is

$$V_{aux1} = V_{cr} + L_r \frac{di_{Lr}}{dt} \tag{26}$$

Equation (26) shows that  $V_{aux1}$  is increased by increasing  $L_r$ . Also, for the same amount of energy transferred to  $C_r$ , increasing  $C_r$  reduces the voltage across it and thus reduces  $V_{aux1}$  as well.

#### 4. Design Procedure and Example

Steady-state characteristic curves like the ones shown in Figure 8 can be used to develop a procedure that can be used to select key component values. Such a procedure is developed in this section of the paper. The procedure shown here will not consider the design of the main boost power circuit as the design of a standard PWM boost converter is well-known—this includes the selection of the number and the type of device to be used for the main power switches. Moreover, it will be assumed that the net output capacitance across the paralleled main power devices is sufficient to slow down the rise in voltage across them after turn-off so that additional external capacitance is not needed.

##### 4.1. Selection of Auxiliary Circuit Inductor $L_r$

The minimum value of  $L_r$  is determined by the inductor’s ability to limit the reverse recovery current of the main power boost diode. The reverse recovery current of this diode can be significantly reduced if the transition of current away from the diode to the auxiliary circuit is made to be gradual. The rate of current transfer is dependent on the value of  $L_r$  so that the larger the value of  $L_r$  is, the less recovery current there will be.

According to [20], an approximate rule of thumb that can be used for the determination of a minimum value of  $L_r$  is to make the current transfer time to be at least three times the reverse recovery time of the diode,  $t_{rr}$ . This can be expressed as

$$L_r \geq 3 \frac{t_{rr} V_{Lr}}{I_D} \tag{27}$$

where  $V_{Lr}$  is the voltage across boost inductor when  $S_{aux1}$  is turned on, and  $I_D$  is the amount of current that passes through boost diode and that should be diverted into the auxiliary circuit.

It should be noted that the voltage across  $C_r$  is zero at the time that  $S_{aux1}$  is turned on so that  $V_{Lr}$  is equal to the output voltage  $V_o$  at this moment. As current is transferred to the auxiliary circuit,  $V_{cr}$  changes as does  $V_{Lr}$  so that it is no longer equal to  $V_o$ . It is assumed in (27) that  $C_r$  is sufficiently large so that the change in  $V_{cr}$  and thus in  $V_{Lr}$  is small during the current transfer time.

Another thing to note about the value of  $L_r$  is that it cannot be too large. Very large values of  $L_r$  can result in increased peak voltage stresses in  $S_{aux1}$  and can increase the time required to discharge the net

capacitances across the paralleled main switches, according to the graphs in Figure 8. As a result, the value of  $L_r$  should be close to the determined minimum value.

#### 4.2. Selection of Auxiliary Circuit Capacitor $C_r$

If the value of  $C_r$  is too small, then the peak voltage stress of diode  $D_3$  increases which is equal to  $V_o + V_{Cr,P}$  where

$$V_{Cr,P} = \sqrt{\frac{L_r I_{Lr}(t_4)^2}{C_r} + V_{Cr}(t_4)^2} \quad (28)$$

If the value of  $C_r$  is too large, however, then the length of time needed to change the polarity of  $C_r$  after  $S_{aux2}$  may become excessive and thus place a limit on the acceptable range of duty cycle  $D$  that the main switches can operate with. A trade-off must be considered when selecting a value for  $C_r$  and the extent of this trade-off can be determined from steady-state characteristic curves like the ones shown in Figure 8.

#### 4.3. Selection of Auxiliary Switches $S_{aux1}$ and $S_{aux2}$

The maximum voltage across  $S_{aux1}$  is shown in Figure 8d and this switch should handle maximum drain-source voltage equal to 500 V. Maximum voltage across  $S_{aux2}$  is the output voltage  $V_o$ . The peak current of these switches can be found from graphs of steady-state characteristic curves like the one shown for  $I_{Lr}$  in Figure 8b.

#### 4.4. Design Example

The following example is given to clarify the design procedure. The converter is to be designed according to the following specifications: Input voltage  $V_{in} = 75$  Vdc, output voltage  $V_o = 375$  Vdc, maximum output power  $P_{o,max} = 700$  W, and switching frequency  $f_s = 100$  kHz. The devices that are to be used in the main power circuit are two paralleled IRFP460 MOSFETs for the main power switch and a 15ETX06 device for the main power diode. It will be assumed that the efficiency of the converter is about 90%, that  $C_S = 2$  nF, and the reverse recovery time of the main boost diode is  $t_{rr} = 75$  ns and that the maximum voltage across  $S_{aux1}$  is not be more than 450 V so that a 500 V MOSFET device can be used for this switch.

The steps of the procedure are as follows:

- (1) Based on above-mentioned characteristics of the converter, the current of the boost inductor when  $S_{aux1}$  turns on is

$$I = \frac{P_o}{V_{in}\eta} (1 - \Delta I_{in,rip}) = \frac{700}{75 \cdot 0.90} (1 - 0.2) = 8.3 \text{ A} \quad (29)$$

- (2) The value of  $L_r$  can be fixed by using (27)

$$L_r = \frac{3(75 \text{ ns})}{8.3} (300 \text{ V}) = 8.13 \text{ } \mu\text{H} \quad (30)$$

Referring to Figure 8a, in order to keep the value of  $V_{cr}$  less than 200 V, the value of  $L_r$  should not be more than 8.2  $\mu\text{H}$ . The maximum reverse voltage across  $D_3$  is  $V_o + V_{cr}$ , which is

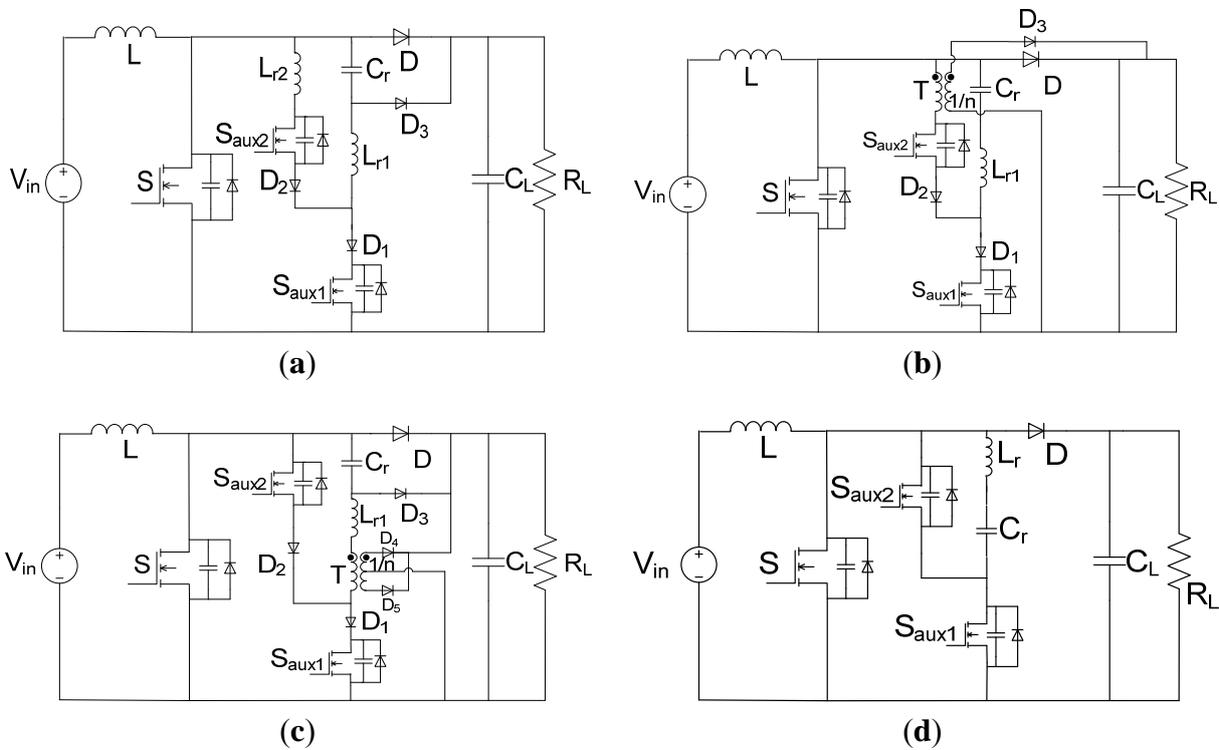
$$V_{r,max D3} = V_o + V_{cr,P} = 375 + 300 = 575 \text{ V} \tag{31}$$

- (3) Referring to Figure 8c, the ZVS time with the selected  $C_r$  and  $L_r$  is 450 ns. This is the time window during which the main power switches can be turned on with ZVS.
- (4) Referring to Figure 8b, with the selected value for  $L_r$  and output capacitance of the main switches which is 2 nF, the peak current in  $L_r$  is 15 A. This means that the auxiliary switches should be able to handle this peak current.
- (5) Figure 8d shows that if the  $L_r$  is 8.2  $\mu\text{H}$ ,  $C_r$  should be less than 45 nF to keep the maximum voltage across  $S_{aux1}$  about 450 V, which allows MOSFETS with maximum drain-source voltage equal to 500 V to be used as  $S_{aux1}$ . It should be noted that maximum voltage of  $S_{aux2}$  is equal to output voltage.

**5. Variations of the Auxiliary Circuit**

The basic structure of the new auxiliary circuit can be modified in several ways, either to improve performance or to reduce cost. Several of these modified circuits are shown in Figure 9.

**Figure 9.** Modified structures of new aux circuit.



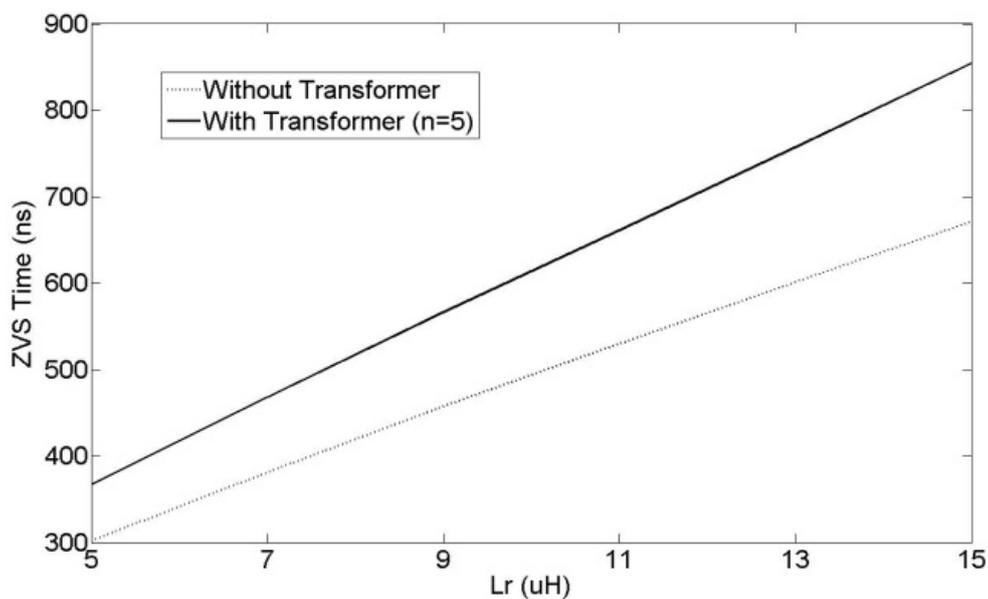
The circuit shown in Figure 9a is an auxiliary circuit that has a different resonant inductance when auxiliary switch  $S_{aux2}$  is conducting current than when  $S_{aux1}$  is conducting current. Having the resonant inductance be different under these two sets of circumstances allows the resonant inductance to be tailored to achieve the best performance for each set of circumstances.

The circuits shown in Figure 9b,c are auxiliary circuits with transformers in them. The presence of a transformer in the auxiliary circuit helps reduce circulating current losses after  $S_{aux2}$  has been turned on. The transformer allows energy to be transferred from the auxiliary circuit to the load instead of it just being trapped in the auxiliary circuit, where it contributes to losses. Moreover, the presence of a transformer in the auxiliary circuit makes the design of this circuit more flexible as it provides an additional degree of freedom.

The circuit shown in Figure 9d is a simplified version of the basic auxiliary circuit. The circuit has been simplified by Figure 4. What this does is to make current continuously flow in the auxiliary circuit inductor. Since this can happen, auxiliary circuit conduction losses may increase. This circuit variation can be considered for lower currents if it is desired to save on the cost of two diodes.

Figure 10 shows a graph of ZVS time interval vs. auxiliary circuit inductor value for the basic auxiliary and for the circuit in Figure 9c, implemented with an auxiliary circuit transformer turns ratio of  $n = N_2/N_1 = 5$ . It can be seen that implementing the auxiliary circuit with a transformer can result in extending the amount of time that is available for the main converter switches to turn on with ZVS. This allows for greater flexibility in the design and the performance of the converter.

**Figure 10.** Graph of characteristic curves of ZVS time values vs.  $L_r$  for different values of  $n$  with  $C_r = 50$  nF and  $C_s = 3$  nF.



## 6. Experimental Results

An experimental proof-of-concept prototype of the proposed converter was built to confirm its feasibility. The converter was built according to the same specifications as in the design example with input voltage  $V_{in} = 70$  V, output  $V_o = 375$  V, maximum output power  $P_{o,max} = 700$  W and switching frequency  $f_{sw} = 100$  kHz. The main power boost circuit was implemented as described in the design example. IRFP840 MOSFETs were used for the two auxiliary switches and 15ETX06 diodes for diodes  $D_1, D_2, D_3$ . The values of  $L_r$  and  $C_r$  were  $L_r = 8.2$   $\mu$ H and  $C_r = 44$  nF.

Typical experimental waveforms are shown in Figure 11. Figure 11a,b shows the current waveform of  $L_r$ ,  $I_{Lr}$ , and the gating signals of the two auxiliary switches. Since the positive part of  $I_{Lr}$  and the negative part of  $I_{Lr}$  represent the currents through  $S_{aux1}$  and  $S_{aux2}$  respectively, it can be seen that both switches can be turned off softly with ZCS. Figure 11c shows the gating signal and the drain source voltage of a main power switch. It can be seen that the switch turns on with ZVS, as the voltage across the switch is zero before it is turned on. Figure 11d shows the auxiliary inductor current and capacitor voltage waveforms. It can be seen that whatever energy is placed in  $C_r$  is removed before the auxiliary circuit is reactivated.

**Figure 11.** Experimental waveforms. (a) Upper Signal: Gating signal  $V_{GS}$  of  $S_{aux1}$  ( $V = 20$  V/div.) Lower Signal: Current of  $L_r$  resonant inductor ( $I = 5$  A/div.) Time:  $t = 2.5$   $\mu$ s/div. (b) Upper Signal: Current of  $L_r$  ( $I = 5$  A/div.) Lower Signal: Gating signal  $V_{GS}$  of  $S_{aux2}$  ( $V = 10$  V/div.) Time:  $t = 2.5$   $\mu$ s/div. (c) Upper Signal:  $V_{GS}$  of main switch ( $V = 10$  V/div.) Middle Signal: Current of  $L_r$  ( $I = 5$  A/div.) Lower Signal:  $V_{DS}$  of main switch ( $V = 200$  V/div.) Time:  $t = 2.5$   $\mu$ s/div. (d) Upper Signal: Current of  $L_r$  ( $I = 5$  A/div.) Lower Signal: Voltage of  $C_r$  ( $V = 100$  V/div.) Time:  $t = 2.5$   $\mu$ s/div.

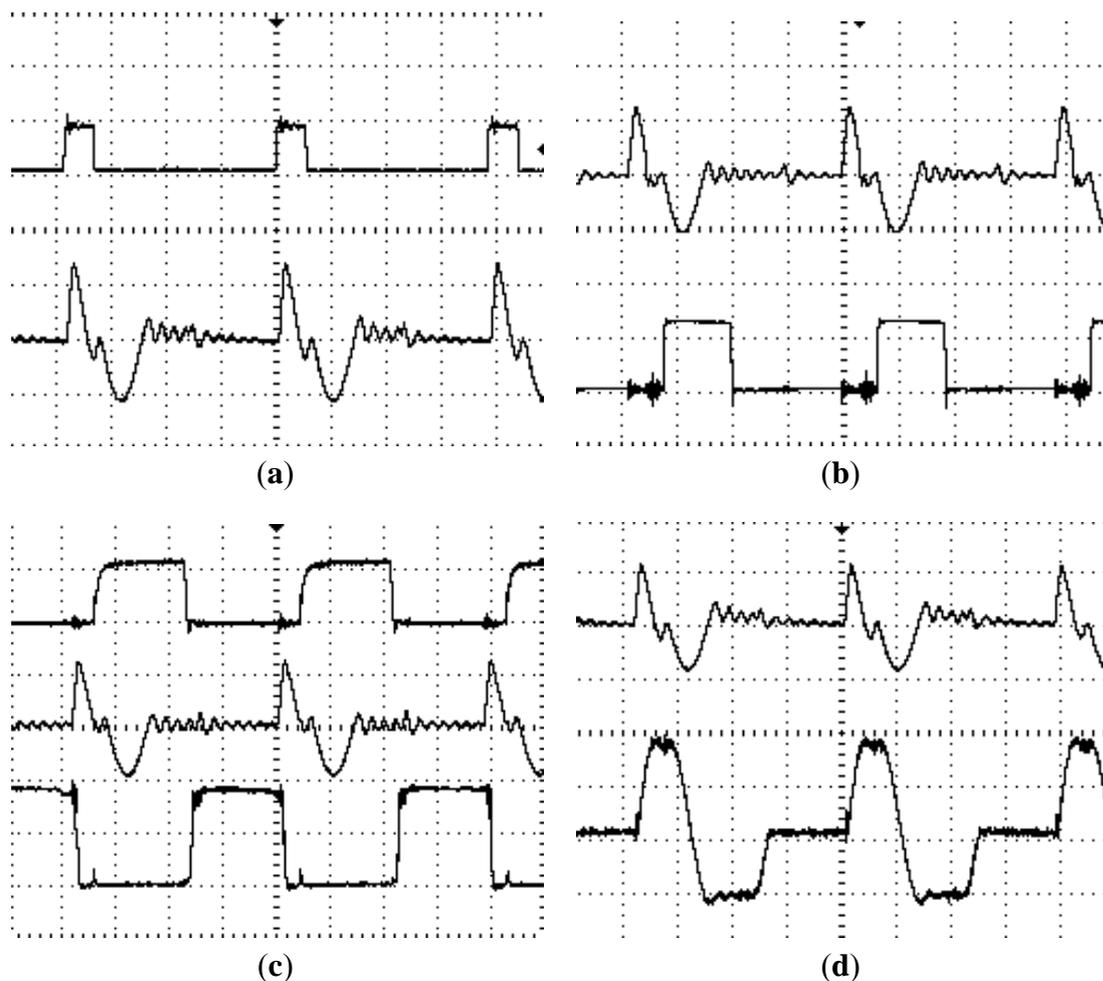
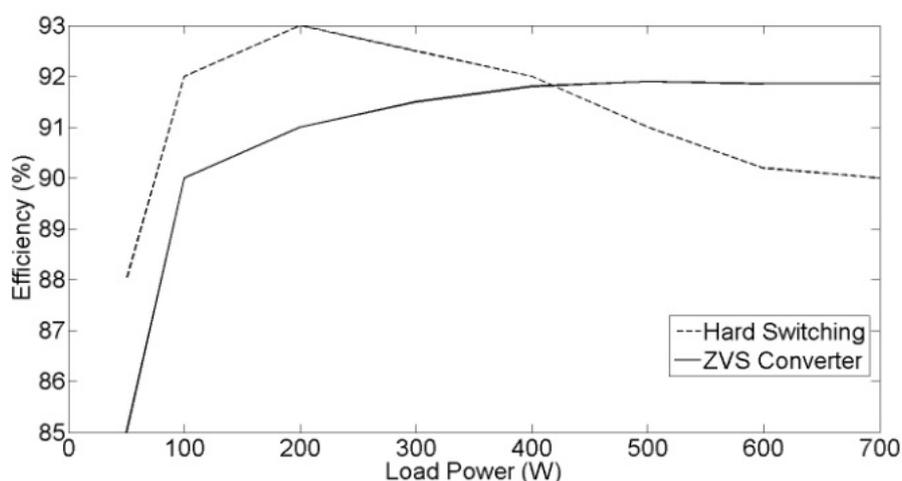


Figure 12 shows a graph of converter efficiency vs. load for the cases of the prototype with and without the basic auxiliary circuit. It can be seen that the converter efficiency dips sharply when the converter is operating with a heavy load while this does not happen when the converter has the basic

auxiliary circuit. The comparison was limited to 700 W as the efficiency of the hard-switched converter becomes very poor past this point, while this is not the case for the ZVS converter. The reason for the sharp fall off in efficiency is the fact that the converter was operated with a high input current—higher than what is normally considered for a boost converter [15]. High current boost applications can include boost converters for solar power systems and telecom systems.

For the low power range, the efficiency of the hard switching circuit is better because there is relatively little current in the circuit so that turn-on switching losses, which depend on the product of switch voltage and current during switch turn-on, are low. Moreover, the hard-switching converter does not have any losses that are caused by an auxiliary circuit, which consumes some energy. When the load is low, the energy saved by the auxiliary circuit is less than its consumption. For the high power range, the turn-on losses for the hard-switching converter become very high and are greater than the power consumed by the auxiliary circuit of the soft-switching converter, which has ZVS, so that the soft-switching converter is more efficient.

**Figure 12.** Efficiency vs. load power.



## 7. Conclusion

A new auxiliary circuit for ZVS-PWM converters that are implemented with paralleled MOSFETs for higher current applications was proposed in the paper. The auxiliary circuit has two auxiliary switches to overcome the drawbacks of typical standard single-switch auxiliary circuits that are limited to lower current applications.

In the paper, the operation of a ZVS-PWM boost converter implemented with the new auxiliary circuit was described, its steady-state operation was analyzed, and a procedure for its design was derived and then demonstrated with an example. The feasibility of the new converter was confirmed by experimental results obtained from a prototype converter.

It should be noted that the proposed converter is being proposed for higher current applications where ZVS-PWM converters are not typically used. For typical ZVS-PWM converter applications, simpler, cheaper, and more conventional approaches are more suitable.

## References

1. Streit, R.; Tollik, D. A high efficiency telecom rectifier using a novel soft-switching boost-based input current shaper. In Proceedings of the 13th International Telecommunications Energy Conference, Kyoto, Japan, 5–8 November 1991; pp. 720–726.
2. De Freitas, L.C.; da Cruz, D.F.; Farias, V.J. A novel ZCS-ZVS-PWM DC-DC buck converter for high power and high switching frequency: Analysis, simulation and experimental results. In Proceedings of the Eighth Annual Applied Power Electronics Conference and Exposition, San Diego, CA, USA, 7–11 March 1993; pp. 337–342.
3. Yang, L.; Lee, C.Q. Analysis and design of boost zero-voltage-transition PWM converter. In Proceedings of the Eighth Annual Applied Power Electronics Conference and Exposition, San Diego, CA, USA, 7–11 March 1993; pp. 707–713.
4. Da Costa, A.V.; Treviso, C.H.G.; de Freitas, L.C. A new ZCS-ZVS-PWM boost converter with unity power factor operation. In Proceedings of the Ninth Annual Applied Power Electronics Conference and Exposition, Orlando, FL, USA, 13–17 February 1994; pp. 404–410.
5. Hua, G.; Leu, C.-S.; Jiang, Y.; Lee, F.C. Novel zero-voltage-transition PWM converters. *IEEE Trans. Power. Electron.* **1994**, *9*, 213–219.
6. Filho, N.P.; Farias, V.J.; deFreitas, L.C. A novel family of DC-DC PWM converters using the self-resonance principle. In Proceedings of the 25th Annual IEEE Power Electronics Specialists Conference, Taipei, Taiwan, 20–25 June 1994; pp. 1385–1391.
7. Noon, J.P. A 250 kHz, 500 W power factor correction circuit employing zero voltage transitions. In Proceedings of the Unitrode Power Supply Design Seminar, Sem-1000, Dallas, TX, USA, 1994; pp. 1-1–1-16.
8. Moschopoulos, G.; Jain, P.; Joos, G. A novel zero-voltage switched PWM boost converter. In Proceedings of the 26th Annual IEEE P Power Electronics Specialists Conference, Atlanta, GA, USA, 18–22 June 1995; pp. 694–700.
9. Smith, K.M.; Smedley, K.M. A comparison of voltage-mode soft-switching methods for PWM converters. *IEEE Trans. Power Electron.* **1997**, *12*, 376–386.
10. Xi, Y.; Jain, P.K.; Joos, G.; Jin, H. A zero voltage switching forward converter topology. In Proceedings of the 19th International Telecommunications Energy Conference, Melbourne, Vic, Australia, 19–23 October 1997; pp.116–123.
11. Tseng, C.-J.; Chen, C.-L. Novel ZVT-PWM converter with active snubbers. *IEEE Trans. Power Electron.* **1998**, *13*, 861–869.
12. Moschopoulos, G.; Jain, P.; Joos, G.; Liu, Y.-F. Zero voltage switched PWM boost Converter with an energy feedforward auxiliary circuit. *IEEE Trans. Power Electron.* **1999**, *14*, 653–662.
13. Kim, T.-W.; Kim, H.-S.; Ahn, H.-W. An improved ZVT PWM boost converter. In Proceedings of IEEE 31st Annual Power Electronics Specialists Conference, Galway, Ireland, 18–23 June 2000; pp. 615–619.
14. Kim, J.-H.; Lee, D.Y.; Choi, H.S.; Cho, B.H. High performance boost PFP (Power Factor Pre-regulator) with an improved ZVT (zero voltage transition) converter. In Proceedings of the Sixteenth Annual IEEE Applied Power Electronics Conference and Exposition, Anaheim, CA, USA, 4–8 March 2001; pp. 337–342.

15. Jain, N.; Jain, P.; Joos, G. A zero voltage transition boost converter employing a soft switching auxiliary circuit with reduced conduction losses. *IEEE Trans. Power Electron.* **2004**, *19*, 130–139.
16. Martins, M.L.; Grundling, H.A.; Pinheiro, H.; Pinheiro, J.R.; Hey, H.L. A ZVT PWM boost converter using auxiliary resonant source. In Proceedings of the Seventeenth Annual IEEE Applied Power Electronics Conference and Exposition, Dallas, TX, USA, 10–14 March 2002; pp. 1101–1107.
17. Wang, C.-M. Zero-voltage-transition PWM dc-dc converters using a new zero-voltage switch cell. In Proceedings of the 25th International Telecommunications Energy Conference, Yokohama, Japan, 23–23 October 2003; pp. 784–789.
18. Gurunathan, R.; Bhat, A.K.S. A zero-voltage transition boost converter using a zero-voltage switching auxiliary circuit. *IEEE Trans. Power Electron.* **2002**, *17*, 658–668.
19. da Silva, E.R.C.; Cavalcanti, M.C.; Jacobina, C.B. Comparative study of pulsed DC-link voltage converters. *IEEE Trans. Power Electron.* **2003**, *18*, 1028–1033.
20. Bazinet, J.; O'Connor, J. Analysis and design of a zero-voltage-transition power factor correction circuit. In Proceedings of the Ninth Annual Applied Power Electronics Conference and Exposition, Orlando, FL, USA, 13–17 February 1994; pp. 591–600.
21. Wu, X.; Zhang, J.; Ye, X.; Qian, Z. Analysis and derivations for a family ZVS converter based on a new active clamp ZVS cell. *IEEE Trans. Power Electron.* **2008**, *5*, 773–781.
22. Zhao, Y.; Li, W.; Deng, Y.; He, X. Analysis, design, and experimentation of an isolated ZVT boost converter with coupled inductors. *IEEE Trans. Power Electron.* **2011**, *26*, 541–550.
23. Li, W.; Liu, J.; Wu, J.; He, X. Design and analysis of isolated ZVT boost converters for high-efficiency and high-step-up applications. *IEEE Trans. Power Electron.* **2007**, *22*, 2363–2374.
24. Wai, R.; Lin, C.; Liaw, J.; Chang, Y. Newly designed ZVS multi-input converter. *IEEE Trans. Ind. Electron.* **2011**, *58*, 555–566.
25. Cheng, H.; Hsieh, Y.; Lin, C. A Novel single-stage high-power-factor AC/DC converter featuring high circuit efficiency. *IEEE Trans. Ind. Electron.* **2011**, *58*, 524–532.
26. Chattopadhyay, S.; Baratam, S.; Agrawal, H. A new family of active clamp PWM DC-DC converters with ZVS for main switch and ZCS for auxiliary switch. In Proceedings of the Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition, Fort Worth, TX, USA, 6–11 March 2011; pp. 851–858.
27. Park, S.; Choi, S. Soft-switched CCM boost converters with high voltage gain for high-power applications. *IEEE Trans. Power Electron.* **2010**, *25*, 1211–1217.