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Benefits of Considering More than Temperature Acceleration for GaN HEMT Life Testing

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Abstract: The purpose of this work was to investigate the validity of Arrhenius accelerated-life testing when applied to gallium nitride (GaN) high electron mobility transistors (HEMT) lifetime assessments, where the standard assumption is that only critical stressor is temperature, which is derived from operating power, device channel-case, thermal resistance, and baseplate temperature. We found that power or temperature alone could not explain difference in observed degradation, and that accelerated life tests employed by industry can benefit by considering the impact of accelerating factors besides temperature. Specifically, we found that the voltage used to reach a desired power dissipation is important, and also that temperature acceleration alone or voltage alone (without much power dissipation) is insufficient to assess lifetime at operating conditions.

Keywords: gallium nitride; HEMT; lifetime testing; reliability; device degradation

1. Introduction

Gallium nitride (GaN) high electron mobility transistors (HEMTs) offer gains in increased capability and lower costs due to their ability to operate at high power, high frequencies, and high temperatures [1]. Although extremely attractive for many U.S. Department of Defense applications, insertion of this emerging technology is risky because of the little to no long-term use data that ensures the needed lifetimes are possible. Most estimates of GaN HEMT lifetimes have used conventional temperature-accelerated direct current (DC) operational-life test predictions. The Arrhenius extrapolations reported in the literature [2–4] have extremely long predicted median times to failure. While encouraging, the long estimates and high activation energies may not be indicative of the actual lifetimes at use conditions.

Despite the commercialization of GaN HEMTs for some ground-based applications, mysteries about the device reliability remain [5], as evidenced by the continued research of their life expectancy. These unanswered questions have inhibited their use for military and space applications, where demonstrated long product lifetimes are required.

The GaN HEMT is a complex electrothermomechanical system that will be used at high channel temperatures, extreme bias, and high radio frequency (RF) drive. Is the conventional temperature-accelerated Arrhenius extrapolation sufficient to describe the long-term behavior of the system? Are these extrapolations adequate to compare one generation of GaN HEMTs from a single vendor to another generation, or to compare GaN HEMTs from multiple vendors?

In using the Arrhenius model to estimate lifetimes, several assumptions are made that will be investigated. Using the Arrhenius model assumes that a dominant failure mechanism exists and is accelerated by temperature. In other words, the high temperatures cannot “turn on” different and more temperature-sensitive mechanisms or mask unknown lower-temperature mechanisms. Other assumptions of the Arrhenius technique, such as the existence of one unique temperature (i.e., T_1) that describes the device at a specific bias condition, are known issues but will not be investigated in detail are whether or not surface, channel, or hot electron temperatures should be used as the critical temperature for analysis [5]. The estimation of the temperature at the site of degradation/failure is critical. Direct measurement and characterization of the actual temperature in the area of interest was impractical because the area of interest is sub-micron in size and is located, within the structure of the device, under a metal stack that cannot be removed without affecting device operation and/or the intended temperature to be measured [6,7]. Therefore, we relied on the commonly accepted approach of using simulation data and indirect measurements versus directly collecting measured data. Other important sources of error in thermal estimation are that the degrading region of a power device is not at a single uniform temperature during operation [6] and that the thermal resistance estimates usually only consider the total power dissipated within the device. These thermal resistance estimates do not account for different bias conditions causing different temperature distributions within the device [7]. Finally, the value of the thermal resistance between the GaN buffer and the substrate varies greatly from vendor to vendor due to differences in device fabrication and packaging [8].

In addition to the query of the critical temperature for analysis in [5], the authors explored the validity of the assumption that the failure mechanisms in GaN HEMTs follow the Arrhenius model. Furthermore, [9,10] reported that the gate degradation in GaN HEMTs depends strongly on electric field but weakly on temperature. The authors concluded that this weak temperature dependence can lead to optimistic lifetime estimates if conventional high-temperature acceleration is used and voltage-accelerated tests are needed.

The Arrhenius model is $r(T) = A \cdot \exp(-E_A/kT)$, where r is the reaction rate, T is the temperature in Kelvin (K) at the site of failure in the device (typically attributed to the channel), A is a constant, E_A is the activation energy in electron-volts (eV), and k is Boltzmann’s constant (8.617×10^{-5} eV/K) [11]. The activation energy parameter in the Arrhenius model is experimentally determined and denotes the sensitivity of the reaction (degradation, in the case of reliability testing) to temperature.

An acceleration factor AF —in this case, due to elevated temperatures—relates an Arrhenius reaction rate at one temperature to an Arrhenius reaction rate at a different temperature. The acceleration factor is defined mathematically as [12]:

$$AF = \frac{r(T_2)}{r(T_1)} = \frac{Ae^{(-E_A/kT_2)}}{Ae^{(-E_A/kT_1)}} = \exp\left(\frac{E_A}{k} \left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right). \quad (1)$$

With failure time measurements from samples operating at two or more temperatures, the activation energy E_A can be found. Once the activation energy has been computed, an acceleration factor is calculated with Equation (1) using a temperature other than the elevated temperatures, such as operating temperatures, as T_1 , and one of the elevated temperatures as T_2 . An estimate for the time to failure at T_1 is then this AF multiplied by the time to failure at T_2 .

2. Materials and Methods

Tested devices came from the same lot and had the same structure, which consisted of a semi-insulating silicon carbide (SiC) substrate [13], one 0.5- μm length optically defined gate with a

gate-integrated field plate [13], and a source-connected field plate [4]. Gate width was $2 \times 50 \mu\text{m}$. The gate contained a nickel Schottky barrier and thick gold overlay for low gate resistance. The highly resistive GaN buffer was grown by organometallic vapor phase epitaxy (OMVPE) [13]. The gate-to-drain gap was greater than the gate-to-source gap [13].

Two different sets of test conditions were used: one was a high DC drain voltage ($V_{DS} = 60$ and 100 V) and low current with the gate pinched off ($V_{GS} = -10 \text{ V}$), and the other was high DC power dissipation ($\geq 11 \text{ W/mm}$). These conditions may occur during the RF sweep of device operation. Table 1 shows the initially observed parameter values of the two different sets of test conditions. The rationale for selecting Conditions 1, 2, and 3 was to map the boundaries of life for the tested devices with increasing voltages. Conditions 2 and 3 were to have the same power dissipation (P_{diss}) and Condition 1 half that power. Conditions 1 and 2 were to have the same drain current (I_D). The base-plate temperatures (T_{bp}) of the power test Conditions 1, 2, and 3 were selected so that the devices had similar estimated peak channel temperatures (T_{ch}), while the high-voltage test Conditions 4 and 5 would also have similar peak channel temperatures and were chosen to investigate the effect voltage. All peak channel temperature estimates are based on bias-dependent electrothermal modeling of the full device [6]. In all cases, testing was conducted in the dark under dry nitrogen in an Accel-RF/DC test station. Two different test durations were used.

Table 1. Initial measured parameter values.

Condition	Device	Measured T_{bp} ($^{\circ}\text{C}$)	Measured V_{DS} (V)	Measured I_D (mA/mm)	Measured V_{GS} (V)	Calculated P_{diss} (W/mm)	T_{ch} ($^{\circ}\text{C}$) Estimate
1	55	245.2	20.011	568.9	2.011	11.4	399
	56	245.2	19.994	547.9	2.004	11.0	393
	57	245.2	20.000	532.8	2.017	10.7	389
2	58	133.0	40.012	552.8	2.016	22.1	393
	59	133.2	40.010	576.8	1.806	23.1	406
	60	133.2	40.012	571.9	1.708	22.9	404
3	28	130.3	60.005	380.8	0.3028	22.8	403
	29	130.3	60.015	349.4	0.4022	21.0	378
	30	130.2	60.018	366.7	0.25	22.0	391
6	25-024	245.2	17.494	655.3	3.033	11.5	397
	26-025	245.3	17.509	658.9	3.034	11.5	399
	27-026	245.3	17.507	658.5	3.028	11.5	398
Approximate I_D (mA/mm)							
4	31	245.0	60.005	<0.026	-10.002	<0.00156	245
	33	245.1	59.996	<0.026	-9.992	<0.00156	245
5	25	245.1	99.995	<2.0	-9.996	<0.19999	246–248
	27	245.1	100.005	<2.0	-9.999	<0.20001	246–248

Base-plate temperatures (T_{bp}), drain to source voltage (V_{DS}); drain current (I_D); gate to source voltage (V_{GS}); power dissipation (P_{diss}); channel temperatures (T_{ch}).

2.1. 300-h Test

For a 300-h test, three devices were placed under testing for each of conditions 1, 2, and 3, and two devices were tested for each of Conditions 4 and 5, for a total of 13 successfully tested devices. For high-power Conditions 1, 2, and 3, the drain voltage V_{DS} was set and the gate voltage V_{GS} was adjusted until the target drain current I_D was reached. After the initial setting of V_{GS} , V_{GS} was maintained for the duration of the test. The expected values of V_{GS} for Conditions 1, 2, and 3 were based on previous testing and were not anticipated to cause forward gate current based on the previous testing of parts from the same lot at $V_{GS} = 2 \text{ V}$. For the high-voltage Conditions 4 and 5, both V_{DS} and V_{GS} were set, and the expected I_D is based on the values seen during step-stress testing on four on-wafer devices in a probe station. The range of T_{ch} estimates for Condition 5 is based on the range of I_D values seen during the step-stress testing.

The test sequence for the power test conditions was an initial characterization, followed by stress. The test was ended at 300 h to conduct post-stress characterization.

Since drain current degradation during stress was expected to be small in the devices in the high-voltage set, these devices were periodically characterized. Their degradation was tracked with I_{DSS} and I_{Dmax} rather than with the stress drain current. One-hundred hours was arbitrarily chosen for the time between characterizations.

The automated characterization is supported by the test stand (the sample did not leave the test module), and consisted of transfer curves collected at $T_{bp} = 70^\circ\text{C}$ with Agilent power supplies (model E5280B Precision High Power modules in a model E5270B 9-Slot Precision Measurement Mainframe, City, Country of Agilent). The transfer curve was conducted at $V_{DS} = 10\text{ V}$, with V_{GS} being swept from -5 to 1 V . The characterization was shown to be benign in on-wafer testing. I_{DSS} is defined as the current when measured at $V_{DS} = 10\text{ V}$ and $V_{GS} = 0\text{ V}$. I_{Dmax} is defined as the drain current when measured at $V_{DS} = 10\text{ V}$ and $V_{GS} = 1\text{ V}$. The resulting 300-h test data were tabulated in Section 3 below. Traditional IV plots were not possible since all of the data were collected at fixed values of V_{DS} and V_{GS} .

2.2. 600-h Test

A test similar to the 300-h high-power test was conducted for 600 total stress hours on three devices. The differences were (Condition 6 in Table 1) rest periods at 200 and 400 stress hours, and hourly characterizations at the stress base-plate temperature. In addition and similar to the 300-h test, transfer curve characterizations occurred at $T_{bp} = 70^\circ\text{C}$ before and after each stress period.

Prior to conducting this 600-h test, three packaged devices were tested in a probe station to determine bias conditions at which very little ($<1\text{ mA/mm}$) forward gate current would flow. With the thermal stage set at 245°C , the voltages of Condition 6 were observed to cause very little forward gate current. The average drain current at these biases was 690 mA/mm . The resulting 600-h test data were tabulated in Section 3 below. Traditional IV plots were not possible since all of the data were collected at fixed values of V_{DS} and V_{GS} .

3. Detailed Results

3.1. 300-h Test

The devices showed a very apparent “burn-in” effect, with a rapid change in electrical characteristics followed by slow and more consistent (part-to-part) change. Due to this apparent burn-in effect, some of the following comparisons will treat the first post-stress characterization for the high-voltage-tested parts as the “initial” values; doing so is sufficient to remove the burn-in effect for all parts. Since the first post-stress characterization for the high-power-tested parts is also the last characterization for these devices, the pre-stress characterization will be treated as the initial values for the high-power-tested devices.

The nominal pre-stress conditions for the devices tested for 300 h follow: the average peak transconductance (g_{mp}) was 201.2 mS/mm ; the average threshold voltage was 2.88 volts ; the average maximum drain current (I_{Dmax}) was 745.5 mA/mm ; and the average maximum source current (I_{Smax}) was 573.8 mA/mm .

Table 2 contains the changes at the end of the test period for each device. Most changes are listed as percentages, but the threshold voltage change is absolute. The initial values for the high-voltage-tested parts are from the 100-h characterization to remove the burn-in effect, as explained above. All devices trended as indicated by the signs in Table 2. All devices exhibited a positive threshold voltage shift. The high-power conditions caused more change than the high-voltage conditions as seen in the greater magnitude changes shown in Table 2.

To ensure that the positive gate biases used in some test conditions were not the cause of degradation, we subjected devices from the same family as reported herein to high forward gate

bias (+6 V) and current (>1.8 A/mm) for >17.5 h. The HEMTs survived this condition and exhibited only a slight change in gate diode characteristic, little decrease in maximum drain current, with only a 0.1 V positive threshold voltage shift, and remarkably, a persisting breakdown voltage exceeding 200 V.

Table 2. Parameter changes by condition in 300-h test: g_{mp} , V_T , I_{Dmax} , and I_{DSS} .

Condition	Device	g_{mp}	ΔV_T (mV)	I_{Dmax}	I_{DSS}
1	55	−2.37%	253	−7.9%	−10.1%
	56	−1.20%	310	−8.6%	−11.9%
	57	−2.57%	365	−10.0%	−13.6%
2	58	−2.29%	316	−11.6%	−14.2%
	59	−3.50%	312	−12.1%	−14.1%
	60	−1.64%	263	−9.0%	−11.2%
3	28	−5.37%	603	−18.3%	−24.6%
	29	−2.03%	356	−10.7%	−14.9%
	30	−2.72%	514	−13.0%	−18.3%
4	31	0.04%	49.6	−1.3%	−1.7%
	33	−0.14%	31.7	−0.7%	−1.4%
5	25	0.01%	71.4	−1.7%	−2.4%
	27	−1.02%	12.3	−1.2%	−1.2%

Transconductance (g_{mp}); change in threshold (ΔV_T); maximum drain current (I_{Dmax}); steady state drain current (I_{DSS}).

Our commercially purchased reliability test station monitored gate leakage current, but not with sufficient accuracy to provide any useful data for this research. While some reports show increased gate current after exceeding a “critical voltage” [14], we tested two representative devices to the limits of our power supplies ($V_D = +200$ V, $V_G = -100$ V) and did not see any such “critical voltage” breakdown. Instead, the bias conditions used in this study were chosen because they represent realistic device operating conditions and they closely follow industry standard accelerated life test (ALT) methodologies where saturated RF power and DC saturated drain current are key metrics for assessing device performance and degradation [15,16].

While determining the physical cause of the observed degradation was not an objective of this paper, there are published mechanisms that could apply. Degradation due to hot electrons is discussed in [17,18]. A prominently reported degradation mechanism in GaN HEMTs is the physical alteration of the drain side of the gate after stress [15,17,19,20]. In [21], we reported our observations of physical damage after stress.

Based on the averages of the parameter data presented in Table 2, there appears to be a correlation between higher drain biases (when power dissipation and channel temperature are held constant) and greater degradation. Although the estimated channel temperatures were similar for the high power tests and separately for the high voltage tests, the average change for the four parameters generally increased in magnitude with drain voltage. For high-power Condition 3, the degradation was more than it was for the other two high-power conditions.

Using the averages of the activation energies presented in [2–4]—2.09 eV—and the averages of each condition’s channel temperatures estimates in Table 1, the acceleration factors from Equation (1) between the test conditions were calculated. The acceleration factors (AF) suggest that the devices tested at Condition 1 should have, based on the AF alone, degraded slightly more than the Condition 3 devices (AF = 1.19), and Condition 2 more than Condition 3 (AF = 1.72). However, we see in Table 2 that Condition 3 degraded the fastest as would be expected for a positive degradation correlation with drain voltage. To be fair, Conditions 2 and 3 are more comparable to each other than Condition 1 since Conditions 2 and 3 experienced similar power dissipation; error in the estimate of the thermal resistance of the sub-micron-sized channel region will affect Conditions 2 and 3 in about the same

way and still leave them comparable to each other. Still, we see that the degradation caused by the high-power electrical conditions overshadows the degradation that may be caused by temperature for Condition 3.

On the other hand, high-voltage Condition 5 may have had a channel temperature between 246 and 248 °C versus 245 °C for the channel temperature of the other high-voltage condition. This implies $1.09 < AF < 1.31$ for Condition 5 versus Condition 4. As such, for the changes shown in Table 2 for the high voltage tests, we do not rule out agreement with the expectations of the Arrhenius model.

Figure 1 shows the pre- and post-stress values of I_{Dmax} and I_{DSS} , respectively, normalized to the pre-stress values for the high-power conditions. The plots of the Condition 1 and 2 drain currents overlap, indicating that these conditions had similar responses to their stresses, despite different drain voltage and power dissipation levels. The plots of the Condition 3 drain currents are distinctly separate from those of Conditions 1 and 2, despite the similar T_{ch} estimates for all three conditions and the same power dissipation as Condition 2. Condition 3 shows a marked difference to Conditions 1 and 2. In fact, $\pm 15\%$ ranges around Conditions 1 and 2 slope averages overlap each other, while the $\pm 15\%$ range around the Condition 3 average does not overlap the $\pm 15\%$ ranges of either Condition 1 or 2 averages.

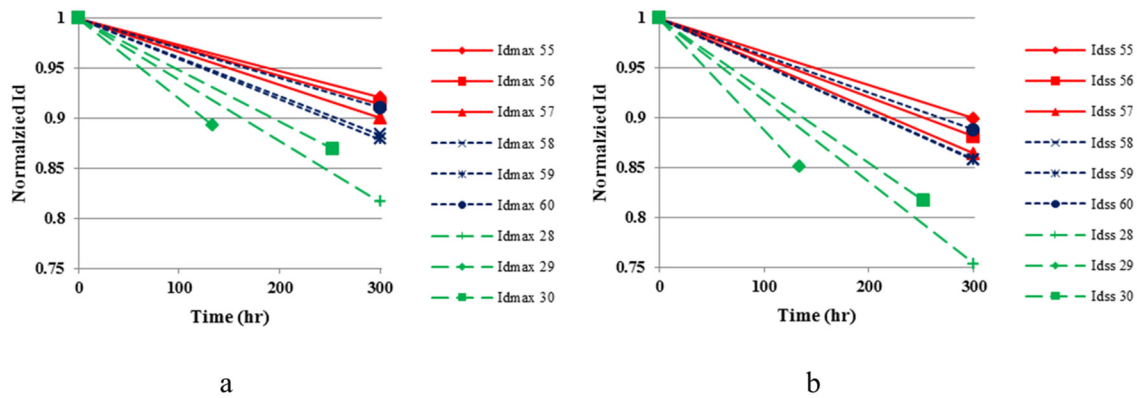


Figure 1. Normalized (to the 0 h measurements) pre- and post-stress values of (a) maximum drain current (I_{Dmax}) and (b) steady state drain current (I_{DSS}) for the 300 h high-power conditions. The top three lines (red) of the legend are Condition 1, the middle three (blue) Condition 2, and the bottom three (green) Condition 3.

A similar analysis of the slopes of the I_{Dmax} and I_{DSS} lines can be performed for the high-voltage conditions. Figure 2 shows the pre- and post-stress values of I_{Dmax} and I_{DSS} , respectively, normalized to the 100 h values. The plots of I_{Dmax} overlap, and the Condition 5 I_{DSS} lines encompass the Condition 4 I_{DSS} lines, indicating that both conditions had similar responses to their stresses, despite different drain voltages. Ranges of $\pm 15\%$ around the Condition 4 and 5 I_{DSS} linear-fit slope averages overlap, but $\pm 15\%$ ranges around the I_{Dmax} linear-fit slope averages do not. Although the slope averages increase with drain voltage and the $\pm 15\%$ I_{Dmax} slope average ranges do not overlap, the overlapping I_{Dmax} and I_{DSS} plots indicate similar behavior for the high voltage test.

The following is an analysis of the sensitivity of the high power test to different sources of variation. To examine the effect of the test station on device degradation measurements, the initial parameters were first recorded. Table 1 contains the values of parameters of interest at time 0 of the stress period as measured by the test station while at the stress base-plate temperature. There are multiple sources of measurement variation within the test station: ± 2 °C for base-plate temperature, ± 50 mV for drain voltage, and ± 1.5 mA (equivalently 15 mA/mm) for drain current. In addition to the measurement variation, the setability accuracy for drain current is 1.5 mA, and base-plate temperature is ± 2 °C. The drain current measurements (and calculated power dissipations) are the largest sources of variation in the channel temperature estimates in Table 1 for the high-power conditions.

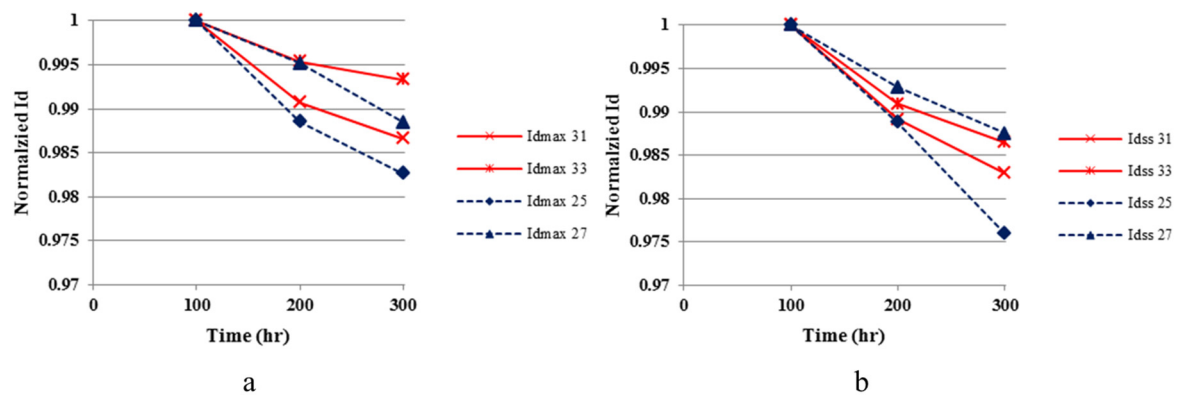


Figure 2. Normalized (to the 100 h measurements) pre- and post-stress values of (a) maximum drain current (I_{Dmax}) and (b) steady state drain current (I_{DSS}) for the 300 h high-voltage conditions. The top two lines (red) of the legend are Condition 4, and the bottom two (blue) are Condition 5.

Assuming the initial measured values had persisted throughout the test, a correlation between the channel temperature estimates of Table 1 and the degradation for each device (Table 2) for the high-power conditions can be investigated. For comparison purposes, the high-power-tested device values are compared to nominal values of $T_{ch} = 395^\circ\text{C}$ (the average of the T_{ch} estimates in Table 1), -2% g_{mp} , a ΔV_T of $+300$ mV, -10% I_{Dmax} , and -10% I_{DSS} . With the nominal T_{ch} value as T_1 in Equation (1), acceleration factors are calculated to compare each high-power-tested device to the nominal values. This analysis indicates there is no correlation between the acceleration factors and the observed degradation, which means that the observed degradation was not caused by the variation in initial measured parameter values.

The following analysis investigates the initial T_{ch} estimates of Table 1 and the measurement error from the Agilent power supplies during initial and final characterizations. Based on the Agilent specifications [22], the drain current measurement error depends on the measured current value and the output voltage, which also has a measurement error dependent on the measured output voltage. The drain voltage measured 10 V and the error was ± 7 mV. For the high-power-tested devices, the maximum drain current error for the initial characterizations was 0.108 mA, and, for the final characterizations, was 0.102 mA. The maximum drain current error for the initial and final characterizations of the high-voltage-tested devices was 0.107 mA. Degradation rates (linear-fit slopes from Figures 2 and 3) are calculated from the initial and final I_{Dmax} characterizations and times. Finally, the magnitudes of the degradation rates are plotted against the temperatures ($1/kT$) in Figure 4. The center points are the average T_{ch} estimates and the average rates in a condition. The endpoints are the minimum and maximum rates along the line of average temperatures and the minimum and maximum T_{ch} estimates along the line of average rate in a condition. Conditions 4 and 5 have greater rate ranges since there was little difference between the initial and final drain current values, which resulted in the same maximum error of 0.107 mA. Also included in Figure 3 are reference lines that pass through the center point of Condition 1 and assume activation energies of 2.09 (used previously in this paper), 1.6 , and 2.47 eV (the range of values surveyed in [5] that resulted from DC testing).

As can be seen from Figure 3, Conditions 1 and 2, and separately 4 and 5, have overlapping ranges and are similar. Notice that the reference lines through Condition 1 do not approach Conditions 4 and 5. Conditions 4 and 5 appear related to each other by the Arrhenius model. Since the high power test results are clustered closely in Figure 3, the portion of the graph containing these conditions is magnified in Figure 4.

In Figure 4, the error bars are replaced with error boxes, and individual device data are plotted. As seen in Figure 4, the ranges of Condition 3 do not overlap those of Conditions 1 and 2, which suggests that Condition 3's behavior may not have been caused by temperature, even with measurement error and variation of initial biases. However, the reference lines could be shifted to the

right such that the lines intersect all three boxes, suggesting an Arrhenius relationship between the conditions. The inconsistency, though, is that Condition 3's box is up and to the right of Condition 1, when it should be down and to the right for its lower average T_{ch} estimate (see Table 1).

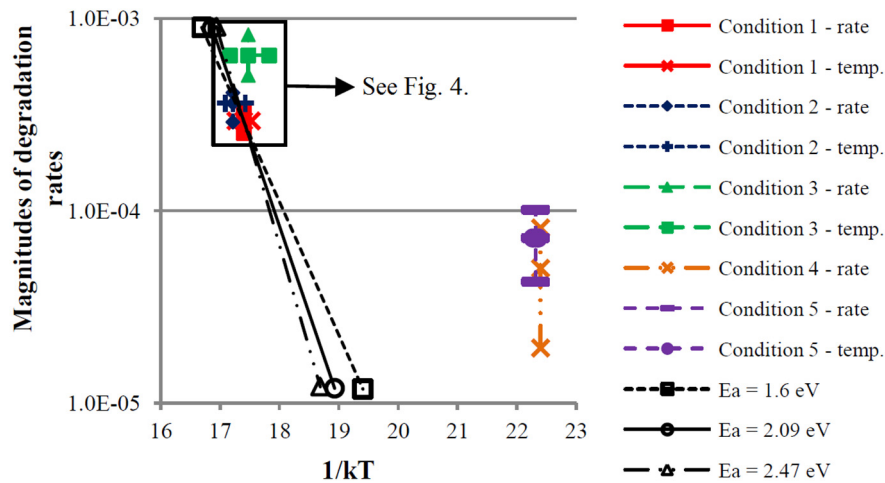


Figure 3. Comparison of Agilent power supply (San Jose, Ca, USA) measurement error and initial channel temperature (T_{ch}) estimates in the 300-h test.

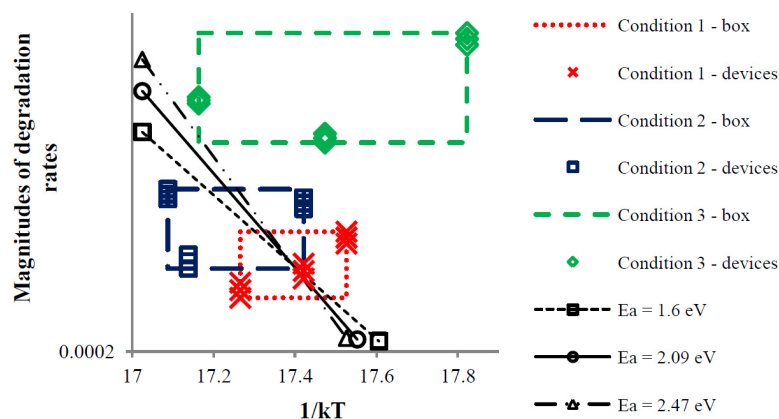


Figure 4. Magnified portion of Figure 3.

Finally, an analysis of the sensitivity of Conditions 1, 2, and 3 to thermal resistance (R_{th}) changes in the thermal model is investigated. The accuracy of any thermal resistance estimate for these devices is subject to significant error [6,7,23], and it is an underappreciated fact that the sensitivity of conclusions drawn in an accelerated life test to the thermal resistance assumed should be considered [7]. The analysis computes new T_{ch} estimates with $[(T_{ch} - T_{bp}) \times (\pm 20\%)] + T_{bp}$ for a $\pm 20\%$ change in thermal resistance. Then, acceleration factors between test conditions are calculated with the new T_{ch} estimates. Table 3 lists the new T_{ch} estimates and acceleration factors (AF), as well as the original T_{ch} estimates and acceleration factors. The new AF's generally indicate the same behavior as the original AF's for Condition 2 versus 3: Condition 2 should degrade more than Condition 3. Depending on the error, though, Condition 1 may degrade much more or less than Conditions 2 and 3 based on AFs. Recall that the observed behavior was not what was indicated by the Arrhenius model—Condition 3 degraded more than Conditions 2 and 3.

Based on the foregoing data, the evidence indicates that temperature was not the cause of degradation in the high-power tested devices, especially, since there were significant differences in the responses of Conditions 2 and 3. From the sensitivity analysis, the variation of the test station bias

setting and measurements in initial measured parameter values, the characterization measurement error, and the thermal resistance error in the thermal model are not sufficient to discount the differences in degradation or the conclusion that temperature did not cause the degradation. In contrast, for the high-voltage-tested parts, there is sufficient similarity and overlap in degradation values and plots to indicate that the observed changes may have been caused by temperature. Therefore, the Arrhenius model may be valid for some bias conditions, but not for others.

Table 3. Sensitivity analysis of thermal model for R_{th} for Conditions 1, 2, and 3.

Condition	T_{ch} (°C)	T_{ch} (°C)	T_{ch} (°C)	Comparison	AF	AF	AF
	(−20% R_{th})	(Model R_{th})	(+20% R_{th})		(−20% R_{th})	(Model R_{th})	(+20% R_{th})
1	364	394	424	1 to 2	2.84	0.69	0.227
2	347	401	455	1 to 3	4.73	1.18	0.397
3	339	391	443	2 to 3	1.67	1.72	1.75

Thermal resistance (R_{th}).

3.2. 600-h High-Power Test

Similar to the burn-in effect observed in the 300 h test above, the devices of the 600 h test showed a more rapid decrease in the first hour of stress than in subsequent hours. Consequently, the 1 h characterizations at 245 °C are considered to be the “initial” data points for the pre- and post-stress characterizations.

The nominal pre-stress conditions for the devices tested for 600 h follow: the average peak transconductance (g_{mp}) was 202.1 mS/mm; the average threshold voltage was −2.96 volts; the average maximum drain current (I_{Dmax}) was 760 mA/mm; and the average maximum source current (I_{Smax}) was 591 mA/mm. The devices were from the same lot as the devices used for the 300-h test. Table 4 contains the changes at the end of the 200 and 600 h for each device.

Table 4. Parameter changes by device and stress time in the 600-h test: g_{mp} , V_T , I_{Dmax} , and I_{DSS} .

Y (hours)	Device	g_{mp}	ΔV_T (mV)	I_{Dmax}	I_{DSS}
200	25-024	−4.1%	0.31	−10.4%	−13.5%
	26-025	−3.2%	0.25	−8.1%	−10.6%
	27-026	−2.4%	0.24	−7.1%	−9.7%
600	25-024	−3.2%	0.25	−8.3%	−10.9%
	26-025	−2.4%	0.17	−5.8%	−7.3%

Transconductance (g_{mp}); change in threshold (ΔV_T); maximum drain current (I_{Dmax}); steady state drain current (I_{DSS}).

Figure 5 shows the normalized values (to the 1 h, 245 °C measurements) of I_{Dmax} over time for the devices in the 600 h test. Interestingly, after initially degrading, the devices began to recover during stress. This recovery is evident in decreased magnitudes of averages, from 200 to 600 h, of the parameter data in Table 4.

As with Conditions 2 and 3 of the 300 h test, Condition 1 of the 300 h test and Condition 6 of the 600 h test are comparable since they experience similar power dissipation. However, the T_{ch} estimate for Condition 6 is 405 °C, and the acceleration factor between Conditions 6 and 1 is 1.80, indicating that Condition 6 should be different than the other conditions. Therefore, Condition 6 was expected to degrade more than Condition 1. Figure 6 contains plots of the 70 °C characterization data for the 300-h and 600-h tests. As in Figure 5, the drain current recovers in the 600-h test devices. Interpolating the 600-h test data at 300 h reveals that Condition 6, in fact, did not degrade more than Condition 1, contrary to Arrhenius expectations.

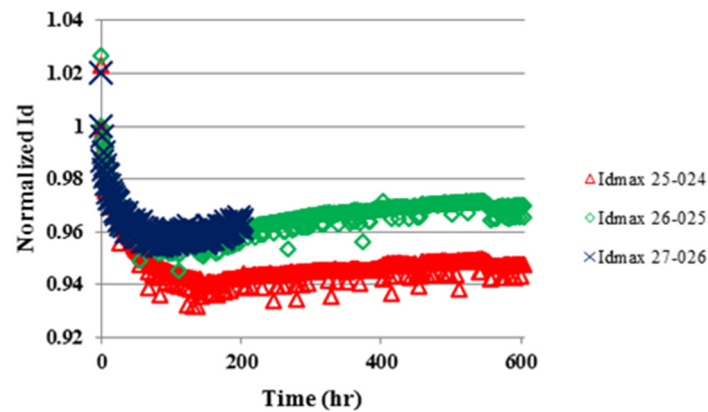


Figure 5. Normalized values (to the 1 h, 245 °C measurements) of I_{Dmax} over time during the 600 h test.

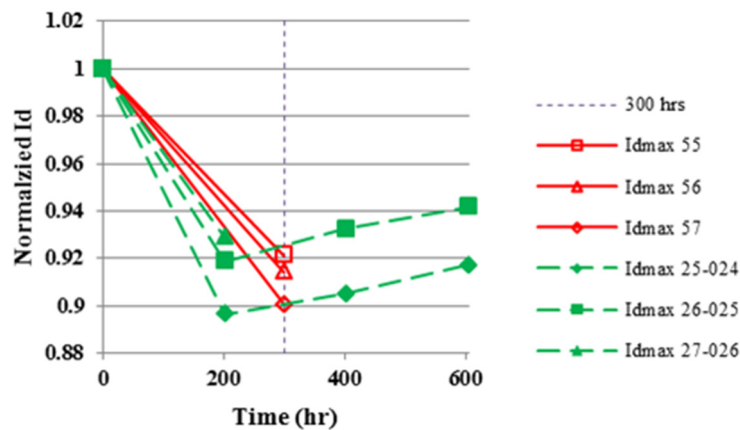


Figure 6. Normalized values (to the 0 h, 70 °C measurements) of maximum drain current (I_{Dmax}) over time during the 300-h test, Condition 1 (lines 2–4 in the legend in red) and the 600-h test, Condition 6 (lines 5–7 in the legend in green) tests.

The following is a brief analysis of the sensitivity of Conditions 1 and 6 to the initial measured parameter values. To begin, the initial measured parameter values of Conditions 6 are listed. Table 1 contains the values of parameters of interest at time 0 of the stress period as measured by the test station while at the stress base-plate temperature.

Then, the initial T_{ch} estimates for Conditions 1 and 6 in Table 1 and the measurement error from the Agilent power supplies during the initial 300-h characterizations are analyzed in direct analogy to the analysis of Figures 4 and 5. Linear interpolations of the 200 h and 400 characterizations of Devices 25-024 and 26-025 are used to obtain 300 h characterization estimates for these devices. A 300-h characterization estimate is extrapolated for Device 27-026 from its 200-h characterization using the average of the slopes calculated for the linear interpolations of Devices 25-024 and 26-025. Based on the Agilent specifications [22], the error for the measured drain voltage of 10 V is ± 7 mV. For Condition 1, the maximum drain current error for the initial characterizations is 0.108 mA, and for the 300-h characterizations is 0.102 mA. For Condition 6, the maximum drain current error for the initial characterizations is 0.109 mA, and for the 300-h characterization estimates is 0.103 mA. Degradation rates are calculated from the initial and 300 h I_{Dmax} characterizations and times. Finally, the magnitudes of the degradation rates are plotted against the temperatures ($1/kT$) in Figure 7. The center points are the average T_{ch} estimates and the average rates in a condition. The endpoints are the minimum and maximum rates along the line of average temperature and the minimum and maximum T_{ch} estimates along the line of average rate in a condition.

As can be seen in Figure 7, Conditions 1 and 6 have overlapping ranges and the reference lines could be moved left to intersect both boxes, indicating similar behavior. The initial T_{ch} estimates for Condition 6 are generally higher than those of Condition 1, yet the degradation rates are generally similar. The average initial T_{ch} estimates for Condition 6 is 398 °C, and the average initial T_{ch} estimates for Condition 1 is 394 °C. The Arrhenius acceleration factor between these average temperatures is 1.24. The inconsistency here with the Arrhenius model is that the Condition 6 box is down and to the left of the Condition 1 box, when it should be up and to the left for its higher average initial T_{ch} estimate.

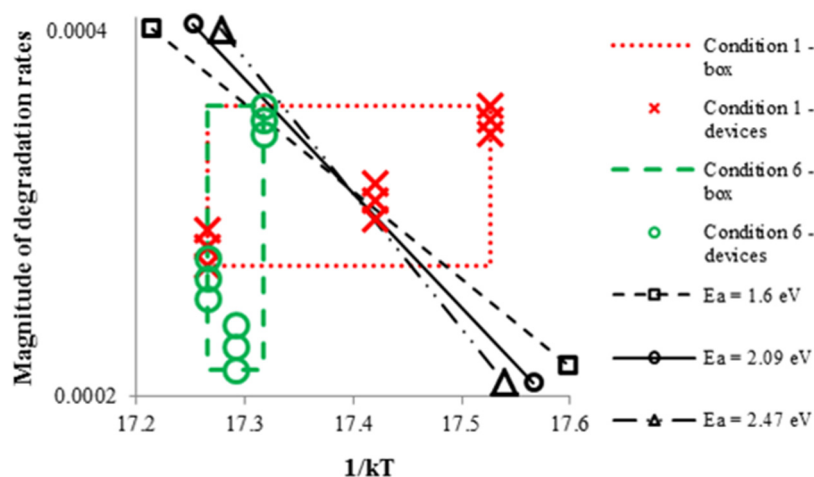


Figure 7. Comparison of Agilent power supply measurement error and initial T_{ch} estimates in Conditions 1 and 6.

3.3. Discussion

In the data presented, there are two instances where the Arrhenius model seems reasonable. These instances occur when GaN HEMTs were tested at a similar channel temperature estimates. These instances are between Conditions 1 and 2 and between Conditions 4 and 5 (although the average degradation for these conditions has a positive correlation to drain voltage).

Conversely, there are two instances of inconsistency with the Arrhenius model. Both instances occur when the test conditions are similar. One instance—between Conditions 2 and 3—occurs when similar degradation was expected, but the two conditions exhibited different degradation. The other instance—between Conditions 1 and 6—occurs when different behavior was expected, but similar behavior was observed. In addition, the error boxes of Conditions 3 and 6 are not where they are expected to be based on the Arrhenius relation.

Another instance of inconsistency is between the high-voltage conditions and the high-power conditions. Reference lines assuming activation energies do not intersect the error regions of the two different sets of conditions (see Figure 3). This inconsistency indicates that GaN HEMT degradation depends on the test conditions.

The average points of all the test conditions follow a positive correlation to drain bias. For the high-voltage conditions, the average degradation rate is higher for Condition 5 ($V_{DS} = 100$ V) than for Condition 4 ($V_{DS} = 60$ V). For the high-power conditions, the progression from lowest to highest average degradation rate is Condition 6 ($V_{DS} = 17.5$ V), Condition 1 ($V_{DS} = 20$ V), Condition 2 ($V_{DS} = 40$ V), and Condition 3 ($V_{DS} = 60$ V) (see Figures 3, 4 and 7).

Reliability evaluation of aluminum gallium nitride (AlGaIn)/GaN HEMT's will benefit from considering other accelerants besides temperature. Based on the observations from this study, drain bias showed a positive correlation to degradation in a high-power test condition. Voltage acceleration would be a primary additional accelerant to pursue. To adequately consider other accelerants, the design of experiment methodology could be applied to create the multi-variable tests. Then,

multi-stress models could be used in place of the single-stress Arrhenius model to analyze the data. Possible multi-stress models to use include the Generalized Eyring model [12] Generalized Log-Linear relationship, and the Proportional Hazards model [24]. Each model allows more than two stressors to be applied as accelerants.

Reliability assessments that employ more and different accelerants than temperature will result in more accurate lifetime estimates of AlGaIn/GaN HEMTs since they will account for the failure mechanisms of the electrothermomechanical system that are not primarily thermally activated. For example, if a temperature-accelerated life test was conducted near Conditions 1 and 2, but device operation occurred near Condition 3, the Arrhenius extrapolations would be optimistic.

Based on this study, and [9,10], the need for different accelerants when assessing GaN HEMT reliability is shown. Additionally, [14,19,20] investigated the effect of increasing drain-to-gate voltage I_{Dmax} . They observed that higher drain-to-gate voltages degraded drain current, especially after a “critical voltage”. These authors showed, in effect, that GaN HEMT degradation for some devices could be accelerated with voltage. In contrast to [14,19,20], our devices required high voltage in conjunction with power dissipation for degradation; higher voltages without power did not cause similar degradation. Similar devices to ours from the same vendor, tested independently, behaved similarly without degradation according to the inverse piezoelectric effect, as expected by the “critical voltage” model [25,26].

4. Conclusions

We have studied the degradation of AlGaIn/GaN HEMTs subjected to the conditions of high DC power and high voltage with the gate pinched off, conditions which are typical during normal device operation. We observed that device degradation, in the devices stressed by only DC, can not be modeled using the classic temperature accelerated model. The experimental data showed that single-DC-stress, temperature accelerated life testing does not account for the critical degradation in a GaN HEMT. Further work will investigate the stress effects of RF operation, to assess whether or not DC-only accelerated-life tests can properly identify dominant end-of-life degradation mechanisms.

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References

1. Mishra, U.K.; Parikh, P.; Wu, Y.-F. AlGaIn/GaN HEMTs—An overview of device operation and applications. *Proc. IEEE* **2002**, *90*, 1022–1031. [[CrossRef](#)]
2. Conway, A.M.; Chen, M.; Hashimoto, P.; Willadsen, P.J.; Micovic, M. Accelerated RF life testing of GaN HFETs. In Proceedings of the 45th Annual 2007 IEEE International Reliability Physics Symposium, Phoenix, AZ, USA, 15–19 April 2007; pp. 472–475.
3. Singhal, S.; Hanson, A.W.; Chaudhari, A.; Rajagopal, P.; Li, T.; Johnson, J.W.; Nagy, W.; Therrien, R.; Park, C.; Edwards, A.P.; et al. Qualification and reliability of a GaN process platform. In Proceedings of the CS MANTECH Conference, Austin, TX, USA, 14–17 May 2007; pp. 83–86.
4. Lee, S.; Vetury, R.; Brown, J.D.; Gibb, S.R.; Cai, W.Z.; Sun, J.; Green, D.S.; Shealy, J. Reliability assessment of AlGaIn/GaN HEMT technology on SiC for 48V applications. In Proceedings of the 2008 IEEE International Reliability Physics Symposium, Phoenix, AZ, USA, 27 April–1 May 2008; pp. 446–449.

5. Leach, J.H.; Morkoç, H. Status of reliability of GaN-based heterojunction field effect transistors. *Proc. IEEE* **2010**, *98*, 1127–1139. [[CrossRef](#)]
6. Heller, E.R. Simulation of life testing procedures for estimating long-term degradation and lifetime of AlGaIn/GaN HEMTs. *IEEE Trans. Electron Devices* **2008**, *55*, 2554–2560. [[CrossRef](#)]
7. Heller, E.R.; Crespo, A. Electro-thermal modeling of multifinger AlGaIn/GaN HEMT device operation including thermal substrate effects. *Microelectron. Reliab.* **2008**, *48*, 45–50. [[CrossRef](#)]
8. Kuball, M.; Killat, N.; Manoi, A.; Pomeroy, J.W. Benchmarking of thermal boundary resistance of GaN-SiC interfaces for AlGaIn/GaN HEMTs: US, European and Japanese suppliers. In Proceedings of the CS MANTECH Conference, Portland, OR, USA, 17–20 May 2010; pp. 109–110.
9. Marcon, D.; Kauerauf, T.; Medjdoub, F.; Das, J.; van Hove, M.; Srivastava, P.; Cheng, K.; Leys, M.; Mertens, R.; Decoutere, S.; et al. A comprehensive reliability investigation of the voltage-, temperature- and device geometry-dependence of the gate degradation on state-of-the-art GaN-on-Si HEMTs. In Proceedings of the 2010 IEEE Electron Devices Meeting (IEDM), San Francisco, CA, USA, 6–8 December 2010.
10. Marcon, D.; Kauerauf, T.; Decoutere, S. Unraveling the mysteries of HEMT degradation. *Compt. Semicond.* **2001**, *17*, 14–19.
11. Trew, R.J.; Green, D.S.; Shealy, J.B. AlGaIn/GaN HFET reliability. *IEEE Microwave Mag.* **2009**, *10*, 116–127. [[CrossRef](#)]
12. Ebeling, C.E. *An Introduction to Reliability and Maintainability Engineering*; Waveland Press: Long Grove, IL, USA, 2005.
13. Brown, J.D.; Green, D.S.; Gibb, S.R.; Shealy, J.B.; McKenna, J.; Poulton, M.; Lee, S.; Gratzner, K.; Hosse, B.; Mercier, T.; et al. Performance, Reliability, and Manufacturability of AlGaIn/GaN High Electron Mobility Transistors on Silicon Carbide Substrates. *ECS Trans.* **2006**, *3*, 161–179.
14. Del Alamo, J.A.; Joh, J. GaN HEMT reliability. *Microelectron. Reliab.* **2009**, *49*, 1200–1206. [[CrossRef](#)]
15. Gajewski, D.A.; Sheppard, S.; McNulty, T.; Barner, J.B.; Milligan, J.; John Palmour Cree Inc. Reliability of GaN/AlGaIn HEMT MMIC technology on 100-mm 4H-SiC. In Proceedings of the 26th Annual JEDEC ROCS Workshop, Indian Wells, CA, USA, 16 May 2011.
16. Burgaud, P.; Constancias, L.; Martel, G.; Savina, C.; Mesnager, D. Preliminary reliability assessment and failure physical analysis on AlGaIn/GaN HEMTs COTS. *Microelectron. Reliab.* **2007**, *47*, 1653–1657. [[CrossRef](#)]
17. Smith, K.V.; Brierley, S.; McAnulty, R.; Tilas, C.; Zarkh, D.; Benedek, M.; Phalon, P.; Hooven, A. GaN HEMT reliability through the decade. *ECS Trans.* **2009**, *19*, 113–121.
18. Meneghesso, G.; Verzellesi, G.; Danesin, F.; Rampazzo, F.; Zanon, F.; Tazzoli, A.; Meneghini, M.; Zanoni, E. Reliability of GaN high-electron-mobility transistors: State of the art and perspectives. *IEEE Trans. Dev. Mat. Reliab.* **2008**, *8*, 332–343. [[CrossRef](#)]
19. Joh, J.; del Alamo, J.A. Critical Voltage for Electrical Degradation of GaN High-Electron Mobility Transistors. *IEEE Electron Device Lett.* **2008**, *29*, 287–289. [[CrossRef](#)]
20. Makaram, P.; Joh, J.; del Alamo, J.A.; Palacios, T.; Thompson, C.V. Evolution of structural defects associated with electrical degradation in AlGaIn/GaN high electron mobility transistors. *Appl. Phys. Lett.* **2010**, *96*, 233509. [[CrossRef](#)]
21. Christiansen, B.D.; Coutu, R.A.; Heller, E.R.; Poling, B.S.; Via, G.D.; Vetury, R.; Shealy, J.B. Reliability testing of AlGaIn/GaN HEMTs under multiple stressors. In Proceedings of the 2011 IEEE Reliability Physics Symposium (IRPS), Monterey, CA, USA, 10–14 April 2011; pp. CD.2.1–CD.2.5.
22. Agilent Technologies, Agilent E5270B 8 Slot Precision Measurement Mainframe Technical Overview. September 2004. Available online: <http://cp.literature.agilent.com/litweb/pdf/5989--1355EN.pdf> (accessed on 1 July 2011).
23. Kim, J.; Freitas, J.A., Jr.; Klein, P.B.; Jang, S.; Ren, F.; Pearton, S.J. The effect of thermally induced stress on device temperature measurements by Raman spectroscopy. *Electrochem. Solid State Lett.* **2005**, *8*, G345–G347. [[CrossRef](#)]
24. ReliaSoft Corp. Multivariable relationships: General log-linear and proportional hazards. Available online: http://www.weibull.com/AccelTestWeb/general_log_linear_relationship_chap_.htm (accessed on 15 July 2011).

25. Hodge, M.D.; Vetry, R.; Shealy, J.; Adams, R. A robust AlGaN/GaN HEMT technology for RF switching applications. In Proceedings of the 2011 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), Waikoloa, HI, USA, 16–19 October 2011; pp. 1–4.
26. Hodge, M.D.; Vetry, R.; Shealy, J. Fundamental failure mechanisms limiting maximum voltage operation in AlGaN/GaN HEMTs. In Proceedings of the 2012 IEEE Reliability Physics Symposium (IRPS), Anaheim, CA, USA, 15–19 April 2012; pp. 3D.2.1–3D.2.6.



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