Online Optimal Switching Frequency Selection for Grid-Connected Voltage Source Inverters

Saher Albatran [1,*] **, Issam A. Smadi** [1] **, Hamzeh J. Ahmad** [1] **and Ahmed Koran** [2]

[1] Department of Electrical Engineering, Faculty of Engineering, Jordan University of Science and Technology, Irbid 22110, Jordan; iasmadi@just.edu.jo (I.A.S.); hjahmad13@eng.just.edu.jo (H.J.A.)
[2] Department of Electrical Power Engineering, Hijjawi Faculty for Engineering Technology, Yarmouk University, Irbid 21163, Jordan; akoran@yu.edu.jo
[*] Correspondence: saalbatran@just.edu.jo; Tel.: +962-272-01000

Abstract: Enhancing the performance of the voltage source inverters (VSIs) without changing the hardware structure has recently acquired an increased amount of interest. In this study, an optimization algorithm, enhancing the quality of the output power and the efficiency of three-phase grid connected VSIs is proposed. Towards that end, the proposed algorithm varies the switching frequency (f_{sw}) to maintain the best balance between switching losses of the insulated-gate-bipolar-transistor (IGBT) power module as well as the output power quality under all loading conditions, including the ambient temperature effect. Since there is a contradiction with these two measures in relation to the switching frequency, the theory of multi-objective optimization is employed. The proposed algorithm is executed on the platform of Altera® DE2-115 field-programmable-gate-array (FPGA) in which the optimal value of the switching frequency is determined online without the need for heavy offline calculations and/or lookup tables. With adopting the proposed algorithm, there is an improvement in the VSI efficiency without degrading the output power quality. Therefore, the proposed algorithm enhances the lifetime of the IGBT power module because of reduced variations in the module's junction temperature. An experimental prototype is built, and experimental tests are conducted for the verification of the viability of the proposed algorithm.

Keywords: grid-connected inverter; power electronics; multi-objective optimization; switching frequency; total demand distortion; switching losses

1. Introduction

Renewable energy resources play a major role in the current world's energy generation. To interconnect renewable energy resources, grid connected three-phase VSIs are widely utilized [1]. However, the increased number of connections between the VSIs and the grid should never degrade the power quality, particularly at the point of common coupling (PCC), while the total harmonic distortion (THD) should never go beyond a specific limit to prevent harmonics related problems. It is possible to reduce the THD with the switching frequency (f_{sw}) being increased. However, when the f_{sw} is increased, the switching losses are likewise increased and, therefore, this can result in a reduction in the inverter's efficiency as well. Consequently, f_{sw} is typically, but not optimally, chosen as a trade-off between the output power quality and the efficiency at a specific loading condition. Since the operating conditions of the VSI are continuously varying, the variable switching frequency (VSF) enables the inverter switching losses to be decreased in regions where the harmonic content is insignificant, and, in the same sense, the harmonic content can be reduced in the regions where the inverter losses are highly insignificant.

The performance of the three-phase grid connected VSIs is highly dependent on the selected f_{sw}. Therefore, literature has proposed numerous algorithms of the VSF to enhance the inverter's efficiency [2,3], inverter's transient response [4], and the acoustic noise of induction motor [5]. Switching frequency is varied either within the fundamental period [6–9], or based on the operating conditions [10–12], such that the switching losses or the THD are minimized. In [6], the proposed algorithm is formulated based on the current-ripple analysis of the three-phase inverters in a time-domain. The idea was geared toward the reduction of f_{sw}, while maintaining the peak current ripple under a certain limit; consequently, there is a reduction in the average f_{sw}, and thus a reduction in switching losses. Application of the above algorithm can be found in [7,8] as well. In [9], the switching frequency trajectory was derived using calculus of variations and based on the current ripples analysis relative to the single-phase inverters in time-domain, in order to reduce the switching losses while meeting certain THD requirements. This method suffers from computational complexity and requires heavy offline calculations. In [10], the efficiency of single-phase inverter is incrementally enhanced, while satisfying standard THD; the result of the algorithm was an increase in the efficiency of the inverter in comparison with the conventional sinusoidal pulse-width modulation (SPWM) as well as the space-vector pulse-width modulation (SVPWM). In any case, the aim of the aforementioned methods was to enhance the efficiency of the inverter, while ensuring that the THD is continuously positioned to the highest allowable limit. An offline technique was proposed by the authors of [11] for the minimization of the losses of VSIs based on multi-objective optimization, where the proposed algorithm was used to control synchronous motors. Meanwhile, the target is characterized based on the weighted combination of the peak-to-peak ripple of electromagnetic torque and switching losses, in a way that a fair balance is achieved. In [12], an optimization process was applied on the electric and hybrid vehicle motor drive, in which f_{sw} was varied with different modulation indices or input voltages. Concurrent switching losses minimization and dead-time compensation study was presented in [13] under various power levels and different power factors. Compared with discrete pulse width modulation techniques, switching losses were reduced by 15%.

The switching losses were reduced at high current-levels in [14] by proposing new SVPWM strategies in which the number of switch commutations of the quasi-Z-source inverter is reduced. In [15], a lower number of commutations is achieved by the proposed optimization. The variable switching frequency reduces about 19% of the switching losses compared with constant switching frequency for similar output current quality. Analytical variable switching frequency is presented in [16] according to the modulation index and a predefined current ripple band. The switching frequency varies within the fundamental cycle (sub-fundamental) to reduce the switching losses of two level inverter traction drive system. In [17], the switching loss is analyzed under different discontinuous SVPWM techniques for balanced two-phase load fed by a three-leg inverter. The algorithm tried to balance the switching losses of each phase-leg at lower current ripple. In [18], 3D-SVPWM of four-leg VSI was presented to reduce the switching losses of the proposed shunt compensator by 33%. The efficiency of a grid-tied full bridge inverter is improved in [19] using the variable switching frequency scheme. The authors minimize the switching losses at predefined THD using a bipolar modulation scheme. Variable switching frequency was used in [20] to reduce switching losses and electromagnetic interference (EMI) noise of a common voltage oriented SPWM rectifier considering the restrictions on voltage ripple at the direct current (DC) link.

The THD and the maximum torque ripple of the permanent magnet synchronous machine are optimized in [21]. For this target, the authors presented a finite control set model based on a predictive control scheme. A new behavioral model for losses in power semiconductors was proposed in [22] where the impacts of gate resistance and gate voltage are considered. A summary of the several behavioral models existing in literature and industry was listed.

The major contribution this paper puts in place is the proposition of an efficient and practically sound VSF algorithm whereby there is an online variation of f_{sw} at various loading conditions, including the ambient temperature effect. The intensive calculations that are typically required with the exiting f_{sw}

variation-laws are avoided in the proposed algorithm. Moreover, the benefits of the proposed algorithm include the improvement of the inverters' switching devices and packaging reliability by reducing the variations in the junction temperature, which has a direct effect on the lifetime of the inverter. The attractiveness of this algorithm lies in its simplicity, in which the online computation of the optimal switching frequency can be easily done. Most of the algorithms that have been introduced in the literature suffer from computational complexity that makes them lack practical sound. The advantages of this new proposed algorithms can be summarized in four main points: (1) easy to be implemented using micro-controllers; and (2) the proposed procedure can be generalized for any power converter that includes multi-level inverters regardless of the control mode and the used technology of the power device. However, the proposed mathematical derivations are discussed on an IGBT power module of Infineon® FP50R06KE3 (Neubiberg, Germany). The same procedures are valid for different technologies that have different power loss analysis. (3) The proposed procedure does not require offline computations and lookup tables; and, (4) since the temperature is considered in the proposed algorithm, the algorithm can reduce the thermal stress on the inverter during high ambient temperature by reducing the switching frequency. Conversely, if the energy loss parameters are not directly given from the manufacturer datasheets, the parameters can be experimentally characterized.

The remaining parts of this study are organized as follows. Short summary of the architecture and the control mode of operations of VSIs are presented in Section 2. Section 3 presents the estimation of power losses. Section 4 presents the thermal modeling of the IGBT power module. Section 5 presents the time-domain current ripple analysis. Section 6 presents the proposed variable switching algorithm. Section 7 presents a discussion of the experimental validation. Finally, Section 8 concludes the paper.

2. Voltage Source Inverters

VSIs are crucial components in the alternating current (AC) microgrids and modern power systems. To ensure power system reliability, integrating distribution generators (DGs) with existing power systems has some technical and practical constraints. One of these main limitations is power system stability. Voltage stability becomes more important if the microgrid is off-grid (i.e., isolated microgrid) or if connected with a relatively weak power system. The controllability of the VSIs and the DGs adds effective and supportive actions that can improve the performance of the power systems and microgrids in steady state and transient modes of operation [23].

VSIs can be categorized into three main modes of operation and control schemes. The first one is usually named as a grid-forming power converter in which the VSI is working as a conventional AC source. The voltage and the frequency are controlled and stabilized; however, the output current is load dependent. The uninterruptible power supply (UPS) is an appropriate example of grid-forming VSI. The UPS delivers certain voltage and frequency, where the input of the UPS is also considered as a DC, regardless of being from isolated batteries or converted from an online AC power supply.

The second category is known as grid-feeding power converters. Under this mode of operation, the voltage control is not targeted in the control scheme of the VSI. Moreover, the VSI is working as a current source to supply the desired real and reactive powers. Feeding an energized power system adds more restrictions to the VSI and synchronizing the voltage at PCC is crucially important to track the desired real and reactive power set points. In the previous two modes of operation, either the voltage or the current is controlled. For power system stability, it is occasionally important to control both the output voltage and current. This category is known as grid-supporting power converters and can be classified into two modes: (1) besides supplying the demanded active and reactive powers, it must contribute to stabilizing the voltage and/or the frequency of the grid-connected systems; and (2) the supplied active and reactive powers are subjected to the output voltage magnitude. The voltage magnitude and frequency have higher priority in the second mode than the first mode, and, hence, they can be implemented either in islanded or grid connected microgrids [23].

The proposed algorithm is not limited to one topology or control mode from the aforementioned architectures. However, for the sake of discussion and clarity, the grid-forming scheme is taken as

an example in this paper. Figure 1 shows the grid-forming scheme associated with the proposed algorithm, as executed in the FPGA, which will be discussed in detail throughout the paper. To this end, any control scheme ends by generating the power reference to the pulse width modulator. The second and the important side for the modulator is generating the carrier signal and the switching frequency that are related to the proposed work. The inputs of the VSF algorithm are the loading measurements and the measured temperature.
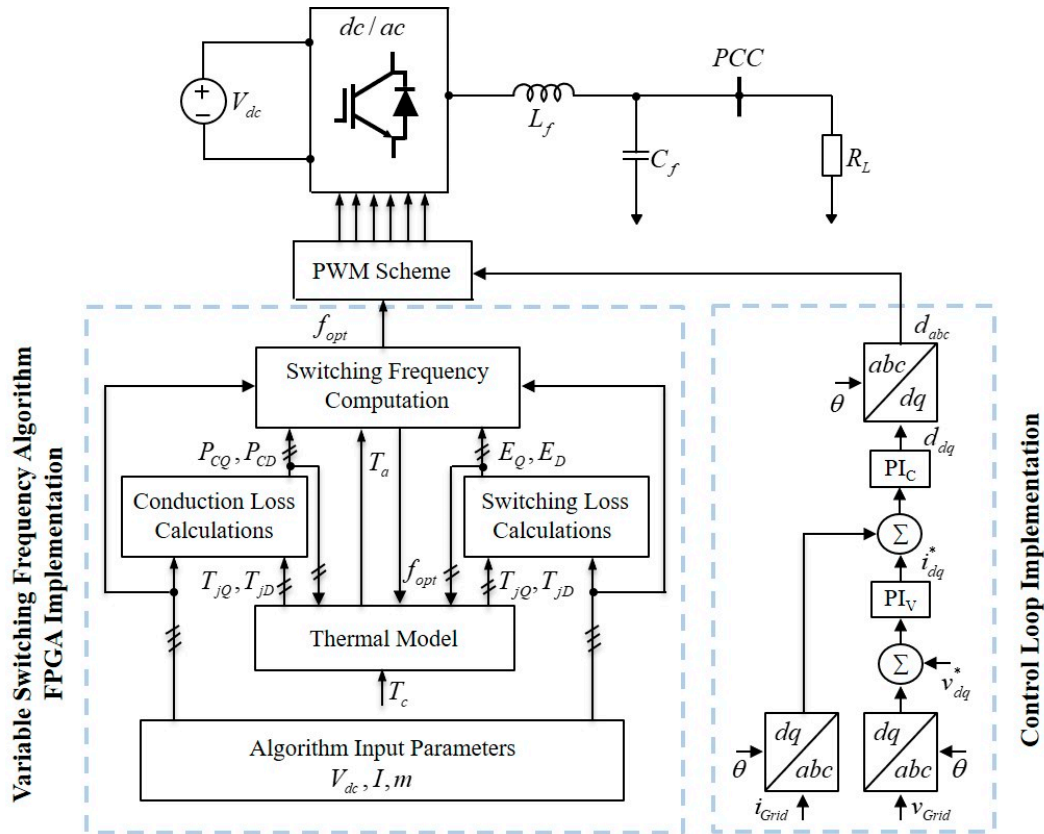

Figure 1. Grid-feeding VSI associated with the proposed VSF algorithm. PWM: pulse width modulation.

3. Estimation of Power Losses in IGBT Power Modules

Basically, the occurrence of power losses in the inverters must be appropriately dissipated to prevent system malfunction because of overheating. The design of the cooling systems, which take responsibility for the dissipation of power losses should be optimized to prevent system failure due to insufficient design or higher costs due to overestimation. The power losses rely on the utilized modulation scheme, loading conditions and the used semiconductor switch. The behavioral model alongside loss parameters taken from the device datasheet has been adopted in this paper due to its simplicity as in [24]. Moreover, in [25,26], the adopted behavioral model provides a good estimate of the actual losses as can be deduced from their comparative analysis.

Furthermore, the antiparallel diode and IGBT encounter power losses, which include driving losses and blocking losses. These losses tend to be insignificant and can be ignored [27]; the diode turn-on losses can be ignored as well [28]. Therefore, significant power losses are usually caused by: (i) the conduction losses [26,29], (ii) the switching losses (IGBT turn on and off losses), (iii) and the diode turn-off losses (the reverse recovery losses). A typical inverter module datasheet is comprised of valuable information regarding switching and conduction losses of its specific IGBT and diode. The datasheet information will be utilized for the estimation of the significant power losses that occur in the inverter, which will be further discussed and derived in detail in the subsections that follow.

3.1. Conduction Losses

The on-state voltage of IGBT (V_{CE}) varies with the collector current as depicted from the device voltage–current (V–I) curves at different junction temperatures (T_j) as shown in Figure 2. Due to this, it is possible to find the IGBT's on-state voltage as a function of the collector current. Moreover, the IGBT's on-state voltage relies on the on-state resistance (R_{CE}), including the threshold voltage of the IGBT (V_{CE0}). In Figure 3, R_{CE} is the reciprocal of the slope connecting points 1 and 2 of the linearized V–I curve while V_{CE0} is the extrapolation of this curve to the voltage-axis. Meanwhile, the on-state resistance and the threshold voltage are temperature dependent, and, hence, this dependency should be considered. This can be achieved by interpolating R_{CE} and V_{CE0} for a given junction temperature as in Equations (1) and (2) and Figure 4:
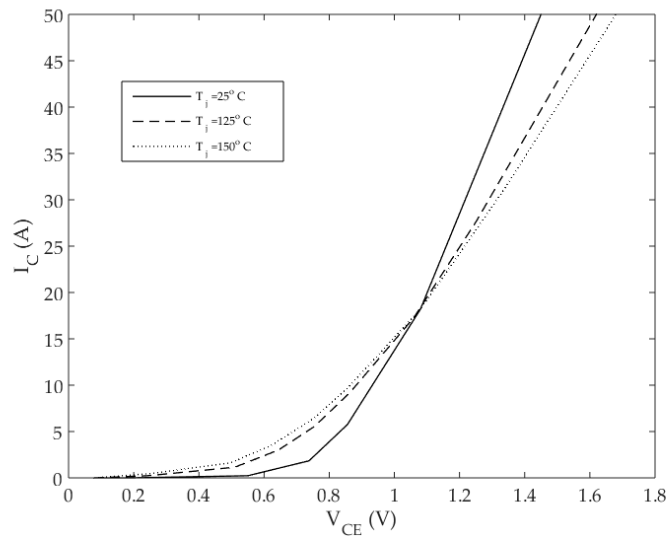
$$R_{CE}(T_j) = 5.82 \times 10^{-7} T_j^2 - 3.07 \times 10^{-5} T_j + 2.38 \times 10^{-2}, \tag{1}$$

$$V_{CE0}(T_j) = -9.10 \times 10^{-6} T_j^2 + 22.76 \times 10^{-5} T_j + 71.54 \times 10^{-2}. \tag{2}$$

As a result, an approximation of the IGBT on-state voltage can be given as
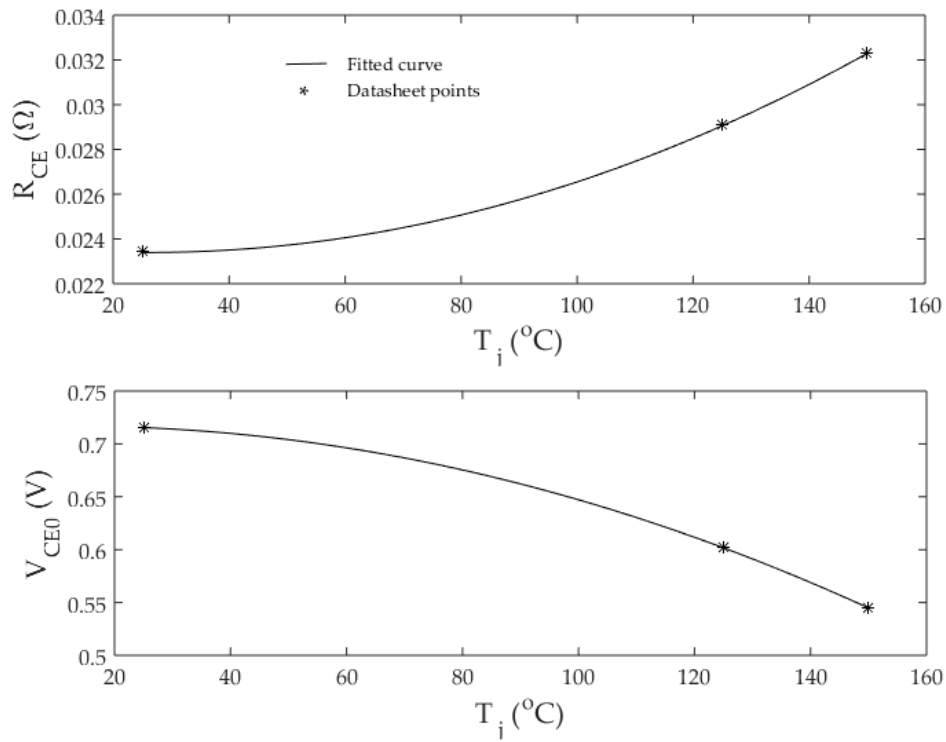
$$V_{CE}(t) = V_{CE0} + R_{CE} i_c(t), \tag{3}$$

where $i_c(t) = i_{pk}\sin(\omega t)$ is the phase-current that flows through the entire IGBT while conducting, $i_{pk}(t)$ is the output phase current peak value and ω is the angular frequency in rad/s.

Figure 2. Infineon IGBT V–I curves for power module (Part number: FP50R06KE3) under different junction temperatures [30].
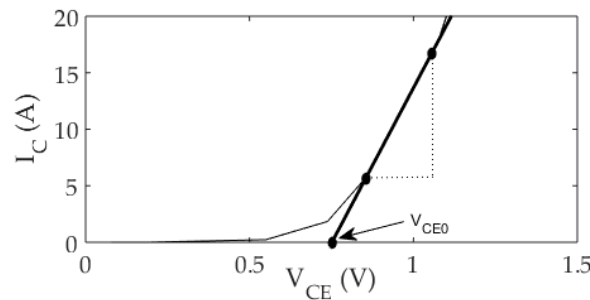
Figure 3. Linearization of V–I curves for IGBT.

Figure 4. Interpolation of R_{CE} and V_{CE0} for different junction temperatures.

To estimate the average conduction losses of the IGBT for one fundamental phase–current period (P_{CQ}), the average losses in each switching period (T_{sw}) are lumped together, and then divided by the total number of the switching pulses as

$$P_{CQ} = \frac{1}{N}\sum_n \frac{1}{T_{sw}} \int_{(n-1)T_{sw}}^{nT_{sw}} i_c(t)V_{CE}(t)dt, \tag{4}$$

where N is considered as the total sum of pulses for each fundamental period and n is the switching pulse index.

In a case whereby f_{sw} is highly relative to the fundamental frequency, which is the typical case for SPWM inverter, it is possible to assume that the collector current is constant during every T_{sw}, that is,

$$i_c((n-1)T_{sw}) \cong i_c(nT_{sw}). \tag{5}$$

The IGBT is conducting for D_nT_{sw} at the nth switching cycle, where D_n is the duty cycle of the voltage pulses. Therefore, Equation (4) can be rewritten as

$$P_{CQ} = \frac{1}{N}\sum_n \frac{1}{T_{sw}} \int_{(n-1)T_{sw}}^{(n-1+D_n)T_{sw}} i_c(t)V_{CE}(t)dt. \tag{6}$$

Taking Equations (3) and (5) into account, and evaluating the integral in Equation (6) yields

$$P_{CQ} = \frac{1}{N}\sum_n \frac{1}{T_{sw}} i_c(nT_{sw})[V_{CE0} + R_{CE}i_c(nT_{sw})]D_nT_{sw}. \tag{7}$$

For the summation given in Equation (7), integration can be used to approximate it considering the assumption of f_{sw} is much higher than the fundamental frequency, and this assumption will be used throughout this study. Subsequently, the current flows through the IGBT at half period when its antiparallel diode is not conducting, and the integration is evaluated over half of the fundamental period (T) as in Equation (8):

$$P_{CQ} \cong \frac{1}{T} \int_0^{T/2} i_c(t)[V_{CE0} + R_{CE}\ i_c(t)]D(t)dt. \tag{8}$$

For SPWM modulation, the duty cycle as a function of time can be written as in Equation (9) [24]:

$$D(t) = \frac{1 + m\sin(\omega t + \theta)}{2}, \tag{9}$$

where θ is considered as the angle difference between the output phase current and output phase voltage in radian and m is the modulation index. Then, an evaluation of the integral yields:

$$P_{CQ} = \frac{V_{CE0}\ i_{pk}}{2\pi} + \frac{R_{CE}i_{pk}{}^2}{8} + \left(\frac{V_{CE0}i_{pk}}{8} + \frac{R_{CE}i_{pk}{}^2}{3\pi}\right)m\ \cos(\theta). \tag{10}$$

The same procedure used to compute the IGBT conduction losses will be used to compute the conduction losses of the antiparallel diode as well. A linear approximation of the V–I characteristics of the diode can be given as

$$V_f(t) = R_f\ i_f(t) + V_{f0}, \tag{11}$$

where V_{f0} is the threshold voltage of the diode and R_f is the forward resistance of the diode. The dependency of V_{f0} and R_f on the junction temperature is expressed in Figure 5 and Equations (12) and (13):

$$R_f(T_j) = -4.16 \times 10^{-8}T_j^2 + 5.27 \times 10^{-6}T_j + 2.14 \times 10^{-2}, \tag{12}$$

$$V_{f0}(T_j) = -9.22 \times 10^{-6}T_j^2 - 39.76 \times 10^{-5}T_j + 86.91 \times 10^{-2}. \tag{13}$$
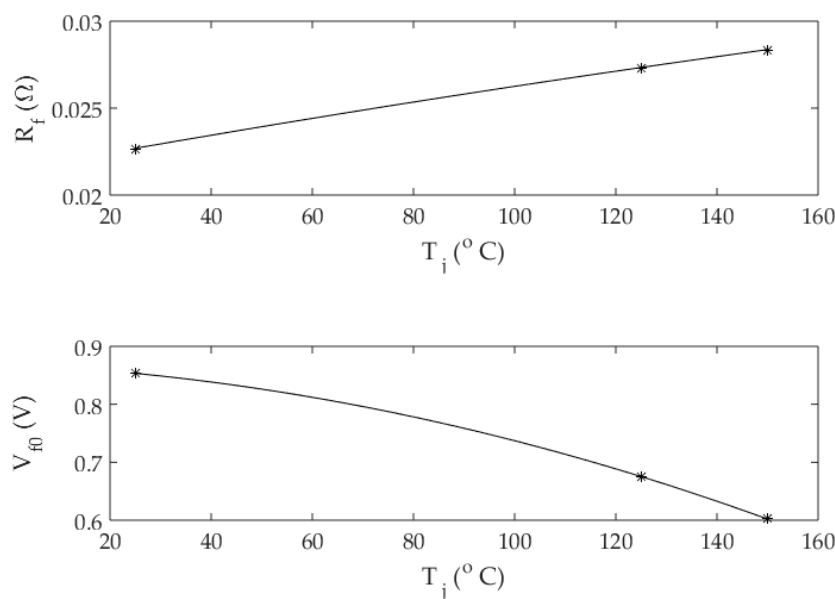

Figure 5. Interpolation of V_{f0} and R_f for different junction temperatures.

The diode is conducting for $(1 - D_n)T_{sw}$ at the nth switching cycle. Taking this into consideration and following the same adopted procedure in deriving the conduction losses in the IGBT, the diode conduction losses can be written as in Equation (14):

$$P_{CD} = \frac{V_{f0}\, i_{pk}}{2\pi} + \frac{R_f i_{pk}^2}{8} - \left(\frac{V_{f0} i_{pk}}{8} + \frac{R_f i_{pk}^2}{3\pi} \right) m\, \cos(\theta). \tag{14}$$

3.2. Switching Losses

The turn-on and off energy losses for every T_{sw} are provided in the device datasheet. Those are losses that rely substantially on the collector current (i_c), the IGBT's junction temperature (T_{jQ}), DC-link voltage (V_{dc}), and turn-on ($R_{g,on}$) and turn-off ($R_{g,off}$) gate resistances. For all the previous dependencies to be considered, 3D-curve fitting techniques are used for energy losses to be expressed based on the parameters above. With the use of the surface fitting, the turn-on and the turn-off energy losses (E_{on} and E_{off}) are expressed in terms of i_c and T_{jQ}, as shown in Figure 6 and Equations (15) and (16). After that, the derived equations must be scaled to include the effect of a specific $R_{g,on}$, $R_{g,off}$ and V_{dc} as in Equations (17) and (18):

$$E_{on}(i_c, T_j) = 30.34 \times 10^{-3} i_c + 75.79 \times 10^{-6} i_c^2 + 1.2 \times 10^{-4} i_c T_j, \tag{15}$$

$$E_{off}(i_c, T_j) = 46.92 \times 10^{-3} i_c - 3.939 \times 10^{-4} i_c^2 + 6 \times 10^{-5} i_c T_j, \tag{16}$$

$$E_{on} = \frac{V_{dc}}{V_{dc,test}} \frac{E_{on}(R_{g,on})}{E_{on}(R_{g,on,test})} E_{on}(i_c, T_{jQ}), \tag{17}$$

$$E_{off} = \frac{V_{dc}}{V_{dc,test}} \frac{E_{off}(R_{g,off})}{E_{off}(R_{g,off,test})} E_{off}(i_c, T_{jQ}) . \tag{18}$$
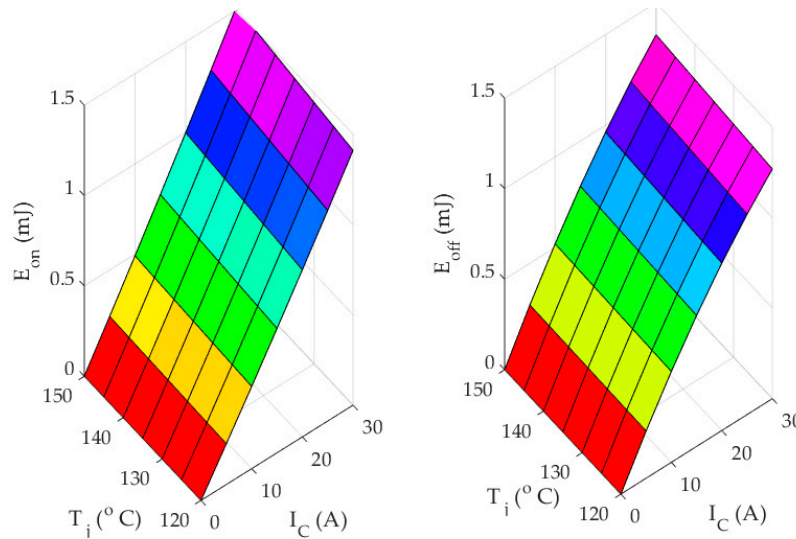
Figure 6. Interpolation of E_{on} and E_{off} for different collector currents and junction temperatures.

The notation 'test' represents the value that is utilized in the measurements of the energy losses test. Based on Equations (17) and (18), the average losses due to switching for every fundamental period (P_{swQ}) are given as in Equation (19):

$$P_{swQ} = \frac{1}{NT} \sum_n \left(E_{on} + E_{off} \right). \tag{19}$$

In Equation (19), E_{on} and E_{off} are functions of the collector current ($i_c(t) = i_{pk}\sin(\omega t)$). Based on estimation, it is assumed that the switching power losses are sinusoidal, while Equations (17) and (18) define the sine function peak of E_{on} and E_{off}, respectively, at the peak evaluation of the collector current. An approximation of the summation in Equation (19) can be given by the integration as in Equation (20):

$$P_{swQ} = \frac{1}{T}\left[\left(E_{on} + E_{off}\right)f_{sw}\right]\int_0^{T/2}\sin(\omega t)dt = \frac{E_{on} + E_{off}}{\pi}f_{sw}. \tag{20}$$

3.3. Reverse Recovery Losses

Following the same procedure in Section 3.2 but for the diode, Figure 7 shows the reverse recovery energy losses as functions of i_f and T_j and Equation (21) is the corresponding 3D-curve fitted equation:

$$E_{rec}(i_f, T_j) = 20.64 \times 10^{-3}i_f - 4.827 \times 10^{-4}i_f^2 + 7 \times 10^{-5}i_f T_j. \tag{21}$$

As a result, the formulations for the reverse recovery losses are expressed as:

$$E_{rec} = \frac{V_{dc}}{V_{dc,test}}\frac{E_{rec}(R_{g,on})}{E_{rec}(R_{g,on,test})}E_{rec}(i_f, T_j)\,, \tag{22}$$

$$P_{swD} = \frac{E_{rec}}{\pi}f_{sw}. \tag{23}$$

The total IGBT module power losses can be finally formulated as in Equation (24):

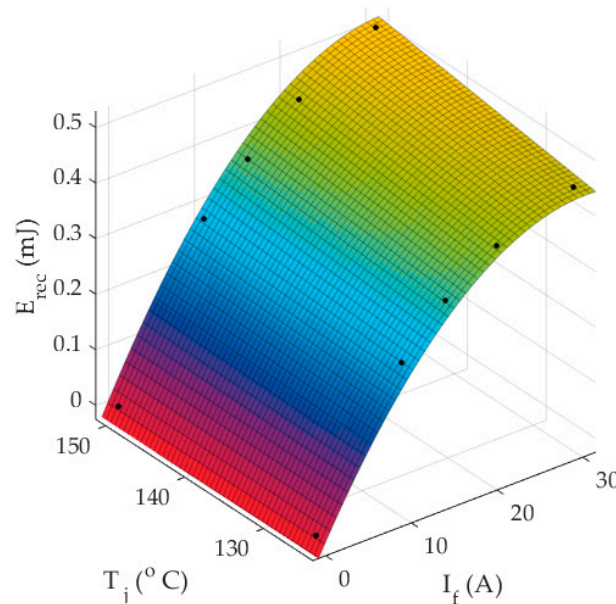$$P_T = 6\left(P_{CQ} + P_{CD} + P_{swQ} + P_{swD}\right). \tag{24}$$

Figure 7. Interpolation of E_{rec} for different diode currents and junction temperatures.

4. Thermal Modeling of the IGBT Power Module

Power losses that occur in a semiconductor switch are the main cause of rise of its junction temperature; therefore, a thermal model that estimates the junction temperature from the power losses has to be constructed. Thermal models can be steady-state models such as thermal resistance networks in which only the steady-state temperatures can be estimated, or dynamic models such as

the well-known Foster and Cauer models that can estimate the transient behavior of the temperature when it changes from one steady-state point to another [31]. For gird-tied inverters, the time interval between two consecutive active-power set-points is much larger than the time constant of the thermal model in general. Since the aim of this study is to develop an algorithm that changes the switching frequency with the change in the steady-state operating conditions (mainly the active-power) as will be described later, thermal transients can be ignored. Hence, a steady-state thermal model is adopted in this study. In steady-state operating conditions, a specific IGBT conducts for a half-cycle, whereas its anti-parallel diode conducts for the other half, which causes the junction temperature to increase during the half-cycle of conduction and decrease during the other one; this causes a junction temperature ripple that the steady-state thermal model cannot estimate. However, for 50–60 Hz operation, the junction temperature ripple is much smaller than the average value of the junction temperature; therefore, a steady-state thermal model can be used. To account for the rise of the instantaneous junction temperature above its average value, the maximum junction temperature that corresponds to the maximum power dissipation is set to a value lower than the maximum operating junction temperature defined in the datasheet of the semiconductor device; this practice is a norm when it comes to the design of cooling systems of semiconductors.

Using the analogy between the electrical and thermal systems, it becomes possible to construct a thermal network whereby each resistor represents the thermal resistance regarding a particular material or path, while each current source represents a source of power loss. Moreover, the temperature difference across a particular material is represented by the voltage difference across the resistor [32].

The thermal resistance of a material in °C/W is defined as its resistance to heat flow across a temperature gradient. In the datasheet of the IGBT modules, the thermal resistances (R_x) of the major heat flow paths are provided, the notation 'x' can be {j,C,S,A} to denote the junction, case, sink and ambient, respectively. In addition, the zero-order thermal resistance network [26] of the IGBT module shown in Figure 8, is adopted in this study. This thermal model matches the fast-computational time associated with the proposed online variable switching frequency algorithms. The thermal resistance of the heat sink is denoted as (R_{SA}). Based on Figure 8, the following relations can be deduced:

$$T_s = 6(P_Q + P_D)R_{SA} + T_a, \tag{25}$$

$$T_c = 6(P_Q + P_D)R_{CS} + T_s, \tag{26}$$

$$T_{jQ} = P_Q R_{jCQ} + T_c, \tag{27}$$

$$T_{jD} = P_{loss,D} R_{jCD} + T_c, \tag{28}$$

where T_s is the heat sink temperature, T_a is the ambient temperature, T_c is the case (or base-plates), T_{jQ} is the IGBT's junction temperature, and T_{jD} is the diode's junction temperature. All the temperatures are in °C.
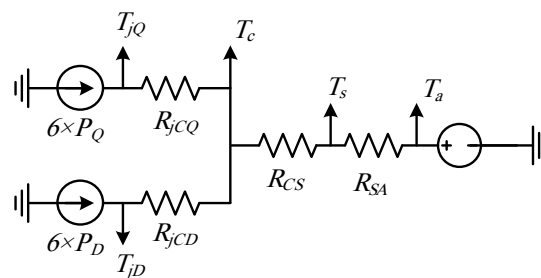

Figure 8. The IGBT power module's thermal resistance network.

5. Time Domain Current Ripple Analysis

Figure 9 shows the circuit diagram of the grid connected inverter, which includes an inductor (*L*) to represent the grid-inductance in series with a sinusoidal voltage source (v_g) for the grid to be represented. This representation is valid for any inverter that supplies motor loads and/or grids [33].
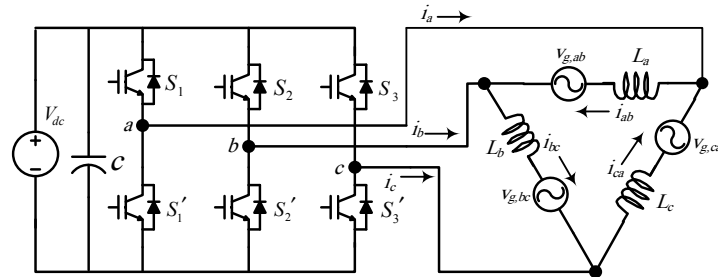

Figure 9. Δ-load connected to VSI.

Before proceeding with the current-ripple analysis based on time domain, the following assumptions are made:

- The input voltage is ripple-free.
- f_{sw} is relatively higher compared to the fundamental frequency.
- The modulating signals during each T_{sw} remain constant.
- The impact of dead-time is neglected.

From the circuit diagram of Figure 9, the voltage between phases *a* and *b* can be written as

$$v_{ab} = v_{g,ab} + L\frac{di_{ab}}{dt}, \tag{29}$$

where v_{ab} is the inverter's output line-line voltage, i_{ab} is the phase-current, and $v_{g,ab}$ is the line-line grid voltage.

As mentioned earlier, the load current consists of the ripple component and the fundamental-frequency component. Therefore, i_{ab} can be written as

$$i_{ab} = \bar{i}_{ab} + \hat{i}_{ab}, \tag{30}$$

where $\bar{i}_{ab}$ is the load current fundamental component and $\hat{i}_{ab}$ is the load current ripple component. Substituting Equation (30) in Equation (29), yields Equation (31), and then the load current ripple component can be expressed as in Equation (32):

$$v_{ab} = v_{g,ab} + L\left(\frac{d\bar{i}_{ab}}{dt} + \frac{\hat{i}_{ab}}{dt}\right), \tag{31}$$

$$\hat{i}_{ab} = \int \frac{v_{ab} - v_{g,ab}}{L} dt. \tag{32}$$

The term $d\bar{i}_{ab}/dt$ doesn't appear in Equation (32) because of the assumption that the fundamental component is constant within T_{sw}. The inductor resistance can be neglected, and since f_{sw} is much greater compared to the fundamental frequency, the current ripple component is placed under the assumption of rising and falling in a linear manner around the fundamental value. Using linear approximation, each segment of the current ripple is given as

$$\hat{i}_{ab} = \frac{t_2 - t_1}{L}(v_{t2} - v_{t1}), \tag{33}$$

where $\hat{i}_{ab}$ is the current ripple segment over the interval of time $(t_2 - t_1)$, v_{t1} is the voltage at time t_1 and v_{t2} is the voltage at time t_2.

The ripple component and the output line-line voltage of the load current at T_{sw} are shown in Figure 10. The ripple of the load current can be given as

$$\hat{i}_{ab} = -\frac{t - t_0}{L} v_{g,ab}; \text{ for } t_0 \leq t \leq t_1, \tag{34}$$

$$\hat{i}_{ab} = -\frac{T_0}{L} v_{g,ab} + \frac{t - t_1}{L}\left(V_{dc} - v_{g,ab}\right); \text{ for } t_1 \leq t \leq t_3, \tag{35}$$

$$\hat{i}_{ab} = -\frac{t - t_4}{L} v_{g,ab} + \frac{T_1 + T_2}{L}\left(V_{dc} - v_{g,ab}\right) - \frac{T_0}{L} v_{g,ab}; \text{ for } t_3 \leq t \leq t_4. \tag{36}$$
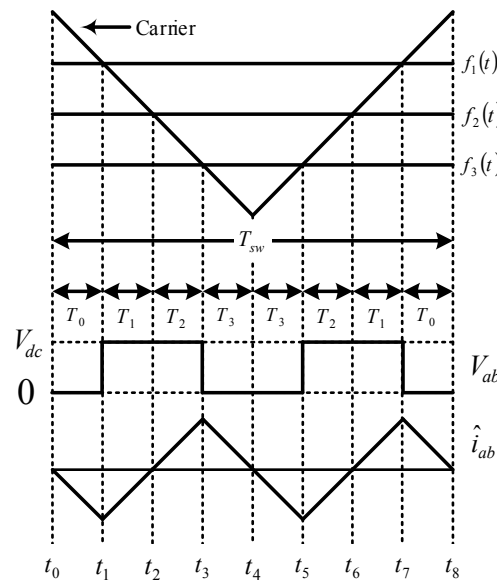

Figure 10. Load current ripple and output line-line voltage during a switching period.

The ripple current mean square value over T_{sw} (i.e., $\hat{I}_{ab}^2$) can be expressed as

$$\hat{I}_{ab}^2 = 2f_{sw}\int_{t_0}^{t_0 + t_4} \hat{i}_{ab}^2 dt = \frac{2V_{dc}^2 f_{sw}}{L^2}\left\{\int_0^{T_0} t^2 dt + \int_0^{T_3} t^2 dt + \int_0^{T_1 + T_2}\left[-T_0 + \left(\frac{V_{dc}}{v_{g,ab}} - 1\right)t\right]^2 dt\right\}, \tag{37}$$

$$\hat{I}_{ab}^2 = \frac{2V_{dc}^2 f_{sw}}{L^2}\left[\frac{T_0^3}{3} + T_0^2(T_1 + T_2) - \left(\frac{V_{dc}}{v_{g,ab}} - 1\right)T_0(T_1 + T_2)^2 + \left(\frac{V_{dc}}{v_{g,ab}} - 1\right)^2\frac{(T_1 + T_2)^3}{3} + \frac{T_3^3}{3}\right]. \tag{38}$$

The time intervals T_0, T_1, T_2 and T_3 can be related to T_{sw} as

$$T_0 = \left(\frac{1}{4} - \frac{1}{4}f_1(t)\right)T_{sw}, \tag{39}$$

$$T_1 = \left(\frac{f_1(t) - f_1(t)}{4}\right)T_{sw}, \tag{40}$$

$$T_2 = \left(\frac{f_3(t) - f_2(t)}{4}\right)T_{sw}, \tag{41}$$

$$T_3 = \left(\frac{1}{4} + \frac{1}{4}f_1(t)\right)T_{sw}, \tag{42}$$

$$f_1(t) = m\sin(\omega t); \; f_2(t) = m\sin\left(\omega t + \frac{2\pi}{3}\right); \; f_3(t) = m\sin\left(\omega t + \frac{4\pi}{3}\right). \tag{43}$$

Substituting Equation (43) in Equations (40), (41), and (42) yields

$$\hat{I}_{ab}^2 = \left(\frac{V_{dc}}{Lf_{sw}}\right)^2 \frac{m^2}{64} \sin^2\left(2\pi ft + \frac{\pi}{6}\right) \times \left[1 - \sqrt{3}m\sin\left(2\pi ft + \frac{\pi}{6}\right) + \frac{3}{4}m^2\right]. \tag{44}$$

To find the current ripple root mean square (*rms*) value over a fundamental period ($\hat{I}_{h,rms}$), Equation (44) is integrated over the fundamental period as in Equation (45):

$$\hat{I}_{h,rms} = \sqrt{\frac{1}{\pi} \int_{-\pi/6}^{5\pi/6} \hat{I}_{ab}^2 \, d\omega t}. \tag{45}$$

It should be noted that the integration was conducted over the period $[-\pi/6, 5\pi/6]$ and the symmetry justifies integration over a half period. Substituting Equation (44) in Equation (45) gives

$$\hat{I}_{h,rms} = \frac{mV_{dc}}{16Lf_{sw}} \sqrt{2 - \frac{16\sqrt{3}}{3\pi}m + \frac{3}{2}m^2}. \tag{46}$$

If it is a Y-connected load, Equation (46) yields

$$\hat{I}_{h,rms} = \frac{mV_{dc}}{16\sqrt{3}Lf_{sw}} \sqrt{2 - \frac{16\sqrt{3}}{3\pi}m + \frac{3}{2}m^2}. \tag{47}$$

The THD in the inductor current THD_i is given as

$$THD_i = \frac{\hat{I}_{h,rms}}{\bar{I}_{ab,rms}}, \tag{48}$$

where $\bar{I}_{ab,rms}$ is the fundamental current's *rms* value.

6. The Proposed VSF Algorithm

Generally, the manufacturers of grid-tied inverters specify the PWM switching frequency f_{sw} as a design value with respect to the rated operating conditions. Increasing f_{sw} reduces the *rms* value of the current ripple and therefore the total demand distortion *TDD* is reduced as well. However, the value of f_{sw} is limited by the heat dissipation capability of the semiconductor power switches and their associated cooling system. When the operating point of the inverter is below the rated conditions, the cooling system appears to be oversized since it is possible to increase the switching frequency and hence enhance the quality of the output current. Using the aforementioned premise, each operating condition can be considered as a design problem; however, the switching frequency is the only degree of freedom that is available in the problem design. Therefore, an algorithm that is able to improve the output power quality of the grid-tied inverter without changing the physical structure of the system is significant from an industrial point of view [34].

Increasing f_{sw} will increase the power losses and hence reduce the efficiency. However, the output power quality is improved. Since increasing or decreasing f_{sw} will improve one feature of the system and degrade the other, this means that a conflict between two desired objectives is met, which is a typical multi-objective optimization problem. In such problems, there is no unique optimal solution but rather a set (maybe infinite) of optimal solutions. The selection of one solution among the set of solutions is a degree of freedom left to the preference of the designer [35,36].

To obtain an optimal solution with a reduced computational complexity that is strictly required for an algorithm that can determine the optimal f_{sw} online (i.e., without heavy offline calculations that are stored in lookup tables), a weighted-sum objective function is defined as follows:

$$Min \quad \Psi(f_{sw}) = (1 - w) \times TDD(f_{sw}) + w \times P_{sw}(f_{sw}), \tag{49}$$

where Ψ is the optimization cost function to be minimized. f_{sw} is bounded by the upper and the lower permissible bounds, $f_{sw,l}$ and $f_{sw,u}$, respectively. $w \in \begin{bmatrix} 0 & 1 \end{bmatrix}$ is the trade-off factor. To this end, since each individual goal has distinct value, it is advisable to normalize both objectives in order to avoid misleading solutions as

$$\Psi_n = w \frac{P_{sw,total} - P_{sw,total}^{ideal}}{P_{sw,total}^{nadir} - P_{sw,total}^{ideal}} + (1 - w) \frac{TDD - TDD^{ideal}}{TDD^{nadir} - TDD^{ideal}}, \tag{50}$$

where Ψ_n is the normalized cost function, TDD^{ideal} is the TDD at $f_{sw,u}$, TDD^{nadir} is the TDD at $f_{sw,l}$, $P_{sw,total}^{ideal}$ is the least expected switching losses, and $P_{sw,total}^{nadir}$ is the highest acceptable switching losses.

Furthermore, the optimal value of f_{sw} (f_{sw}^{opt}) can be found by equating the first order derivative of Equation (50) to zero, that is:

$$\frac{d\Psi_n}{df_{sw}} = w \frac{1}{f_{sw,u} - f_{sw,l}} - (1 - w) \frac{f_{sw,u} f_{sw,l}}{f_{sw,u} - f_{sw,l}} \frac{1}{f_{sw}^2} = 0. \tag{51}$$

Rearranging Equation (51) yields

$$f_{sw}^{opt} = \sqrt{\frac{1 - w}{w} f_{sw,l} \times f_{sw,u}}. \tag{52}$$

As the operation and the loading conditions are varying, there is a change in the energy losses. Therefore, $f_{sw,u}$ changes. In other words, for every new condition that emerges, a new optimization problem is solved. The maximum allowable switching frequency ($f_{sw,u}$) can be expressed based on switching energy losses given in Equation (53). However, $f_{sw,l}$ is restricted by the highest allowable TDD, which is assumed to be 5%. The minimum allowable switching frequency can be expressed as in Equation (54):

$$f_{sw,u} = \frac{\pi \, P_{sw,total}^{nadir}}{6(_{on} + E_{off} + E_{rec})}, \tag{53}$$

$$f_{sw,l} = \left(\frac{mV_{dc}}{16\sqrt{3}L} \sqrt{2 - \frac{16\sqrt{3}}{3\pi}m + \frac{3}{2}m^2} \frac{1}{I_{L,rms}^{rated}} \right) \frac{1}{0.05}. \tag{54}$$

Making use of Equations (53) and (54), (52) can be rewritten as

$$f_{sw}^{opt} = \sqrt{\frac{1}{0.05} \left(\frac{mV_{dc}}{16\sqrt{3}L} \sqrt{2 - \frac{16\sqrt{3}}{3\pi}m + \frac{3}{2}m^2} \frac{1}{I_{L,rms}^{rated}} \right)} \times \sqrt{\frac{\pi \, P_{sw,total}^{nadir}}{6(_{on} + E_{off} + E_{rec})}} \times \sqrt{\frac{1 - w}{w}}. \tag{55}$$

The highest permissible losses are limited by the highest allowable T_{JQ} and T_{JD}. This value has to be evaluated for each new ambient temperature. Based on the thermal layout in Figure 8, the highest permissible total losses for each diode (P_{Dmax}) at a given ambient temperature can be given as in

Equation (56) and the highest permissible losses for each IGBT (P_{Qmax}) can be related to Equation (56) as shown in Equation (57):

$$P_{Dmax} = \frac{T_{jD,max} - T_a}{R_{JCD} + 6\left(R_{CS} + R_{SA} + \frac{R_{jCD}}{R_{jCQ}}(R_{CS} + R_{SA})\right)},$$

(56)

$$P_{Qmax} = \frac{R_{jCD}}{R_{jCQ}}P_{Dmax}.$$

(57)

From Equations (56) and (57), the highest permissible losses ($P_{sw,total}^{nadir}$) can be evaluated with a consideration of just the switching loss aspect as follows:

$$P_{sw,total}^{nadir} = 6\left(P_{Dmax}\left(1 + \frac{R_{jCD}}{R_{jCQ}}\right) - P_{CD} - P_{CQ}\right).$$

(58)

Figure 1 shows the implementation of the proposed algorithm in the FPGA platform. The operating conditions including the modulation index, the DC-link voltage, and grid current, and the power factor are used to estimate the conductions losses utilizing Equations (10) and (14) and the energy switching losses evaluating Equations (17), (18) and (22). From the power and energy losses' estimates, the optimal switching frequency is computed from Equation (55). Since the junction temperatures and power losses are mutually dependent, an iterative solution must be used as in Figure 11. It should be mentioned that the effect of the ambient temperature is taken into consideration as feedback from the case temperature, since the IGBT power module includes a thermistor that can be measured as in Figure 1.
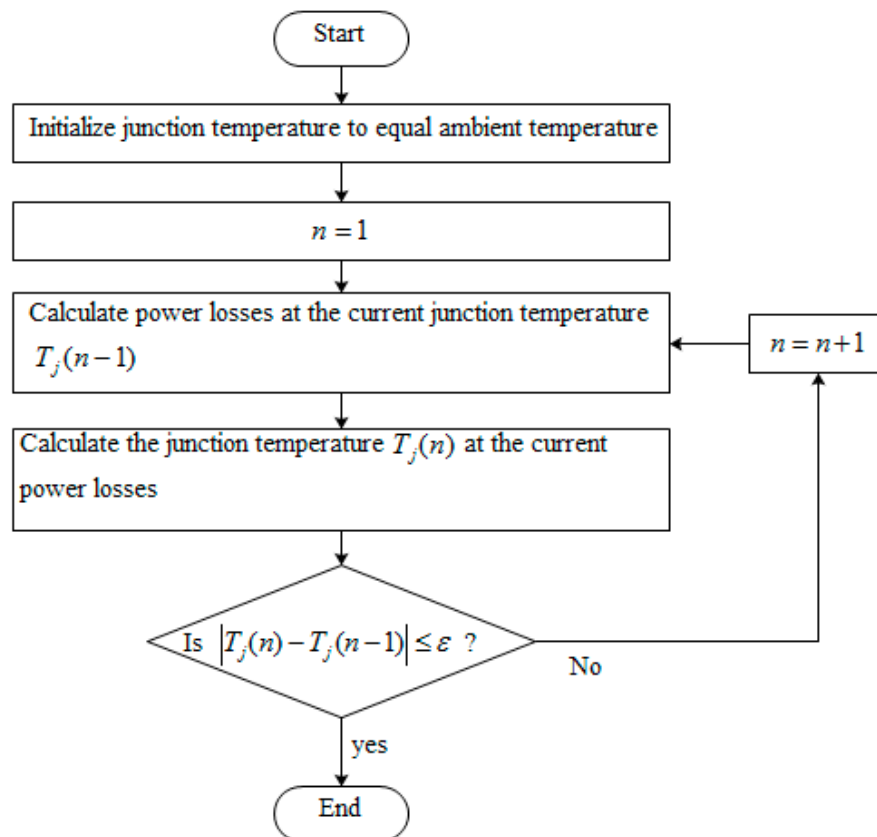

Figure 11. Flowchart of the iterative calculation of junction temperature.

7. The Experimental Results

Validating the significance of this proposed algorithm requires the setup of an experiment as in Figure 12. The experimental tests were performed on three-phase IGBT power module (Part Number: FP50R06KE3) cascaded with passive low pass inductor and capacitor (LC) filter output and supplying a Y-connected resistive load. Table 1 illustrates the system parameters and Table 2 depicts the optimal switching frequency at different loading conditions alongside total switching losses, *TDD*, and case temperature assuming a weighting factor of 0.6. As is evident, the proposed algorithm varies f_{sw} to obtain the best balance between the *TDD* and the switching losses based on inverter's loading conditions including the ambient temperature. When this system is at heavy loads, switching losses are high; therefore, the algorithm reduces f_{sw}, while keeping the *TDD* below the 5% limit (IEEE standard 519-2014). However, at light loads, the switching losses becomes low; hence, the algorithm increases the switching frequency for the output current quality to be enhanced.
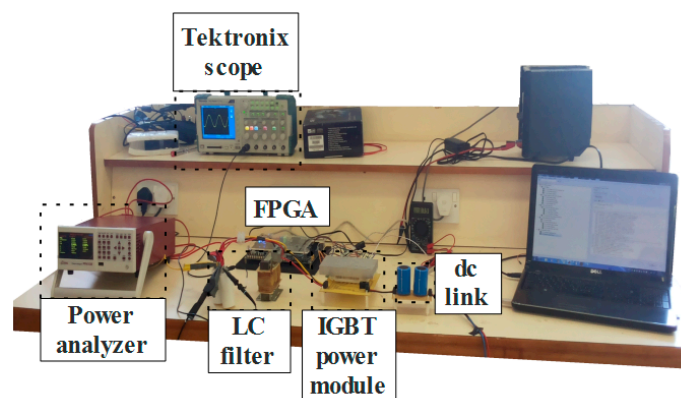

Figure 12. Experimental test-bed.

Table 1. The three-phase system parameters.

Parameters	Values
Ambient temperature (T_a)	20 °C
Filter inductance (L)	1.7 mH
Modulation index (m)	1
Filter capacitance (C)	10 μF
Input dc voltage (V_{dc})	200 V
Rated output current ($I_{L,rated}$)	5 A
Heat sink thermal resistance (R_{SA})	1.5 °C/W

Table 2. Algorithm response to load variation.

% of Rated Power	f_{sw} (kHz)	$P_{sw,total}$ (W)	*TDD* %	T_c (°C)
10	37.5	4.63	1.69	28.08
20	26.5	6.53	2.39	32.08
30	21.7	7.98	2.92	35.47
50	16.9	10.26	3.76	41.51
75	13.8	12.51	4.58	48.53
100	13.0	14.37	4.89	55.41

The measurement of the *TDD* was carried out by measuring the total harmonic distortion of the output current (THD_i) at certain loading conditions using the harmonic analysis functionality provided by a Tektronix oscilloscope (Model Number: TPS2024B). According to IEEE-519 *TDD* is defined as *"the total root-sum-square harmonic current distortion, in percent of the maximum demand load*

current". The calculated *TDD* is obtained from THD_i, the *rms* value of load current (i_{rms}) and the *rms* value of the rated current (i_{rms}^{rated}) as in Equation (59)

$$TDD = THD_i \frac{i_{rms}}{i_{rms}^{rated}}. \tag{59}$$

The measurement of the switching losses is initiated by measuring the steady-state case temperature at each operating condition by which the total power losses can be estimated. To extract the switching losses component, the experiment is performed again with fixed switching frequency while keeping other operating conditions unchanged, and, as a result, the conduction losses are unchanged as well. Since the switching losses are almost linearly related to the switching frequency, the switching losses can be deduced.

The following steps describe the experimental procedure in which switching losses are extracted:

(1) Measure the case (base plate) temperature by the solid state temperature sensors (negative temperature coefficient (NTC) thermistor) R_{NTC}. The temperature characteristic of this thermistor is shown in Figure 13 and Equation (60):

$$T_c = \frac{-26.48R_{NTC}^2 + 346.9R_{NTC} + 211.4}{R_{NTC}^2 + 5.345R_{NTC} + 0.9036}. \tag{60}$$

(2) From the measured case temperature and based on re-arranging of Equations (24)–(28), the total power losses is determined by Equation (61)

$$P_T = \frac{T_c - T_a}{R_{SA} + R_{CS}}. \tag{61}$$

(3) Under the same loading conditions, the switching frequency is varied, case temperature is measured, and losses are calculated.

(4) Based on the calculated power losses, the following set of Equations (62)–(65) can be computed:

$$P_T(f_{sw1}) = P_{CQ} + P_{CD} + \frac{E_{on} + E_{off} + E_{rec}}{\pi} f_{sw1}, \tag{62}$$

$$P_T(f_{sw2}) = P_{CQ} + P_{CD} + \frac{E_{on} + E_{off} + E_{rec}}{\pi} f_{sw2}, \tag{63}$$

$$P_T(f_{sw2}) - P_T(f_{sw2}) = \frac{E_{on} + E_{off} + E_{rec}}{\pi} (f_{sw2} - f_{sw1}), \tag{64}$$

$$P_T = \frac{P_T(f_{sw2}) - P_T(f_{sw2})}{f_{sw2} - f_{sw1}} f_{sw1}, \tag{65}$$

where f_{sw1} is the switching frequency of interest and f_{sw2} is the second switching frequency.

Validating how effective the proposed algorithm requires the experimental system to be tested with a fixed f_{sw} while constantly keeping the *TDD* at 2.5%. f_{sw} is selected as 25 kHz, which is approximately the middle point relative to the variable frequency range, with the system being tested under the same load conditions. Table 3 summarizes the performance of the inverter. Comparing the results from Tables 3 and 4, there is a reduction of the switching power losses at full load by about 51.6% using the proposed VSF algorithm, while the *TDD* is below the 5% limit. The decrease in the switching losses with the use of the proposed VSF algorithm is justified by the fact that the weight of 0.6 automatically leads the algorithm to favor the reduction of the switching power losses. Figure 14 gives the measured efficiency curves, which is for the whole inverter system alongside the fixed and VSF algorithms. It is obvious that the inverter efficiency is enhanced for a large array of load conditions.

Table 4 indicates a comparison between the calculated and experimental results. It can be shown that the power losses and *TDD* models are highly accurate.
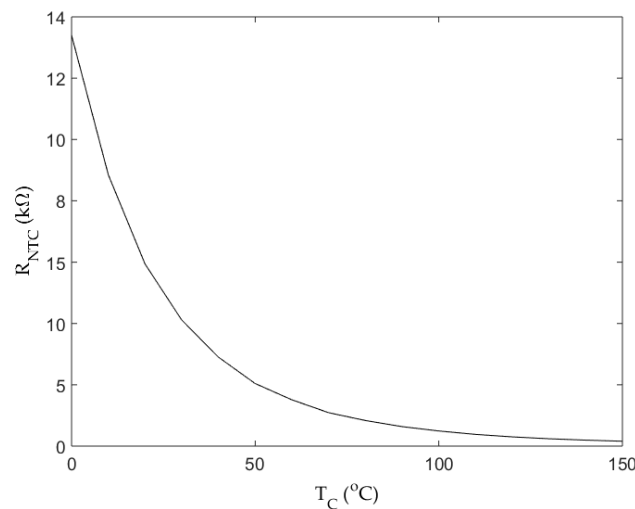
Figure 13. Infineon temperature characteristic of the NTC thermistor [30].

Table 3. Inverter performance f_{sw} = 25 KHz.

% of Rated Power	$P_{sw,total}$ (W)	T_c (°C)
10	3.10	25.73
20	6.14	31.49
30	9.18	37.28
50	15.17	48.97
75	22.53	63.76
100	29.73	78.76

Table 4. Comparison between the experimental and calculated results.

% of Rated Power	f_{sw} (kHz)	$P_{sw,total}$ (W)		TDD %	
		Cal.	Meas.	Cal.	Meas.
10	37.5	4.63	5.31	1.69	1.83
20	26.6	6.53	6.97	2.39	2.28
30	21.7	7.98	8.33	2.92	3.15
50	16.9	10.26	11.42	3.76	3.92

To further highlight the significance of the proposed algorithm, the California Energy Commission (CEC) efficiency of the inverter is measured under the fixed and VSF algorithms, the CEC efficiency is 97.3% using the proposed VSF algorithm, and 96.39% with the fixed f_{sw}. Therefore, it can be deduced from comparing the efficiencies of both algorithms that f_{sw} can be increased without degrading the efficiency of the inverter.

An interesting property related to the proposed VSF algorithm is the fact that the junction temperature variation under different load conditions tends to be lower than that one under fixed f_{sw}. As can be shown in Figure 15, the case temperature rate of change with the VSF algorithm is less than that of the fixed f_{sw}. This property holds even if more weight is given to the *TDD*. In other words, regardless of the selected weighting factor, the temperature profile when using the proposed algorithm will always have a slope that is under the one when using the fixed switching frequency. The importance of this property comes from the fact that the lifetime of the inverter is inversely proportional to the junction temperature difference [37–39].
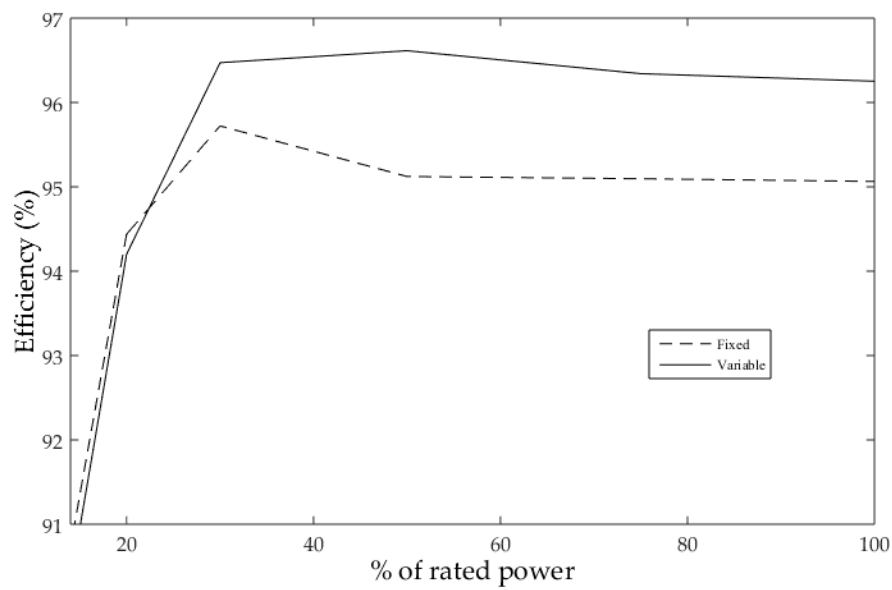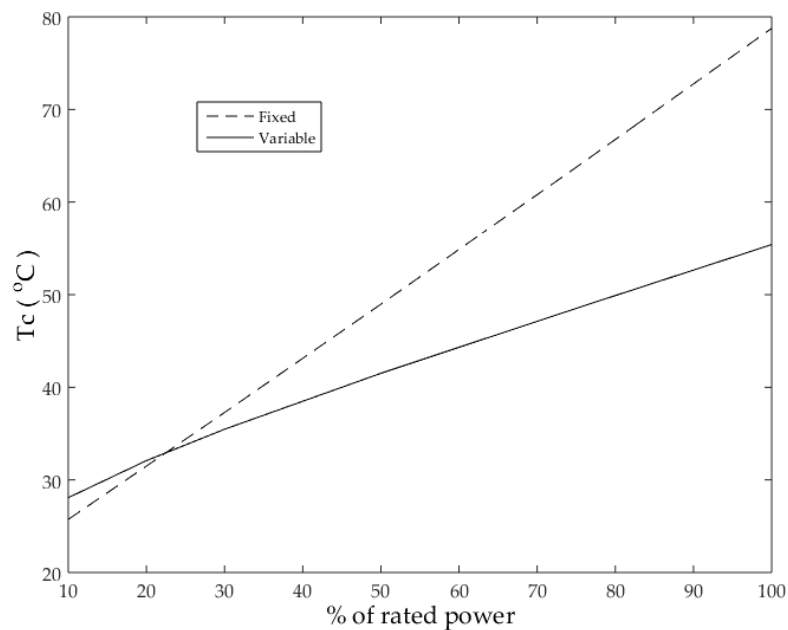
Figure 14. Measured efficiency curves.

Figure 15. Calculated output case temperature variation with fixed and the proposed VSF PWM.

8. Conclusions

This study achieves the development of an online adaptive switching algorithm. In this algorithm, f_{sw} tends to be varied online according to the loading conditions and the ambient temperature. Depending on the models developed in Sections 2 and 3, f_{sw} was expressed based on the operating conditions, and an optimization issue was created using the multi-objective optimization theory. It was shown that the algorithm increases over all the inverter's efficiency from 96.39% to 97.3% at full load without degrading the output power quality. The inverter's lifetime can be increased because of the limited case temperature rate of change as well. The implementation of the developed algorithm is straightforward and the optimization can be performed online without complex computations, by which the intensive offline calculations and lookup tables are totally avoided.

Author Contributions: S.A. and H.J.A. designed the research idea and the experimental setup. I.A.S. and A.K. updated the literature review and improved the quality of presentation. I.A.S. and A.K. reviewed the estimation of power loses equations in IGBT power module. I.A.S. and H.J.A. analyzed the results. A.K. and S.A. did the graphical work. All authors participated in providing answers to all comments from reviewers. All authors read and approved the final manuscript.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Chen, M.-H. Use of Three-Level Power Converters in Wind-Driven Permanent-Magnet Synchronous Generators with Unbalanced Loads. *Electronics* **2015**, *4*, 339–358. [CrossRef]
2. Al-Hoor, W.; Abu-Qahouq, J.A.; Huang, L.; Mikhael, W.B.; Batarseh, I. Adaptive Digital Controller and Design Considerations for a Variable Switching Frequency Voltage Regulator. *IEEE Trans. Power Electron.* **2009**, *24*, 2589–2602. [CrossRef]
3. He, X.F.; Zhang, Z.; Cai, Y.Y.; Liu, Y.F. A variable switching frequency hybrid control for ZVS dual active bridge converters to achieve high efficiency in wide load range. In Proceedings of the 29th Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Fort Worth, TX, USA, 16–20 March 2014; pp. 1095–1099.
4. Arikatla, V.; Qahouq, J.A.A. Dynamic digital variable switching frequency control scheme for power converters. In Proceedings of the 26th Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Fort Worth, TX, USA, 6–10 March 2011; pp. 253–257.
5. Kumar, A.C.B.; Narayanan, G. Variable switching frequency PWM technique for induction motor drive to spread acoustic noise spectrum with reduced current ripple. *IEEE Trans. Ind. Appl.* **2014**, *52*, 1–6. [CrossRef]
6. Jiang, D.; Wang, F. Variable Switching Frequency PWM for Three-Phase Converters Based on Current Ripple Prediction. *IEEE Trans. Power Electron.* **2013**, *28*, 4951–4961. [CrossRef]
7. Yang, F.; Taylor, A.R.; Bai, H.; Cheng, B.; Khan, A.A.; Lee, Y.J.; Nie, Z. Application of variable switching frequency PWM control with power loss prediction in surfaced-mounted permanent magnet synchronous motor. In Proceedings of the Transportation Electrification Asia-Pacific (ITEC Asia-Pacific), Beijing, China, 31 August–3 September 2014; pp. 1–4.
8. Yang, F.; Taylor, A.R.; Bai, H.; Cheng, B.; Khan, A.A. Using d–q Transformation to Vary the Switching Frequency for Interior Permanent Magnet Synchronous Motor Drive Systems. *IEEE Trans. Transp. Electrif.* **2015**, *1*, 277–286. [CrossRef]
9. Mao, X.; Ayyanar, R.; Krishnamurthy, H.K. Optimal Variable Switching Frequency Scheme for Reducing Switching Loss in Single-Phase Inverters Based on Time-Domain Ripple Analysis. *IEEE Trans. Power Electron.* **2009**, *24*, 991–1001.
10. Cao, B.; Chang, L. A variable switching frequency algorithm to improve the total efficiency of single-phase grid-connected inverters. In Proceedings of the 28th Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 17–21 March 2013; pp. 2310–2315.
11. Andersson, A.; Thiringer, T. Inverter losses minimization using variable switching frequency based on multi-objective optimization. In Proceedings of the International Conference on Electrical Machines (ICEM), Berlin, Germany, 2–5 September 2014; pp. 789–795.
12. Cao, W.; Wang, F.; Jiang, D. Variable switching frequency PWM strategy for inverter switching loss and system noise reduction in electric/hybrid vehicle motor drives. In Proceedings of the Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 17–21 March 2013; pp. 773–780.
13. Anuchin, A.; Gulyaeva, M.; Briz, F.; Gulyaev, I. Modeling of AC voltage source inverter with dead-time and voltage drop compensation for DPWM with switching losses minimization. In Proceedings of the International Conference on Modern Power Systems (MPS), Cluj-Napoca, Romania, 6–9 June 2017; pp. 1–6.
14. Abdelhakim, A.; Davari, P.; Blaabjerg, F.; Mattavelli, P. Switching Loss Reduction in the Three-Phase Quasi-Z-Source Inverters Utilizing Modified Space Vector Modulation Strategies. *IEEE Trans. Power Electron.* **2017**. [CrossRef]

15. Oñederra, O.; Kortabarria, I.; de Alegría, I.M.; Andreu, J.; Gárate, J.I. Three-Phase VSI Optimal Switching Loss Reduction Using Variable Switching Frequency. *IEEE Trans. Power Electron.* **2017**, *32*, 6570–6576. [CrossRef]

16. Bhattacharya, S.; Sharma, S.K.; Mascarella, D.; Joós, G. Subfundamental Cycle Switching Frequency Variation for Switching Losses Reduction of a Two-Level Inverter Traction Drive. *IEEE Trans. Transp. Electrif.* **2017**, *3*, 646–655. [CrossRef]

17. Charumit, C.; Kinnares, V. Discontinuous SVPWM Techniques of Three-Leg VSI-Fed Balanced Two-Phase Loads for Reduced Switching Losses and Current Ripple. *IEEE Trans. Power Electron.* **2015**, *30*, 2191–2204. [CrossRef]

18. Golwala, H.; Chudamani, R. New Three-Dimensional Space Vector-Based Switching Signal Generation Technique Without Null Vectors and With Reduced Switching Losses for a Grid-Connected Four-Leg Inverter. *IEEE Trans. Power Electron.* **2016**, *31*, 1026–1035. [CrossRef]

19. Xia, Y.; Roy, J.; Ayyanar, R. Optimal variable switching frequency scheme for grid connected full bridge inverters with bipolar modulation scheme. In Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, OH, USA, 1–5 October 2017; pp. 4260–4266.

20. Li, Q.; Jiang, D. Variable Switching Frequency PWM Strategy of Two-Level Rectifier for DC-link Voltage Ripple Control. *IEEE Trans. Power Electron.* **2017**. [CrossRef]

21. Ramirez, F.; Pacas, M. Finite Control Set Model Based Predictive Control of a PMSM with Variable Switching Frequency and Torque Ripple Optimization. In Proceedings of the PCIM Europe International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 10–12 May 2016; pp. 1–8.

22. Pai, P.; Reiter, T.; Maerz, M. A New Behavioral Model for Accurate Loss Calculations in Power Semiconductors. In Proceedings of the PCIM Europe International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 10–12 May 2016; pp. 1–9.

23. Rocabert, J.; Luna, A.; Blaabjerg, F.; Rodríguez, P. Control of Power Converters in AC Microgrids. *IEEE Trans. Power Electron.* **2012**, *27*, 4734–4749. [CrossRef]

24. You, K.; Rahman, M.F. Analytical Model of Conduction and Switching Losses of Matrix-Z-Source Converter. *J. Power Electron.* **2009**, *9*, 275–287.

25. Reichl, J.; Lai, J.S.; Hefner, A.; Ortiz-Rodriguez, J.; Duong, T. Design Optimization of Hybrid-Switch Soft-Switching Inverters using Multi-Scale Electro-Thermal Simulation. *IEEE Trans. Power Electron.* **2017**, *32*, 503–514. [CrossRef]

26. Bazzi, A.M.; Krein, P.T.; Kimball, J.W.; Kepley, K. IGBT and Diode Loss Estimation under Hysteresis Switching. *IEEE Trans. Power Electron.* **2012**, *27*, 1044–1048. [CrossRef]

27. Bierhoff, Q.M.H.; Fuchs, F.W. Semiconductor losses in voltage source and current source IGBT converters based on analytical derivation. In Proceedings of the 35th IEEE Annual Power Electronics Specialists Conference, Aachen, Germany, 20–25 June 2004; pp. 2836–2842.

28. Blaabjerg, F.; Pedersen, J.K.; Sigurjonsson, S.; Elkjaer, A. An extended model of power losses in hard-switched IGBT-inverters. In Proceedings of the 31st IAS Annual Meeting, San Diego, CA, USA, 6–10 October 1996; pp. 1454–1463.

29. Kharitonov, S.A.; Petrov, M.A.; Korobkov, D.V.; Maslov, M.A.; Zhoraev, T.Y. A principle of calculation dynamic and static power losses with hard-switching IGBT. In Proceedings of the 6th Annual International Siberian Workshop and Tutorials on, Altai, Russia, 1–5 July 2005; pp. 147–149.

30. Infineon. EconoPIMTM 2 600V three phase PIM IGBT module with Trench/Field stop IGBT3, Emitter Controlled 3 diode and NTC. FP50R06KE3 datasheet ver 2.0. April 2013.

31. Albarbar, A.; Batunlu, C. *Thermal Analysis of Power Electronic Devices Used in Renewable Energy Systems*; Springer: New York, NY, USA, 2017.

32. Kojima, T.; Yamada, Y.; Nishibe, Y.; Torii, K. Novel RC Compact Thermal Model of HV Inverter Module for Electro-Thermal Coupling Simulation. In Proceedings of the 4th Power Conversion Conference, Nagoya, Japan, 2–5 April 2007; pp. 1025–1029.

33. Grandi, G.; Loncarski, J.; Dordevic, O. Analysis and Comparison of Peak-to-Peak Current Ripple in Two-Level and Multilevel PWM Inverters. *IEEE Trans. Ind. Electron.* **2015**, *62*, 2721–2730. [CrossRef]

34.　Jamal, H.; Albatran, S.; Smadi, I. Variable switching frequency algorithm for optimal tradeoff between switching losses and total demand distortion in grid-tied three-phase voltage-source inverters. In Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, USA, 18–22 September 2016.

35.　Deb, K. *Multiobjective Optimization Using Evolutionary Algorithms*; Wiley: New York, NY, USA, 2001.

36.　Hillermeier, C. *Nonlinear Multiobjective Optimization*; Birkhauser Verlag: Basel, Switzerland, 2001.

37.　Durand, C.; Klingler, M.; Coutellier, D.; Naceur, H. Power Cycling Reliability of Power Module: A Survey. *IEEE Trans. Device and Mater. Reliab.* **2016**, *16*, 80–97. [CrossRef]

38.　Diaz Reigosa, P.; Wang, H.; Yang, Y.; Blaabjerg, F. Prediction of Bond Wire Fatigue of IGBTs in a PV Inverter under a Long-Term Operation. *IEEE Trans. Power Electron.* **2016**, *31*, 7171–7182. [CrossRef]

39.　Choi, U.M.; Joergensen, S.; Blaabjerg, F. Advanced Accelerated Power Cycling Test for Reliability Investigation of Power Device Modules. *IEEE Trans. Power Electron.* **2016**, *31*, 8371–8386. [CrossRef]