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EMI Filter Design for a Single-stage Bidirectional and Isolated AC–DC Matrix Converter

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Abstract: This paper describes the design of an electromagnetic interference (EMI) filter for the high-frequency link matrix converter (HFLMC). The proposed method aims to systematize the design process for pre-compliance with CISPR 11 Class B standard in the frequency range 150 kHz to 30 MHz. This approach can be extended to other current source converters which allows time-savings during the project of the filter. Conducted emissions are estimated through extended simulation and take into account the effect of the measurement apparatus. Differential-mode (DM) and common-mode (CM) filtering stages are projected separately and then integrated in a synergistic way in a single PCB to reduce volume and weight. A prototype of the filter was constructed and tested in the laboratory. Experimental results with the characterization of the insertion losses following the CISPR 17 standard are provided. The attenuation capability of the filter was demonstrated in the final part of the paper.

Keywords: EMI filter; electromagnetic compatibility; AC–DC power converters; electromagnetic interference filter; matrix converters; current source; power density; battery energy storage systems; battery chargers

1. Introduction

Power electronics is making profound changes within the transportation sector [1,2] and the electric power system [3,4]. Bidirectional AC–DC converters are required for several applications, such as battery energy storage systems (BESS) [2,5], chargers for electric vehicles (EVs) [6–8], uninterruptible power supplies (UPS) [9], solid-state transformers (SST) [10], and DC microgrids [11]. The development of new wide bandgap power semiconductors combined with enhanced modulations and control techniques are contributing for the miniaturization and efficiency improvement of the power electronics converters [12]. This is followed by an increase of the switching frequency of the power semiconductors. As a result, conducted emissions (CE) with higher intensity are generated in the measurement range of the electromagnetic compatibility (EMC) standards. In this way, an additional effort is necessary in the design of the electromagnetic interference (EMI) filter included in the input of the power converters in order to comply with the standards [13]. A careful dimensioning of the EMI filter is also essential to ensure the adequate power factor in all operating range and to achieve a high power quality without penalizing the efficiency, volume and cost of the system.

Matrix converters (MC) are one of the most interesting families of converters due to its unique and attractive characteristics [14]. By employing an array of controlled four-quadrant power switches, the MC enables AC–AC conversion without any intermediate energy storage element [15]. The high-frequency link matrix converter (HFLMC) is a single-stage bidirectional and isolated AC–DC energy conversion system [16]. The new modulation proposed in [17] and patented in [18] allows

independent control of active and reactive power (PQ control) as well as the DC current in the battery pack. By exploring the MC attributes, circuit volume and weight can be reduced, and a longer service life is expected when compared with equivalent DC-link based solutions [16,19,20]. However, due to its complex power structure, it presents EMC challenges that have to be studied in order to ensure compliance with the international standards by designing the necessary EMI filter.

Several approaches for the design of differential-mode (DM) and common-mode (CM) filtering stages for direct and indirect matrix converters (MC) were proposed in [20–33]. However, in spite of the long history of this question, until now there has been no complete systematization regarding which topologies and damping methods should be used for each DM and CM filtering stage. Among these works, there are also some procedures of design and formulas that simply do not match between different papers, which may mislead or confuse the reader. Additionally, these works do not show the complete design process from the requirements specification until the experimental characterization of the insertion losses. According to our best knowledge, this is the first work in literature that propose a complete design of EMI filter for the HFLMC. The main contribution of this paper is setting up a systematic methodology for the design process of the HFLMC's EMI filter for CISPR 11 Class B pre-compliance. This design process also takes into account the modeling of the measurement equipment, such as the Line Impedance Stabilizing Network (LISN) and the Test Receiver (TR), in order to better predict the effectiveness of the designed EMI filter. Furthermore, a practical way to characterize the insertion losses according the CISPR 17 standard is fully described and supported by experimental results. It is worth noting that this is the same procedure followed by the manufacturers to characterize their EMI filters. In addition, this is the typical information available in the EMI filter datasheet and is very useful to compare the effectiveness of different filters.

The manuscript is organized as follows: the HFLMC is briefly presented in Section 2. Then, the applicable standards and the measurement approach of CE are described in Section 3. The detailed design of DM and CM filtering stages is explained in Sections 4 and 5, respectively. Section 6 presents the proposed integration strategy of the different filtering stages. The experimental results are shown in Section 7. Finally, Section 8 draws conclusions and proposes future work.

2. High-Frequency Link Matrix Converter

Figure 1 shows the HFLMC proposed for single-stage bidirectional and isolated AC–DC energy conversion. Each bidirectional switch S_{xy} is composed of two transistors: S_{xy1} and S_{xy2} ($x = a, b, c$ and $y = P, N$) in a common-source configuration. Command signals for the power semiconductors are generated by the modulation proposed in [17] and patented in [18]. The MC applies voltage v_p to the high-frequency transformer (HFT) [34]. The full-bridge produces i_o by impressing v_s in the HFT secondary. Finally, the output filter reduces the ripple in the DC current i_{DC} that charges and discharges the battery pack.

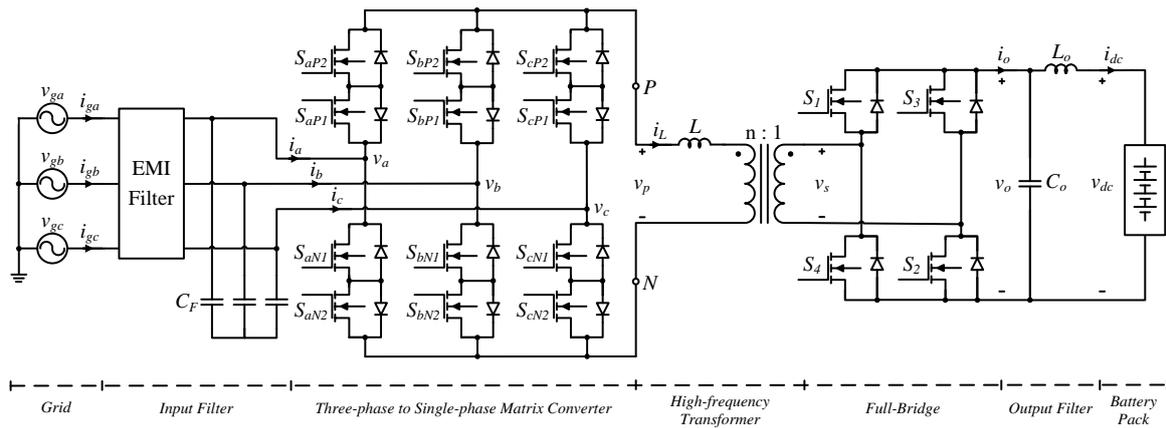


Figure 1. Circuit schematic of the high-frequency link matrix converter.

The EMI filter is projected to attenuate the noise present on currents $i_{a,b,c}$ generated by the three-phase to single-phase matrix converter. For this reason, the matrix converter side is considered the input of the filter and the grid side the output. It is expected that the conducted noise existent in currents $i_{ga,b,c}$ be within the limits specified in the international standards.

3. Standards and CE Measurement

The CE are generated by harmonics present in the input current of the MC, $i_i = [i_a, i_b, i_c]$, where i_a , i_b and i_c are the phase currents. EMC standards classify the CE according to the frequency range [35]. Low-frequency harmonics are typically measured up to 2 kHz (40th harmonic) as defined by IEC 61000-3-2 [36]. Section 6 presents the low-frequency (LF) harmonics measured for this converter and compared with IEC 61000-3-2 Class A limits. Regarding the HF conducted emissions, CISPR 11 [37] specifies the limits for frequencies from 150 kHz to 30 MHz. These emissions can be estimated by simulating the converter operation without any input filter at nominal conditions: $P_{nom} = 10$ kW, line-to-neutral grid voltage $V_{g,ln} = 230$ V, grid frequency $f_g = 50$ Hz and output voltage $V_{DC} = 380$ V. A simulation model of the HFLMC was implemented in GeckoCIRCUITS (v1.7.2 Professional, Gecko-Simulations A.G., Dübendorf, Switzerland) [38]. This software has a measure block that performs analysis according to the CISPR 16 [39] standard using the time domain simulation data. Similar to a test receiver (TR), it is possible to select different signal processing options: average (AVG), quasi-peak (QP) or peak detection. The first step of the filter design is to specify the maximum admissible CE levels. Due to the type of application, the QP limits of the CISPR 11 Class B curve will be considered. A line impedance stabilizing network (LISN) is connected between the grid and the device under test (DUT) in order to provide a known impedance and ensure the reproducibility of the measurements [40]. Then, a TR calculates the CE in "dBμV" through the measurement of the voltage at the LISN output port, V_{TR} . An equivalent impedance of $50 \Omega / 50 \mu\text{H}$ is specified by the CISPR 16 standard for the TR/LISN. The LISN's transfer function from V_{TR} to DUT's input current is [41]:

$$G_{LISN}(s) = \frac{V_{TR}(s)}{I_{dut}(s)} = \frac{s^2 L_{LISN} C_{LISN} R_{TR}}{s^2 L_{LISN} C_{LISN} + s R_{TR} C_{LISN} + 1} \quad (1)$$

where $R_{TR} = 50 \Omega$, $L_{LISN} = 50 \mu\text{H}$ and $C_{LISN} = 250$ nF.

4. Design of Differential-Mode Filter

4.1. Spectrum of the Converter Input Current

Due to the symmetry of the converter and the measurement system, the DM input filter can be projected considering a single-phase equivalent circuit [27]. Figure 2a shows the spectrum of the input

current of one phase, $I_{dm}(j\omega)$, obtained from simulation. Since no circuit element is connected between the lines and the ground (PE), only DM current is present at $I_{dut}(s)$. As can be seen, the first significant harmonic content appears around the switching frequency, $f_s = 20$ kHz. Other harmonics are also present at frequencies multiple of f_s . The first switching frequency harmonic inside the measurement range appears at 160 kHz. A zoom around this frequency is depicted in Figure 2b.

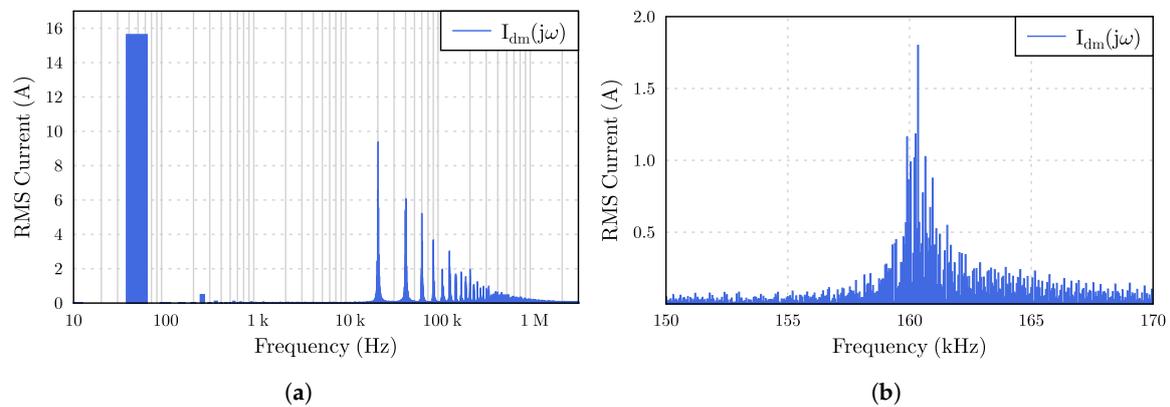


Figure 2. (a) frequency spectrum of the converter input current $I_{dm}(j\omega)$; (b) zoom around the first switching frequency harmonic above 150 kHz.

4.2. Spectrum of the Measured Voltage

The spectrum of V_{TR} can be determined by the multiplication of $I_{dm}(j\omega)$ with Equation (1). Figure 3 depicts the spectrum of $V_{TR}(j\omega)$ at the LISN’s output terminals along with the maximum and minimum estimation of the CE levels using QP detection. The exact QP values will be between the Max_{TR} and Min_{TR} curves. Further details about the modeling of the TR and the determination process of these curves are described in [23].

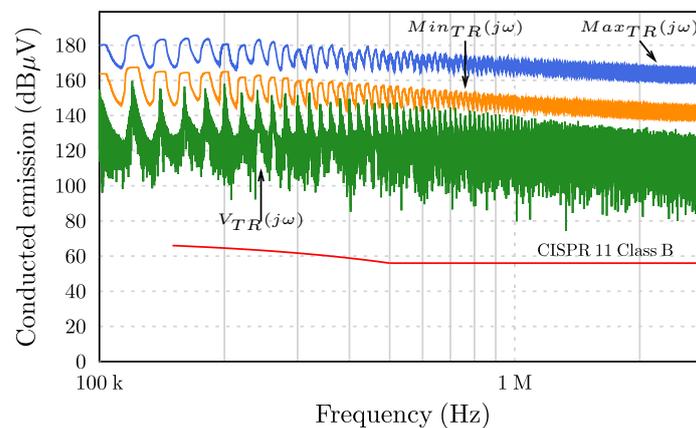


Figure 3. TR measurement without the DM filter: maximum and minimum estimation of CE along with the spectrum of $V_{TR}(j\omega)$.

4.3. Required Attenuation

The required attenuation for the DM filter can be estimated without the need for calculating the exact QP values. The predicted CE level at 160 kHz by Max_{TR} curve is 182.9 dB μ V. By analysing this curve, the next switching frequency harmonic appears at 180 kHz and requires lower attenuation. Thus, the filter design will focus on the emissions at 160 kHz. The limit specified at this frequency by CISPR 11 is $Limit_{CISPR,160kHz} = 65.5$ dB μ V. A margin of 6 dB is added in order to account for possible inaccuracies in CE estimation, and also for the parasitics of the inductive and capacitive

components [41]. In this way, the design process can be faster since the parasitic effects are not considered in the first step. Finally, the required attenuation of the DM filter at 160 kHz is:

$$Att_{req,DM} = Max_{TR,160kHz} - Limit_{CISPR,160kHz} + Margin = 123.4 \text{ dB.} \quad (2)$$

4.4. Topology

In theory, there are a large number of filter topologies that can be employed for EMI filtering. However, a low number of topologies are used due to cost and complexity reasons [41]. The second-order LC circuit is a very common topology employed as the input filter of MC [42]. In order to minimize the resonance that occurs at the filter, natural frequency, active and passive damping solutions were proposed in [21,22,43]. Passive damping is achieved by adding a resistor in series or in parallel with an inductor or capacitor. Considering the simple LC circuit, it was demonstrated in [25] that the minimum power losses are obtained with a resistor connected in parallel with the inductor. Moreover, this solution also reduces the global cost and volume of the input filter [14]. More complex damping networks can be obtained by adding an additional inductor or capacitor in series or in parallel with the damping resistor [22]. The objective of these damping networks is to provide passive damping to a filter without increasing excessively the power dissipation. By modifying the peak output impedance, this damping aims to facilitate the controller design and avoid large oscillations during transients [41]. Figure 4 shows two LC filter topologies with single resistor damping networks [22]. Both have a high frequency attenuation asymptote given by $1/(\omega^2 L_f C_f)$, which is identical to the original undamped LC filter. For the shunt RC damping network, C_{fd} blocks the DC current in order to avoid significant power losses in R_d . However, the large total capacitance reduces the power factor for low-power operation making this solution unattractive.

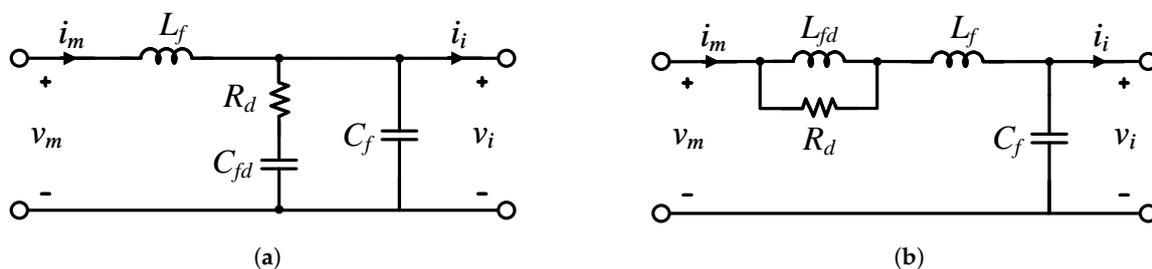


Figure 4. Two LC filter topologies with single resistor damping networks. (a) shunt RC damping network; (b) series RL damping network.

Regarding the series RL damping network, L_{fd} provides a DC bypass to avoid significant power dissipation in R_d . Therefore, both inductors must be rated for the peak DC current. The output impedance of the LC filter is dominated by the inductor impedance at a low frequency and by the capacitor impedance at a high frequency [44]. Both asymptotes intersect at the filter resonant frequency:

$$f_0 = \frac{1}{2\pi\sqrt{L_f C_f}}. \quad (3)$$

As previously discussed, $V_{TR}(j\omega)$ is dependent on the DUT's input current. Therefore, $I_{dm}(j\omega)$ must be reduced in order to generate CE within the imposed limits. Transfer function $H_{lcr1}(s)$, which relates I_{dm} with I_i , is defined in Equation (4). The magnitude of $H_{lcr1}(s)$ characterizes the attenuation capability of a single-stage LC filter with series RL damping network (cf., Figure 4b):

$$H_{lcr1}(s) = \frac{sL_{fd} + R_d}{s^3 C_f L_f L_{fd} + s^2 C_f R_d (L_f + L_{fd}) + sL_{fd} + R_d}. \quad (4)$$

A compromise between damping and the size of L_{fd} must be done during the design process [44]. The damping ratio n_d defines the relation between inductor L_{fd} and L_f . For practical purposes, a unitary damping ratio is interesting since only one type of inductor needs to be built/purchased. According to [41], this solution also results in acceptable losses on R_d . As demonstrated in [22], the optimum damping resistance for the series RL damping network can be calculated as:

$$R_d = \sqrt{\frac{L_f}{C_f} \frac{1+n_d}{n_d}} \sqrt{\frac{2(1+n_d)(4+n_d)}{(2+n_d)(4+3n_d)}} \tag{5}$$

Figure 5 shows the impact of different damping factors in terms of resonance of $H_{lcr1}(s)$ for $C_f = 20 \mu\text{F}$ and $L_f = 60 \mu\text{H}$. As expected, the peak in the magnitude is reduced when the damping is increased. Simultaneously, the frequency at which this peak occurs also decreases as damping rises. Nevertheless, the low and high frequency asymptotes are not affected by the damping factor.

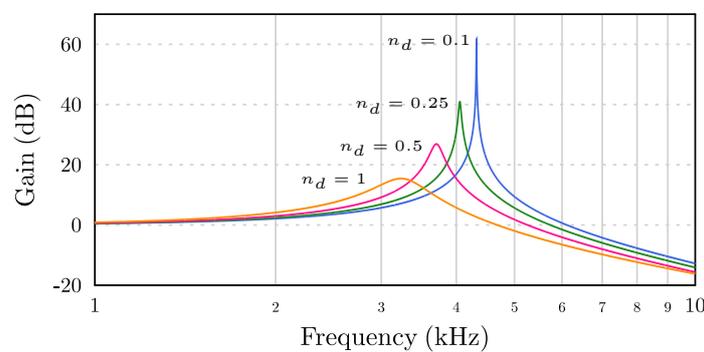


Figure 5. Impact of different damping factors in transfer function $H_{lcr1}(s)$.

For a given attenuation, the cascade connection of multiple LC filter stages allows the reduction of volume and weight when compared to a single-stage LC filter [44]. This is achieved by increasing the cutoff frequencies of the multiple stages resulting in smaller inductance and capacitance values. Nevertheless, the interaction between cascaded LC filter stages can provoke additional resonances and increased output impedance. An approach to reduce this interaction is by selecting gradually smaller cutoff frequencies as it nears the filter output [22]. In other words, higher attenuation is required for the stages near the filter output to improve system stability.

4.5. Components

In order to provide the required attenuation, a three-stage filter as shown in Figure 6 is employed. Stage 1 and Stage 2 are formed by LC filters with series RL damping networks, and Stage 3 is an undamped LC filter formed by C_3 and L_3 .

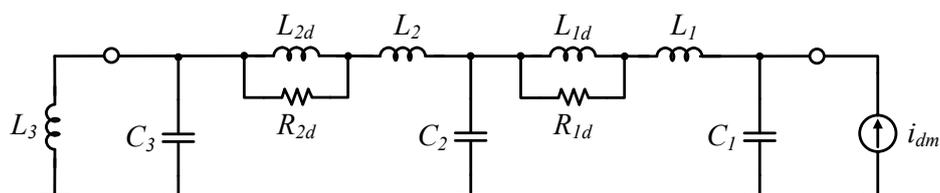


Figure 6. Equivalent single-phase circuit of the DM filter.

The DM capacitors draw reactive current from the grid, which decreases the operating power factor (PF). In order to have a minimum power factor during a light load operation, the total capacitance must be limited to the converter nominal power. In [45], the authors suggest that the PF must be at least 0.9 for operation at 10% of P_{nom} . Other authors consider that a 0.8 power factor for the same

operating conditions is reasonable [28]. The capacitance limitation can also be specified in terms of the absolute value for the reactive power. For instance, in [20], it is proposed that the reactive power drawn by the input filter must be restricted to 15% of P_{nom} . Assuming a small voltage drop for the fundamental component across the filter inductors, the total reactive power absorbed can be calculated by Equation (6). Considering this last criteria, the maximum capacitance per phase must be restricted to $C_{f,total} \leq 30 \mu\text{F}$:

$$Q_{C_f} \approx 3 \cdot 2\pi \cdot f_g \cdot C_{f,total} \cdot V_{g,ln}^2 \quad (6)$$

4.5.1. Stage 1

The matrix converter is a voltage-fed topology and behaves as a current source at its input. Capacitor C_1 (C_F in Figure 1) is placed at the MC input in order to limit the voltage ripple and ensure a correct system operation. For the worst operations conditions, the peak current at the MC input is $\hat{I}_i = 37 \text{ A}$. By defining $\delta_{vC_f,pp}$ as the maximum peak-to-peak voltage ripple, the minimum required capacitance can be calculated as [46]:

$$C_1 \geq \frac{\hat{I}_i}{1.1 \cdot V_{g,ln} \cdot 2\pi \cdot f_s \cdot \delta_{vC_f,pp}} \quad (7)$$

By limiting $\delta_{vC_f,pp}$ to about 5–10% of the nominal input voltage [41,46], the minimum required capacitance must be between 11.6 and 23.2 μF . Due to the discrete availability of capacitance values and also for practical implementation reasons, capacitor C_1 is selected to 20 μF .

The magnitude of the LF current harmonics can be affected if the resonant frequency (f_0) of the different filter stages is near the measurement range (up to 2 kHz). However, the resonant frequency must be significantly lower than the switching frequency in order to provide sufficient attenuation at $f = f_s$. Therefore, it is common to choose a resonant frequency between 20 times the grid frequency and about one-third of the switching frequency [26]. Considering this criteria, the resonant frequency for Stage 1 must be between 1 and 6.66 kHz. As previously discussed, the attenuation for this stage must be higher than the other stages, resulting in a lower resonant frequency for Stage 1 when compared to Stage 2. The attenuation for Stage 1 is selected as $Att_{Stage1} = 0.5 \cdot Att_{req,DM}$, which by the following:

$$f_{0,Stage1} = \frac{160\text{kHz}}{\sqrt{10^{\frac{Att_{Stage1}}{20}}}} \quad (8)$$

results in $f_{0,Stage1} = 4588 \text{ Hz}$. Considering C_1 and Equation (3), L_1 is calculated as 60 μH . For $n_{1d} = 1$, the damping network is composed by $L_{1d} = 60\mu\text{H}$ and $R_{1d} = 3.4 \Omega$ according to Equation (5).

4.5.2. Stage 2

For practical reasons, L_2 and L_{2d} are selected to be equal to L_1 and L_{1d} . By defining $Att_{Stage2} = 0.35 \cdot Att_{req,DM}$, the resonant frequency of Stage 2 needs to be $f_{0,Stage2} = 13316 \text{ Hz}$. Considering L_2 and Equation (3), C_2 is calculated as 2.3 μF . Due to the discrete availability of capacitance values, C_2 is selected to be 2.2 μF . Finally, the unitary damping ratio results in $R_{2d} = 10 \Omega$.

4.5.3. Stage 3

The third stage of the filter is composed by C_3 in combination with L_3 . During test experiments, L_3 corresponds to the inner inductance of the LISN, L_{LISN} . For normal operation, L_3 coincides with the grid inductance, L_g . Although the grid inductance can vary significantly depending of the PCC, for this analysis, $L_g = 50 \mu\text{H}$ is considered, following the reference network defined in IEC 61000-3-3 [47]. This stage must provide the remainder attenuation, which can be written as $Att_{Stage3} = Att_{req,DM} - Att_{Stage1} - Att_{Stage2}$. Therefore, the resonant frequency of Stage 3 needs to be $f_{0,Stage3} = 53204 \text{ Hz}$. Considering $L_3 = 50 \mu\text{H}$, the respective capacitor is chosen to be $C_3 = 180 \text{ nF}$.

4.6. Evaluation of the DM Filter

By combining all three stages, the complete transfer function H_{dm} from I_i to I_{dm} can be obtained. Figure 7 depicts the frequency response of the DM filter. As required, a 123 dB attenuation is provided at 160 kHz. The effect of the damping networks is perceptible by comparing the gain at $f_{0,Stage1}$ and $f_{0,Stage2}$ with the gain at $f_{0,Stage3}$.

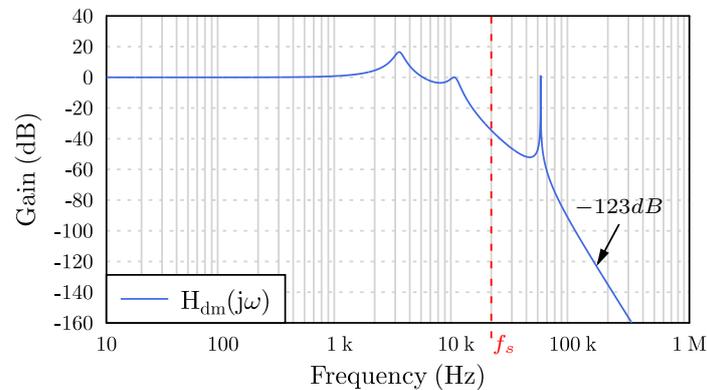


Figure 7. Frequency response of the DM filter: magnitude of H_{dm} , the transfer function from I_i to I_{dm} .

Figure 8 depicts Max_{TR} and Min_{TR} for the converter operation with the DM filter. As can be seen, the maximum curve for the predicted QP values is below the limits specified by the CISPR 11 Class B curve and the selected margin of 6 dB can be observed. Thus, the DM filter design is considered to be concluded.

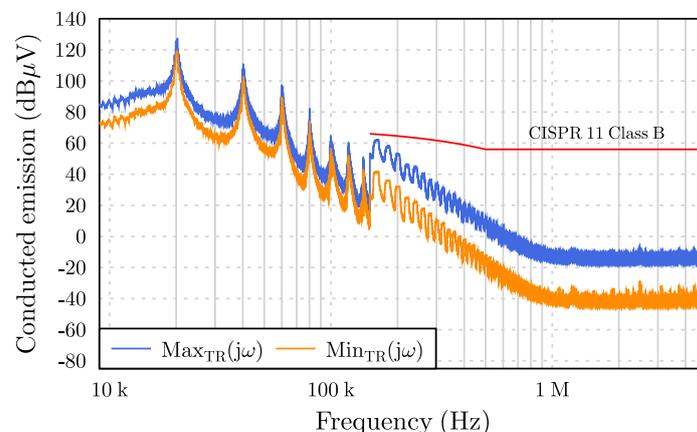


Figure 8. TR measurement with DM filter: maximum and minimum estimation of CE.

5. Design of the Common-Mode Filter

5.1. Common-Mode Voltage

The CM voltage generated by the matrix converter induces a circulating current, i_{cm} , through the converter and the ground (see Figure 9). This current closes the loop through the TR/LISN impedance resulting in CE that must be within the limits specified by CISPR 11. Silicon Carbide (SiC) MOSFET C2M0025120D is used for the converter implementation. The parasitic capacitance from the semiconductor to the heat sink per unit area is approximated by 20 pF/cm^2 [32]. Considering this reference value, the parasitic capacitance of all the matrix converter's semiconductors is $C_{gh} = 600 \text{ pF}$. Regarding the transformer interwinding capacitance and the stray primary side wiring capacitance, it is difficult to estimate these values without making measurements. For this reason, a 1.2 nF capacitance is added to the simulated circuit in order to take into account these parasitics. Thus, a total parasitic

capacitance to ground $C_g = 1.8 \text{ nF}$ is considered. The resulting CM voltage, v_{cm} , impressed by the MC is represented in Figure 9. This voltage has approximately $110 V_{rms}$ and a peak equal to $\hat{V}_{g,In}$.

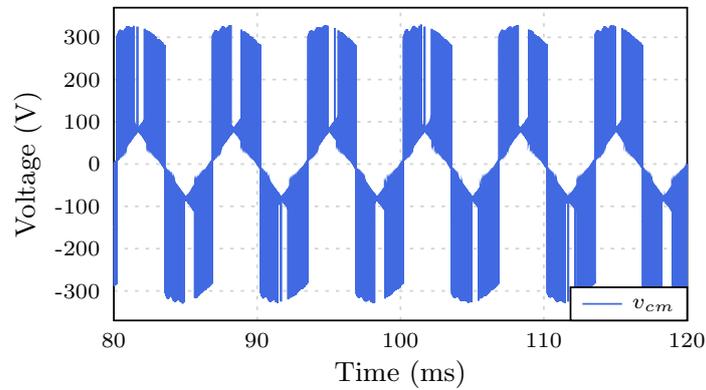


Figure 9. Common-mode voltage impressed by the matrix converter.

The frequency spectrum of the simulated RMS common-mode current ($i_{cm}(j\omega)$) for this operating point is shown in Figure 10. A zoom around the first switching harmonic inside the measurement range is shown in Figure 10b.

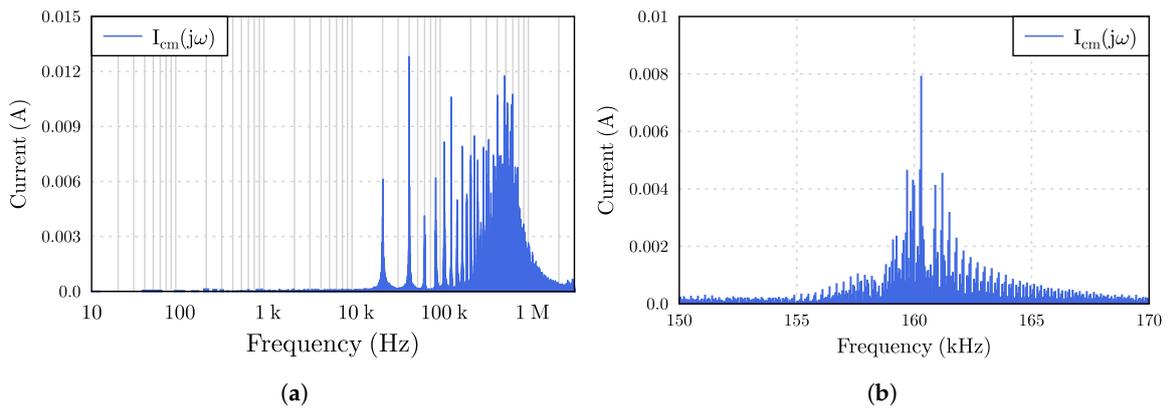


Figure 10. (a) frequency spectrum of the common-mode current $I_{cm}(j\omega)$; (b) zoom around the first switching frequency harmonic above 150 kHz.

5.2. Spectrum of the Measured Voltage

The converter and the measurement system can be reduced to its single-phase equivalent CM circuit as represented in Figure 11. It is important to note that, from the CM point of view, the three line-to-ground capacitors of each stage are in parallel. Thus, the effective common-mode capacitance is equal to the sum of the three capacitor values [48]. The LISN and the TR are modeled by its equivalent CM impedance. v_{cm} is modeled by an ideal voltage source.

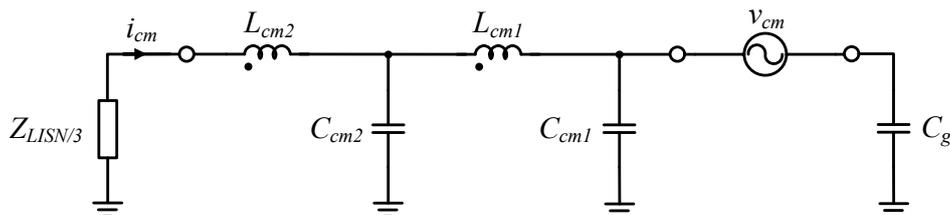


Figure 11. Equivalent single-phase circuit of the CM filter.

The C_g connected to the ground represents the parasitic capacitance. The spectrum of V_{TR} can be determined by the multiplication of $I_{cm}(j\omega)$ with the LISN's transfer function $G_{LISN,CM} = G_{LISN}/3$. Figure 12 depicts the spectrum of V_{TR} at the LISN output terminals along with the Max_{TR} and Min_{TR} using QP detection.

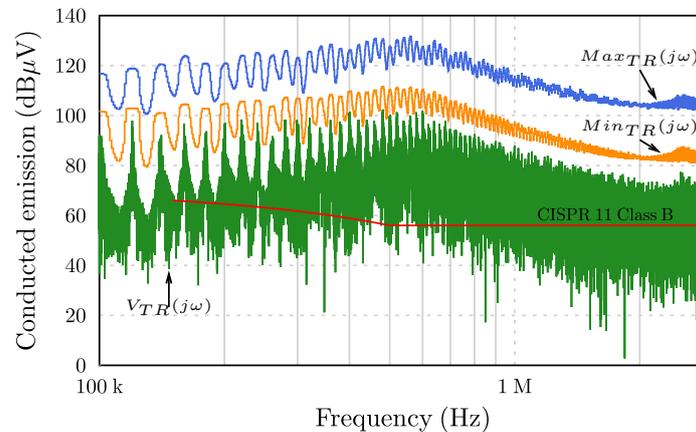


Figure 12. TR measurement without CM filter: maximum and minimum estimation of CE along with the spectrum of $V_{TR}(j\omega)$.

5.3. Required Attenuation

The required attenuation for the CM filter can be estimated without the need of calculating the exact QP values. The predicted CE at 160 kHz by $Max_{TR}(j\omega)$ curve is 123.7 dB μ V. The limits specified in the CISPR 11 Class B for CM are equal to the DM. Considering the limit at 160 kHz and including a margin of 6 dB, the required attenuation of the CM filter at 160 kHz is $Att_{req,CM} = 64.2$ dB μ V.

5.4. Topology

In order to limit i_{cm} , the EMI filter must maximize the mismatch between the power source and the converter impedances [49]. LC circuits are usually employed for the common-mode filter [50]. In contrast with the DM filter, no additional damping needs to be added by external elements. The CM inductors are connected in series with the lines in order to provide a high-impedance for the common-mode noise. The three windings of the inductor are wound on the same core, which forms a common-mode choke. Because the power line currents are symmetrically displaced in each winding, the magnetic flux produced in the core by these currents cancels.

5.5. Components

In order to provide the required attenuation a two-stage CM filter is employed (see Figure 11). Stage 1 and Stage 2 are formed by undamped LC filters that make the connection between the lines and the ground (PE). The maximum value of the line-to-ground capacitance is limited by the leakage requirements imposed by several safety agencies [48]. This safety measure is necessary for protection of personnel against electric shock under fault conditions.

According to IEC 60950, the ground leakage current for Class I equipment must be limited to $I_{leak,max} = 3.5$ mA at 50 Hz. This requirement has a great impact on the CM filter design. Considering the upper limit of the grid RMS voltage, a maximum total CM capacitance per phase of $C_{cm,max} = 44$ nF is calculated by:

$$C_{cm,max} = \frac{I_{leak,max}}{1.1 \cdot V_{g,ln} \cdot 2\pi \cdot f_g} \quad (9)$$

According to [41], for maximum attenuation given a minimum total capacitance, each stage shall present the same value. In order to provide some margin to the imposed limit of $C_{cm,max}$, a total capacitance per phase of 20 nF is chosen. Therefore, capacitors C_{cm1} and C_{cm2} must be 10 nF. Considering this capacitance, the value of the CM choke of each stage is then chosen to provide half of the required CM attenuation ($Att_{Stage1-2,CM} = 0.5 \cdot Att_{req,CM}$). Thus, the cut-off frequency should be $f_{0,Stage1-2,CM} = 25.2$ kHz. Taking this frequency into account, inductor L_{cm1} and L_{cm2} are selected to 1.3 mH.

5.6. Evaluation of the CM Filter

By combining the two stages, the complete transfer function H_{cm} from I_i to I_{cm} is obtained. Figure 13 depicts the gain of the CM input filter. As required, a 64 dB attenuation is provided at 160 kHz.

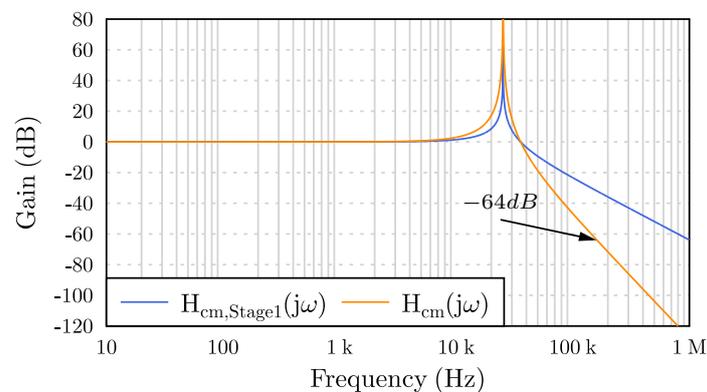


Figure 13. Frequency response of the CM filter: magnitude of H_{cm} , the transfer function from I_i to I_{cm} .

Figure 14 depicts the maximum and minimum estimation of the CE for the converter operation with the CM filter. As can be seen, the maximum curve for the predicted QP values is below the limits specified by CISPR 11. Thus, the CM filter design is considered to be concluded.

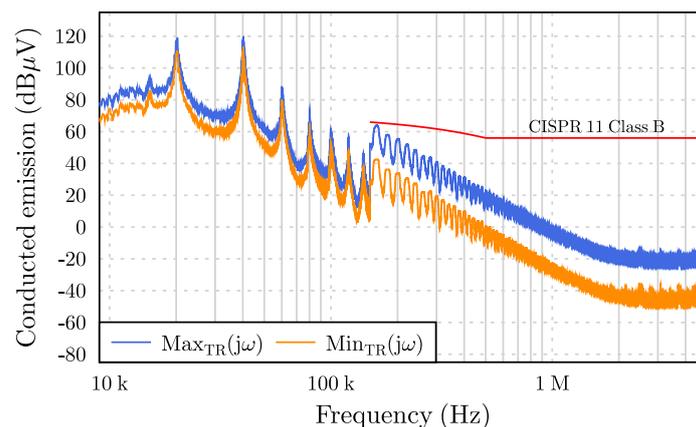


Figure 14. TR measurement with CM filter: maximum and minimum estimation of CE.

6. Integration of DM and CM Filter

The final step for the design of the EMI filter is the integration of the DM and CM stages. There are several ways to perform this integration. Due to the imperfect coupling between the three windings of a CM choke, some leakage inductance is present in L_{cm1} and L_{cm2} . The inductors of both DM and CM filters can be combined in each stage, so that this leakage inductance can be employed as part of the required DM inductance. Using this strategy, a small DM inductor can be employed reducing

the volume and weight of the filter. Figure 15 shows the complete circuit of the EMI filter. All of the components are listed in Table 1.

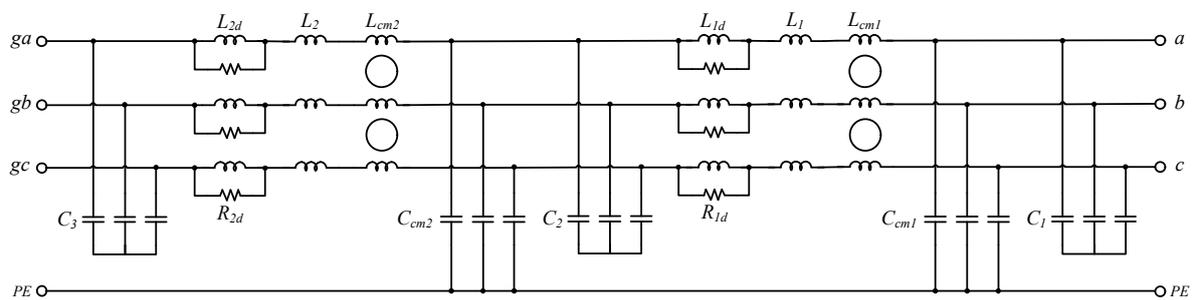


Figure 15. Complete circuit of the EMI filter comprising the DM and the CM filtering stages.

Table 1. Components for the EMI filter.

Component	Specification
C_1	EPCOS, MKP B32928C3206K, X2, 20 μF , 305 V_{ac}
C_2	EPCOS, MKP B32924C3225K, X2, 2.2 μF , 305 V_{ac}
C_3	Murata, GA3 GB563K, X7R, 56 nF, 250 V_{ac} ($\times 3$)
L_1, L_2, L_{1d}, L_{2d}	Micrometals, Iron Powder T184-52, 21 turns, 12 AWG
R_{1d}	Bourns, SMD CRS, 3.3 Ω , 2 W
R_{2d}	Bourns, SMD CRS, 10 Ω , 2 W
C_{cm1}, C_{cm2}	Murata, Ceramic DE2F3KY, Y2, 10 nF, 250 V_{ac}
L_{cm1}, L_{cm2}	Schaffner, RB8532-16-1M3, 1.3 mH, 16 A

Toroidal cores are preferred for the DM inductors (L_1, L_{d1}, L_2, L_{d2}) since they create a low external magnetic field, reducing the magnetic coupling with other elements in the circuit. Iron powder material is selected since it presents a much higher saturation flux density than ferrites, resulting in a more compact inductor [41]. The distributed air-gap is also a constructive advantage when compared with ferrites. Cores from Micrometals [51] were chosen mainly due to its low-cost and availability in the market. The –52 material is suitable to be used in differential-mode filter applications. This material features a nominal saturation flux of 1.0 T and can be operated at temperatures up to 110 °C. Core size T184 was selected in order to maintain inductance for the required energy storage. The inductor was constructed in a single layer in order to reduce the winding parasitic parallel capacitances. Furthermore, a solid round conductor is employed to take advantage from the increased resistance with frequency [41]. Using GeckoMAGNETICS software (v1.4.4 Professional, Gecko-Simulations A.G., Dübendorf, Switzerland) [52], the required number of turns was projected so as to obtain the nominal inductance at half of the peak current. This criterion takes into account the 9.1 μH leakage inductance of the CM chokes (L_{cm1}, L_{cm2}). The losses for the designed DM inductors are estimated at 2.1 W with a 15 °C temperature rise at P_{nom} . Core T184-52 has a product of number of turns by the current (NI) of 951 at 80% saturation flux density, B_{sat} . Dividing this number by 21 turns, it can be concluded that at least 45.3 A can flow in this inductor without provoking saturation while keeping a 20% margin.

Voltage surges due to electrical discharges and under voltages during load steps can appear at the MC input. Since the aforementioned voltages are usually high, metallized polypropylene capacitors (MKP) are selected for C_1 and C_2 due to its higher ripple current capacity and lower ageing when compared with electrolytic capacitors [45]. Moreover, capacitors from class X2 need to be chosen

since they are specifically for “across-the-line” applications. Capacitors from class X2 can withstand pulse peak voltages up to 2.5 kV in accordance with IEC 60664. Ceramic capacitors for C_3 , C_{cm1} and C_{cm2} are preferred since a small capacitance is required, leading to a compact construction and low parasitics. Due to safety reasons, CM capacitors are from class Y2, which is specifically for “line-to-ground” applications.

According to the IEC 60950 standard, the capacitors connected across the lines should be discharged to a voltage lower than 60 V in less than 10 seconds after a supply disconnection. This is required since both DM and CM capacitors remain charged to the value of the mains supply voltage at the instant of disconnection. If a hand or any other body part touch two pins of the mains supply plug at the same time, the capacitors will discharge through that body part. This discharge can be quite painful and for this reason, resistors of large value are connected across the lines in parallel with such capacitors. In this EMI filter, 130 k Ω SMD resistors with a power rating of 2 W are employed.

Figure 16 shows a photo of the assembled EMI filter. The PCB also includes current sensors, relays and fuses for protection. C1 capacitors are mounted in another board near the SiC MOSFETS in order to reduce the parasitic inductances.

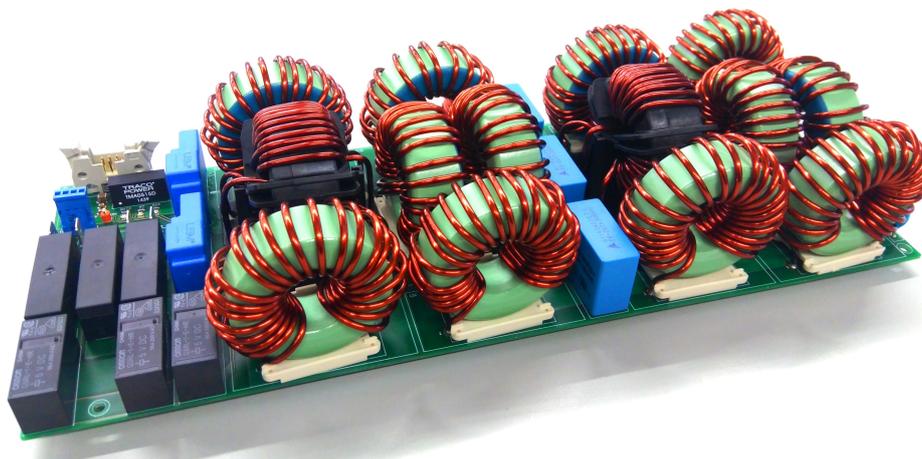


Figure 16. Photo of the EMI filter implementation.

As discussed in Section 3, low-frequency current harmonics are generated by the converter and are mainly dependent of the employed modulation. However, the resonant frequencies of the EMI filter could make interference in this measurement range. A final simulation with the integration of the DM and CM filters was performed. Figure 17 shows the measured low-frequency harmonics of the grid current and compares it with the IEC 61000-3-2 [36] Class A limits. As can be seen, the limits of the standard were not exceeded and the effectiveness of the EMI filter is verified.

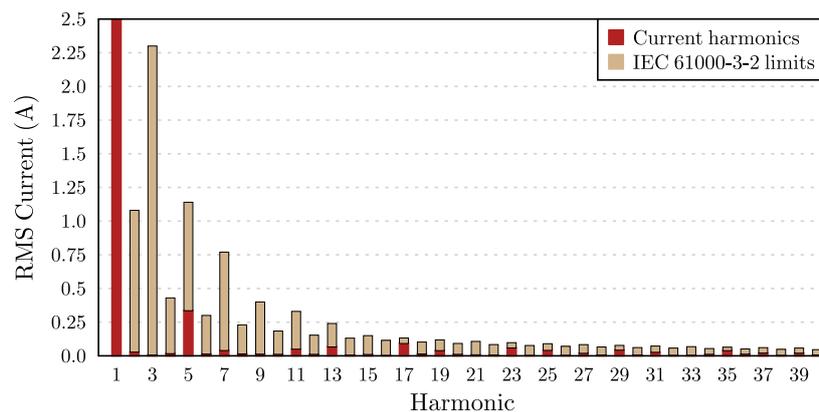


Figure 17. Low-frequency harmonics of grid current compared to IEC 61000-3-2 limits: simulation with the EMI filter comprising the DM and CM filters.

7. Experimental Results and Discussion

A prototype of the HFLMC was designed and built to test the capability to generate grid currents with a high-power quality [17]. Figure 18 shows the three grid currents and the battery current in both charger and inverter mode. As can be seen, the grid currents are well controlled (d - q control) and form a perfectly symmetric three-phase system. Since the HFLMC performs a single-stage power conversion, there is no significant energy storage between the grid and the battery. As a consequence, the battery current has a very fast dynamic response when a power flow inversion occurs at the grid side, such as at instant 140 ms.

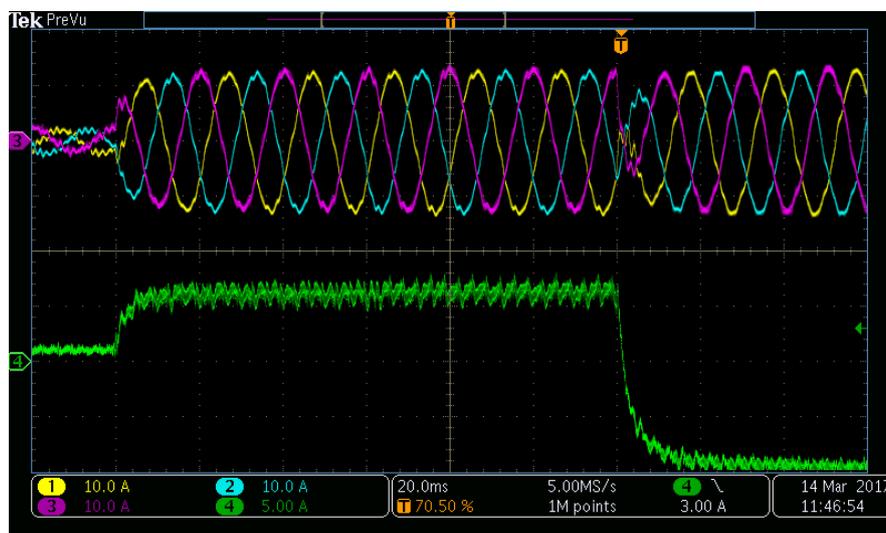


Figure 18. Experimental results of the HFLMC operating in charger and inverter mode: grid currents (i_{ga} , i_{gb} , i_{gc}) [yellow, blue, magenta] and battery current (i_{DC}) [green].

The low-frequency harmonics of the grid currents were also measured in the laboratory using the PA1000 Power Analyzer from Tektronix (Beaverton, OR, USA). The total harmonic distortion (THD) is 2.58 % at 10.2 Arms in charger mode and 3.44 % at 9.0 Arms in inverter mode. From the measurements, all the harmonics are within the limits specified by the IEC 61000-3-2 standard.

EMI filters are usually characterized by the insertion loss (IL) that is a measure of the interference suppression capability of a filter [35]. IL can be determined by using the scattering s -parameters defined for the 2-port network circuits. The most accurate way to measure s -parameters is using a vector network analyzer (VNA) [53]. The test procedure is specified in CISPR 17 [54] standard. Figure 19 shows the test circuits used for measuring the IL for the DM and CM stages. The VNA

generates a signal with a pre-defined power and variable frequency at its port 1. This signal is then propagated through the DUT and measured at the VNA port 2. CISPR 17 specifies that the source and load impedances of the VNA must be equal to $Z_0 = 50 \Omega$. Since the impedances are matched, IL coincides with the magnitude of the forward transmission coefficient S_{21} , as defined by Equation (10):

$$IL = -20 \cdot \log_{10}|S_{21}|, dB. \tag{10}$$

Balanced-unbalanced transformers, also known as “baluns”, must be connected to the VNA ports in order to isolate the DUT from the ground plane during DM measurements, as represented in Figure 19a. Moreover, the baluns are essential to provide very high CM rejection.

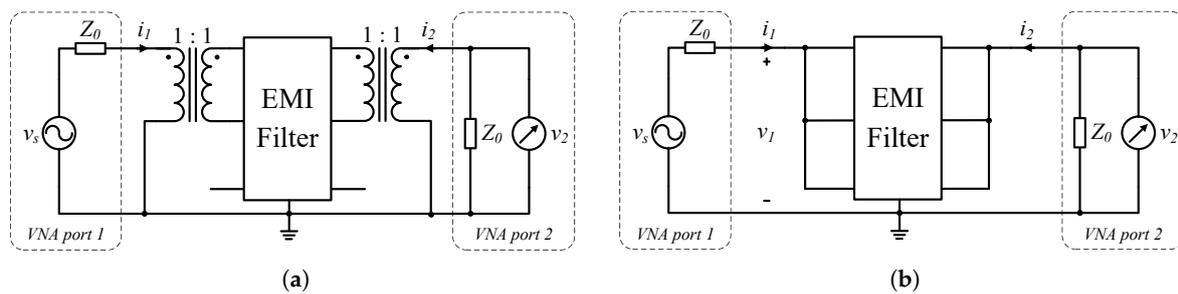


Figure 19. Test circuits for measuring the insertion losses in EMI filters. (a) differential-mode (symmetrical); (b) common-mode (asymmetrical).

The Coilcraft PWB1010LB [55] wideband transformer (Coilcraft, Cary, IL, USA) was mounted in a shielded housing with BNC receptacles as shown in Figure 20a, resulting in a $50 \Omega : 50 \Omega$ balun with a 3.5 kHz to 125 MHz bandwidth. A Rohde–Schwarz ZVL 3 (Rohde–Schwarz, Munich, Germany) with an operating frequency range from 9 kHz to 3 GHz was employed for the measurements. Coaxial cables with a characteristic impedance of 50Ω were used to connect the DUT to the measurement equipment. The test bench with the baluns and the VNA is shown in Figure 20b.

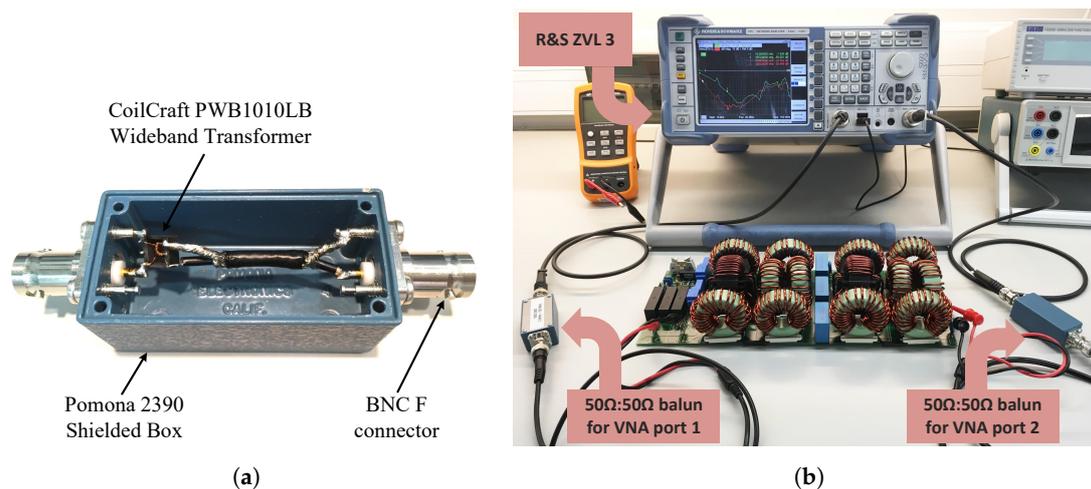
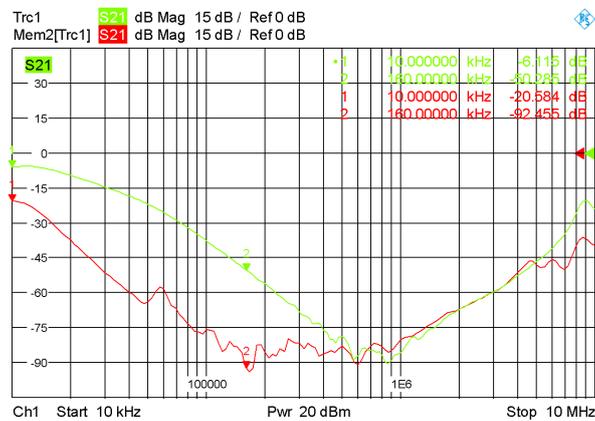


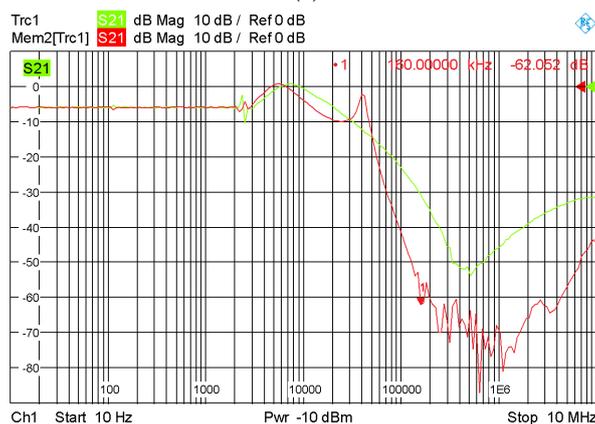
Figure 20. Differential-mode S_{21} parameter measurement. (a) photo of the constructed balun; (b) photo of the test bench.

The DM S_{21} parameter was measured between phase A and B while the other lines remained unconnected. Figure 21a depicts the obtained results for the DM Stage 2 and also for the series of Stage 1 and 2. As measured by the R&S ZVL 3, $S_{21, dm, Stage2} = -50.2$ dB for Stage 2 and $S_{21, dm, Stage1-2} = -92.4$ dB for Stage 1 and 2. The former result is inferior when compared with

the expected 104.9 dB. This is justified since the measurements are performed with a power of 20 dBm (equivalent to 100 mW). For this power level, the DM inductors have a higher inductance as explained in Section 6. Consequently, a shift in the resonant frequency occurs, resulting in a smaller attenuation. However, this is not a problem since, for higher currents, the effective inductance is within the expected range.



(a)



(b)

Figure 21. S_{21} parameter of the EMI filter measured with R&S ZVL 3 VNA. (a) differential-mode $S_{21,dm,Stage2}$ [Trc1] and $S_{21,dm,Stage1-2}$ [Mem2]; (b) common-mode $S_{21,cm,Stage1}$ [Trc1] and $S_{21,cm,Stage1-2}$ [Mem2].

For the CM S_{21} parameter measurement, the baluns are not needed since the ground plane of the VNA is directly connected to the PE terminal of the EMI filter. Figure 21b depicts the obtained results for the CM Stage 1 and also for the series of Stage 1 and Stage 2. As specified in Section 5, each stage must provide half of the required attenuation, more specifically 32.1 dB. As can be seen, $S_{21,cm,Stage1} = -31.2$ dB for one stage and $S_{21,cm,Stage1-2} = -62.0$ dB for the complete CM filter. These values are clearly aliened with the predicted ones.

With the results exported by the R&S ZVL 3, the insertion losses were computed using Equation (10) and depicted in Figure 22. It is clearly noticed that parasitic effects limit the achievable insertion losses and degraded the EMI filter performance for frequencies above 1 MHz. This can be explained by the parasitic series inductance of capacitors and the capacitance across the choke coils [56]. There are modeling methods for passive components that can be used to predict the high frequency parasitic effects that typically create EMC degradation [57]. For the current project, the required attenuation at these high-frequencies is less than the attenuation required at 160 kHz. This margin can be observed at the curves represented in Figures 8 and 14. Therefore, the performance of the filter is not compromised and complies with the specifications.

Electromagnetic field (EMF) simulation tools for analyzing EMI offer more accurate results than the tools based on circuit simulators. However, EMF simulation needs a high number of computational resources and are expensive tools. In order to meet the time requirements of the development cycle of the products, it is often only applied to very simplified models. The main weakness of this method is precisely the fact that parasitic elements of the components are not modeled, since it would require significant additional effort that is not compatible with the straightforward design approach that proposed. As a consequence, some components could have to be changed after the experimental pre-compliance tests in order to ensure the expected attenuation capability in the high-frequency range.

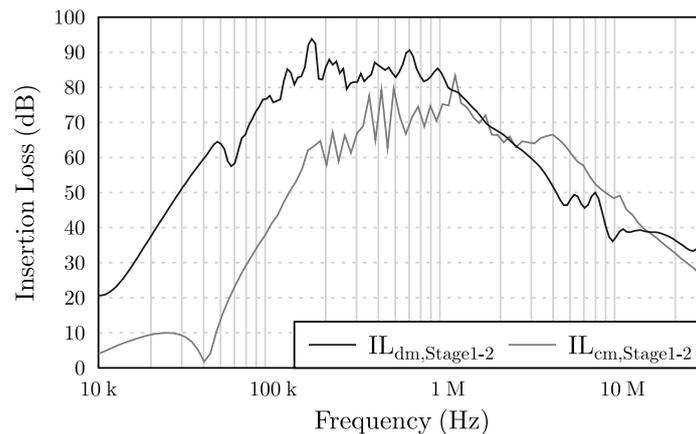


Figure 22. Measured insertion losses for DM filter [$IL_{dm,Stage1-2}$] and CM filter [$IL_{cm,Stage1-2}$].

The main strength of this design method is to present a framework for quickly obtaining a project of the EMI filter that can be also extended to other current source converters. This can be of high value for engineers that need a practical and guided way to design an EMI filter for their projects. For sure, some time-savings can be obtained since the main input for this project is the frequency spectrum of the converter input current and the common-mode voltage. As previously demonstrated, these inputs can be obtained through simulation or experimental measurements.

8. Conclusions

This paper details a step-by-step design method for the DM and CM filters of the HFLMC. This procedure can be extended to other current source converters provided that the spectrum of the input current is known. The conducted emissions are determined by a simulation model that includes the modeling of the measurement system. Each filtering stage is projected based on the required attenuation for CISPR 11 Class B pre-compliance. Both filters are integrated in a synergistic way in order to reduce volume and weight. A prototype of the filter was constructed and tested in the laboratory. An experimental test bench was mounted to determine the insertion losses according to the CISPR 17 standard. The obtained results confirm that the attenuation capability of the filter is in the expected range. Therefore, the effectiveness of the EMI filter regarding both LF harmonics and HF conducted emissions is confirmed.

9. Patents

D. Varajao, L. M. Miranda, and R. E. Araujo, “AC/DC converter with a three to single phase matrix converter, a full-bridge AC/DC converter and HF transformer,” U.S. Patent 9,973,107 B2; United States Patent and Trademark Office (USPTO), Alexandria, VA, USA, 15 May 2018 (Priority date: 13 August 2014).

Author Contributions: D.V. made the step-by-step design of the filter including the verification based on software simulation. R.E.A. supervised the filter design and suggested the the experimental validation approach. L.M.M. and D.V. constructed the EMI filter and implemented the test bench for insertion losses' characterisation. All of the authors participated in the discussion of the results. D.V. and R.E.A. wrote the paper in consultation with L.M.M. and J.A.P.L.

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

AC–DC	Alternating Current to Direct Current
AVG	AVG
BESS	Battery Energy Storage Systems
BNC	Bayonet Neill–Concelman
CE	Conducted Emissions
CISPR	International Special Committee on Radio Interference
CM	Common-Mode
DM	Differential-Mode
DUT	Device Under Test
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EV	Electric Vehicles
HF	High-Frequency
HFLMC	High-Frequency Link Matrix Converter
HFT	High-Frequency Transformer
IEC	International Electrotechnical Commission
LISN	Line Impedance Stabilizing Network
LF	Low-frequency
MC	Matrix Converter
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MKP	Metallized Polypropylene Capacitors
PCB	Printed Circuit Board
PE	Protective Earth (Ground)
PF	Power Factor
PK	Peak
QP	Quasi-Peak
RMS	Root Mean Square
THD	Total Harmonic Distortion
TR	Test Receiver
VNA	Vector Network Analyzer

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