

Review

A Comprehensive Review of Recent Progress on GaN High Electron Mobility Transistors: Devices, Fabrication and Reliability

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Abstract: GaN based high electron mobility transistors (HEMTs) have demonstrated extraordinary features in the applications of high power and high frequency devices. In this paper, we review recent progress in AlGaN/GaN HEMTs, including the following sections. First, challenges in device fabrication and optimizations will be discussed. Then, the latest progress in device fabrication technologies will be presented. Finally, some promising device structures from simulation studies will be discussed.

Keywords: AlGaN/GaN; high-electron mobility transistor (HEMTs); p-GaN; enhancement-mode

1. Introduction

Nitride-based wide band-gap semiconductors (WBS), such as GaN and related alloys, have been intriguing to high power and high frequency researches and applications over the past two decades, as reviewed in the literatures [1–10]. They are promising because of their intrinsic superior material properties, especially with their outstanding electrical performance exhibited in the GaN-based high-electron mobility transistors (HEMTs), also known as the heterojunction field-effect transistor (HFET). GaN-based HEMTs on silicon substrate are particularly appealing to the IC industry due to its compatibility with the industry-matured Si-CMOS IC technologies. Tremendous research and development work has been conducted and reported in the recent years with significant progresses on GaN-on-Si HEMTs covering the full scope of a new IC-chain, including the industrial acceptable-low defect quality of GaN-on-Si epitaxial materials, the optimized GaN-based HEMT devices and integration [11–17], the significantly enhanced reliability [18–24], the comprehensive circuit and device modeling [25–27] and the product designs [19,28–34].

The GaN-based HEMTs possess better performance than the silicon counterparts, such as they can be operated at higher frequency, higher power and higher temperature conditions. These advantages are benefited from III-nitrides' high electron saturation velocity, high breakdown electrical field, high electron mobility and high carrier density of the two-dimensional electron gas (2DEG) formed at the heterointerface between AlGaN and GaN layers in the GaN HEMTs.

GaN power transistors have been in volume production since 2010. AlGaN/GaN HEMT, however, is inherently normally-ON (depletion-mode, D-mode) as it was first reported in 1993 [35]. Thus their primary applications having been initially focused on the low-voltage and high-frequency applications.

For the power switching applications, on the other hand, normally-OFF (enhancement-mode, E-mode) transistors are required. It is not only for the concern of safety but also necessary to reduce the current leakages thus minimize the power loss, simplify the driving circuit and improve the device stability. Ever since the initial demonstration of the enhancement-mode AlGaIn/GaN HEMT in 1996 [36] and furthermore in 2000 [37], several approaches have been used to make normally-OFF GaN-based HEMTs as reviewed previously [38] and more recently [8,39]. Besides the hybrid approach with GaN HV-HEMT and Si LV-MOSFET in a cascade configuration, AlGaIn/GaN-on-Si HEMTs with direct GaN gate control [40,41] have attracted much attention commercially in the recent years due to its size thus cost. GaN-on-Si is acknowledged as a promising device platform for further exploration of commercial high-power modules with higher power density [4,9,33,34]. Moreover, owing to the availability of both depletion-mode and enhancement-mode of GaN HEMTs, they have invoked research interests and efforts in the IC industry for complementary logic applications [9,31].

This paper reviews the recent progress in the GaN-on-Si normally-OFF AlGaIn/GaN HEMTs based on recent literature. The following aspects will be covered: devices in Section 2, device fabrication in Section 3 and some promising structures from simulation studies in Section 4.

2. AlGaIn/GaN HEMT Device

For conventional semiconductor materials, the free charges come from the impurity ionization. In an AlGaIn/GaN heterojunction, the polarization effects give rise to a high density ($>1 \times 10^{13} \text{ cm}^{-2}$) of electron gas at the interface between AlGaIn and GaN, even without intentional doping. The AlGaIn/GaN HEMTs can provide not only high electrical conductivity with low on-state resistance but also low input and output capacitance, thus inherently promising for high voltage and high frequency applications.

A conventional Schottky gate D-mode GaN HEMT device structure is schematically shown in Figure 1a. The source and drain metal stacks facilitate the Ohmic contacts. The gate metal stack provides a Schottky contact. As a voltage bias of V_{DS} is applied between the drain and source, a lateral electrical field is built and the 2DEG under the gate flows along the channel of AlGaIn/GaN heterojunction as HEMT's current, I_{DS} . If the gate voltage is below the threshold voltage of HEMT while the drain is biased high, the device runs into the block region.

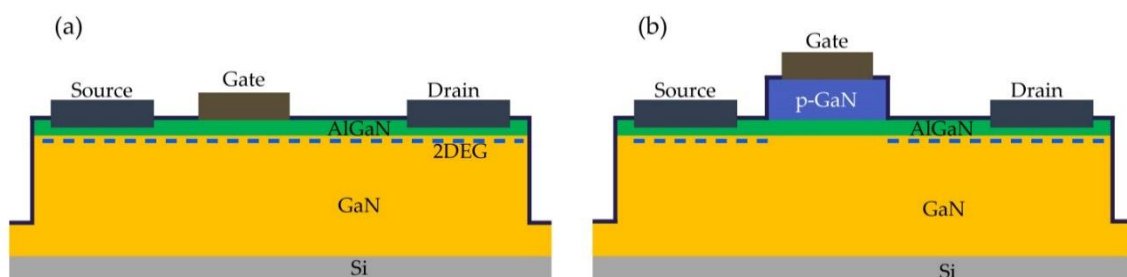


Figure 1. Structures of the GaN HEMTs, (a) the D-mode device and (b) the p-GaN E-mode device.

When the AlGaIn/GaN HEMT in Figure 1a is inserted with a p-type GaN layer between the gate electrode and the AlGaIn barrier layer, it forms a so-called p-GaN E-mode HEMT as shown in Figure 1b. With sufficiently high p-type doping (e.g., Mg) and an adequately thick p-GaN layer, the 2DEG below the gate would be depleted, which lead to a positive threshold voltage for the normally-OFF operation. Meanwhile, the low on-state resistance and high driving capability can be preserved with the 2DEG in the region between the gate edge and the drain. More advanced research work has been done in order to solve dynamic on-state resistance issues in GaN HEMTs. One of these successful examples has the current collapse suppressed up to 850 V [42]. There are also several varieties of p-GaN HEMTs as thoroughly reviewed in References [8,39], such as the gate injection transistor (GIT) [42].

Several advanced types of AlGaIn/GaN FET devices have been explored recently. Among of them, the GaN MOS or MIS (metal-insulator-semiconductor) HEMTs has drawn most of the attention [9,14,28,43], so do the MISHEMTs with high-K gate dielectric [17,31,44]. Other new devices with a regrowth of AlGaIn layer [41], or a regrowth of GaN drift channel layer [45] have also been reported. The MIS HEMT has the advantages over the Schottky gate GaN HEMT in terms of gate leakage and gate swing [46]. The gate dielectrics reliability, however, is one of the most important aspects to be well investigated and understood before it can be commercialized.

The performance of some recently published p-GaN HEMT devices [19,42,47,48] is compared and shown in Figure 2. It depicts the p-GaN HEMTs with excellent specific on-resistance $R_{on,sp}$ as low as a few $m\Omega \cdot cm^2$ while with the breakdown voltages larger than the theoretical limit of silicon.

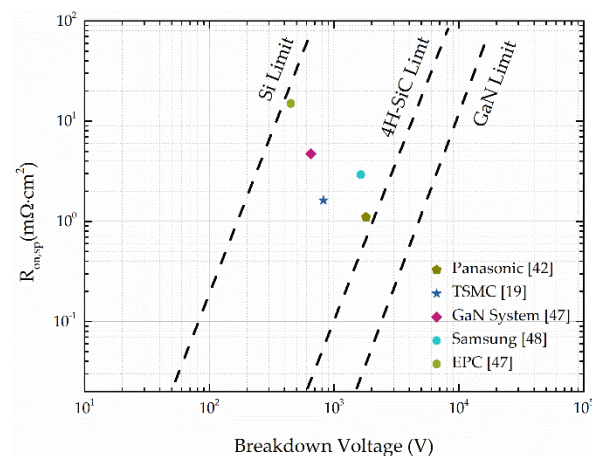


Figure 2. Specific on-resistance versus device breakdown voltage of the p-GaN HEMTs.

Figure 3 demonstrates the preliminary DC characteristics of the fabricated p-GaN E-mode AlGaIn/GaN HEMT. The device gate width is about 500 μm . The metal stack for the source and drain Ohmic contacts was formed with Ti/TiN/Al/TiN and was annealed at 650 $^{\circ}C$ for 30 s. And the metal stack for Schottky contact for the p-GaN gate was formed with Ti/Al. The detailed process information will be discussed in a subsequent publication. The measurements were carried out with Keithley 4200-SC. The transfer characteristics ($I_{DS}-V_G$) of the device is shown in Figure 3a and the output characteristics ($I_{DS}-V_{DS}$) of the device is illustrated in Figure 3b. The threshold voltage (V_{th}) of the fabricated device is about 1.5 V and the gate voltage swing is up to 10 V.

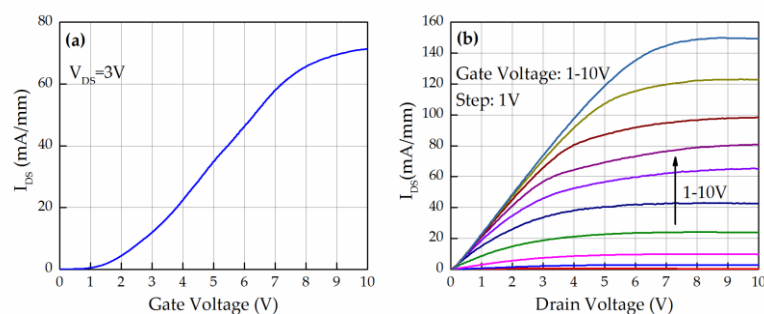


Figure 3. DC characteristics of a p-GaN HEMT, (a) the transfer characteristics, (b) the I-V output characteristics.

One of the challenges of making reliable p-GaN gate enhancement-mode HEMTs is to obtain controllable V_{th} with a reasonable variation across the wafer. It is found that V_{th} is sensitive to the p-GaN gate profiles, p-GaN layer residues, AlGaIn layer thickness around the gate edges and also surface morphology of the AlGaIn layer after the p-GaN etching. The threshold voltage instability can

be explained by the charge control model due to the charge-transferring effect [49,50]. The enhancement of threshold voltage in E-mode AlGaIn/GaN devices is mainly due to the space charge alteration under the gate, while defects can alter the charges via trapping and de-trapping processes during device operations. The fixed defects in the GaN and AlGaIn layers can act like traps offering electron transferring paths between the barrier layer and the substrate, which can generate potential shift and energy band bowing, thus V_{th} drift. Therefore, the reduction of defects is mandatory for reducing the charge variations so as to control the threshold voltage instability and reliability. Achieving low defects in III-nitrides layers, however, requires careful process engineering and optimizations.

Regarding to the device reliability of GaN-on-Si HEMTs [51], it has been recently figured out that the epitaxial quality of materials is related to a key industrial reliability item: the high temperature reverse bias (HTRB) stress-induced on-state drain current degradation [18]. It was confirmed [18] that the optimization of epitaxial layers could significantly improve the device reliability of AlGaIn/GaN HEMTs.

We have also studied the dielectric failure based on the time dependent dielectric breakdown (TDDB) measurement at different temperatures with statistical Weibull analysis [24]. The lifetime of the devices with 35-nm-thick LPCVD SiN_x gate dielectric was predicted to have a 10-year time-to-breakdown. This work also demonstrated the impacts of gate dielectric area and multi-fingers on the SiN_x TDDB characteristics.

3. AlGaIn/GaN HEMT Device Fabrication

Device processing technologies play important roles to achieve the full-potential and remarkable features of AlGaIn/GaN HEMTs. The process modules for the GaN HEMT device fabrication include device isolation, p-GaN gate formation, contacts for source and drain, contact for gate, surface passivation and so forth. In this section, we will focus on some of the key process technologies for the fabrication of p-GaN E-mode AlGaIn/GaN HEMTs, discuss some of the challenges and review recent progresses.

3.1. Device Isolation

Device isolation is the fundamental process to separate the electrical connection of adjacent devices, so as to minimize the impact of current leakage from their neighbors. Mesa dry etching and ion implantation are two of the commonly used and effective isolation approaches as shown in Figure 4.

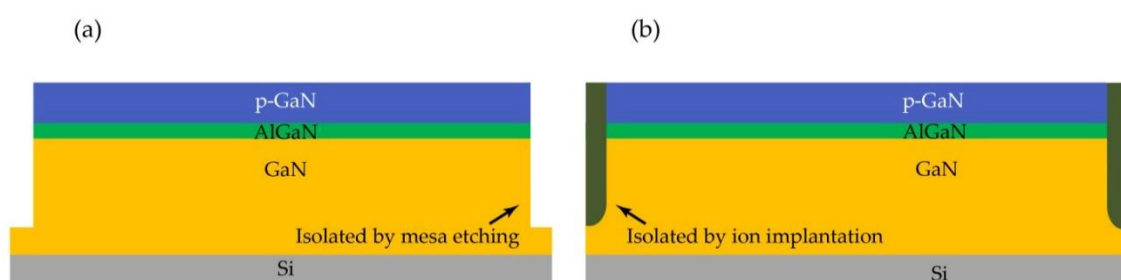


Figure 4. Schematic cross-section of (a) mesa etching and (b) ion implantation for device isolation.

3.1.1. Mesa Etching

The mesa etching step is to form an isolated area for each device and the material is removed physically around the devices by this process, as shown in Figure 4a. The etching depth is crucial for the isolation results or device leakage current. Under-etch of the mesa could result in an incomplete isolation, thus the devices performance would be impacted. The conventional wet etch techniques are not suitable for GaN device fabrication. The large bond energies and wide band-gaps make them highly resistant to acid and alkaline solutions at room temperature. Moreover, the wet etching of GaN shows isotropic profile and a slower etching rate than the dry etching techniques. Therefore, most of III-nitrides etching processes are conducted by dry etching [52].

Dry etching can be carried out by reactive ion etch (RIE), electron cyclotron resonance (ECR), inductively coupled plasma (ICP), electron cyclotron resonance (ECR), magnetron reactive ion etching (MIE) and so forth. [53]. RIE is one of the common methods for III-nitrides dry etching but it has slow etching rate, low degree of anisotropy and large surface damages due to the low plasma density and high operating pressure inherent in this technique [54]. Whereas ICP is expected to produce the etching results with low damages, high etching rates and high uniformity. Thus ICP etching has become the dominant dry etching technique for III-nitrides.

The dry etching rate can reach to the level of micron per minute handily [55,56]. However, many factors need to be considered to evaluate the dry etching quality of GaN and AlGaN, such as the surface morphology, sidewall profile, etching anisotropy, material selectivity, material damage, etching uniformity and so forth. These etching features can be affected by the etching conditions, including reactive chemistries and their fluxes, ICP antenna RF power, bias RF power, chamber pressure, chamber temperature, chamber configuration, etching technique and so forth.

The basic chemistries employed in the III-nitrides dry etching are chlorine based, such as Cl_2 and BCl_3 [57]. Moreover, Ar [52], N [54], H [58] and F [59] based chemistries can also be added to achieve better etching rate, selectivity and surface morphology [60]. Study [57] showed that the etching rate was found to increase with the ICP antenna RF power up to a certain level (e.g., 600 W). But further increased in antenna RF power could decrease the etching rate. It is noticed [54] that a high antenna RF power would cause the decrement of the DC bias voltage and thus resulting in a reduction of the ion-bombardment physical effect introduced by dry etching. High energy ion-bombardment would lead to surface roughness, material surface damages and low etching selectivity. Wakejima et al. [61] reported that the reasonably low bias RF power can be used to get high selectivity and low surface damage. Moreover, chamber pressure also has an impact on the etching rate. Increase chamber pressure (within the range of less than 10 mTorr) can help raise the etching rate. But further increase chamber pressure would not keep increasing the etching rate effectively. The mean free path of reacting molecules is short and the plasma density is low at high pressure. Re-deposition and polymer formation on the surfaces would also be favored at high pressure, which is undesirable [57].

3.1.2. Ion Implantation

Ion implantation is the other isolation process which is promising to product high performance GaN based HEMTs devices [15]. Ion implantation is an adding process, as shown in Figure 4b. The ion species can be used to isolate devices including H, He, N, P, Ar, O and so forth [62–67]. In the implantation process, atoms are added into the nitrides by means of energetic ion beam injection. Ion implantation has a better ability to control both of the dopant concentration and depth. The concentration can be adjusted by the ion beam current and the implantation duration, while the depth can be controlled by the ion energy.

The ion implantation is a room-temperature process; thus photoresist can be used as the mask. The ion species that implanted can be exactly selected by the mass analyzer, thus the contamination risk can be reduced. Moreover, the ion implantation is an anisotropic process, the side boundary of the implanted ions in the semiconductors can be straight. Thus the isolated area can be precisely defined. However, for the purpose of minimizing the channeling effect, the wafers are always placed with a tilted angle of about 7° .

Comparing to the mesa etching process, the ion implantation creates the isolation boundary under the surface, which can protect the device sidewalls. Therefore, better device electrical performance and reliability are expected.

3.2. P-GaN Gate Formation

To achieve the E-mode GaN based HEMTs, the structure of p-GaN HEMTs has been widely used [51]. As shown in Figure 5, the basic structure of the p-GaN HEMT consists of the p-GaN cap layer, AlGaN barrier layer, GaN buffer layer, Si substrate and so forth. The energy bands of AlGaN

are lifted up by the p-GaN cap layer, leading to the depletion of the 2DEG underneath. The p-GaN should be removed except for the gate area. The dry etching is widely used for this step. One of the key factors to achieve high performance device and high yield is the selectivity etching of GaN over AlGaN. The selectivity of Cl_2/BCl_3 plasma between GaN and AlGaN is unable to meet the requirement. Therefore, two approaches have been recommended to achieve this process of selective dry etching. One is the fluorine based chemistries etching technique and the other is oxygen based chemistries etching technique.

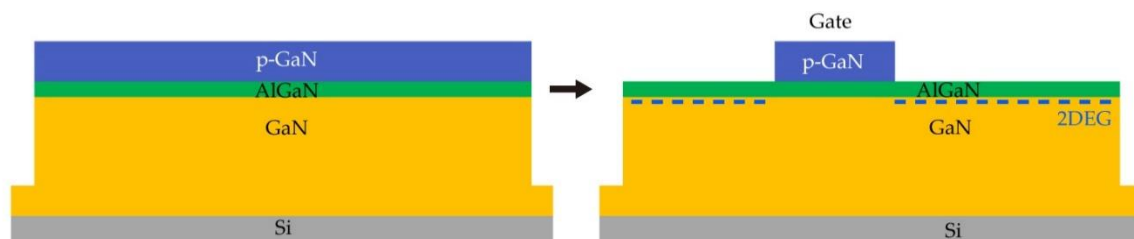


Figure 5. Gate area definition of a p-GaN HEMT.

The etching selectivity of compound semiconductor films containing Al can be optimized in Cl-based plasmas by adding F-containing gases. For example, the BCl_3/SF_6 selective dry etching on AlGaN/GaN, the decrease in AlGaN etching rate is due to the formation of non-volatile AlF_3 residues on AlGaN surface. This non-volatility of AlF_3 reduces the etching efficiency of chlorine, achieving selective etching of GaN over AlGaN.

The other option is to use the O_2 and chlorine based gases. Shawn et al. [68] demonstrated a cyclical two-step etching technique using separate O_2 and BCl_3 plasmas. The low power oxygen plasma creates an oxidized layer on the surface of AlGaN/GaN and then the low-power BCl_3 plasma is used to remove the surface oxide. The etching rate per cycle is about 0.7–2.5 nm, depending on the process parameters. Wong et al. [69] investigated highly selective dry etching with O_2 and chlorine gases. Their study showed that the O_2 flow has evident impacts on the etching rate and selectivity of AlGaN/GaN structure. Increasing O_2 flow (0–5 sccm) resulted in decrease etching rates for both GaN and AlGaN. The selectivity was increased at the O_2 flow range of 0–2 sccm and then descended when O_2 flow arrived at 3 sccm. Moreover, they reported that the surface roughness was improved with a higher O_2 flow.

To achieve high etching selectivity, some new structures have been developed. Chiu et al. [70] reported that they added an AlN etching stop layer between p-GaN and AlGaN, that is, the p-GaN/AlN/AlGaN/GaN structure, to improve the p-GaN etching selectivity. With the BCl_3 and CF_4 gas mixture, the etching rate can be slowed down remarkably on AlN layer due to the non-volatility of AlF_3 . Then they obtained a better uniformity of V_{th} compared with the conventional structure. The standard deviation of V_{th} from the devices with AlN stop layer was about 0.06 V, whereas the data from the traditional ones was 0.2 V. Moreover, they further employed N_2O as the oxidant [71] with the same AlN stop layer and achieved further improved uniformity. The p-GaN was oxidized to Ga_2O_3 by N_2O plasma and then the Ga_2O_3 was removed using HCl solution in one cycle. After p-GaN was fully removed, the AlN etching stop layer was exposed and oxidized to Al_2O_3 by N_2O plasma. Since the etching rate of this Al_2O_3 in HCl solution was extremely low, the selective etching of AlGaN/GaN was achieved. They claimed that the uniformity of device on-state resistance (R_{on}) and the surface leakage current were improved both by this technique.

For the purpose of controlling the uniformity of threshold voltage, reducing the device leakage current and improving device reliability performance, more efforts have to be made to achieve smooth surface morphology, low material damages, high etching selectivity and outstanding etching uniformity.

3.3. Ohmic Contacts for Source and Drain

The Ohmic contacts provide the access points for the device to connect with external circuitry. Their resistance should be very low with respect to that of the channel drift region to reduce the device specific on-resistance. It is rather challenging to make good Ohmic contacts on GaN based materials, owing to the wide band-gap which naturally facilitates Schottky contacts. For the high performance p-GaN HEMT, the source/drain Ohmic contact resistance (R_c) should be minimized. Thus the work function metal layers, the thickness of metal layers, annealing temperature, semiconductor doping level, recess depth of AlGaIn layer and so forth. are all important factors to be optimized. The structure of source and drain contacts are displayed in Figure 6.

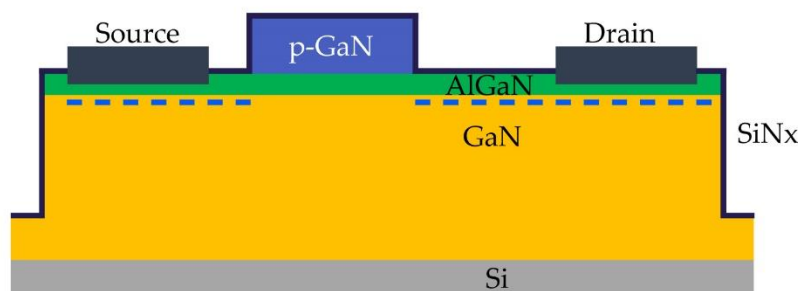


Figure 6. Ohmic contacts structure for source and drain of a p-GaN HEMT.

Single metal layer is not commonly used such as Ti or Al, due to their chemical activity with oxidant, especially for high power devices which often work at high temperatures. Therefore, different metal stacks with multiple layers have been proposed and explored. These metal stacks can be categorized into two groups, Au-based metal stacks and Au-free metal stacks. Au-based metal stacks have been studied for many years and become mature gradually. The most used stacks include Ti/x/x/Au structures [72], where x represents metals such as Al, Ni, Ti, Mo and so forth. On the other hand, the Au-free metal stacks are highly recommended recently for CMOS compatible process. The process compatibility with current Si wafer line is a fundamental factor of whether the GaN based devices can be fabricated in foundries, or even in the reused 6 or 8 inch Si wafer process lines. This means metals such as Au and Cu need to be excluded from the front-end-of-line.

Ti/Al/Ni/Au is widely used for source and drain Ohmic contacts. Studies [73,74] showed that the formation of Ohmic contacts for Ti based metal stacks is due to the reaction between Ti and GaN. TiN is formed at the interface by which N vacancies are created as donors to increase the carrier concentration resulting in a thinner barrier for electron tunneling [73]. In the Ti/Al/Ni/Au metal stack, thickness of each metal layer needs to be optimized to achieve low contact resistance and smooth surface. Ti/Al thickness ratio in the metal stack is one of the key factors for the formation of low contact resistance [75]. Research showed that for a given Ni/Au thickness ratio, the lowest contact resistance is obtained at Ti/Al ratio of 1/6 when annealing at 900 °C in N₂ ambient [76]. Moreover, the total thickness of Ti/Al also strongly influences the final contact resistance. Generally, the contact resistance below 0.6 Ω·mm can be commonly obtained in the Ti/x/x/Au metallization.

Au-free processes have been reported for many kinds of metal stacks. Beyond the consideration of compatibility with the Si-wafer-process-line, the research of Piazza et al. [77] demonstrated that long term thermal stress of Ti/Al/Ni/Au metal stack could lead to a dramatic degradation of the structure. This could be a barrier for the high power applications of the GaN based devices. Lee et al. [11] reported Ti/Al/W metal stack for Ohmic contacts. The contact resistance was lower than 0.5 Ω·mm with the annealing temperature of 870 °C. The surface morphology of the Ti/Al/W metal stack was much smoother than that of the Ti/Al/Ni/Au metal stack.

Annealing temperature of metal stack is important for the formation of Ohmic contacts. Most Au-based and Au-free metal structures are annealed around 800 °C [72,78], while some work reported low temperature (lower than 700 °C) annealing to achieve Ohmic contacts [79,80].

Liu et al. [81] reported the Hf/Al/Ta metal stack on InAlN/GaN with the annealing temperature of 600 °C. The results from TEM and SIMS measurements revealed contacts with smooth metal-semiconductor interface and showed the formation of Hf-N and Hf-Al alloys near the interface. They achieved a specific contact resistance (ρ_c) of $6.7 \pm 0.58 \times 10^{-6} \Omega \cdot \text{cm}^2$ at 600 °C annealing temperature. Lin et al. [82] presented a low Ohmic contacts resistance formed by sidewall contacts with Ohmic recess. They used a Ta/Al/Ta metal stack with the annealing temperature of lower than 600 °C. For the recess depth of 10 nm, they achieved contact resistance of lower than 0.25 $\Omega \cdot \text{mm}$. Ti/Al/TiN metal stack is also used for Ohmic contacts. Firrincieli et al. [80] employed the Ti/Al/TiN metal stack annealing at 550 °C in N₂ ambient and achieved a contact resistance of 0.62 $\Omega \cdot \text{mm}$. This metal stack was also shown to pass a high current of 0.6 A/mm when 10 V bias was applied.

Recently, Yoshida and Egawa [83] reported Ti/Al/W Ohmic contacts on AlGaN/GaN. The contact resistance was about 0.358 $\Omega \cdot \text{mm}$ with a low annealing temperature of 500 °C. They found that thinner Ti layer can lead to a lower annealing temperature, because Al needs to diffuse through the Ti layer in order to make Ohmic contact with AlGaN. Pozzovivo et al. [84] studied the effects of a special SiCl₄ plasma treatment prior to the Ohmic metallization. They achieved a sufficiently low contact resistance of 0.7 $\Omega \cdot \text{mm}$ at a reduced anneal temperature of 600 °C. The contact surfaces of AlGaN were directly treated by the SiCl₄ plasma for 15 s in RIE with self-induced bias of about 300 V. They suggested that the SiCl₄ plasma treatment of AlGaN surface would help to enhance the generation of N vacancies, which may be responsible for the high carrier concentration at the AlGaN surface to form a low contact resistance. The work from Graff et al. [75] exhibited consistent results of low contact resistance with the pre-treatment of SiCl₄.

The low annealing temperatures and the Au-free metal stacks would be beneficial to the device electrical and reliability performance [83] and are also compatible with foundry CMOS processes which is plausible for transferring to large scale production.

3.4. Contact for Gate

For the p-GaN E-mode HEMTs, the Schottky contacts on gate are generally adopted because it is expected to have lower gate leakage current and higher thermal stability. Figure 7 illustrates the gate structure of a typical p-GaN HEMT. The metal-semiconductor Schottky barrier height is depending on the difference between the work function of metal and the electron affinity of semiconductor. Metal with lower work function should give a higher barrier height for p-GaN contact. The Ti/Al [85], Ni/Au [86], W [87] and so forth. are used for gate metals. Greco et al. [85] studied the impacts of the thermal budget on the Schottky gate metals of Ti/Al. They found annealed with 800 °C of Ti/Al stack resulted in a higher gate leakage current than that of annealed at lower temperature. The decrease of the Schottky barrier height from 2.08 to 1.60 eV with annealing temperature increased to 800 °C was attribute to the structural modification occurring at the interface, which explained the increase of the leakage current.

Ľapajna et al. [88] studied the Schottky gate reliability under forward bias stress of a p-GaN HEMT. They concluded that the generation-recombination centers were created during stress due to the defect percolation process. This stress-induced generation of defects formed the leakage path across the structure once sufficient defects are generated. Wu et al. [89] revealed that the gate breakdown phenomenon could be explained by the avalanche multiplication in the space charge region of the Schottky metal/p-GaN junction. Tallarico et al. [90] concluded that the time to failure is a function of the initial Schottky gate leakage and the breakdown mechanism is ascribed to the percolation path in the p-GaN layer. Stockman et al. [91] studied the Schottky gate leakage current under the reverse gate bias. Two efficient methods to suppress the perimeter-dependent leakage current were found. One is by improving Schottky/p-GaN interface quality to reduce the supply of carriers from the gate metal,

the other is by making proper passivation of the p-GaN sidewalls to reduce the interface states and surface roughness.

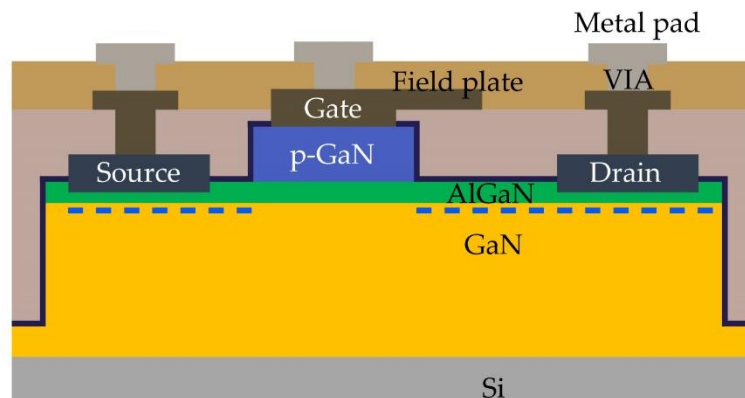


Figure 7. Schematic cross-section for gate structure of a p-GaN HEMT.

Yu et al. [92] also concluded that the gate leakage current is likely due to a highly doped and/or highly defective surface layer, resulting in carrier transport by tunneling across the Schottky barrier. Lu et al. [86] demonstrated the results of employing surface treatment and post-gate annealing to improve the Schottky gate leakage. The surface treatment reduced the lateral surface leakage by removal of the surface traps. The vertical gate tunneling current, on the other hand, was lowered through improved Schottky contact quality after thermal annealing. The off-state leakage current was reduced by about 7 orders after the implementation of the two-step treatment.

Besides the approaches of using the Schottky contacts, an Ohmic gate contact is suggested by Panasonic [42]. They reported that the hole-injection from the p-GaN gate into the GaN channel could have a positive impact on the p-GaN gate module.

As we can see, the gate metallization for p-GaN E-mode HEMTs has profound impacts on the device performance. For Schottky gate contacts, low gate leakage current and high thermal stability are required.

3.5. Surface Passivation

Although significant progress has been achieved to improve the performance of GaN devices, noticeable gaps still remain between demonstrated device performance in the real market applications and the theoretical expectations. The existence of large amount of surface states in AlGaIn and GaN have been found to be the root cause of device current collapse and some reliability issues, which is one of the main challenges in fabricating high performance AlGaIn/GaN HEMTs [93–97]. These surface states may come from dangling bonds of the surface atoms, defects at the surface as grown, plasma damages during the processes, the foreign contaminations and so forth. And they behave like carrier traps thus can seriously deteriorate the device performance. Furthermore, the charged surface states can act as a virtual gate and lead to the depletion of channel electrons, thus decreasing the channel 2DEG density [98]. The trapped charges at the surface can also contribute to the remote Coulomb scattering to the channel electrons. Therefore, surface passivation should be carefully optimized to prevent negative effects on device performance such as current collapse, frequency dispersion, large dynamic on-resistance and so forth.

The basic structure of surface passive layer is illustrated in the Figure 6. Many different insulation materials have been explored as the surface passivation layer for AlGaIn/GaN HEMTs, including SiO₂ [93,99], Si₃N₄ [100], ZrO₂ [94,101], HfO₂ [95,96], Ga₂O₃ [43,102], AlN [103–106], Sc₂O₃ [107], TiO₂ [108], ZnO₂ [109], NiO [110], Ta₂O₅ [111], Al₂O₃ [112–114], AlON [43] and so forth. In addition to the surface passivation, dielectric-free passivation technologies have also been proposed and demonstrated, for example, oxygen plasma oxidization [115,116], ozone oxidization [117],

chemical oxidization [118], SiH₄ treatment [119] and so forth. AlN is found to be a good surface passivation layer which can create a sharp interface and suppress GaN surface oxidation effectively [120]. Recently, Panasonic developed a passivation technology with AlON layer [43]. The AlON layer was deposited by atomic layer deposition (ALD) possessing a better performance with less process damage, less extra fixed charges and less electron traps in comparison with Al₂O₃ layer. Moreover, O₂ annealing after the AlON deposition could further reduce the Al/Ga dangling bonds at the surface.

It is known that GaN can be oxidized in the air forming a layer of native gallium sub-oxide (GaO_x) on the surface. Defect states associated with the GaO_x further exacerbate gate leakage current and lead to drain-current collapse at high frequency [121–123]. Dong et al. [124] have proposed a method to reduce the surface states by changing the GaO_x morphology via an elevated-temperature. The ordering of native GaO_x layer can be improved towards the structure of bulk Ga₂O₃, therefore surface states can be reduced. Bae et al. [125] used a low-temperature treatment to enhance the quality of GaO_x formed at the SiO₂/GaN interface and thus reduce the interface defect density. Therrien et al. [126] demonstrated a microscopic mechanism that could reduce the defect density at the high-K/GaN interface through the formation of a high-quality Ga₂O₃ layer during remote-plasma-assisted oxidation. It should be noted that the high dielectric constant of the surface passivation layer can also increase the parasitic capacitance between the gate and source (C_{pgs})/drain (C_{pgd}) metals and thus decrease the device's speed [127]. In summary, surface passivation with dielectric layers should be carefully selected to improve device performance, eliminate the current collapse and reduce the dynamic on-resistance.

3.6. Field Plates

As we have mentioned above, GaN based HEMTs suffer the effect of current collapse [128], which can temporary increase the dynamic on-resistance due to the charge trapping effects. One reason is that the strong electric field at the gate edge on the drain side could enhance the charge trapping in the states at the interface between passivation and III-nitrides. Moreover, the hot-electron injection effect is considered to be the other reason for the current collapse [129]. Surface passivation [130] and field-plate [131] are two effective solutions for this issue.

The employment of a field plate on dielectric layer of the AlGaIn/GaN HEMT has brought some of the most significant and exciting improvements on current collapse [129]. The function of the field plate is to redistribute the electric field profile and decrease the electric field peak value, hence reducing trapping effect and increasing breakdown voltage, as presented in Figure 7. Recently, Wong et al. [132] demonstrated a novel asymmetric field plate structure. The electric field was appropriately distributed by the slanted field plate. They obtained a uniform electric field distribution with the slant field plate, achieved a reduced dynamic on-resistance of 2.3 Ω·mm at the drain voltage of 50 V with a high breakdown voltage up to 138 V. Ma et al. [133] studied the effects of surface treatment and field plate structures on the current collapse of the AlGaIn/GaN HEMTs. Their results showed that the gate field plate predominantly reduced the emission time constant of the trapped electron and O₂ plasma treatment decreased the density of traps. And they confirmed that the current collapse can be mitigated by the combination of these two methods.

4. AlGaIn/GaN Device Simulation

The technology-computer-aided-design (TCAD) simulations are often applied to study the AlGaIn/GaN HEMT. The focus is mainly on the E-mode mechanism as well as the methods of increasing the threshold voltage of the HEMTs [134,135]. And the simulations have also been used to study the gate leakage current [136,137], the device reliability [138], the short channel effects [139], current collapse [140] and so forth. For the simulation of the AlGaIn/GaN HEMTs, the most important work is to solve the 2DEG concentration which is generated by spontaneous polarization (P_{sp}) and piezoelectric polarization (P_{pe}) [141], as shown in Figure 8. The two polarizations are influenced by many factors, such as the materials of substrate and epitaxial layers, crystallographic plane orientation of III-nitrides, AlN composition of AlGaIn layer, thickness of AlGaIn layer, relaxation of

AlGaN layer, doping concentration in AlGaN layer, thickness of GaN cap layer, fabrication process and so forth [142–149]. For the p-GaN HEMTs simulation, there are many valuable studies have been reported [39,142–145,150]. For example, Fujii et al. [151] presented the control of threshold voltage by the variation AlGaN barrier layer thickness and AlN molar fraction. Efthymiou et al. [152] investigated effects of the p-GaN doping and gate metal work function on the threshold voltage of devices. Bakeroot et al. [153] developed an analytical model for calculation of the threshold voltage for p-GaN HEMTs, they studied the contributions of p-type doping profile, AlN molar fraction of AlGaN layer and AlGaN layer thickness to the threshold voltage.

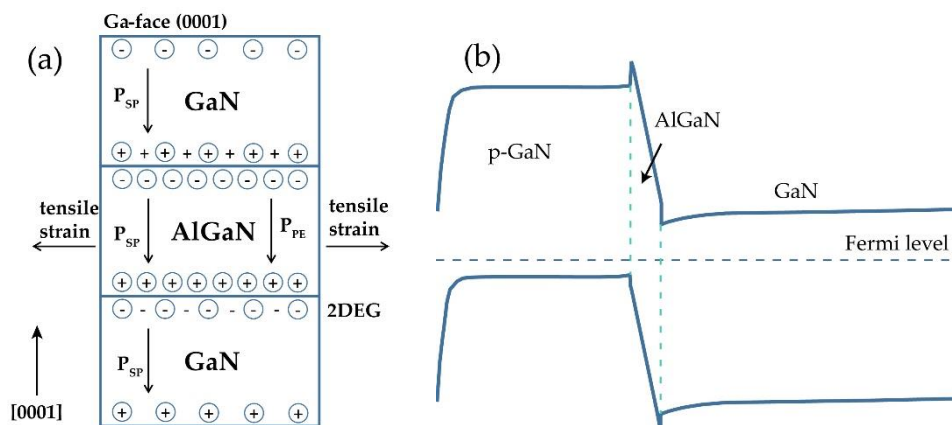


Figure 8. The schematics of (a) polarizations of AlGaN/GaN structure and (b) energy bands profile of the p-GaN HEMTs.

Moreover, in addition to the structures of p-GaN gate, recess gate and F-treatment, some novel E-mode HEMTs have been also proposed and studied through simulations. Huang et al. [154] simulated an E-mode HEMT with a floating gate in the gate dielectric. The results showed that combining with the gate recess, the V_{th} of the devices could be larger than 3 V with a low sheet density of $\sim 10^{12} \text{ cm}^{-2}$. Wang et al. [155,156] simulated an E-mode HEMT with spilt floating gate. It is shown that such kind of device can improve the charge retention time comparing with the single floating gate HEMTs [157]. Duan et al. [158] simulated an E-mode HEMT with Groove-type channel and the normally-off function was based on the anisotropic polarization of GaN.

5. Summary

In this review, we have evaluated the recent progress of GaN based E-mode HEMTs. First, the typical device performance has been presented. And then we focused on some of the key technologies for fabricating p-GaN E-mode AlGaN/GaN HEMTs, including device isolation, p-GaN gate formation, Ohmic contacts for source and drain, contact for gate, surface passivation and field plate. For the material and device simulations, we reviewed some of the promising structures for achieving high performance E-mode devices. In summary, this paper provides the recent developments and existing challenges of p-GaN E-mode AlGaN/GaN HEMTs, we hope this could be useful for the study of E-mode AlGaN/GaN HEMTs.

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