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Review

Review of Multilevel Voltage Source Inverter Topologies and Analysis of Harmonics Distortions in FC-MLI

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Abstract: We review the most common topology of multi-level inverters. As is known, the conventional inverters are utilized to create an alternating current (AC) source from a direct current (DC) source. The two-level inverter provides various output voltages [(Vdc/2) and (−Vdc/2)] of the load. It is a successive method, but it makes the harmonic distortion of the output side, Electromagnetic interference (EMI), and high dv/dt. We solve this problem by constructing the sinusoidal voltage waveform. This is achieved by a "multilevel inverter" (MLI). The multilevel inverter creates the output voltage with multiple DC voltages as inputs. Many voltage levels are combined to produce a smoother waveform. During the last decade, the multilevel inverter has become very popular in medium and high-power applications with some advantages, such as the reduced power dissipation of switching elements, low harmonics, and low EMIs. We introduce the information about several multilevel inverters such as the diode-clamped multilevel inverter (DC-MLI), cascaded H-bridge multilevel inverter (CHB-MLI), and flying-capacitor multilevel inverter (FC-MLI) with Power systems CAD (PSCAD) simulation. It is shown that THD is 28.88% in three level FC-MLI while THD is 18.56% in five level topology. Therefore, we can decrease the total harmonic distortion adopting the higher-level topology.

Keywords: multilevel inverter; diode clamped multilevel inverter; flying capacitor multilevel inverter; cascade H bridge multilevel inverter; total harmonic distortion; PWM control techniques; PSCAD/MULTISIM simulation

1. Introduction

Inverters are very useful for various industrial applications. In the last few years, the voltage-driving method has been adopted. To reduce the semiconductor transient voltage and current rating, a series and parallel connection method is needed. Moreover, the limited standard three-phase converter is also adopted up to the maximum allowable voltage of the load. Also, both the primary and the Pulse width modulation (PWM) switching frequency can be useful. The reduced switching frequency shows the low disappearance and the higher efficiency. In order to synthesize the spectrum signals of the harmonics caused by the capacity, the multi-level inverter has received more attention in recent times. Moreover, a multilevel inverter has a key role in providing improved operating voltage beyond the voltage limits of conventional semiconductors.

The following clarification defines the significance of the multilevel converter. The explanation of a multilevel inverter is: "The multilevel inverter can demonstrate the switching skill very effectively with different voltage and current levels of its input or output nodes". It is a practical reply to raise the power capacity with a comparably low elements load and decreasing the output harmonics.

The Concept of Multilevel Inverters

Two level inverters are shown in Figure 1. The input voltage of a direct current (DC) is converted to the required alternating current (AC) voltage and frequency [1]. When an inverter operates with Vdc, a two-level inverter can create two different output voltage for a load, Vdc/2 or (−Vdc)/2. To generate an AC voltage, both voltages are generally allowable in the PWM. Compared to multilevel inverters, this two-level method creates harmonic distortion, Electromagnetic interference (EMI), and huge dv/dt [2]. The idea of a multilevel inverter is not based on the two-voltage level AC. Alternatively, some voltage levels are connected to get a better waveform and less dv/dt and harmonic distortion. If the voltage level of the inverter is higher than the waveform, it is much better. However, the designs are simple, but increasing voltage levels and more components are needed. The dividing voltage and extending its control scheme become more complex in a three-phase setup [3]. Series-connected multilevel inverters are connected to the capacitor-composing energy tank of the inverter. That provides many nodes in the inverter connecting to the different phases. The term level does not correspond to the voltage level that can be provided by the output inverter. Diodes can provide the path of reactive source from the load to the power supply at the current and voltage of Resistance Inductor load (RL) load having opposite polarity.

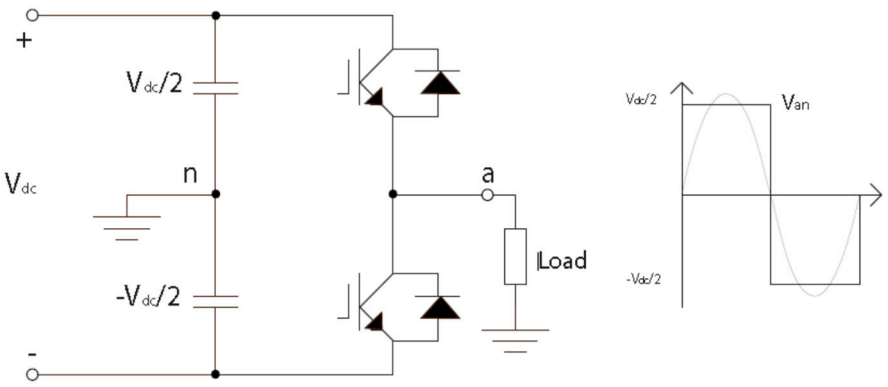


Figure 1. Two-level inverter.

A multilevel inverter has positive points compared with the two-level inverter using the PWM method. Also, a multilevel inverter produces very small distortions and dv/dt in the output side. In addition, it produces a common-mode voltage and operates at a lower switching frequency [2] than a two-stage inverter. Besides, there are several features of a multilevel inverter that can be summarized as the following: (1) the multilevel inverter does not produce low distortion output voltage, but it also decreases the dv/dt stresses. Consequently, problems with electromagnetic compatibility are cleared. (2) The multi-level inverter produces a lower voltage in a common mode; as a result, the motor attached load of the multilevel inverter may be decreased. (3) A multilevel inverter draws a small input current distortion. (4) To obtain more output voltage levels using fewer switching devices, many recently structured multilevel inverters have been presented in this publication [4–16].

In this paper, various multilevel inverter topologies are presented along with their analysis and comparative assessments. Furthermore, these topologies have been checked with the simulation results using PSCAD software. Then a comparison of different types of multilevel inverter topologies and describe PWM control techniques and we can choose one topology for further implementation and selected from the simulation results derived from the MULTISIM software.

2. Topologies of Multilevel Inverter

Normally, these inverters can be classified as voltage source or current source inverters as shown in Figure 2.

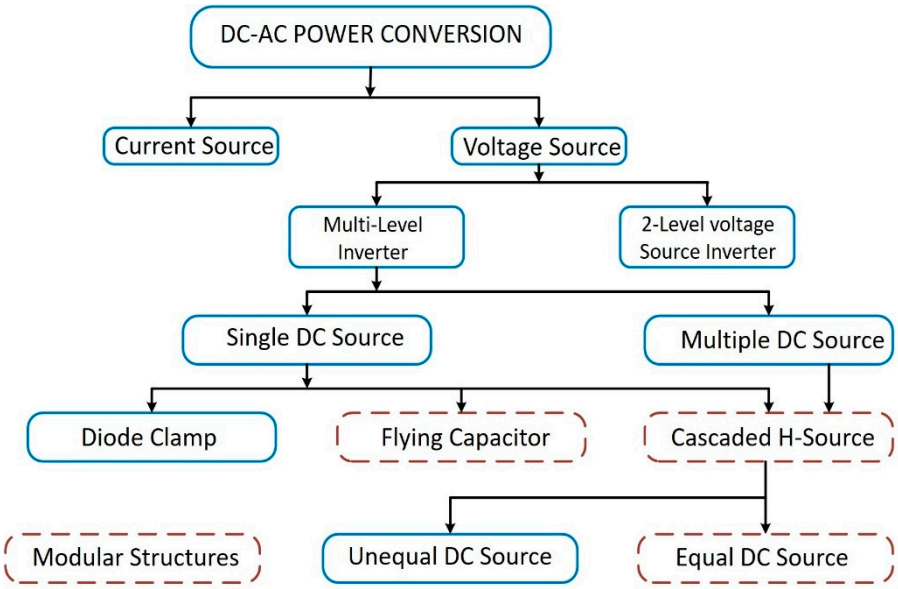


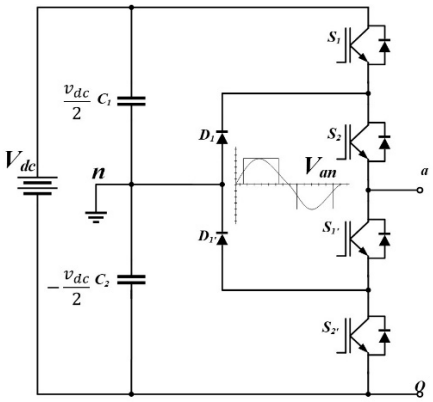
Figure 2. Voltage source or current source inverters.

Three major multilevel inverter configurations applied in industrial applications and mentioned in several literatures; cascaded H-bridges inverter with separate DC sources, Diode Clamp, and flying capacitors used virtually in low, medium and high-power applications are briefly discussed.

2.1. Diode-Clamped Multilevel Inverter (DC-MLI)

The multilevel inverter was invented in 1975, which was a cascade diode inverter. After a few years, it was called the diode-clamped multilevel inverter (DC-MLI) [2]. In DC-MLI, voltage clamping diodes are required to regulate the voltage on the DC bus to reach output voltage levels; but the multilevel inverter level should be unique because the neutral point is not available even in number levels [17]. For DC bus with a neutral point and a capacitor, there is a clamping diode attached to the number of valve pairs (m-1), where m is the level of voltage in the inverter. The explanation as to why the frequency converter is connected to the series with a diode; means that all diodes have the same rated voltage and may block a correct voltage level [18].

A 3-level DC-MLI, a voltage per capacitor and switch is Vdc/2. The equations are utilized to decide the number of devices forming a given level of a DC-MLI. If m is the number of levels, the number of capacitors on the DC side (C) can be determined through Equation (1). The number of switches (S) per phase and the clamp diodes (D) can be determined through Equations (2) and (3), respectively. Consequently, 4 switches, 2 diodes, and 2 capacitors are needed as shown in Figure 3a. The intermediate circuit voltage is divided into three phases, with two capacitors C1 and C2 which are attached in series; "n" is a neutral point which is the center point of the capacitors. There are 3 levels of output voltage Vdc/2, 0, (−Vdc)/2, for voltage level Vdc/2, S1 and S2 are activated, for voltage level (−Vdc)/2, S1′ and S2′ are activated, and for 0 level voltage, S2 and S1′ are activated. When S2′ and S1′ are connected, the load is shortened, and the reactive power released.



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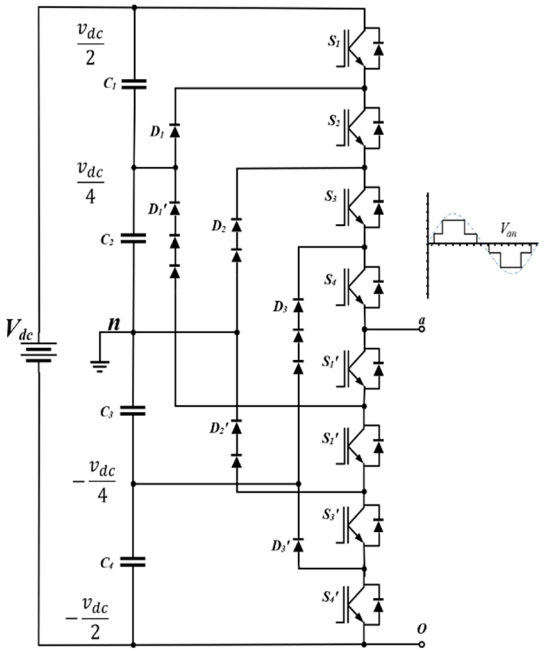

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Figure 3. (**a**) Three-level diode-clamped multilevel inverter (DC-MLI); (**b**) 5-level DC-MLI.

For the 5-level diode clamped multilevel inverter, m is 5. Following Equations (1), (2) and (3), therefore, 8 switches, 4 diodes, and 4 capacitors are needed. Figure 3b shows that all diodes are designed for Vdc/4, and diodes D1′ block 3Vdc/4. Hence, 3 diodes are connected in a series. At 5 voltage levels, Vdc/2, Vdc/4, 0, (−Vdc)/4, (−Vdc)/2 are five states output. To get various output voltage levels, combinations of switching states are utilized. For Vdc/2, top all switches are activated and, for Vdc/4, S2, S3, S4, and S1′ are activated and a voltage is maintained through a clamping diodes D1 and D1′. For 0 level voltage, S3, S4, S1′ and S2′ are activated, for a voltage (−Vdc)/4, switch S4, S1′, S2′, and S3′ are activated and voltage (−Vdc)/2 the bottom all switches are activated and the diodes D2 and D2′ or D3 and D3′ are maintaining the voltage.

$$C = m - 1 \tag{1}$$

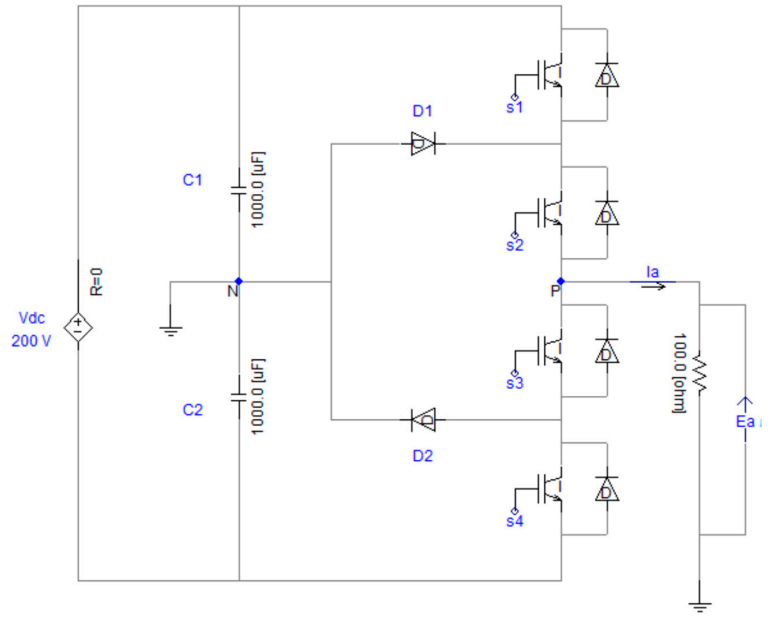
$$S = 2(m - 1) \tag{2}$$

$$D = (m-1)(m-2) \tag{3}$$

There are few advantages of DC-MLI: high efficiency, due to the main switching frequency that can be used for all devices. Capacitors are pre-charged as a group; all stages have the usual DC bus. That reduces the capacitance of the inverter. However, there are a few drawbacks of this topology: it is difficult to flow active power, and controlling is quite difficult for the capacitor voltage balance.

2.1.1. 3-Level DC-MLI PSCAD Simulations

In Figure 4a, consider the source voltage as +2 Vdc. There are total two capacitors connected to source, hence the voltage across each capacitor is Vdc. As shown in the switching Table 1 the voltage levels are available as per the switching sequence.



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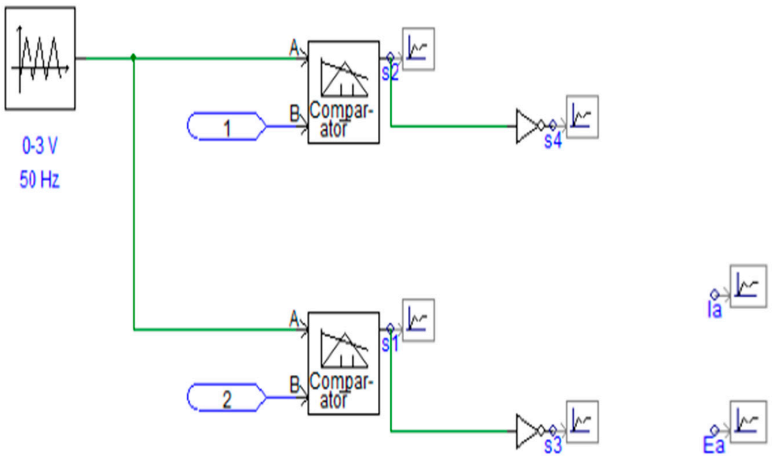

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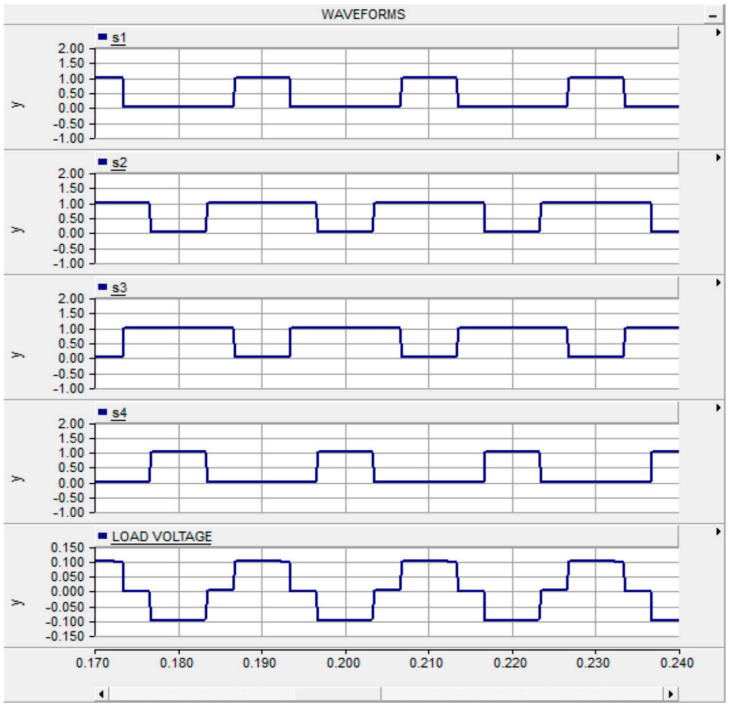


(**c**)

Figure 4. (**a**) Power circuit of 3- level DC-MLI; (**b**) control circuit of 3- level DC-MLI; (**c**) phase output voltage waveform of 3-level DC-MLI.

+Vdc: Switches S1, S2 are ON. In this case, current flows from source (charged capacitors C1) to load through switches S1, S2. 0 voltage: Switches S2 and S3 are ON. Hence no capacitor is discharged through the load. Here the load is directly connected to ground at both the ends (shorted). Hence the voltage across the load is 0 V. −Vdc: Switches S3 and S4 are ON. In this case, current flows from source (charged capacitors C2) to the load through switches S3 and S4.

In Figure 4b, a control circuit there is 4 switch signal generated using two comparators. 0–3 V, 50 Hz cycle, a triangular waveform is used for comparison. A different DC signal is used as a base for a comparator. This will generate four signals S1, and S2 with different widths. The other two, S3 and S4, are obtained using NOT gate. These 4 gate signals are ready to supply to IGBT which are in the 3-level DC-MLI power circuit, which is illustrated in Figure 4a.

Table 1. 3- Voltage levels of DC-MLI and switching states.

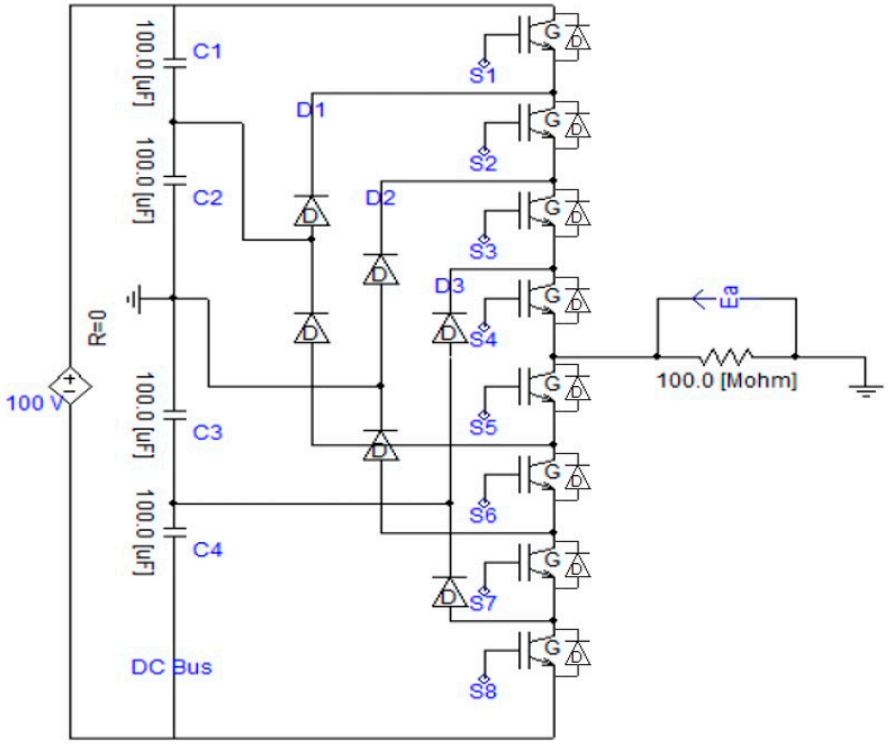
Voltage	S1	S2	S3	S4
Vdc	1	1	0	0
0	0	1	1	0
−*Vdc*	0	0	1	1

2.1.2. 5-Level DC-MLI PSCAD Simulations

In Figure 5a, consider the source voltage as +Vdc. There are total four capacitors connected to source, hence the voltage across each capacitor is +Vdc/4. As shown in the switching Table 2 the voltage levels are available as per the switching sequence.

+Vdc/2: Switches S1, S2, S3, S4 are ON. In this case, current flows from source (charged capacitors C1, C2) to load through switches S1, S2, S3, S4. +Vdc/4: Switches S2, S3, S4, and S5 are ON. Here only capacitor C2 discharges through diode D1 and the switches S2, S3, and S4 to the load. Since only half of the capacitor (only C2) discharges, hence total Vdc/4 voltage is available. 0 voltage: Switches S3, S4, S5 and S6 are ON. Hence no capacitor is discharged through the load. Here the load is directly

connected to ground at both the ends (shorted). Hence the voltage across the load is 0 V. −Vdc/4: Switches S4, S5, S6, and S7 are ON. Hence the capacitor C3 discharges through the ground–load and switch S5, S6, and S7. As the discharge is in the opposite direction the voltage appeared will be negative. −Vdc/2: Switches S5, S6, S7 and S8 are ON. Capacitor C3 and C4 will discharge through the load in the opposite direction (from the ground to load to switches). Hence total voltage –Vdc/2 will appear across the load. In Figure 5b a control circuit there is 8 switch signal generated using four comparators. 0 – 10 V, 50 Hz cycle, a triangular waveform is used for comparison. And different DC signal is used as a base for a comparator. This will generate four signals S1, S2, S3 and S4 with different widths. Other four S5 to S8 are obtained using NOT gate. These 8 gate signals are ready to supply to IGBT which are in the 5-level DC-MLI power circuit, which is shown in Figure 5a.



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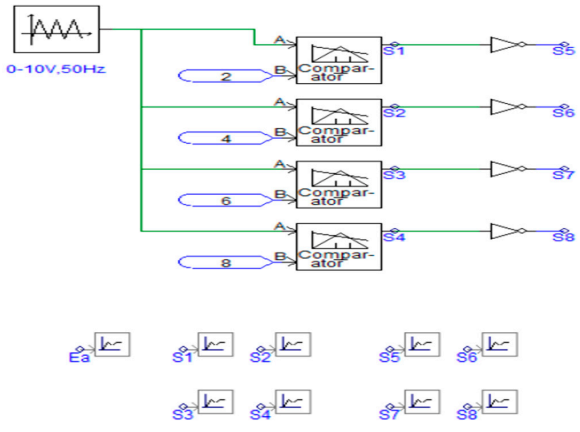

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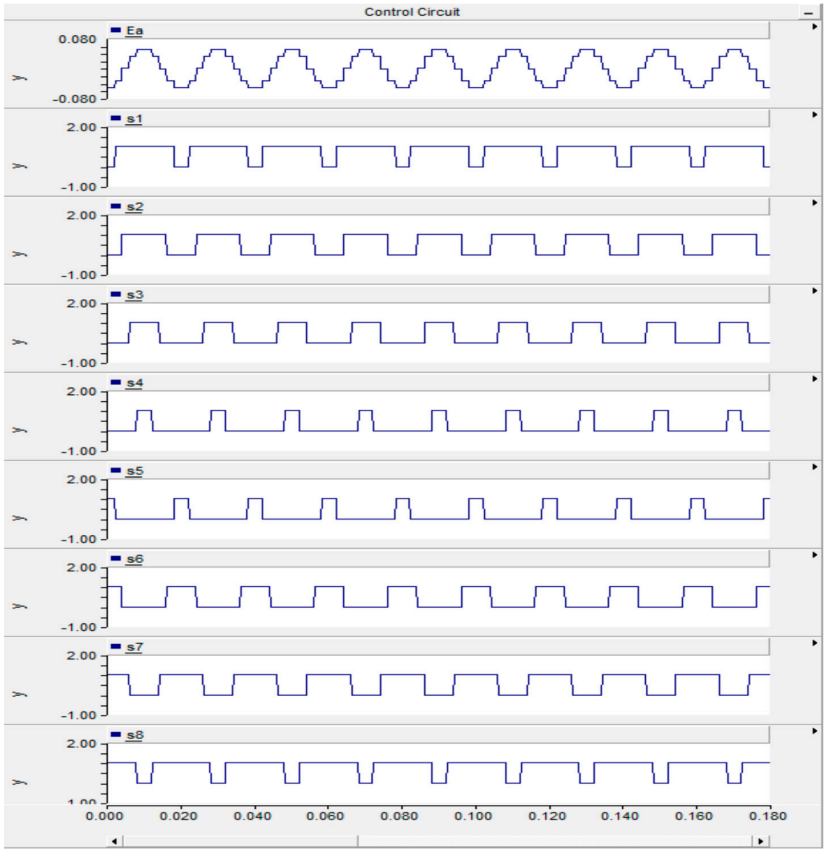


(**c**)

Figure 5. (**a**) Power circuit of 5-level DC-MLI; (**b**) control circuit of 5-level DC-MLI; (**c**) phase output voltage waveform of 5-level DC-MLI.

Table 2. 5-Voltage levels of DC-MLI and switching states.

Voltage	S1	S2	S3	S4	S5	S6	S7	S8
$\frac{Vdc}{2}$	1	1	1	1	0	0	0	0
$\frac{Vdc}{4}$	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
$\frac{-Vdc}{4}$	0	0	0	1	1	1	1	0
$\frac{-Vdc}{2}$	0	0	0	0	1	1	1	1

2.2. *Cascaded H-Bridge Multilevel Inverter (CHB-MLI)*

There are various inverter topologies based on a series single-phase inverter connected to the individual DC source. If an inverter is implemented in an active transfer of source applications, then the sources of each bridge must be separated. Due to this property, it is recommended to use a cascaded H-bridge multilevel inverter (CHB-MLI) in fuel cells or photovoltaic (PV) array to reach a higher level [19–21].

The resulting phase voltage has been synthesized through increasing the generated voltages through different cells. The module of a bridge is a three-level in CHB-MLI, and each module is appended to the cascade. The output voltage for an n-level cascade multilevel inverter is 2n + 1, where n is the source of DC [22]. Switching angles are obtained to reduce the overall distortion of harmonics. Maximum output voltage is decided by using Equation. (6) and minimum output voltage is decided

by using Equation (7). The capacitors at the DC side (C) and several switches (S) per phase, calculated through Equations (4) and (5) respectively.

$$\mathrm{C} = \frac{m-1}{2} \tag{4}$$

$$S = 2(m-1) \tag{5}$$

$$Maximum\ output\ voltage = \frac{m-1}{2}(Vdc) \tag{6}$$

$$Minimum\ output\ voltage = \frac{m-1}{2}(-Vdc) \tag{7}$$

Figure 6a shows 3-level CHB-MLI. Here is a full-bridge that provides 3-levels of output. It is a simple diagram of 3-level CHB-MLI. This provides 3-levels of output; Vdc, 0 and −Vdc, while battery voltage is Vdc, where E = Vdc.

As we have already discussed with Equations (4)–(7), for voltage level 3 m = 3, therefore Vdc is a maximum voltage, and (−Vdc) is minimum output voltage. One DC bus capacitor and four switches are needed. Generally, to get the output voltage, there are two activating switches. Hence, one pair of switches gives a positive result and another pair create a negative result. Therefore, to obtain the output source Vdc, T1, and T2′ are activated, and the output source −Vdc, T2 and T1′ are turned on. If the current does not pass from the full-bridge then the 0-voltage source is obtained through the switch T1 and T2 or lower two switches T1′and T2′.

Figure 6b represents 5-level CHB-MLI. One full-bridge module is a three-step cascade multilevel inverter. Two bridge modules generate five various voltage levels; 2Vdc, Vdc, 0, (−Vdc), and (−2Vdc). As a Vdc battery voltage with E = Vdc. In 5-level CHB-MLI, we take m = 5. Therefore, following Equations (4), (5), (6) and (7), 2 capacitors at the DC side, 8 switches are needed. So, the maximum output voltage is 2Vdc, and a minimum output voltage is −2Vdc.

As discussed in the three-level cascade multilevel inverter, the cross switches are activated, and upper or lower switches obtain a 0-voltage. Thus, to get the output sources 2Vdc, T11 and T12′ or T21 and T22′ to be activated and the current passing through the capacitor C1 and C2. As with a negative voltage, the other four cross switches are connected. For output voltage Vdc, the battery bypassed either top or bottom. Therefore, the current pass throughout C1, T11, a load, T22′, T21′, and T12′. Besides, for the minimum voltage (−Vdc), the current passes in the contrasting path, and its passing by C2, T22, load, T11′, T12′ and T21′. For 0 power, there are two probabilities, 1) switches T11, T12, T21, T22 are activated; 2) switches T11′, T12′, T21′, T22′ are activated. This topology is convenient especially for photovoltaic generation application, where photovoltaics modules are directly connected to an individual DC source [23].

The principle advantages of CHB-MLI are a series of H-bridges demonstrating an advanced design, this will empower the assembling procedure to be rapidly and efficiently, also voltage adjustment is easy. Although there are few disadvantages of CHB-MLI topology, each H-Bridge needs an isolated DC source, which limits its use. That has more access to the SDCS, and no ordinary DC-bus [24].

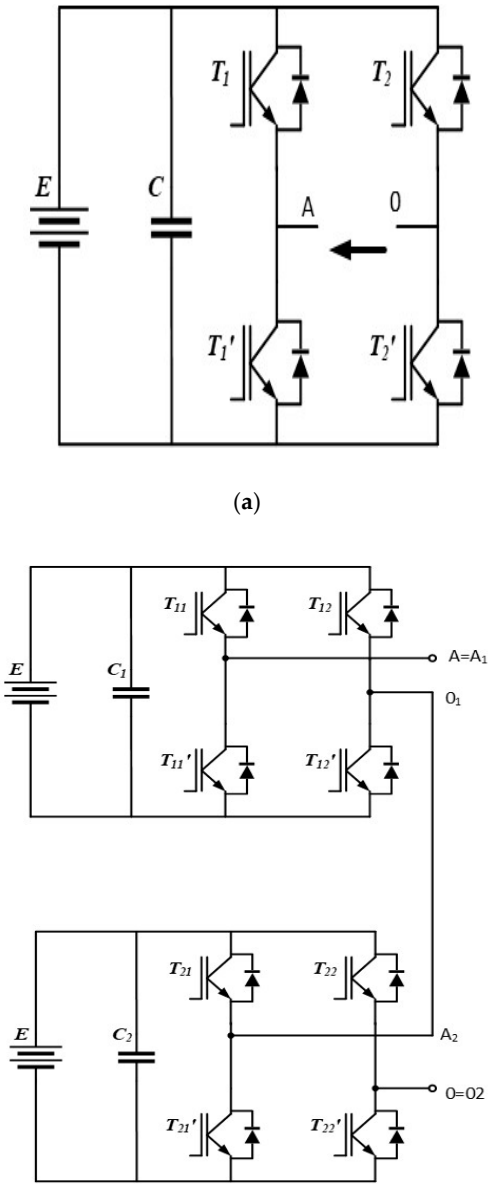


Figure 6. (**a**) Three-level cascaded H-bridge multilevel inverter (CHB-MLI); (**b**) 5-level CHB-MLI.

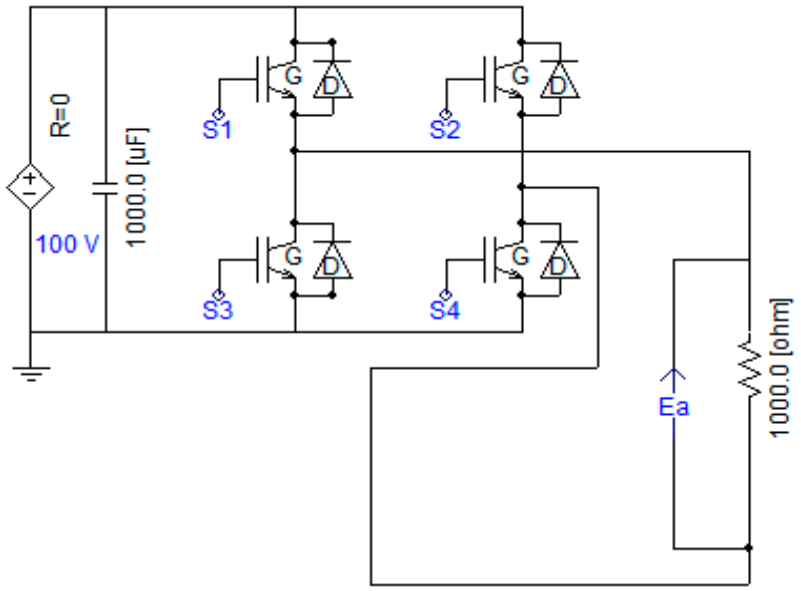
2.2.1. Three-Level CHB-MLI PSCAD Simulations

In Figure 7b, the control circuit has two gate signals S1 and S2. Those are available from the comparator. Another two has the NOT gate with initial two signals. These four signals are ready to supply to IGBT which are in the 3-level CHB-MLI power circuit.

In Figure 7a, all the gate pulses are applied to the different IGBT of CHB-MLI. This follows Table 3 of a sequence of a waveform for gate signals. For Vdc; switched S1 and S4 are conduct. Hence, current flow from the source, S1, load, S4, and source, for 0Vdc; S3 and S4 are conducted and for −Vdc; S2 and S3 are conducted, therefore current flow from the source, S2, load, S3, and source.

Table 3. Voltage levels of 3-level cascade H-bridge multilevel inverter and switching states.

Voltage	S1	S2	S3	S4
Vdc	1	0	0	1
0	0	0	1	1
$-Vdc$	0	1	1	0



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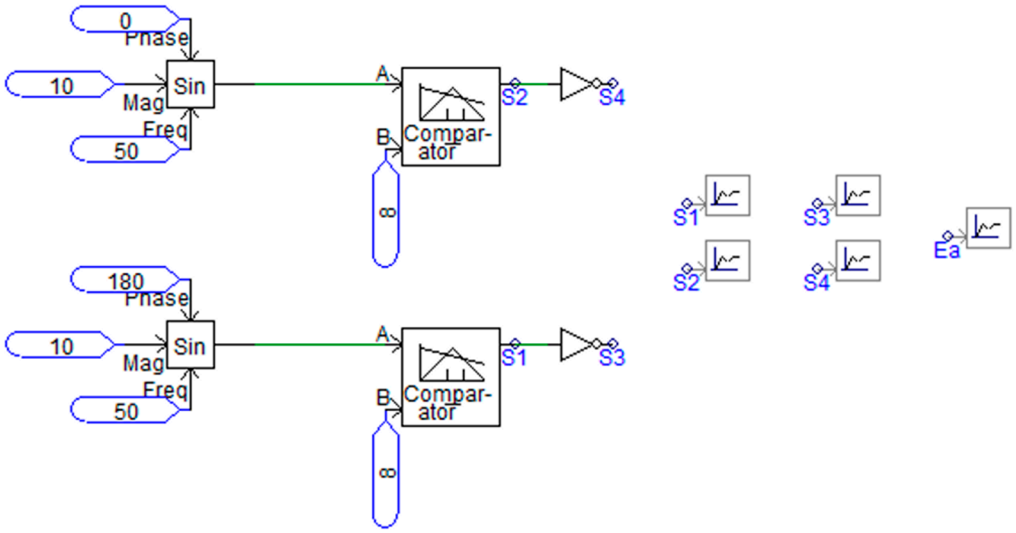

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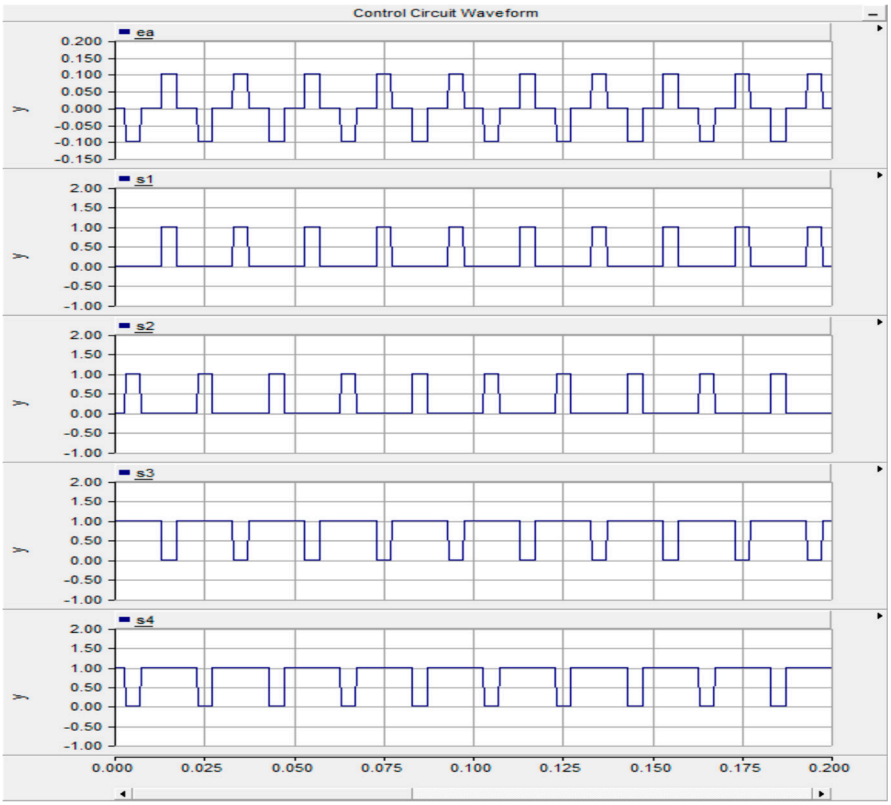


(**c**)

Figure 7. (**a**) Power circuit of 3- level CHB-MLI; (**b**) control circuit of 3- level CHB- MLI; (**c**) phase output voltage waveform of 3-level CHB-MLI.

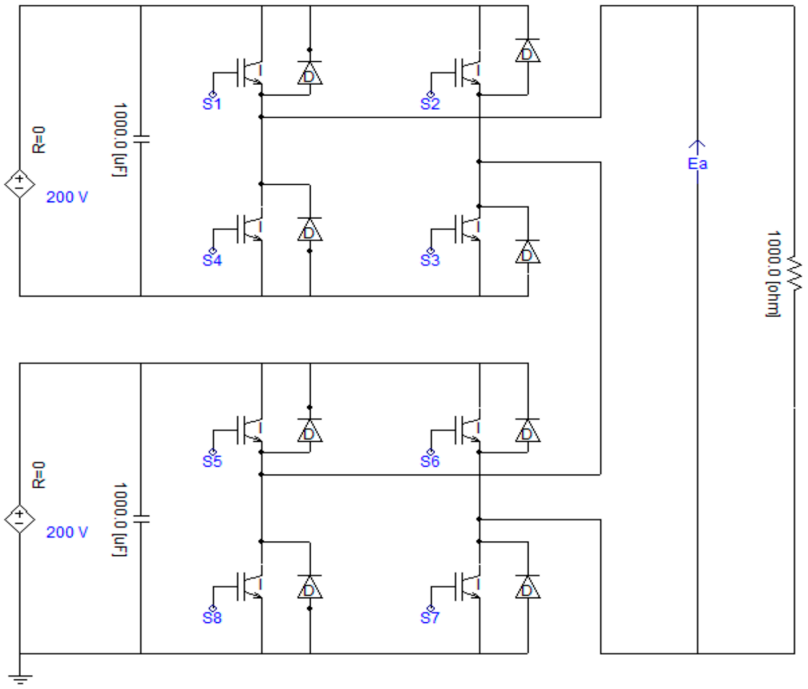
2.2.2. Five-Level CHB-MLI PSCAD Simulation

In Figure 8b, the control circuit waveforms are generated by comparison of DC signal (2 V and 4V) with the triangular waveforms (−10 V to +10 V) changing the values of DC voltage will change the gate pulse widths. Four signals S1, S2, S5, and S6 are available from the comparator. The other four signals are obtained using the NOT gate with initial four signals. These 8 gate signals S1, S2, S3, S4, S5, S6, S7, and S8 are ready to supply to IGBT which are in the 5-level CHB-MLI power circuit, which is shown in Figure 8c.

In Figure 8a, all gate signals are applied to the IGBT of CHB-MLI. The following Table 4 represents the sequence of waveforms for gate signals. Considering for +2 Vdc the corresponding switches such as S1, S3, S5, and S7 are turned ON. Therefore, there is a current path takes from Source-1, S1, Load, S7, Source-2, S5, S3 and Source-1. As a result, the two sources are added to each other and so the voltage +2 Vdc is available. Similarly, for +Vdc, the switches S1, S3, S7, and S8 are turned on and the current flows through the Source-1, S1, load, S7, S8, S3 and back to Source-1. For 0 Vdc, switches S3, S4, S7, and S8 are turned on. For −Vdc, switches S2, S4, S7, S8 are turned on, Current flow through Source-1, S2, S7, S8 Load (the reverse direction), S4, back to source-1. −2Vdc: S2, S4, S6, S8 are turned ON, current flows through the Source-1, S2, S8, Source-2, S6, Load (the reverse direction), S4 and then back to Source-1.

Table 4. Voltage levels of 5-level CHB-MLI and switching states.

Voltage	S1	S2	S3	S4	S5	S6	S7	S8
$2Vdc$	1	0	1	0	1	0	1	0
Vdc	1	0	1	0	0	0	1	1
0	0	0	1	1	0	0	1	1
$-Vdc$	0	1	0	1	0	0	1	1
$-2Vdc$	0	1	0	1	0	1	0	1



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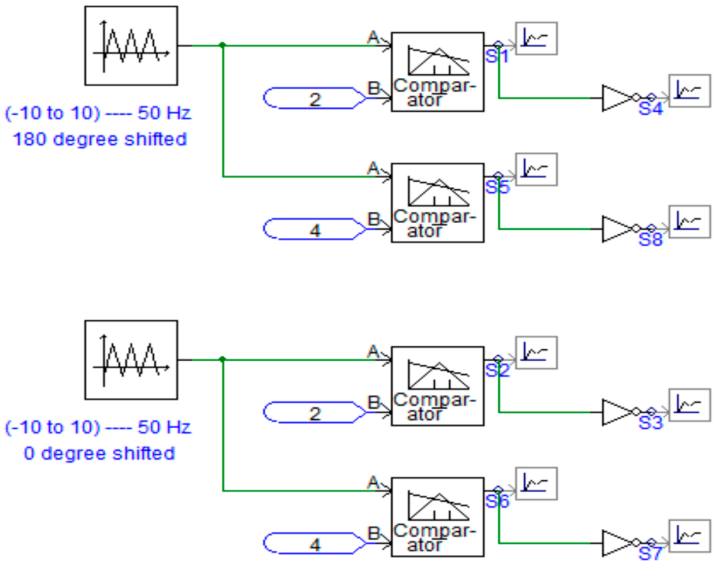

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Figure 8. *Cont*.

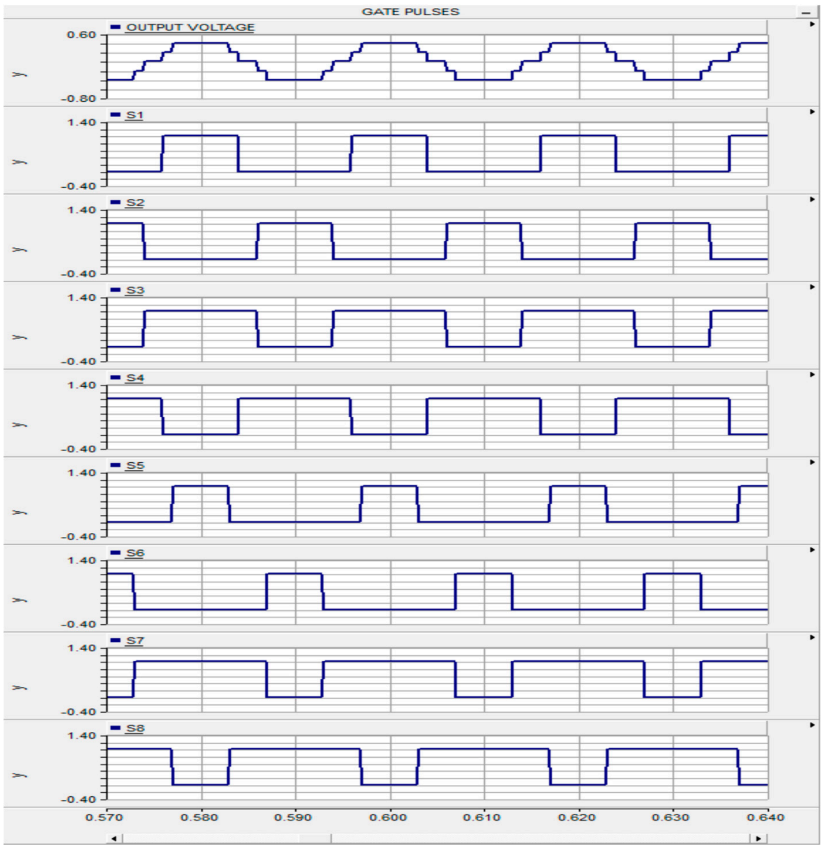

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Figure 8. (**a**) Power circuit of 5-level CHB-MLI; (**b**) control circuit of 5-level CHB-MLI; (**c**) phase output voltage waveform of 5-level CHB-MLI.

2.3. Flying-Capacitor Multilevel Inverter (FC-MLI)

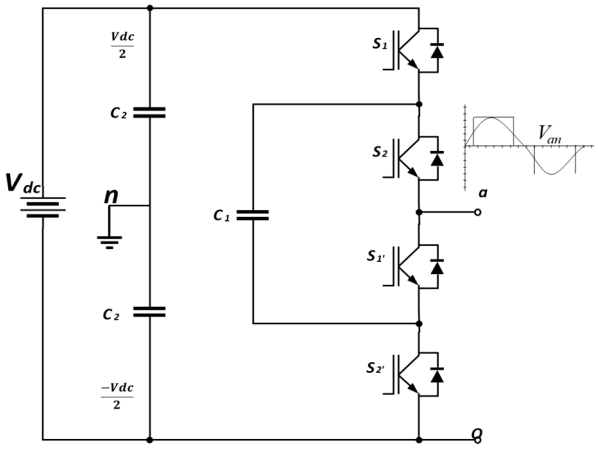
The same topology of the DC-MLI is a capacitor-clamping or flying-capacitor multilevel inverter (FC-MLI) topology in which clamping capacitors are utilized to clamp the voltages [25]. This topology is new compared with other topologies. The voltage between the two capacitors refers to the output voltage at the terminal [26]. The indicated voltage level in the flying-capacitor inverter is the same as like diode-clamped multilevel inverter [27]. Moreover, switching pairs may be different and asymmetrical according to the regulating policy, but the choice of the two pairs leads to the switching state redundancy, which may utilize to attain the voltage balancing of FC-MLI [2,28,29]. The number of output voltage levels is increased through appending some additional switches and a capacitor. Besides this, for FC-MLI (m-1) number of capacitors on a common DC-bus, where m is the level number of the inverter, and 2(m-1) switch-diode valve pairs are used, and [(m-1) (m-2)/2] clamping capacitors per phase are used [28,30,31].

The choice of two pairs leads to a surface moving state, which can be used to obtain the FC-MLI balancing voltage [2,28,29]. In Figure 9a, this indicates 3-level FC-MLI, which has output over a and n points such as Vdc/2, 0, (−Vdc)/2. For voltage Vdc/2, S1 and S2 are activated, while (−Vdc)/2, S1′ and S2′ are activated and for 0 voltage, one pair activated either (S1, S1′) pair or (S2, S2′) pair. If S1 and S1′ are activated, then C1 is charged, and its discharge when S2 and S2′ are deactivated. A C1 is balanced through choosing the right combination of level 0 switches.

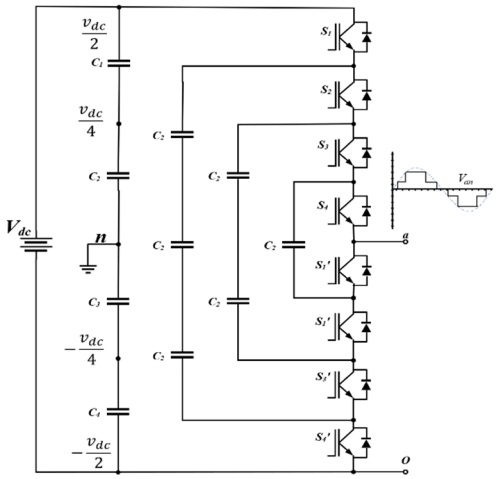
With 5 levels of flying capacitor multilevel inverter, the output voltage is more flexible than a diode clamp inverter. Figure 9b shows a 5-level voltage through the neutral point n, Van is reached through some switching combustions. For voltage Vdc/2, Switch S1–S4 is activated, voltage level Vdc/4, there are 3 amalgamations, 1) S1, S2, S3, and S1′ are activated (Vdc/2 of top C4′s and −Vdc/4 of

C1), 2) S2, S3, S4, and S4′ are activated (3Vdc/4 of C3′s and (−Vdc)/2 of lower C4), 3) S1, S3, S4, and S3′ are activated (Vdc/2 of top C4′, (−3 Vdc)/4 of C3′s or (−Vdc/)/2 of C2), and voltage 0, S3,S4,S1′ and S2′ are activated. For voltage (−Vdc)/4 S1, S1′, S2′ and S3′ are activated (Vdc/2 of top C4′s and (−3 Vdc)/4 of C3), and for (−Vdc)/2, activate all lower switches S1′ − S4′.)

A most essential superiority of FC-MLI is phase redundancy using for balancing the voltage levels or capacitors, easy to regulate an active and reactive power. In addition, using capacitors means, an inverter can move throughout small period outages. However, there are few drawbacks too. It is difficult to remark on the voltage level for capacitors, pre-charged every capacitor is at a similar voltage, starting is difficult, and switching usage and productivity are poor for actual power transmission [24].



(**a**)



(**b**)

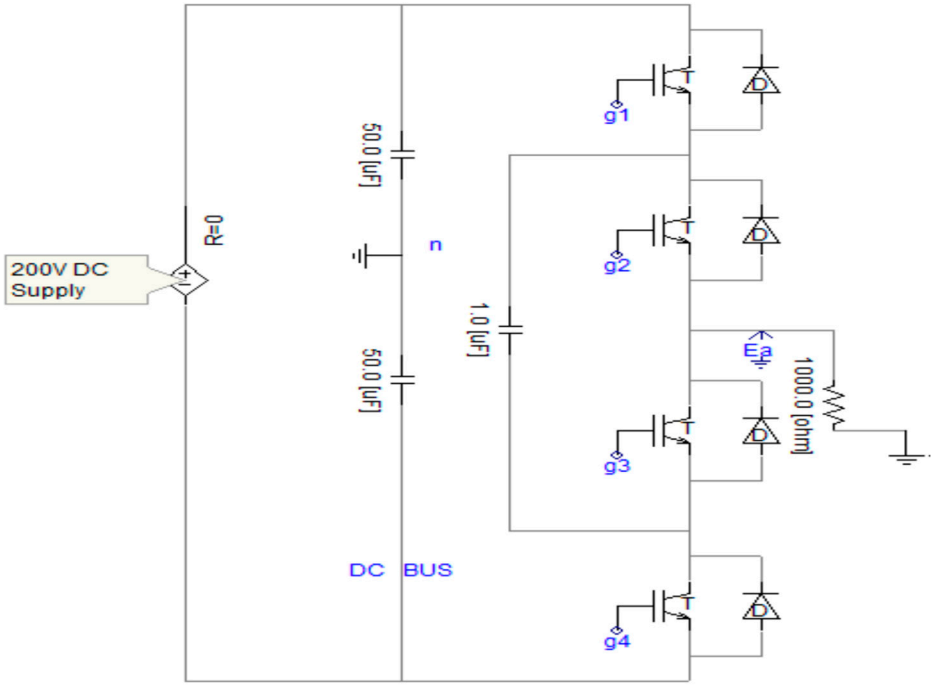
Figure 9. (**a**) Three-level flying-capacitor multilevel inverter (FC-MLI); (**b**) 5-level FC-MLI.

In the above description, positive marks of capacitors are in discharge mode and the negative capacitor marks are in charge mode. With the right choice of capacitor combinations, we can balance a capacitor charge. As with diode clamping, many bulk capacitors are needed to clamp the voltage. Specified nominal voltage of the capacitor used as the main power switch.

2.3.1. Three-Level FC-MLI PSCAD Simulations

In Figure 10b, the control circuit with two gate signals of g1 and g2 are available. Another two are obtained using the NOT gate with initial two signals. These four signals are ready to give to IGBT which are in the 3-level FC-MLI power circuit.

In Figure 10a, all the gate pulses are applied to the different IGBT of FC-MLI following Table 5 of a sequence of a waveform for gate signals. For Vdc; switched g1 and g4 are conduct. For 0Vdc; g1 and g3 are conducted and for −Vdc; g3 and g4 are conducted.



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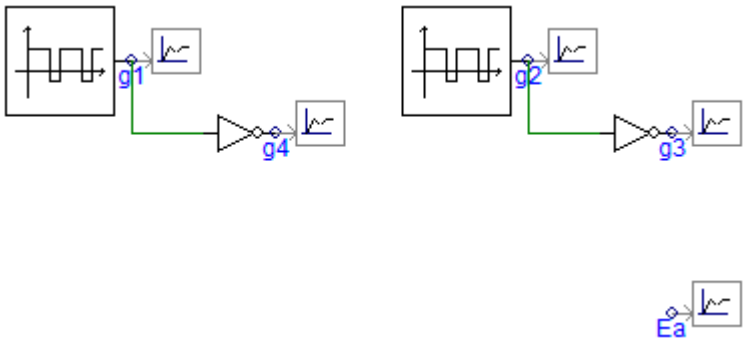
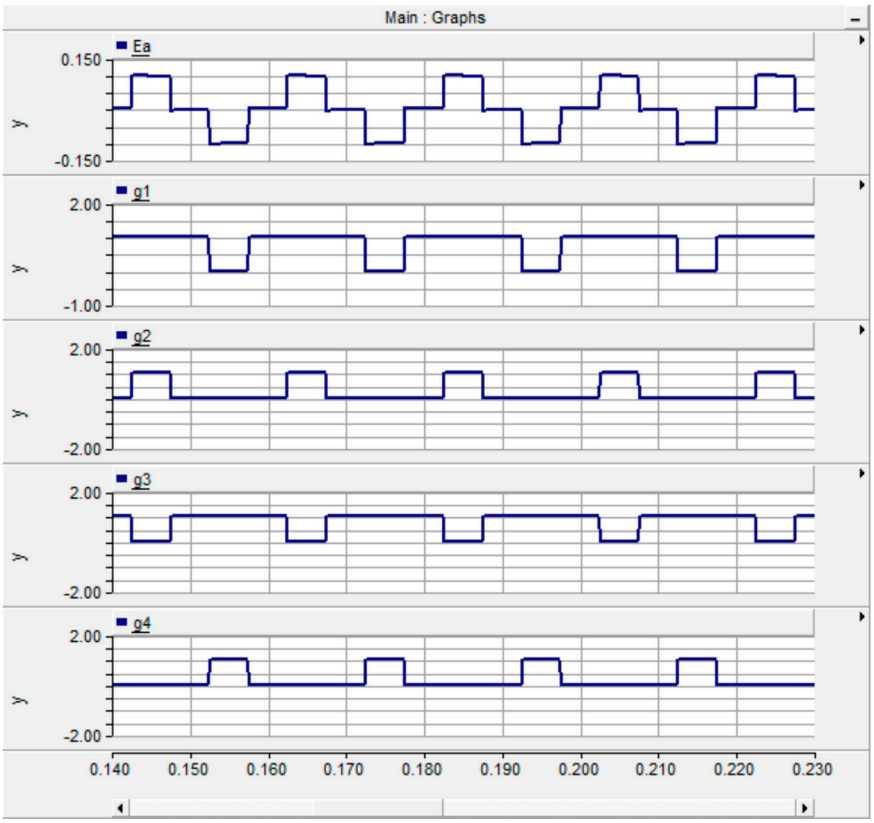


(**b**)

Figure 10. *Cont.*



(**c**)

Figure 10. (**a**) Power circuit of 3- level FC-MLI; (**b**) control circuit of 3- level FC-MLI; (**c**) phase output voltage waveform of 3-level FC-MLI.

Table 5. Voltage levels of 3-level flying-capacitor multilevel inverter and switching states.

Voltage	g1	g2	g3	g4
Vdc	1	1	0	0
0	1	0	1	0
$-Vdc$	0	0	1	1

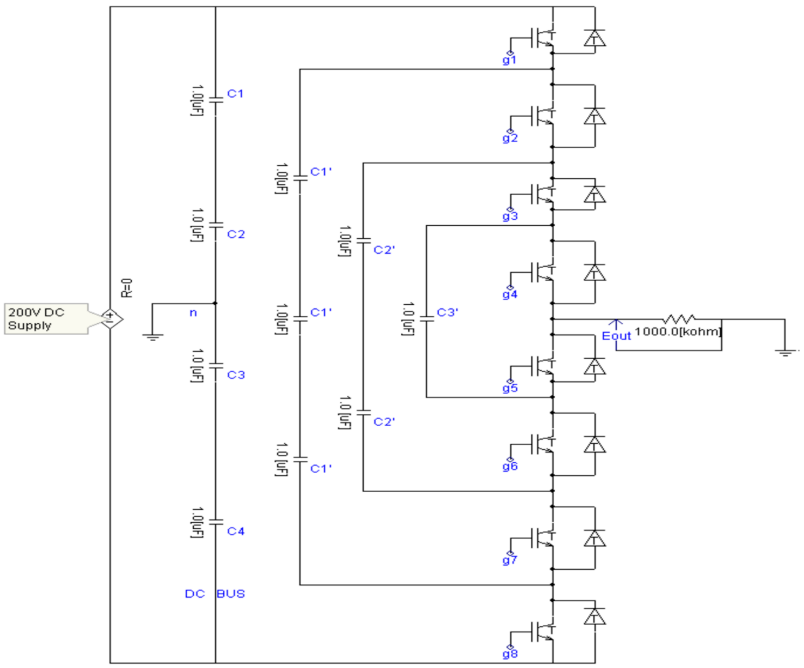
2.3.2. Five-Level FC-MLI PSCAD Simulations

Figure 11b, the control circuit waveforms are generated by comparison of the DC signal (2 V and 4 V) with the sinusoidal waveforms (5 V RMS). Changing the values of the DC voltage will change the gate pulse widths. Four signals g1, g2, g3, and g4 are available from the direct comparator. The other four signals are obtained using the NOT with initial four signals. These 8 gate signals are ready to give to IGBT which are in the FC-MLI power circuit.

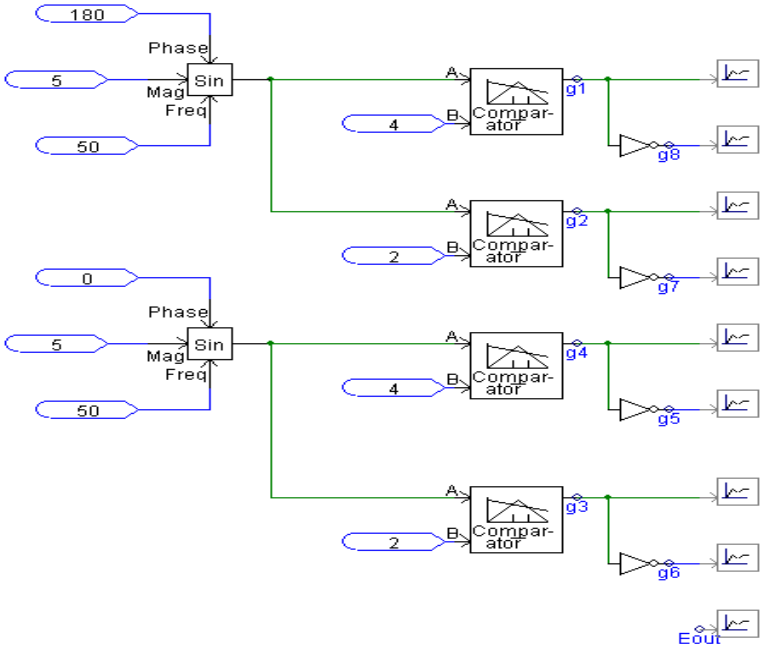
In Figure 11a, all the available gate signals are given to IGBT of FC-MLI Inverter, following Table 6 of the sequence of a waveform for gate signals. Here the total voltage is divided into a capacitor bridge. Each capacitor (C1, C2, C3, and C4) of the first line gets charged with Vdc/4 voltage. Also, each intermediate capacitor (C1′, C2′, and C3′) gets charged by +Vdc/4.

+Vdc/2: Switched g1, g2, g3, and g4 are turned ON. Hence, current flow from capacitor C2, C1, g1, g2, g3, g4 to the load. Hence, by two capacitor-discharge, (+Vdc/4 +Vdc/4) = +Vdc/2 is available at load side. +Vdc/4: Similarly, g1, g2, g3, and g5 are turned on. Current flows, from capacitor C2, C1, g1, g2, g3, C3′ and g5 to the load. Hence the voltage across the load is Vdc/4. In other words, C3′ nullifies the voltage from one of the capacitors (C1 or C2) to load voltage. Hence only half voltage (of +Vdc/2) is available at the load. 0Vdc: g1, g2, g5, g6 are turned on. Similar to the previous operation, both C2′

capacitors provide the opposite voltage to C1 and C2. Hence equivalent voltage at the load is 0, −Vdc/4: g1, g5, g6, g7 are turned on. Current flows through the C2, C1, g1, C2′, C2′, C2′, g5, g6, g7, and load. Now here two capacitors charged with +Vdc/4, +Vdc/4, and three capacitors are in opposite direction and charged by +Vdc/4, +Vdc/4, +Vdc/4 hence the effective voltage at the load is (+2Vdc/4) − (+3Vdc/4) = −Vdc/4. −Vdc/2: g5, g6, g7, g8 are turned ON. Current flows from C4, C3 to load (reverse direction) Back to C4. Hence, the voltage of two capacitors is available at load side (−Vdc/4 + (−Vdc/4) = −Vdc/2.

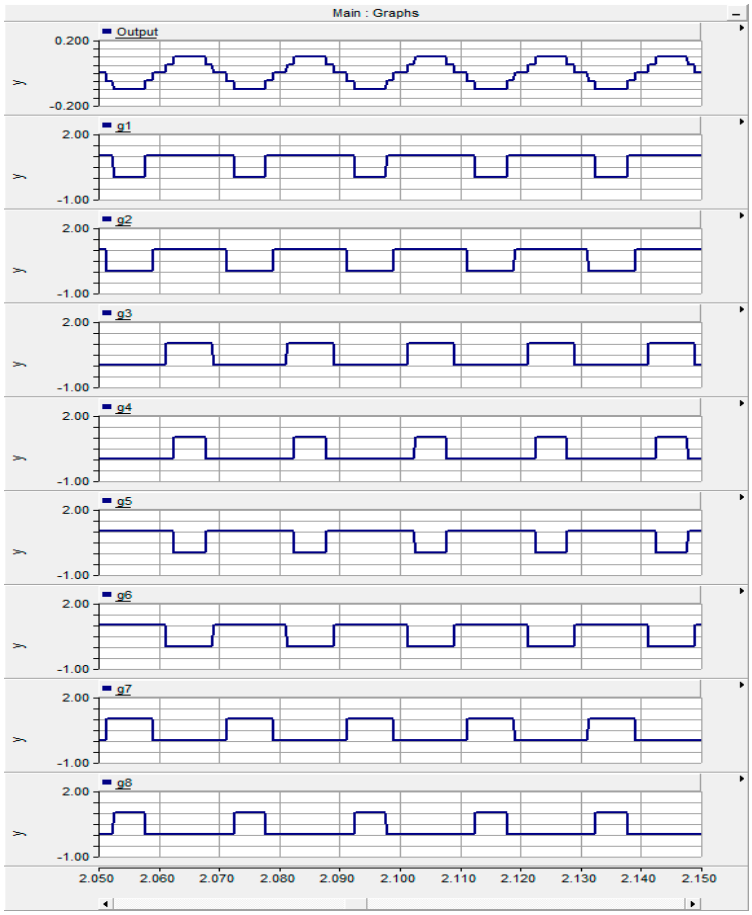


(**a**)



(**b**)

Figure 11. *Cont*.



(**c**)

Figure 11. (**a**) Power circuit of 5-level FC-MLI; (**b**) control circuit of 5-level FC-MLI; (**c**) phase output voltage waveform of 5-level FC-MLI.

Table 6. Voltage levels of 5-level FC-MLI and switching states.

Voltage	g1	g2	g3	g4	g5	g6	g7	g8
$\frac{Vdc}{2}$	1	1	1	1	0	0	0	0
$\frac{Vdc}{4}$	1	1	1	0	1	0	0	0
0	1	1	0	0	1	1	0	0
$\frac{-Vdc}{4}$	1	0	0	0	1	1	1	0
$\frac{-Vdc}{2}$	0	0	0	0	1	1	1	1

3. Performance Evaluations of Different Multilevel Inverters and Characteristics Overview

The various topologies discussed, described, and analyzed till now are comprehensively compared in this section on the basis of different performance parameters such as number capacitors and diodes, switches, flexibility, balancing capacitor, and cost in Table 7.

For high-voltage applications, for instance high-voltage DC (HVDC), a relatively high voltage level can be chosen for a modular multilevel inverter [5,32–53] to the total required current THD, and dv/dt. For medium- and low-voltage applications, five and three-level inverters for A-NPC [54–58] and other FC-MLI inverters may be better suited to current specifications. Currently, multilevel inverters have been suggested in motor drives, flexible AC transmission systems (FACTS) and HVDC. As per the studies conducted in [2,59–67], the positive points, negative points, methods of modulation, and application of these inverters are epitomized in Table 8.

Table 7. Comparative assessment of various multilevel inverters.

IT	DC-MLI	FC-MLI	CHB-MLI	A-NPC	MMC
MS	$2(m-1)$	$2(m-1)$	$2(m-1)$	$3(m-1)$	$2(m-1)$
MD	$2(m-1)$	$2(m-1)$	$2(m-1)$	$3(m-1)$	$2(m-1)$
CD	$(m-1)\,(m-2)$	-	-	-	-
DBC	$(m-1)$	$(m-1)$	$\frac{(m-1)}{2}$	-	-
BC	-	$\frac{(m-1)(m-2)}{2}$	-	-	-
RD	Not Redundant	Redundant	Redundant	Redundant	Redundant
F	Not Flexible	Not Flexible	Flexible	Flexible	Not Flexible
MDV	$2\sqrt{2}$ Va	$2\sqrt{2}$ Va	$2\sqrt{2}$ Va	$2\sqrt{2}$ Va	$2\sqrt{2}$ Va
CVR	$\frac{\text{Vdc}}{m-1}$	$\frac{\text{Vdc}}{m-1}$	$\frac{\text{Vdc}}{m-1}$	$\frac{\text{Vdc}}{m-1}$	$\frac{\text{Vdc}}{m-1}$
ACC	Ia	Ia	Ia	Ia	Ia
C	M	M	M	H	H

Note: IT: inverter types, DC-MLI: diode-clamped multilevel inverter, FC-MLI: flying-capacitor multilevel inverter, CHB-MLI: cascade H-bridge multilevel inverter, A-NPC: active NPC, MMC: modular multilevel converter, MS: main switches, MD: main diodes, CD: clamping diodes, DBC: DC-bus capacitor, BC: balancing capacitor, RD: redundancy, F: flexibility, MDV: minimum DC voltage, CVR: component voltage rating, ACC: active component current, C: cost, H: high, M: medium.

Table 8. Performance summary of multilevel inverter.

R	T	A	D	MT	AP
[2,59–64]	DC-MLI	Low cost and fewer components due to a smaller number of capacitors therefore simple structure; equalized blocking voltage of power.	Unequal distribution of power losses; DC-link voltage balance limits the converter to three-level topology.	Pulse width modulation (PWM) carrier modulation (based zero-sequence injection); Space vector pulse width modulation (SVPWM) method (based space vector selection).	Renewable energy; variable speed motor drive; static var compensation; HVDC/AC transmission lines.
[64–68]	FC-MLI	Modular structure; possessing a large number of redundant states; each branch can be analyzed independently.	The poor dynamic response of dc voltage balancing; large amounts of flying capacitors reduce the system reliability; pre-charging capacitors is difficult.	Phase-shifted carrier PWM (achieves neutral balancing of flying capacitors).	Renewable energy; motor drive; induction motor control using direct torque control circuit; sinusoidal current rectifiers; static var generation.
[69–71]	CHB-MLI	Modular structure is easier to analyses; possessing fault tolerant capability; same switching frequencies for all the switches.	Separate DC sources are required; isolated transformers increase the system volume.	Phase-shifted carrier PWM (achieves equalization of power losses).	Renewable energy; DC power source utilization; Power factor compensators; flexible alternating current transmission system (FACTS); electric vehicle drives.
[32–51,72–76]	MMC	Modular structure; easy to achieve fault tolerant operation.	Low-frequency voltage oscillation of floating capacitors; complex data acquisition and communication for each power cell.	Nearest-level modulation (achieves equalization of power losses and dc voltage balance).	High-voltage DC (HVDC) transmission, A static synchronous compensator (STATCOM)
[54–58]	A-NPC	Simple structure; easily extendable to a higher level by stacking flying.	Unequal usage of switches and flying capacitors; requires series switches to handle high voltage.	Hybrid phase-shifted PWM (low frequency for high voltage switches and high frequency for flying capacitor cells).	Renewable energy

Note: R: Reference, T: Topology, A: Advantage, D: Disadvantage, MT: Modulation Technique, AP: Application.

3.1. Choosing Topology

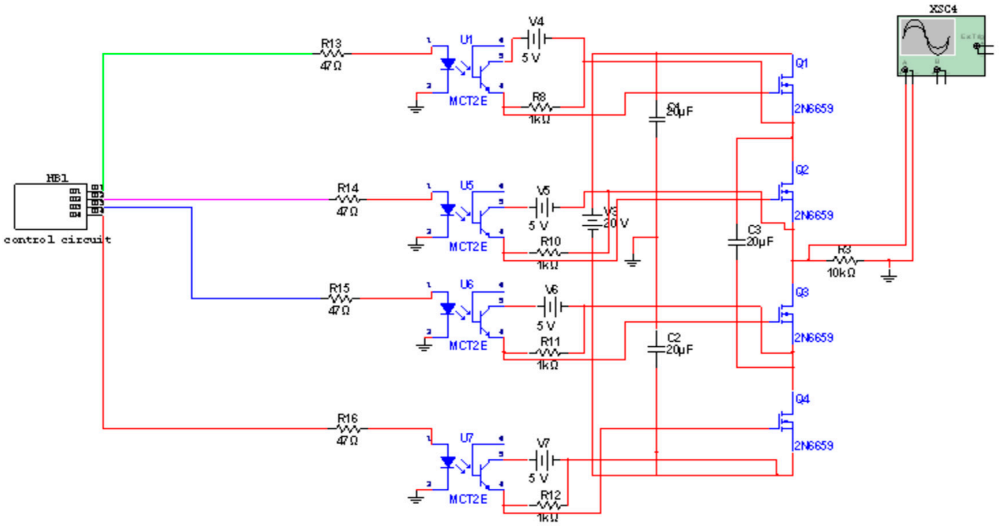
Discussed all multilevel inverters are utilized to generate a smooth waveform, mostly for medium voltage drives. Out of three FC-MLI [19,77–82] is relatively new compared to DC-MLI and CHB-MLI. Moreover, FC-MLI has some unique benefits over DC-MLI, including the truancy of clamp diodes and the ability to adjust the voltage of the flying capacitor by selecting an excess state. Even the voltage level is higher than 3 [81]. Unlike CHB-MLI, no separate voltage sources are required. Also, there are two

types having some deficiencies, such as most DC in CHB-MLI. Losses are higher in the DC-MLI. but FC-MLI has introduced more potential outcomes to regulate the DC-link capacitor's voltage contrasting to another multilevel topology that uses redundant switching arrangements. An FC-MLI topology is designed for higher voltage and lower voltage-distortion performance. Moreover, in an FC-MLI, capacitors are using for clamping the power over the devices. Also, FC-MLI is appropriate to heavy load systems. Meanwhile, induction motors are utilizing as a load in many industrial applications [78].

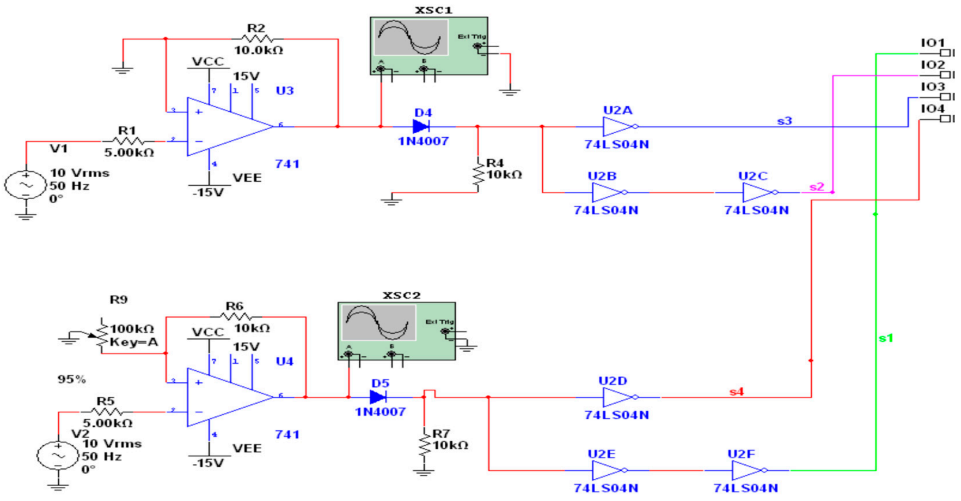
3.2. MULTISIM Simulations of FC-MLI

3.2.1. Three-Level FC-MLI MULTISIM Simulations

In the above Figure 12a, the control circuit has a hierarchical block which will be explained in the next section. Here, the same power circuit is used as the above explained. There are three capacitors. Among three capacitors, two capacitors make the DC bus and remaining capacitor acts as a flying capacitor which is used for the clamping voltage at different levels. Here we have used 20 V DC as source power supply. There are four MOSFET switches which are triggered by the gate pulses that generate from the control circuit. Four optocouplers MCT 2E are used for the isolation purpose.



(**a**)

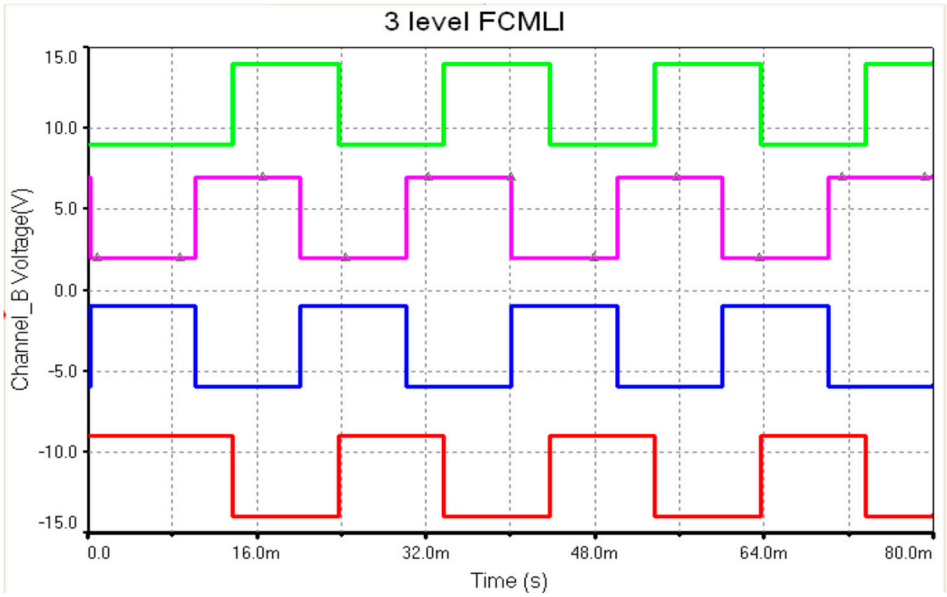


(**b**)

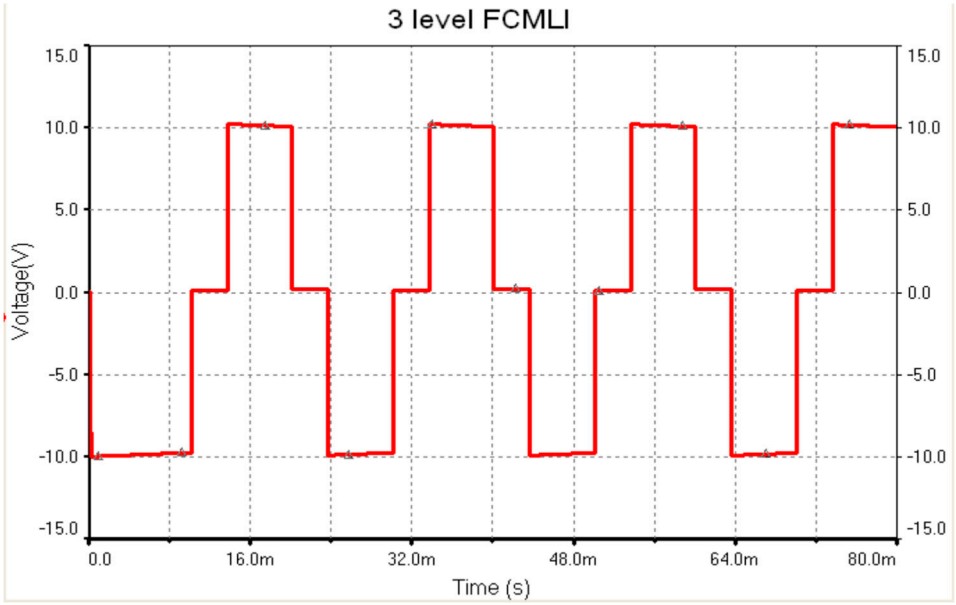
Figure 12. (**a**) Power circuit of 3-Level FC-MLI MULTISIM simulations; (**b**) control circuit of 3-level FC-MLI MULTISIM simulations.

We have generated four gate pulses using the OP-AMPs. In Figure 12b, we have used one OP-AMP as a ZERO CROSSING DETECTOR and another as a SCHMITT TRIGGER. The output of the SCHMITT TRIGGER is a square wave but shifted from the output of the ZERO CROSSING DETECTOR (ZCD). The shifting can vary by varying the POT of 50Kohm. If the shifting is higher than the output, that has the higher width of zero pulses.

As in Figure 13. we can see the all 3 levels of output. Here we used 20 V DC as a power source, therefore we have 2 different levels of (Vdc/2) =10 V, and (−Vdc/2) = −10 V. By changing the DC voltage in the OP-AMP comparator, we can change the width of output zero voltage. This width of zero voltage decides the amount of reactive power flow in the system.



(**a**)

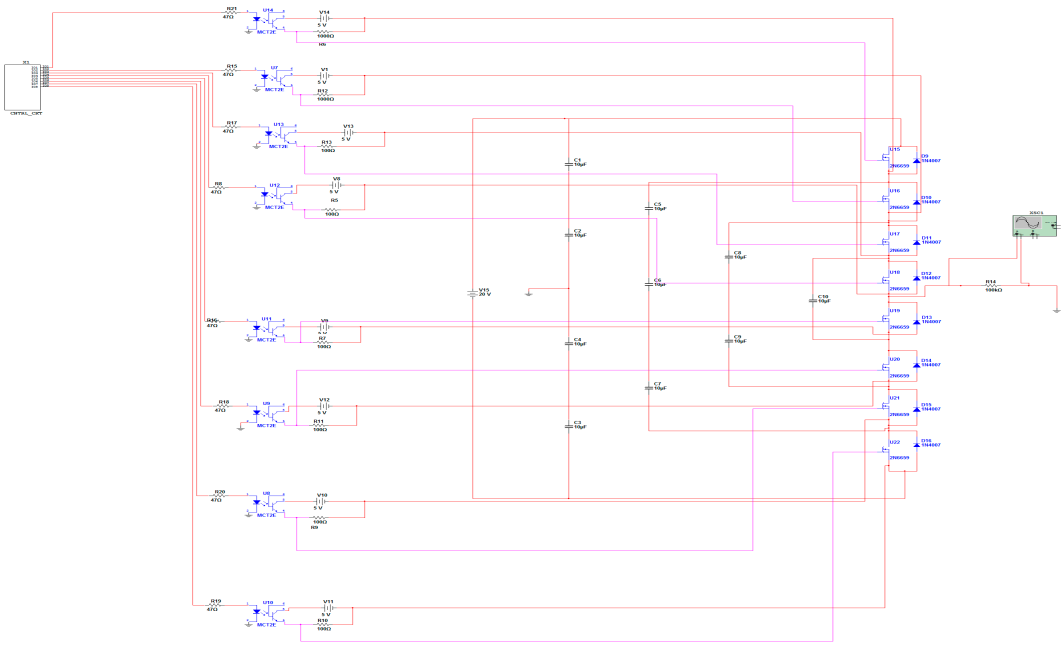


(**b**)

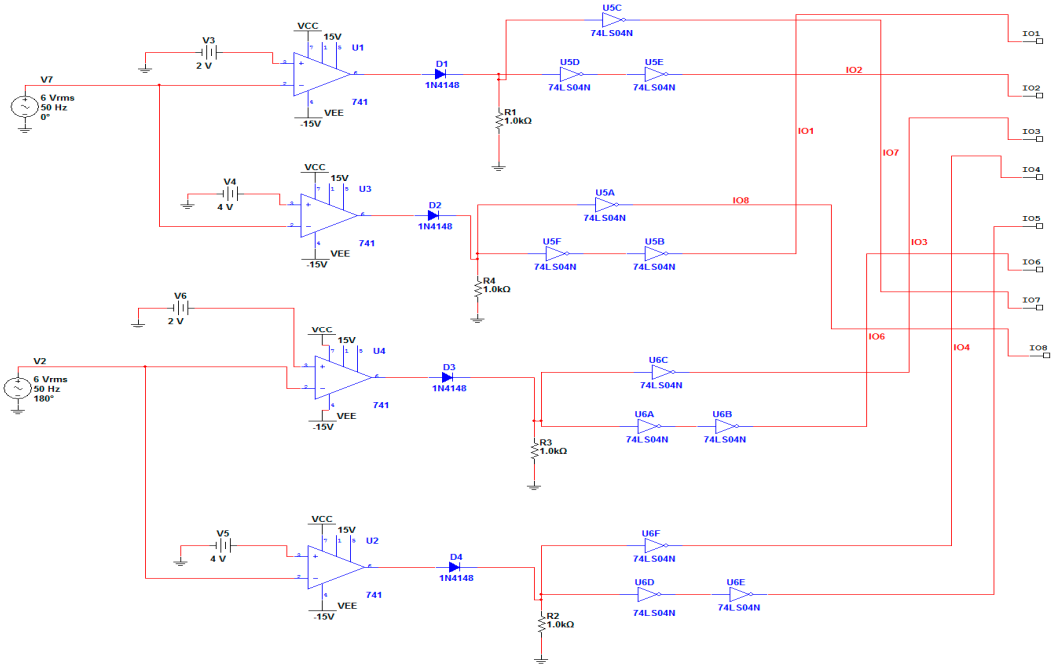
Figure 13. (**a**) Gate pules of 3-level FC-MLI; (**b**) phase output voltage waveforms of a 3-level FC-MLI using MULTISIM.

3.2.2. 5-Level FC-MLI MULTISIM Simulations

The full set-up is shown in Figure 14a. That is divided into the following two parts. That diagram is the same as explained above. Here, we have used MOSFET 2N6659 as a switching device. And the similar three-level optocoupler MCT 2E is used for isolation. We have demonstrated the purely resistive load for the simplicity. We can change the load as per the relevant applications.



(**a**)



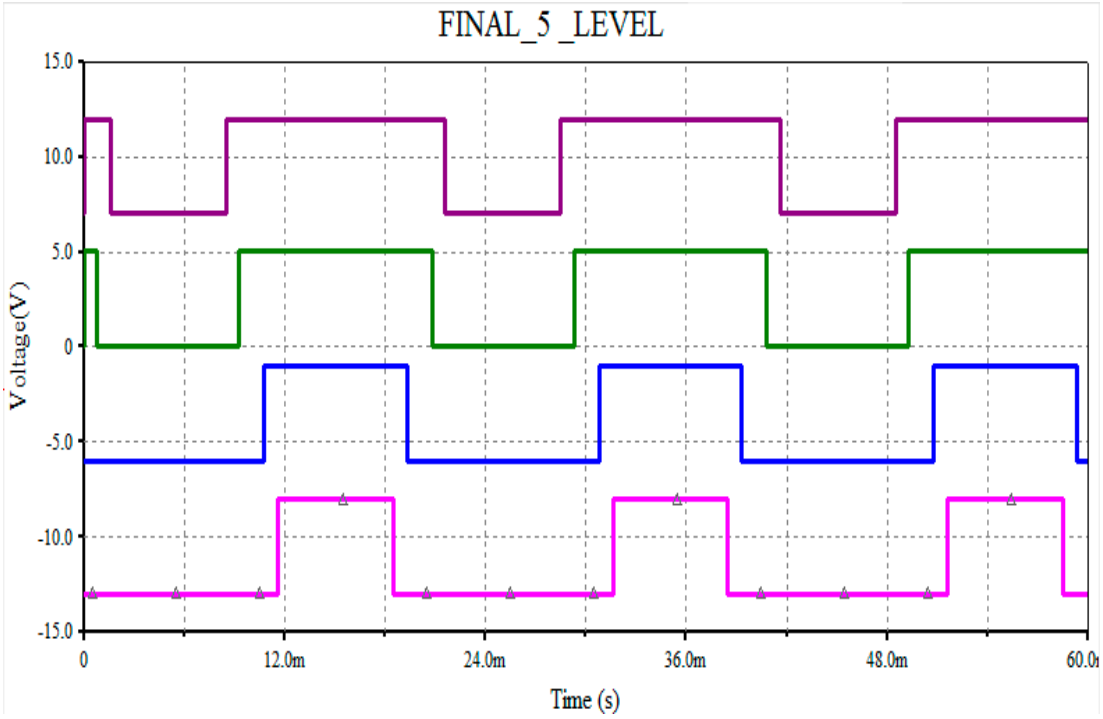
(**b**)

Figure 14. (**a**). Power circuit of 5-Level FC-MLI MULTISIM simulations; (**b**) control circuit of 5-Level FC-MLI MULTISIM simulations.

Now as the above explained theory, 4 switches get turning on at any time and remaining four switches get turning off at any time what you want. Therefore, each switch gets 1/4th voltage of power supply as a reverse burden.

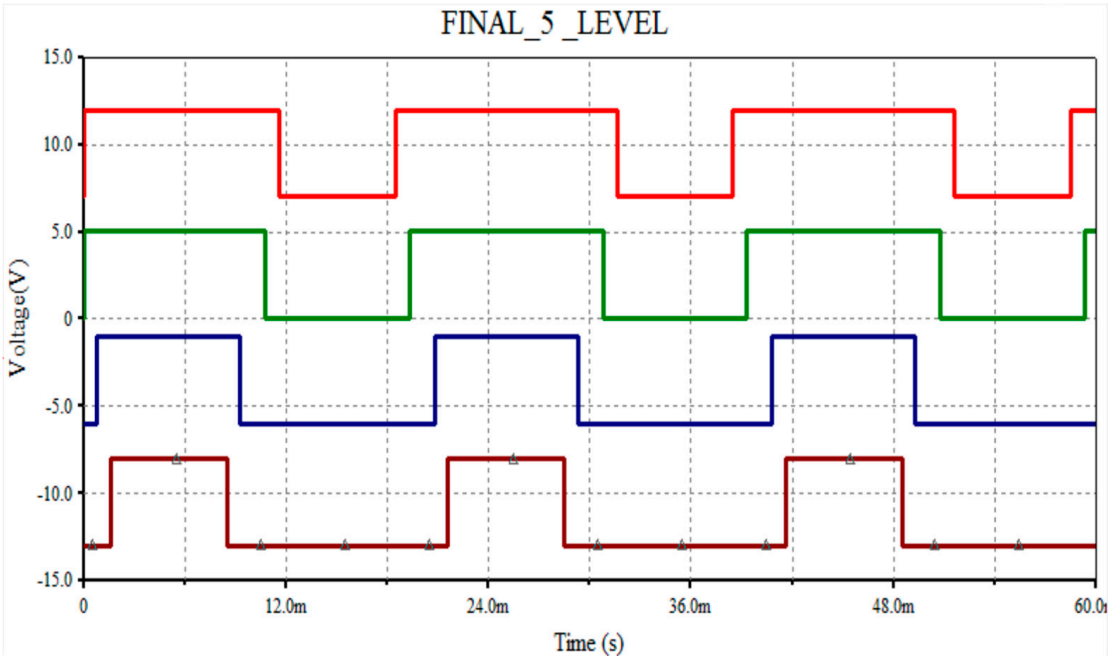
Figure 14b for the control circuit, we have used the two sinusoidal power supplies as the reference by comparing it with DC power supply. We have four different outputs having four gates from the required eight pulses. We can obtain the NOT gate combination from the remaining four pulses. Thus, we can get eight pulses and these pulses are applied to the power circuit through an optocoupler.

In Figure 15a–c we can see all the 5-levels output and gate pulses. Here we have used 20 V DC. As a source, we have 4 different levels of (Vdc/2) = 10 V, (Vdc/4) = 5 V, 0 V, (−Vdc/4) = −5 V, (Vdc/2) = −10 V. By changing the DC. voltage in the OP-AMP comparator; we can change the width of zero for output voltage. This width of zero voltage decides the amount of reactive power flow in the system.



(**a**)

Figure 15. *Cont.*



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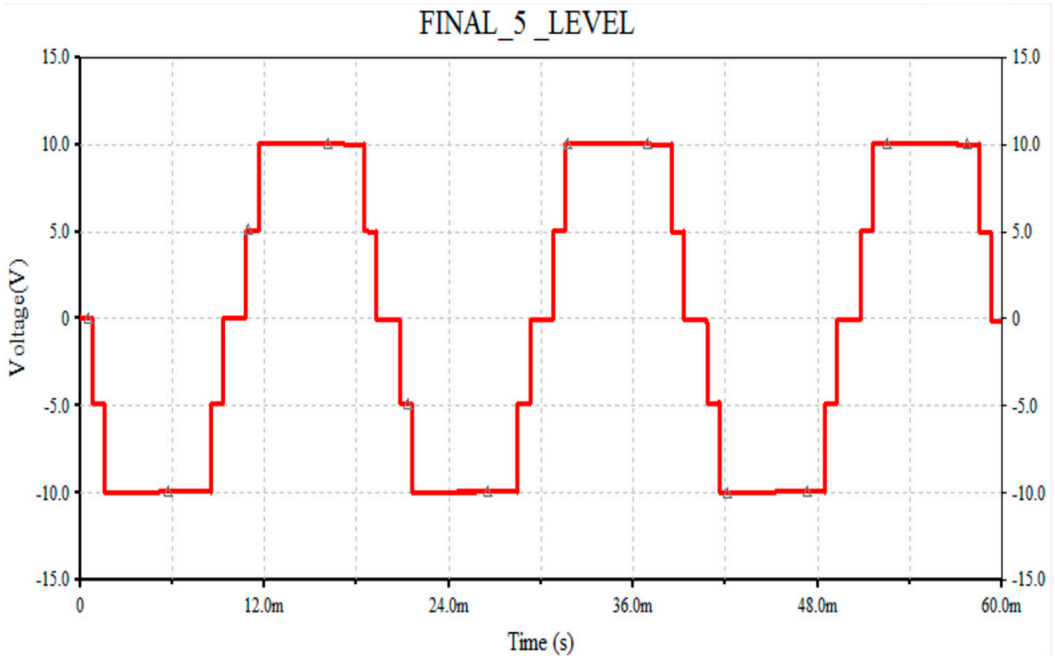


(**c**)

Figure 15. (**a**) S1–S4 gate pules of 5-level FC-MLI; (**b**) S5-S8 gate pules of 5-level FC-MLI; (**c**) Phase output voltage waveforms of a 5-level FC-MLI using MULTISIM.

4. Harmonics Analysis of FC-MLI

4.1. Total Harmonic Distortion (THD)

The THD is a presenting measurement of harmonic distortion and defined the proportion between harmonic components and the fundamental frequency of the power. THD is utilized to characterize the linearity of audio systems and the power quality of electric systems.

If the input signal is sinusoidal, the computation often corresponds to the proportion of the powers of all the harmonic frequencies beyond the power of the 1st harmonic and the main frequency.

$$THD = \frac{P_2 + P_3 + P_4 + \cdots + P_\infty}{P_1} = \frac{\sum_{i=2}^{\infty} P^i}{P_1} \tag{8}$$

Which can equivalently be written as:

$$THD = \frac{P_{total} - P_1}{P_1} \tag{9}$$

It is also defined as the amplitude ratio, not the power ratio which results in the determination of THD given the square root to the above equation.

$$THD = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \cdots + V_\infty^2}}{V_1} \tag{10}$$

4.1.1. Harmonics Analysis of 3-Level FC-MLI

As shown in Figure 16, the analysis can be seen that for lower order mainly 5th and 7th harmonics are predominant. Here the third harmonic has been reduced very much.

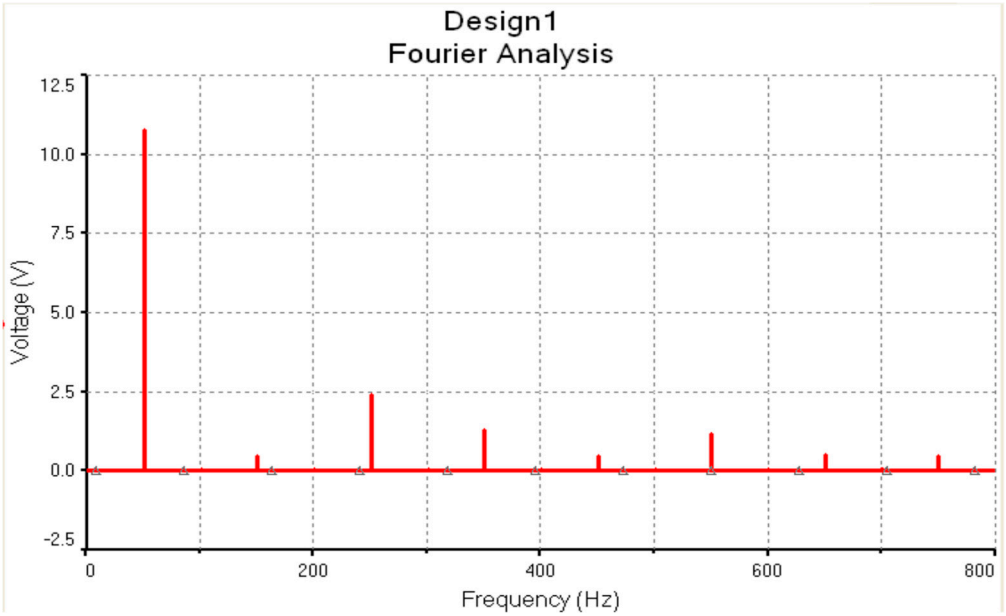


Figure 16. Fourier analysis of 3-level FC- MLI.

If we change the pulse width of our gate pulses then the harmonic reduction can be changed; more specifically, THD can be changed. Because of changing our pulse width, the starting angle of output wave changes and thus the harmonics also changes. However, if we compare this with conventional two-level inverter then we cannot find any harmonics in this topology compared with the two-level inverter.

In Table 9 shows the analysis of THD. The total harmonic distortion shows that how much percentage harmonics are present in the waveform or how much the waveform is disturbed from an actual sine wave.

Table 9. Total harmonic distortion (THD).

Fourier Analysis for V (25)					
DC Components	**0.142395**				
No. Harmonics	**15**				
THD	**28.8803%**				
Grid Size	**512**				
Interpolation Degree	**1**				
Harmonics	**Frequency**	**Magnitude**	**Phase**	**Norm. Mag**	**Norm. Phase**
1	50	10.7723	147.086	1	0
2	100	0.0359127	−87.093	0.00333381	−234.18
3	150	0.482066	−91.605	0.0447506	−238.69
4	200	0.0370429	−90.48	0.00343872	−237.57
5	250	2.40309	−164.03	0.223081	−311.11
6	300	0.0368095	−93.112	0.00341705	−240.2
7	350	1.2825	129.104	0.119056	−17.982
8	400	0.0367623	−94.406	0.00341267	−241.49
9	450	0.470903	−113.53	0.0437143	−260.61
10	500	0.0369758	−96.153	0.0034325	−243.24
11	550	1.14951	178.466	0.106709	31.3803
12	600	0.0368479	−97.806	0.00342062	−244.89
13	650	0.517375	111.212	0.0480284	−35.874
14	700	0.0369105	−99.11	0.00342644	−246.21
15	750	0.454395	−131.73	0.042818	−278.82

The following analysis is carried out by the MULTISIM software; here, we have found 15 numbers of harmonics. While analyzing; the sampling frequency is taken as 16 kHz. This analysis is also carried out with Lagrange's 1st degree of interpolation.

The above tabulated analysis gives us that mainly 5th and 7th harmonics are the predominating and has a major part in THD normal magnitude. A phase is measured by taking the fundamental 50 Hz as a reference.

4.1.2. Harmonics Analysis of 5-Level FC-MLI

In Figure 17, the analysis shows that the major 3rd harmonics is predominant but all other has very low impact. Hence, here THD is also less as given in Table 10.

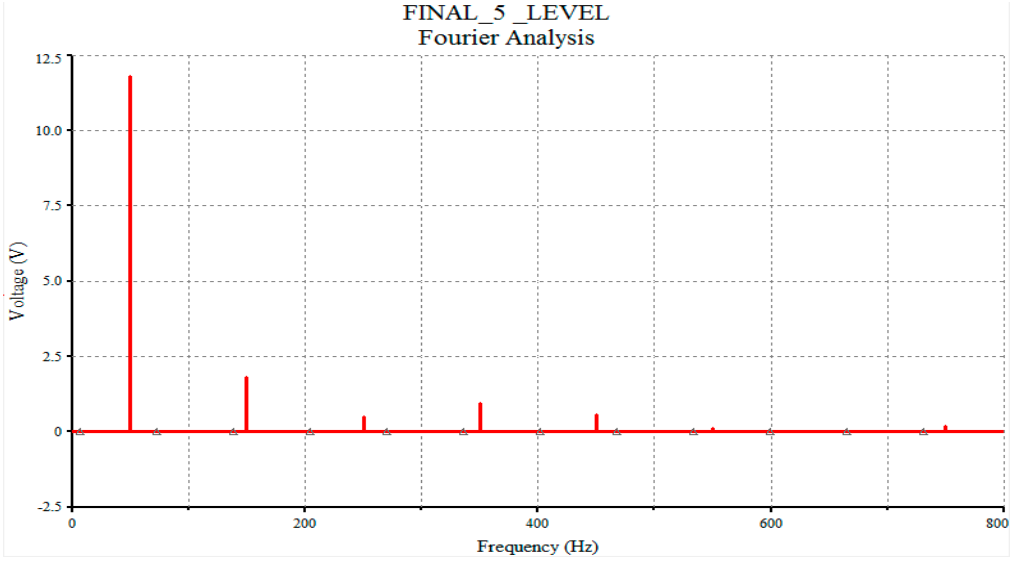


Figure 17. Fourier analysis of 5-level FC- MLI.

Table 10. Total harmonic distortion.

Fourier Analysis for V (47)					
DC components	**−0.037107**				
No. Harmonics	**15**				
THD	**18.5624%**				
Grid Size	**512**				
Interpolation Degree	**1**				
Harmonics	**Frequency**	**Magnitude**	**Phase**	**Norm. Mag**	**Norm. Phase**
1	50	11.8044	−0.86678	1	0
2	100	0.00272927	−87.038	0.0002231207	−86.172
3	150	1.82486	−3.0824	0.154591	−2.2156
4	200	0.000617738	−38.435	0.000052331	−37.568
5	250	0.489755	174.772	0.0414891	175.638
6	300	0.00209954	69.2359	0.00017786	70.1027
7	350	0.930224	172.689	0.0788029	173.556
8	400	0.00315766	75.7679	0.000267498	76.6347
9	450	0.561122	170.638	0.0475349	171.505
10	500	0.00256501	79.3973	0.000217292	80.264
11	550	0.114071	168.906	0.00966337	169.773
12	600	0.000955366	95.2264	8.09328×10^{-05}	96.0932
13	650	0.00525038	−19.574	0.000444781	−18.707
14	700	0.000845858	−137.32	7.16559×10^{-05}	−136.45
15	750	0.195151	164.189	0.016532	165.055

Table 10 shows the analysis of THD. Here, only 3rd harmonic is predominating, and all others are much lower. Now if we change the width of gate pulses the THD can be further reduced. One thing to note is that in 3-level the THD was 28.88% while in the 5-level topology the THD is 18.56%. Hence by increasing the levels of the output, we can reduce the total harmonics distortion. Therefore, if the number of levels are increased, then THD is decreased.

5. Pulse width modulation (PWM) control techniques

Depending on the control strategy, the most important two types of the PWM modulation techniques are categorized as open and closed loop. SPMW, PWM space vector, sigma-delta modulation (SDM) are the part of open-loop PWM methods, and hysteresis, optimized current control; linear methods are identified by closed-loop current control methods.

5.1. Open-Loop PWM Control Techniques

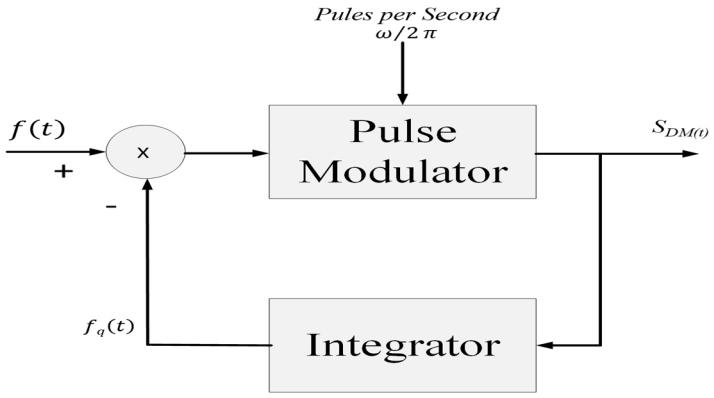
5.1.1. Sigma Delta PWM (SDM)

The SDM method was first classified by Jager in 1952 as a 1-bit PCM (pulse code modification) coding method. A 1-bit coding application is created utilizing the integrated feedback block on a pulse modulator, which is part of the encoding process, as shown in Figure 18a [83]. Sigma delta modulation originally suggested as a way to encode 1-bit audio and video signals in digital control and modulation problems. SDM has been classified to avoid a decrease in the power density of the altered signals with an increase in the sampling frequency. An SDM method was acquired by adding a test and restraint unit to the main SDM modulator, as shown in Figure 18b.

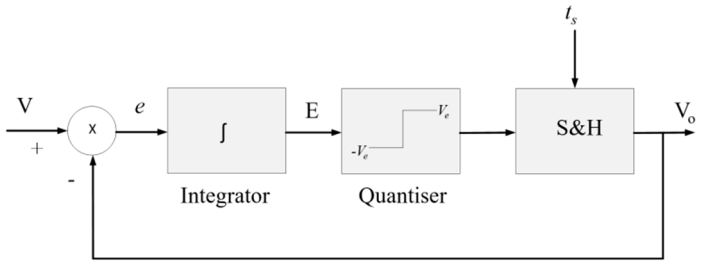
SDM modified the energy transformation operation utilizing analog to digital converters, which are widely used in some applications because of the expansion of semiconductor technologies. Using an inverter with resonant DC-link permits using soft switching applications rather than hard PWM switching. This type of inverter is mainly known as zero switching losses acquired through switching to the present time, and this technique can be adjusted according to the SDM. In Figure 18b, the modulator output signal varies between +Vo, 0 and Vo depending on the sampling period of fs, and the output

signal is compared to the amplitudes of input. The result of the comparison (e) is integrated (E) and the quantizer decide the output signal across from E. The multilevel SDM creates a multi-bit data stream and the output decode creates various output states that might be utilized to regulate the activate/deactivate states of multilevel inverter switches. Figure 19 shows a schematic diagram of a multilevel inverter regulated by SDM. The interaction between the SDM modulator and the inverter is controlled by a multilevel decoding logic block, which receives the SDM signals and decodes the inverter switching signals [84–86].

Studies show that it designed to regulate DC link inverter, SDM might be expanded to regulate multilevel inverters via logical interface. For SDM-regulated multilevel inverters, output faults, for instance, unequal voltage distribution and system imbalances, might be decreased to a high switching frequency up to 200 kHz.



(**a**)



(**b**)

Figure 18. Schematic diagram of delta modulation (**a**) simple delta modulator; diagram of delta modulation (**b**) sigma-delta modulation (SDM).

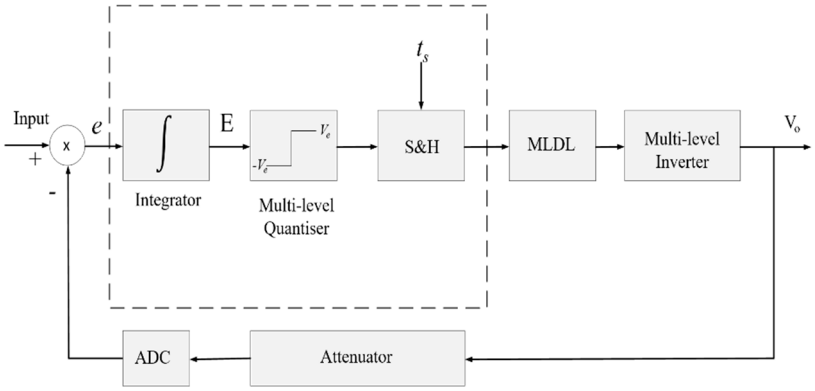


Figure 19. SDM control of a multilevel inverter.

5.1.2. Sinusoidal PWM (SPWM)

The most widely used method among many PWM techniques is the SPWM out of other power switching inverters. In the SPWM, the sine wave of the source voltage when compared to a carrier wave of triangular type to produce gate signals for the inverter switch. Energy debauchery can be considered a major problem for high-power applications. A basic SPWM frequency control method has been suggested to reduce the switching losses. SPWM multi-carrier regulate method has also been executed to enhance the performance of operated multilevel inverters and is categorized as per perpendicular or horizontal carrier signal adjustment. Perpendicular carrier distribution methods are called phase dissipation (PD), phase opposition (POD) and alternative phase dissipation (APOD); however, the horizontal arrangement is called the phase shift control method (PS). Even though PS-PWM is only useful for CHB-MLI and FC-MLI, PD-PWM is more useful for DC-MLI [87].

From the above discussion, multicarrier SPWM regulates methods is shown in Figure 20a PD, (b) POD, (c) APOD, (d) PS. SPWM is the mainly utilized PWM control technique because of its many advantages, such as the simple implementation of lower harmonic output signals per other methods and lower transmission dissipations. In the SPWM, a high-frequency triangular carrier signal is analyzed to a low-frequency sine wave signal in an analog or digital device. The frequency of the sine wave modulation signal determines the required frequency of the line voltage at the output of the inverter [88].

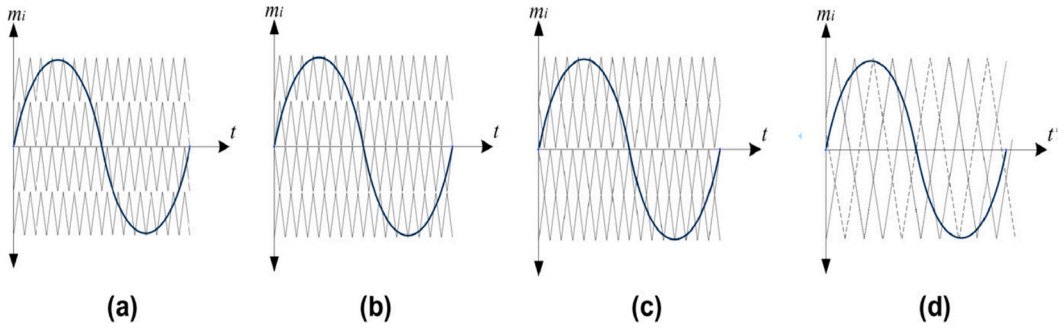


Figure 20. Multi-carrier sinusoidal PWM (SPWM) control methods: (**a**) PD, (**b**) POD, (**c**) APOD, (**d**) PS.

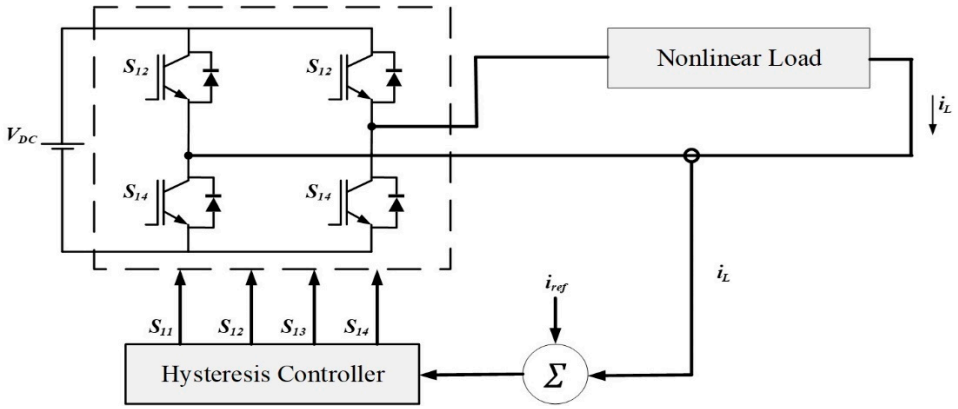
5.2. Closed-Loop PWM Control Techniques

Most widely used applications of PWM converters, like drives of a motor, active filters and many more, need a control form consisting of an inner current feedback loop. A multilevel inverter system uses photovoltaic (PV) or wind power sources to combine renewable power sources into the grid. Several methods have been conducted to reduce harmonics by utilizing current regulate for active power filter or by connecting a photoelectric and wind generator integrated to grid applications of a multilevel inverter. Current control methods are primarily discussed in terms of hysteresis current control and line current control [89–92].

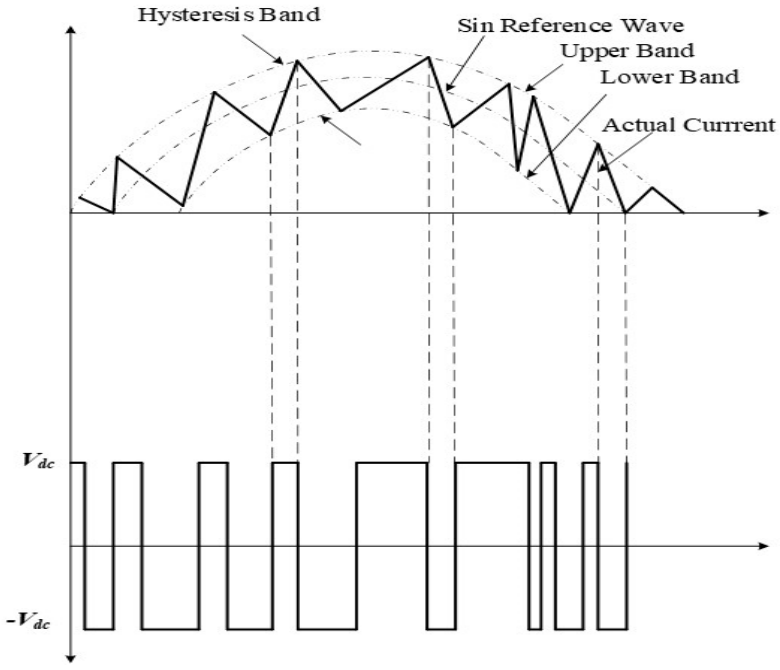
Hysteresis modulation is a current regulate technique in which the load current follows the reference current in the hysteresis band in non-linear load application of multilevel inverter. Figure 21a is a schematic layout of the hysteresis regulation of the H-bridge, and Figure 21b illustrates the fundamental law of the hysteresis modulation. The employed controller creates a sinusoidal source current that of desired magnitude and also frequency, which is analyzed according to the actual current. If the current surpasses the higher level of the hysteresis band, it must choose the next higher voltage level to try to force the current error to zero. However, the voltage level of the inverter might be not enough to reset the current error to zero, and the inverter must move to the further higher voltage level to obtain the correct voltage level. Consequently, the current returns to the hysteresis band and the current follow the reference current in the hysteresis band. The three hysteresis controllers correctly select the voltage level are explained as offset band three-level, double band three-level, and time-based three-level hysteresis controllers [86,91–94].

Considering this to be a different method of multilevel inverter usage, the grid connection to the inverter must need current regulating. Linear current regulators are categorized as ramp comparators, stationary vector, and synchronous vector regulator. The ramp regulator uses the output ripple and feedback to regulate the switching instantly. In a 3-phase isolated neutral load method, the 3-phase current must have a zero-sum. Thus, linear compensation and the required two reference voltages of a three-phase inverter can be determined by utilizing 2 to 3 phase AB/ABC conversion blocks as shown in Figure 22.

The main linear current regulator comprises a tracking controller with an equivalent integrator for photovoltaic converters. Numerous harmonic compensation strategies can be found in the following articles on re-control and a linear resonant harmonic compensator [86,95–97].



(**a**)



(**b**)

Figure 21. Hysteresis current control: (**a**) schematic diagram of a H-bridge cell with hysteresis regulator; hysteresis current control (**b**) hysteresis current band and voltage curves of load feedback.

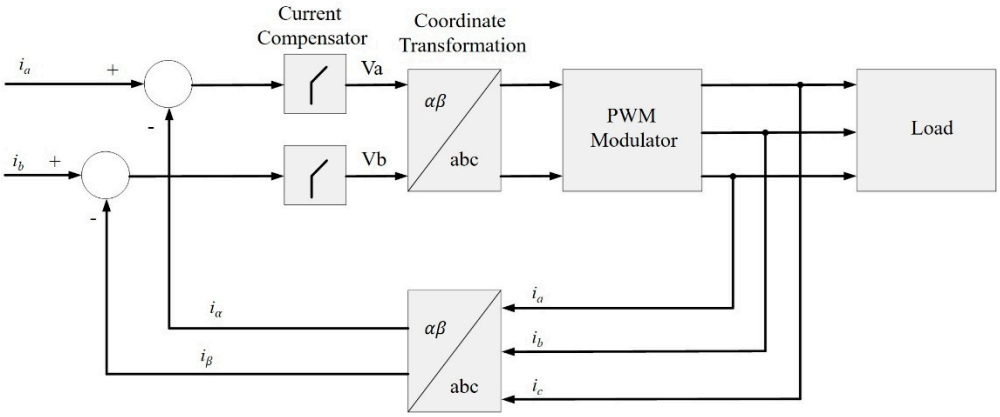


Figure 22. The schematic plot of stationary linear current regulator.

6. Conclusions

Many researchers and industries have acquired a multilevel inverter because of the capacities to regulate high- and medium-power applications. Also, the sustainable power source of DC needs to be changed over to AC. We demonstrate three different types of multilevel inverter, such as a cascade H multilevel inverter, a diode-clamp multilevel inverter, and a flying-capacitor multilevel inverter. Although all multilevel inverters are utilized to produce smoothing signals, the two types mentioned above have some drawbacks. For example, the individual DC sources are required for each inverter in CHB-MLI inverter and DC-MLI inverter switching losses are higher. These topologies are modeled in PSCADS SIMULINK. However, a flying-capacitor multilevel inverter has several features to regulate DC link capacitors compared to another multilevel topology using redundant switch configurations. From the MULTISIM simulation analysis and modeling of a flying-capacitor multilevel inverter in three levels, THD was 28.88% while in the five-level topology the THD was 18.56%. Therefore, we can decrease the total harmonic distortion adopting the higher-level topology.

Author Contributions: This paper was a collaboration effort among all authors. All authors conceived the methodology, conducted the experiment tests, and wrote the paper. R.A.R. and S.A.P. analyzed, designed and development of the experiment methodologies, A.M. and C.w.L. supported the work to perform in real time and, H.-J.K. verified the overall experiment.

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Conflicts of Interest: The authors declare no conflict of interest.

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