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Analysis of a DC Converter with Low Primary Current Loss and Balance Voltage and Current

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Abstract: A dc/dc pulse width modulation (PWM) circuit was investigated to realize the functions of reduced primary current loss and balanced voltage and current distribution. In the presented dc/dc converter, two full bridge pulse width modulation circuits were used with the series/parallel connection on the high-voltage/low-voltage side. The flying capacitor was adopted on the input side to achieve voltage balance on input split capacitors. The magnetic coupling element was employed to achieve current sharing between two parallel circuits. A capacitor-diode passive circuit was adopted to lessen the primary current at the commutated interval. The phase-shifted duty cycle control approach was employed to regulate load voltage and implement soft switching characteristics of power metal-oxide-semiconductor field-effect transistors (MOSFETs). Finally, the experimental results using a 1.68 kW prototype converter were obtained to confirm the performance and feasibility of the studied circuit topology.

Keywords: dc converter; full bridge converter; zero voltage operation

1. Introduction

High power density/efficiency dc/dc converters [1,2] have been proposed to reduce unnecessary power loss in order to reduce environmental pollution and met global energy demands. Clean and renewable energy sources meet these requirements to provide available ac or dc power to ac utilities, dc micro-grids, residential houses and commercial buildings by using power electronic based converters or inverters. High-voltage pulse width modulation (PWM) converters have been presented for industry power units [3,4], dc micro-grid systems [5–7] and dc traction or dc light rail transportation systems [8,9]. For these applications, the dc bus voltage is regulated between 750 V and 800 V. Full bridge circuits with a high switching frequency high-voltage rating SiC MOSFET or high-voltage rating insulated gate bipolar transistor (IGBT) devices can be adopted for high dc voltage applications. However, 1200 V SiC MOSFET devices are expensive and 1200 V IGBT devices have low switching frequency problems. Cost and performance are always the two main issues in the development of the available and high reliability power converters. Therefore, MOSFET power devices have been widely adopted in high efficiency power electronics. To improve the low-voltage drawback of MOSFETs in high-voltage applications, zero voltage switching, multi-level circuit topologies [10–14] have been developed and proposed to decrease conduction and switching losses. The phase shift pulse width modulation (PSPWM) and frequency modulation have normally been adopted to regulate duty cycle or switching frequency. However, the main disadvantage of conventional PSPWM is high circulating current losses at low effective duty cycle. In order to reduce circulating current, an active or passive snubber used on the low-voltage side has been proposed in [15–17]. A modular dc/dc converter [18] using low power rating modular circuits in series or parallel connection has been proposed to increase circuit efficiency and power rating. However, the current between each modular circuit may be unbalanced. To accomplish current balance issue, several current balancing approaches have been presented in [19,20].

A series/parallel-connected dc/dc converter is proposed to accomplish reduced primary circulating current, a soft switching operation, and balanced input voltages and output currents. Two full bridge circuits with series/parallel connection on input/output side are used in the studied circuit to achieve voltage and current sharing for the high voltage input and current output. Therefore, power devices on each full bridge circuit have $V_{\text{in}}/2$ voltage stress. To prevent input split voltages imbalance, a voltage balance capacitor was used on the input side to automatically achieve split voltages balance. Passive snubber circuits were employed on output side to create a positive voltage on the secondary rectified terminal under the commutated state so that the primary current at the commutated state can be reduced. To realize current sharing of two full bridge circuits, a current-balance magnetic component was adopted on the high-voltage side. If two currents are unbalanced, then one induced voltage of MC component is decreased to lessen the larger converter current. Therefore, two converter currents can be compensated automatically. PSPWM was adopted to control power devices and accomplish soft switching operation of active switches. The organization of this paper is as follows: The circuit structure and the principle of operation are discussed in Section 2. The steady state operation of the presented converter is shown in Section 3. Test results with a laboratory prototype are presented and investigated in Section 4. The conclusions of the studied converter are discussed in Section 5.

2. Circuit Structure and Principle of Operation

High-voltage converters were researched and presented for industry power supplies, dc traction vehicle and dc micro-grid systems. Ac/dc power converters with low harmonic currents, high power factor (PFC) and a stable dc voltage shown in Figure 1a are required for industry power converters. Normally, the dc voltage V_H is controlled at 760 V. Then, a high-frequency link converter is adopted to provide low-voltage output. Figure 1b illustrates the basic power distributed diagrams on dc light rail vehicle. A high-voltage dc converter can convert a 760 V input to supply a low-voltage output for battery charger, control, and communication demands. Figure 1c demonstrates the blocks of a bipolar dc micro-grid system to integrate ac utility system, clean energy generators and industry load and residential load into a common dc bus voltage.

Figure 2 gives the converter configuration of the developed circuit with series/parallel connection of full bridge circuits to achieve low circulating current loss, soft switching for power MOSFETs, and balanced input split voltages and output current sharing. The first full bridge circuit has power MOSFETs S_1-S_4 with the output capacitors C_1-C_4, leakage or external inductor L_{r1}, transformer T_1, magnetic core MC, filter inductor L_{o1}, secondary-side rectifier diodes D_1 and D_2, and passive circuit including C_{a1}, D_{a1} and D_{b1}. Likewise, the second full bridge circuit includes the components S_5-S_8, C_5-C_8, L_{r2}, T_2, MC, L_{o2}, D_3, D_4, C_{a2}, D_{a2} and D_{b2}. $C_{in,1}$ and $C_{in,2}$ are input split capacitors and C_b is the balance capacitor. Each circuit can transfer one-half rated power to the secondary side. The magnetic core [20] is used to balance i_{Lr1} and i_{Lr2}. Under the balanced primary currents ($|i_{Lr1}| = |i_{Lr2}|$), the induced voltages V_{L1} and V_{L2} are zero. If i_{Lr1} and i_{Lr2} are unbalanced (such as $|i_{Lr1}| > |i_{Lr2}|$), the induced voltage V_{L1} of MC cell is decreased in order to decrease i_{Lr1} and V_{L2} is increased to increase i_{Lr2}. Thus, i_{Lr1} will equal i_{Lr2} and $V_{L1} = V_{L2} = 0$. PSPWM is used to control S_1~S_8 and have zero voltage switching on the MOSFETs. Power switches S_1~S_4 and S_5~S_8 have identical PWM waveforms. The balance capacitor C_b is linked between points a and c. If S_1 and S_5 are on and S_2 and S_6 are off, then $V_{Cb} = V_{Cin,1}$. Likewise, $V_{Cb} = V_{Cin,2}$ if S_2 and S_6 are on and S_1 and S_5 are in the off. Since the duty cycle $d_{S1} = d_{S2} = 0.5$, it is obvious that $V_{Cb} = V_{Cin,1} = V_{Cin,2} = V_{\text{in}}/2$. Thus, the drain voltages of S_1~S_8 are $V_{in}/2$. To decrease the primary-side circulating currents, passive snubbers, C_{a1}, D_{a1}, D_{b1}, C_{a2}, D_{a2}, D_{b2}, are used on the presented circuit. At the same time, the filter inductor voltages $v_{Lo1} = v_{Ca1} - V_o$ and $v_{Lo2} = v_{Ca2} - V_o$ rather than $-V_o$ in the traditional full bridge duty cycle converters.

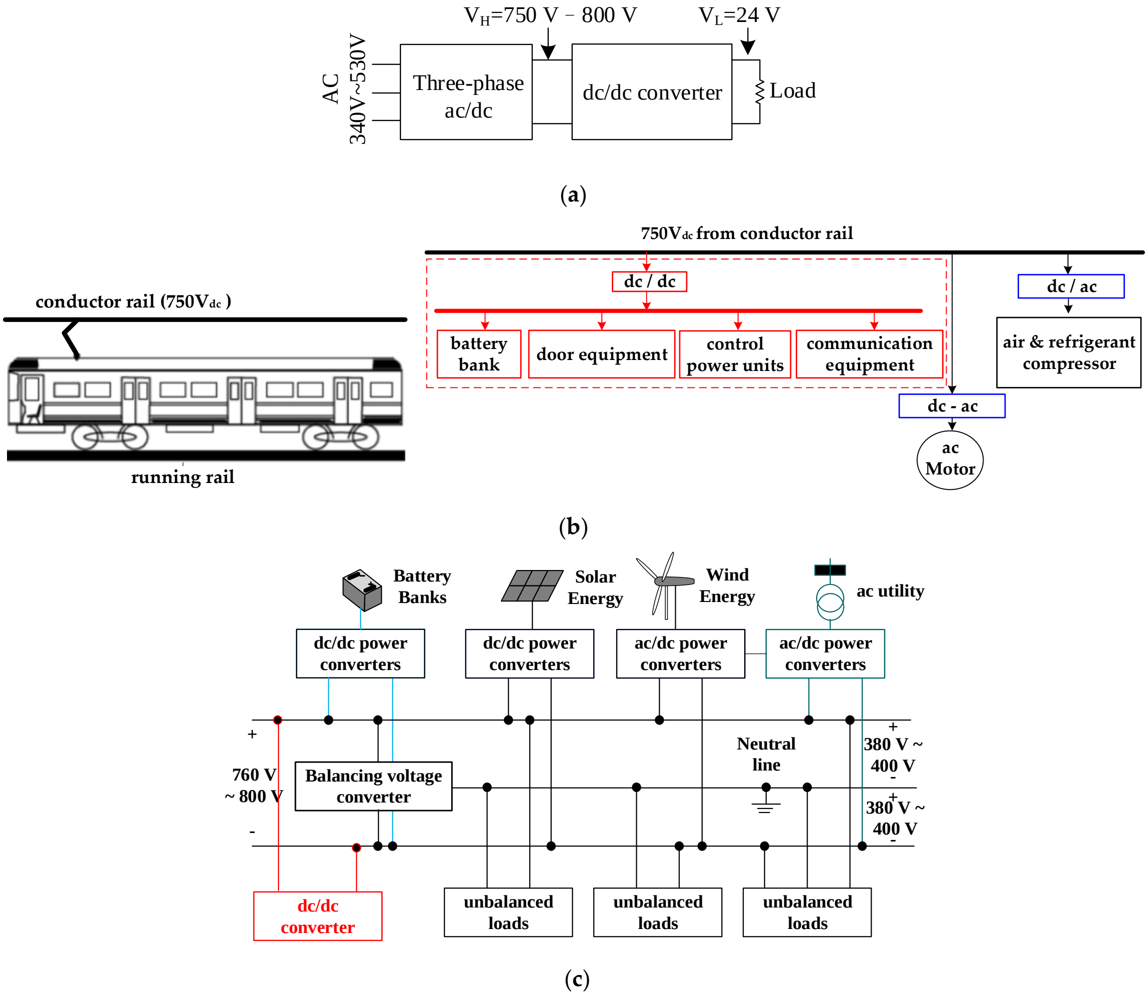


Figure 1. High-voltage dc/dc converters in (**a**) ac/dc converters, (**b**) dc light rail transportation vehicle, (**c**) dc micro-grid system with bipolar voltages.

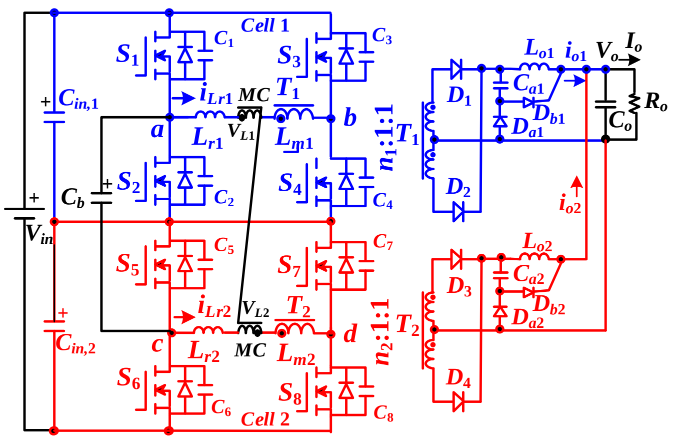


Figure 2. Circuit configuration of the studied converter.

The operation principle of the presented circuit is discussed with the assumptions: (1) $C_{in,1}$ = $C_{in,2}$; (2) $C_1 = \ldots .= C_8 = C_{oss}$; (3) $C_{a1} = C_{a2} = C_a$; (4) $L_{m1} = L_{m2} = L_m$; (5) $L_{o1} = L_{o2} = L_o$; (6) $L_{r1} = L_{r2} = L_r$; (7) $V_{Cb} = V_{Cin,1} = V_{Cin,2} = V_{\mathrm{in}}/2$; and (8) $n_1 = n_2 = n$. Figure 3 shows the PWM waveforms of the studied converter. The duty cycle of S_1~S_8 is 0.5. The gating signals of S_4 (S_3) is shifted to S_1 (S_2), respectively. Due to the switching states of power devices, the converter has fourteen steps in a switching period. The PWM waveforms are symmetrical for every half cycle. Therefore, only the first seven steps are discussed and the circuits of first seven operating steps are illustrated in Figure 4.

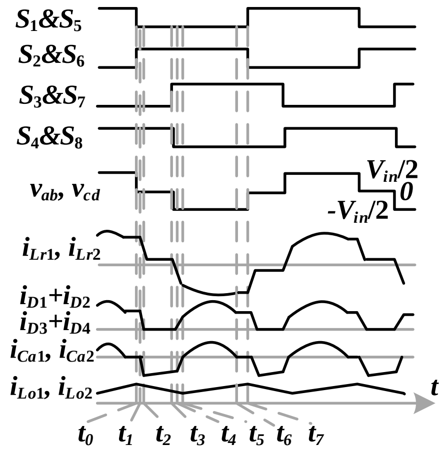


Figure 3. Pulse width modulation (PWM) waveforms of the presented converter.

Step 1 [t_0, t_1]: Before t_0, S_1, S_4, S_5, S_8, D_1 and D_3 conduct, $i_{Lr1} > 0$ and $i_{Lr2} > 0$. After t_0, power MOSFETs S_1 and S_5 turn off. C_1 and C_5 are charged and C_2 and C_6 are discharged. The energy on L_{r1}, L_{r2}, L_{o1} and L_{o2} can discharge C_2 and C_6. Equations (1) and (2) give the soft switching conditions of S_2 and S_6.

$$(L_{r1} + n_1^2 L_{o1}) i_{Lr1}^2(t_0) \geq C_{oss} V_{in}^2/2 \tag{1}$$

$$(L_{r2} + n_2^2 L_{o2}) i_{Lr2}^2(t_0) \geq C_{oss} V_{in}^2/2 \tag{2}$$

If these conditions are satisfied, then $v_{C1} = v_{C5} = V_{in}/2$ and $v_{C2} = v_{C6} = 0$ at t_1. The time duration in step 1 is obtained in Equation (3).

$$\Delta t_{01} = t_1 - t_0 = \frac{C_{oss} V_{in}}{i_{Lr1}(t_0)} \approx \frac{n_1 C_{oss} V_{in}}{i_{Lo,peak}} \approx \frac{2 n_1 C_{oss} V_{in}}{I_o} \tag{3}$$

The time duration Δt_{01} is related to the load current and input voltage.

Step 2 [t_1, t_2]: At t_1, $v_{C2} = v_{C6} = 0$. The positive primary currents i_{Lr1} and i_{Lr2} will flow through the body diode of S_2 and S_6. Thus, power MOSFETs S_2 and S_6 can achieve zero-voltage switching after t_1. The ac side voltages $v_{ab} = v_{cd} = 0$ and i_{Lr1} and i_{Lr2} decrease. Therefore, D_{a1} and D_{a2} conduct at this freewheeling state. The magnetizing voltages v_{Lm1} and v_{Lm2} are clamped at v_{Ca1} and v_{Ca2}, respectively. The primary inductor voltages $v_{Lr1} = -n_1 v_{Ca1}$ and $v_{Lr2} = -n_2 v_{Ca2}$ and the filter inductor voltages $v_{Lo1} = v_{Ca1} - V_o < 0$ and $v_{Lo2} = v_{Ca2} - V_o < 0$. Therefore, i_{Lr1}, i_{Lr2}, i_{Lo1} and i_{Lo2} are all decreased in this step.

$$i_{Lr1}(t) \approx i_{Lr1}(t_1) - \frac{n_1 v_{Ca1}}{L_{r1}}(t - t_1) \tag{4}$$

$$i_{Lr2}(t) \approx i_{Lr2}(t_1) - \frac{n_2 v_{Ca2}}{L_{r2}}(t - t_1) \tag{5}$$

$$i_{Lo1}(t) \approx i_{Lo1}(t_1) + \frac{v_{Ca1} - V_o}{L_{o1}}(t - t_1) \tag{6}$$

$$i_{Lo2}(t) \approx i_{Lo2}(t_1) + \frac{v_{Ca2} - V_o}{L_{o2}}(t - t_1) \tag{7}$$

Thus, the circulating current is decreased under the commutated state. In this step, the balance capacitor voltage $V_{Cb} = V_{Cin,2}$.

Step 3 [t_2, t_3]: At time t_2, $i_{D1} = i_{D3} = 0$ and D_1 and D_3 are off. Then, $i_{Ca1} = -i_{Lo1}$, $i_{Ca2} = -i_{Lo2}$, $i_{Lr1} = i_{Lm1}(t_2)$ and $i_{Lr2} = i_{Lm2}(t_2)$. Since $i_{Lm1}(t_2)$ and $i_{Lm2}(t_2)$ are close to zero, the circulating current is removed. The filter inductor voltages $v_{Lo1} = v_{Ca1} - V_o < 0$ and $v_{Lo2} = v_{Ca2} - V_o < 0$. The secondary-side currents i_{Lo1} and i_{Lo2} are lessened.

Step 4 [t_3, t_4]: At t_3, power MOSFETs S_4 and S_8 turn off. C_3 and C_7 are discharged and C_4 and C_8 are charged. The energy on L_{r1} and L_{r2} can discharge C_3 and C_7 and the soft switching conditions of S_3 and S_7 are expressed in Equations (8) and (9).

$$L_{r1} i_{Lr1}^2(t_3) \geq C_{oss} V_{in}^2/2 \tag{8}$$

$$L_{r2} i_{Lr2}^2(t_3) \geq C_{oss} V_{in}^2/2 \tag{9}$$

Step 5 [t_4, t_5]: This step starts at t_4 when $v_{C3} = v_{C7} = 0$. Due to $i_{Lr1}(t_4) > 0$ and $i_{Lr2}(t_4) > 0$, the body diodes of S_3 and S_7 conduct. Then, S_3 and S_7 naturally conduct at zero-voltage switching after t_4. In this step, $v_{ab} = -V_{Cin,1}$, $v_{cd} = -V_{Cin,2}$, $V_{Cb} = V_{Cin,2}$, $v_{Lm1} = -n_1 v_{Ca1}$, $v_{Lm2} = -n_2 v_{Ca2}$, $v_{Lo1} = v_{Ca1} - V_o$ and $v_{Lo2} = v_{Ca2} - V_o$. In order to balance i_{Lr1} and i_{Lr2}, the magnetic core MC is employed on the high-voltage side. Under current balance condition, $V_{L1} = V_{L2} = 0$. Therefore, $v_{Lr1} \approx n_1 v_{Ca1} - V_{\text{in}}/2$ and $v_{Lr2} \approx n_2 v_{Ca2} - V_{\text{in}}/2$. It can be observed that i_{Lr1}, i_{Lr1}, i_{Lo1} and i_{Lo2} all decrease in this step. When the secondary-side diode currents $i_{D2} = i_{Lo1}$ and $i_{D4} = i_{Lo2}$ at time t_5, diodes D_{a1} and D_{a2} are reverse biased. In this step, i_{D2} and i_{D4} increase from zero to i_{Lo1} and i_{Lo2}, respectively and the time duration in step 5 can be obtained as:

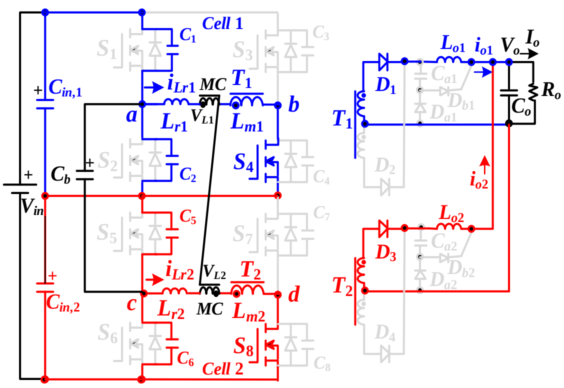
$$\Delta t_{45} = \frac{L_{r1} I_{Lo1,\min}}{n_1 V_{in}/2 - n_1^2 v_{Ca1}} \approx \frac{L_{r1} I_o}{n_1 V_{in} - 2n_1^2 v_{Ca1}} \tag{10}$$

Since D_{a1} and D_{a2} are still conducting in this step, the duty loss is calculated in Equation (11).

$$d_{5,loss} \approx \frac{L_{r1} I_o f_{sw}}{n_1 V_{in} - 2n_1^2 v_{Ca1}} \tag{11}$$

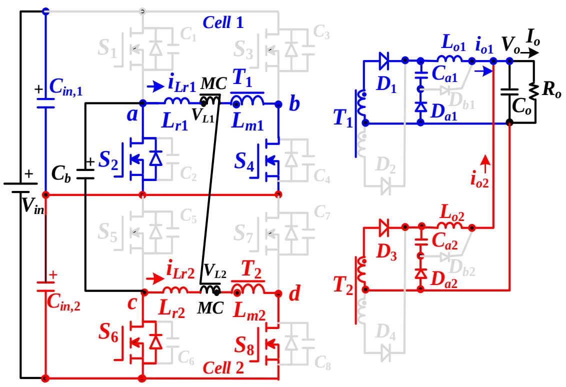
Step 6 [t_5, t_6]: At time t_5, $i_{D2} = i_{Lo1}$ and $i_{D4} = i_{Lo2}$. Then, the secondary-side diodes D_{a1} and D_{a2} are off and D_{b1} and D_{b2} are on in this step. The inductances $L_{r1}/(n_1)^2$ ($L_{r2}/(n_2)^2$) and C_{a1} (C_{a2}) are resonant with frequency $f_R = n_1/(2\pi\sqrt{L_{r1}C_{ca1}})$. Since $v_{Lo1} = v_{Ca1}$ and $v_{Lo2} = v_{Ca2}$, i_{Lo1} and i_{Lo2} both increase in this step. In order to force $i_{Db1} = i_{Db2} = 0$ at t_6, the half resonant cycle $1/(2f_R)$ must be less than $d_{eff,min} T_{sw}/2$. The primary magnetizing voltages $v_{Lm1} = n_1(v_{Ca1} + V_o)$ and $v_{Lm2} = n_2(v_{Ca2} + V_o)$ and the primary inductor current $i_{Lr1} \approx -(i_{Lo1} + i_{Ca1})/n_1$ and $i_{Lr2} \approx -(i_{Lo2} + i_{Ca2})/n_2$.

Step 7 [t_6, t_7]: At time t_6, $i_{D2} = i_{Lo1}$ and $i_{D4} = i_{Lo2}$. Then diodes D_{b1} and D_{b2} are off. The filter inductor voltages $v_{Lo1} \approx V_{\text{in}}/(2n_1) - V_o$ and $v_{Lo2} \approx V_{\text{in}}/(2n_2) - V_o$ so that i_{Lo1} and i_{Lo2} increase. At t_7, S_2 and S_6 turn off.

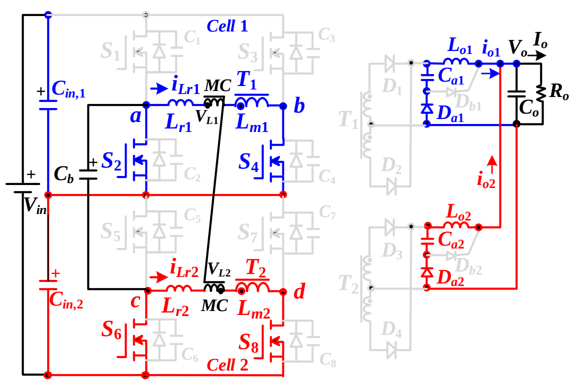


(a)

Figure 4. *Cont.*



(**b**)



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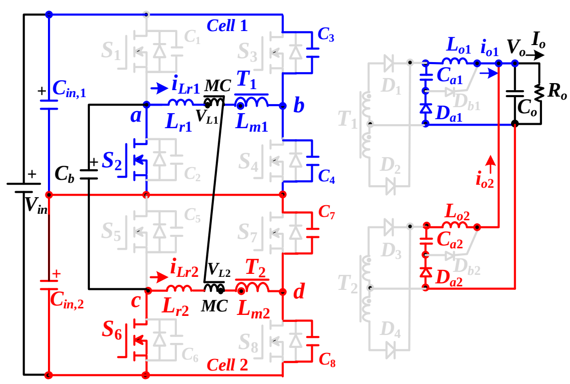

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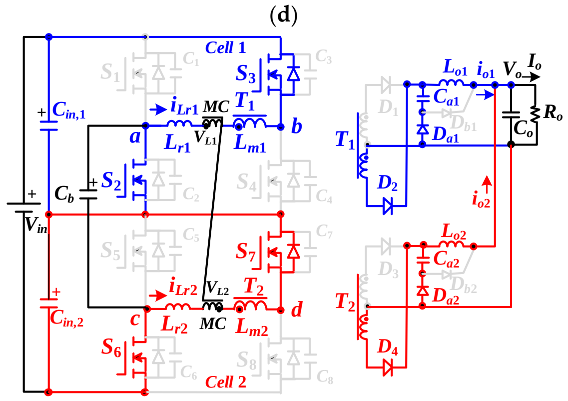
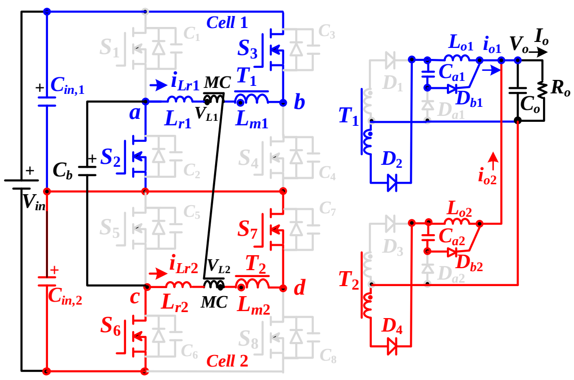


(**e**)

Figure 4. *Cont.*



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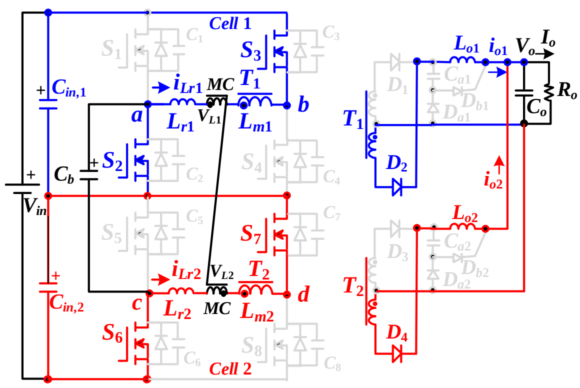


(**g**)

Figure 4. Equivalent circuits in first seven steps (**a**) step 1, (**b**) step 2, (**c**) step 3, (**d**) step 4, (**e**) step 5, (**f**) step 6, (**g**) step 7.

3. Steady State Analysis

Each full bridge converter in the presented converter supplies one-half of load power to low-voltage side. To balance i_{Lr1} and i_{Lr2}, the magnetic component MC is employed in the studied converter. Under current balance condition, $V_{L1} = V_{L2} = 0$. It can be observed that the average voltages $V_{Ca1} = V_{Ca2} = V_{\text{in}}/(2n_1) - V_o$ in step 6. Under steady state operation, i_{Lo1} and i_{Lo2} at t_0 and $t_0 + T_{sw}$ in every switching period are identical, $i_{Lo1}(t_0) = i_{Lo1}(t_0 + T_{sw})$ and $i_{Lo2}(t_0) = i_{Lo2}(t_0 + T_{sw})$. Thus, Equation (12) is derived according to voltage-second balance condition.

$$(d - d_5 - d_6)\left(\frac{V_{in}}{2n_1} - V_o\right) + d_6 V_{Ca1} = \left(\frac{1}{2} - d + d_5\right)(V_o - V_{Ca1}) \tag{12}$$

where d_5 and d_6 are duty cycles in steps 5 and 6, respectively. Based on $V_{Ca1} = V_{\text{in}}/(2n_1) - V_o$, V_o can be derived in Equation (13) under steady state.

$$V_o = \frac{V_{in}}{4n_1(1 - d + d_5)} = \frac{V_{in}}{4n_1(1 - d_{eff})} \tag{13}$$

where $d_{eff} = d - d_5$ is an effective duty ratio and δ is duty ratio when S_1 (S_2) and S_4 (S_3) are conducting. From Equation (13), the voltage gain is expressed in Equation (14).

$$G_{dc} = V_o/V_{in} = \frac{1}{4n_1(1 - d_{eff})} \tag{14}$$

From the given input and output voltages, the turns ratio n is derived as:

$$n = n_1 = n_2 = \frac{V_{in}}{4V_o(1-d_{eff})} \tag{15}$$

Therefore, the minimum primary turns n_p and secondary turns n_s are derived in Equation (16).

$$n_p \geq \frac{V_{Lm} d T_{sw}}{\Delta B_{\max} A_e},\ n_s = \frac{n_p}{n} \tag{16}$$

where ΔB_{max}: maximum flux density range, A_e: effective cross area, and V_{Lm}: primary voltage. In steady state, $I_{Lo1} = I_{Lo2} = I_o/2$, $V_{Cin,1} = V_{Cin,2} = V_{Cb} = V_{\text{in}}/2$ and $v_{S1,ds} = \ldots = v_{S8,ds} = V_{\text{in}}/2$. If the effective duty cycle is defined, then the ripple currents ΔL_{o1} and ΔL_{o2} can be obtained in Equation (17).

$$\Delta i_{Lo1} = \Delta i_{Lo2} = (V_o - V_{Ca1})(0.5 - d_{eff})T_{sw}/L_o \approx (2V_o - \frac{V_{in}}{2n_1})(0.5 - d_{eff})T_{sw}/L_o \tag{17}$$

If the ripple currents $\Delta i_{Lo1} = \Delta i_{Lo2} = \Delta i_{Lo}$ are given or selected, then output inductances are achieved in Equation (18).

$$L_{o1} = L_{o2} = L_o \geq (2V_o - \frac{V_{in}}{2n_1})(0.5 - d_{eff})T_{sw}/\Delta i_{Lo} \tag{18}$$

The winding turns of filter inductors L_{o1} and L_{o6} are expressed as:

$$n_{Lo1} = n_{Lo2} \geq \frac{L_{o1} i_{Lo1,peak}}{B_{\max} A_e} \tag{19}$$

The voltage ratings and average currents on D_1~D_4 are expressed in Equations (20)–(23).

$$V_{D1,rating} = \ldots = V_{D4,rating} \approx V_{in}/n_1 \tag{20}$$

$$V_{Da1,\text{rating}} = V_{Da2,\text{rating}} = V_{Db1,\text{rating}} = V_{Db2,\text{rating}} \approx V_o \tag{21}$$

$$I_{D1,\text{av}} = I_{D2,\text{av}} = I_{D3,\text{av}} = I_{D4,\text{av}} \approx I_o/4 \tag{22}$$

$$I_{Da1,\text{av}} = I_{Da2,\text{av}} = I_{Db1,\text{av}} = I_{Db2,\text{av}} \approx dI_o/2 \tag{23}$$

Based on Equation (11), the necessary inductances L_{r1} and L_{r2} are obtained as:

$$L_{r1} = L_{r2} \approx \frac{d_{5,loss}(n_1 V_{in} - 2n_1^2 v_{Ca1})}{I_o f_{sw}} \tag{24}$$

4. Test Results

The studied circuit was verified through a prototype. In the prototype circuit, V_{in} was between 750 V and 800 V, V_o was 24 V, $I_{o,rated}$ was 70 A, f_{sw} is 60 kHz, the effective duty cycle d_{eff} was 0.35, and the duty loss in step 5 was 0.01. Therefore, the turn-ratio and the primary-side inductances were obtained as:

$$n = n_1 = n_2 = \frac{V_{in,\min}}{4V_o(1-d_{eff})} \approx 12 \tag{25}$$

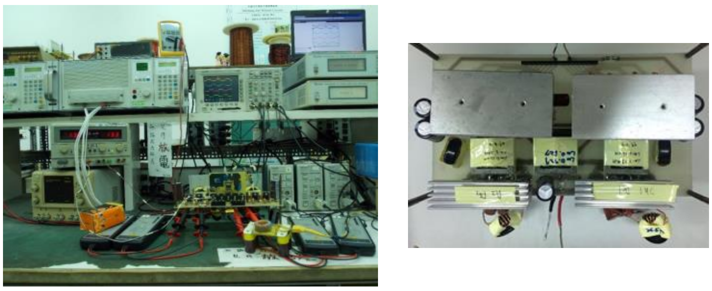
$$L_{r1} = L_{r2} \approx \frac{d_{5,loss}(n_1 V_{in\min} - 2n_1^2 v_{Ca1})}{I_o f_{sw}} \approx 16.5\ \mu\text{H} \tag{26}$$

In the prototype circuit, the actual magnetizing inductance, $L_{m1} = L_{m2} = 2$ mH, the primary turns $n_{1,p}$ and $n_{2,p}$ were 48 and the secondary turns $n_{1,s}$ and $n_{2,s}$ were 4 with TDK EER-42 magnetic core. The maximum ripple currents Δi_{Lo} was assumed as 4 A. The L_{o1} and L_{o2} can be obtained in Equation (27).

$$L_{o1} = L_{o2} = (2V_o - \frac{V_{in,\min}}{2n_1})(0.5 - d_{eff})T_{sw}/\Delta i_{Lo} \approx 10.5\ \mu\text{H} \quad (27)$$

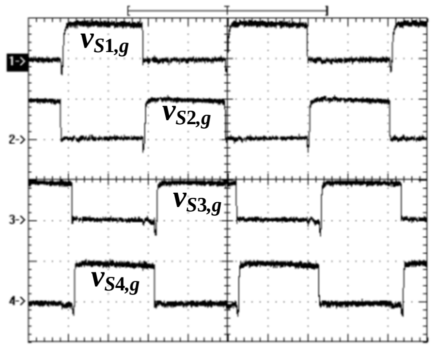
MOSFETs SiHG20N50C with 500 V/20 A ratings were selected for S_1~S_8. MBR40100PT with 100 V/40 A ratings were selected for D_1~D_4 and D_{a1}~D_{b2}. The magnetic coupling (MC) transformer n_p:n_s = 24 turns:24 turns. The adopted capacitors were $C_{in,1}$ = $C_{in,2}$ = 240 µF/450 V, C_b = 1 µF, C_{a1} = C_{a2} = 8.8 µF and C_o = 2200 µF/100 V. The PSPWM integrated circuit UCC3895 was selected as a controller to control S_1~S_8.

The experimental test bench is given in Figure 5. The dc power source was using a two Chroma 62016P-600-8 programmable dc power supply connected in series to supply 800 V at the input side of the proposed circuit. The dc electronic load was a Chroma 63112A programmable dc load. The digital oscilloscope Tektronix TDS3014B was adopted to measure the test waveforms. Figure 6 illustrates the test waveforms of the gate voltages of switches S_1~S_4 in first full bridge circuit at rated power. The phase-shift angle between S_1 and S_4 depended on the input voltage. The gating voltages of S_5~S_8 in second full bridge circuit were identical to S_1~S_4, respectively. The gating voltages $v_{S1,g}$ and $v_{S4,g}$ and ac voltages v_{ab} and v_{cd} at rated power are demonstrated in Figure 7. Three-level voltages were observed on v_{ab} and v_{cd}. Figure 8 illustrates the test waveforms v_{ab}, v_{cd}, i_{Lr1} and i_{Lr2} under 20% power and rated power. Two primary-side currents were well balanced with each other due to the current balance magnetic core is used to achieve current sharing. Figure 9 gives the test results of V_{Cin1}, V_{Cin2} and V_{Cb} at rated power. Split capacitor voltages were well balanced with V_{Cin1} = 401.6 V and V_{Cin2} = 398.4 V. Figure 10 gives the measured waveforms of output side currents. Figure 11 provides the test waveforms of i_{Lo1}, i_{Db1}, i_{o1} and i_{o2} under different load conditions. It is clear that i_{o1} and i_{o2} were balanced. Figure 12 provides the measured results of S_1 under 20% power and rated power. The soft switching of S_1 was succeeded from 20% power to rated power. The other switches such as S_2, S_5 and S_6 had the same characteristics as S_1. Therefore, S_2, S_5 and S_6 were also turned on with soft switching turn-on from 20% power. Figure 13 demonstrates the measured waveforms of S_4 under half and full loads. The soft switching of S_4 are realized from 50% load due to the energy on L_{m1} and L_{m2}. Likewise, S_3, S_7 and S_8 have same characteristics as S_4 and S_3, S_7 and S_8 with soft switching turn-on from 50% power. The test efficiencies of the presented circuit are 91.7% at 20% power, 93.5% at 50% power and 92.9% at 100% power and shown in Figure 14.



(**a**) (**b**)

Figure 5. Pictures of the presented circuit in the laboratory: (**a**) experimental setup and (**b**) prototype circuit.



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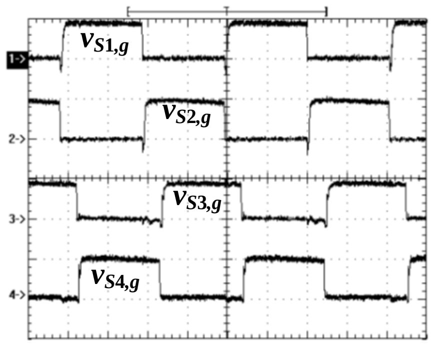
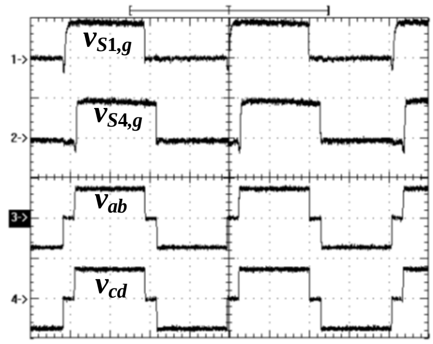


(**b**)

Figure 6. Measured gate voltages of S_1~S_4 in first full bridge circuit at full load and (**a**) V_{in} = 750 V and (**b**) V_{in} = 800 V ($v_{S1,g}$~$v_{S4,g}$: 10 V/div; time: 4 µs/div).



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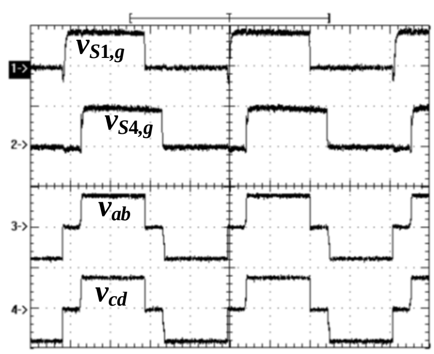
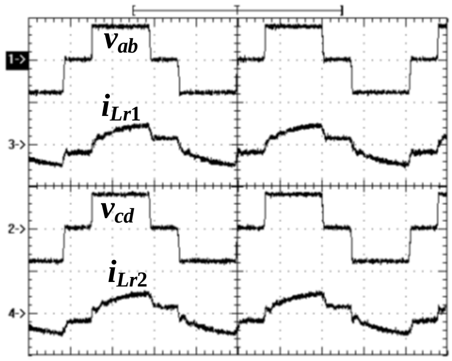


(**b**)

Figure 7. Experimental results of $v_{S1,g}$, $v_{S4,g}$, v_{ab} and v_{cd} at full load (**a**) V_{in} = 750 V and (**b**) V_{in} = 800 V ($v_{S1,g}$, $v_{S4,g}$: 10 V/div; v_{ab}, v_{cd}: 500 V/div; time: 4 µs/div).



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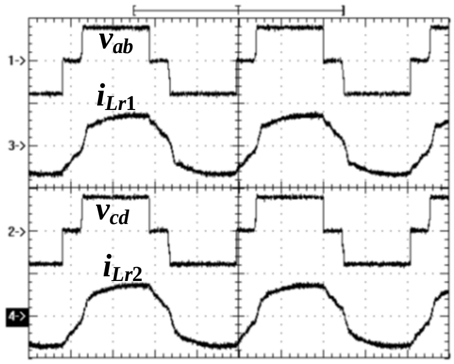


(**b**)

Figure 8. Measured waveforms of v_{ab}, v_{cd}, i_{Lr1} and i_{Lr2} at 800 V input (**a**) 20% load (v_{ab}, v_{cd}: 500 V/div; i_{Lr1}, i_{Lr2}: 2 A/div; time: 4 μs/div) and (**b**) full load (v_{ab}, v_{cd}: 500 V/div; i_{Lr1}, i_{Lr2}: 5 A/div; time: 4 μs/div).

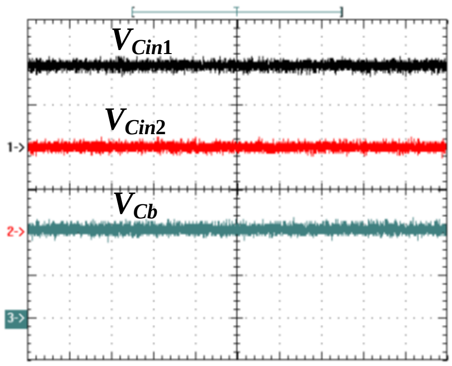
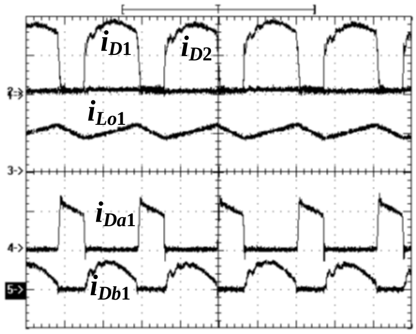


Figure 9. Measured waveforms of split voltages V_{Cin1} and V_{Cin2} and balance capacitor voltage V_{Cb} at 800 V input and full load (V_{Cin1}, V_{Cin2}, V_{Cb}: 200 V/div; time: 4 μs/div).



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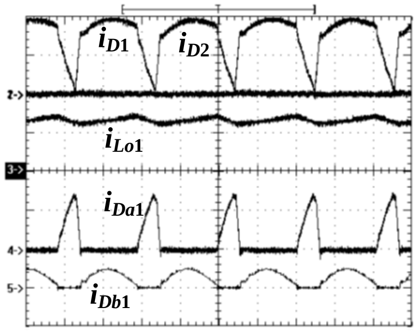
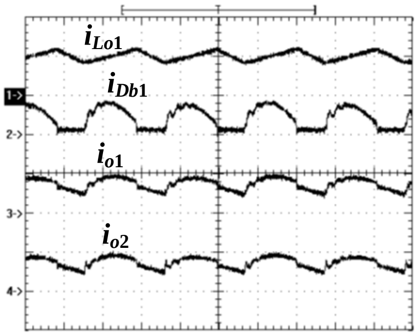


(**b**)

Figure 10. Measured waveforms of the secondary-side currents in first full bridge circuit (**a**) 20% load (i_{D1}, i_{D2}, i_{Lo1}, i_{Da1}, i_{Db1}: 5 A/div; time: 4 μs/div) and (**b**) full load (i_{D1}, i_{D2}, i_{Lo1}, i_{Da1}, i_{Db1}: 20 A/div; time: 4 μs/div).



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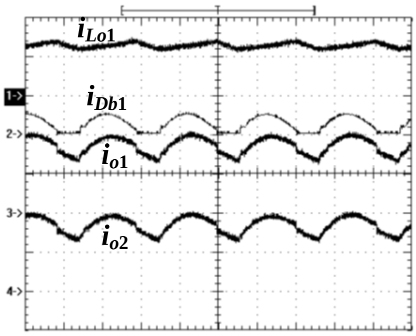
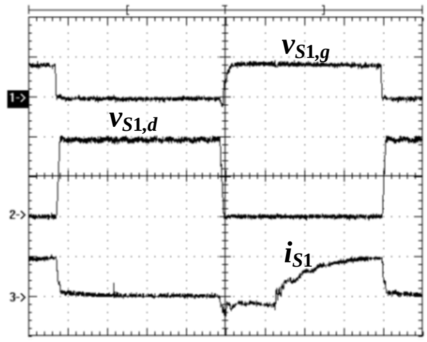


(**b**)

Figure 11. Measured waveforms of the secondary-side currents i_{Lo1}, i_{Db1}, i_{o1} and i_{o2} (**a**) 20% load (i_{Lo1}, i_{Db1}: 5 A/div; i_{o1}, i_{o2}: 10 A/div; time: 4 μs/div) and (**b**) full load (i_{Lo1}, i_{Db1}, i_{o1}, i_{o2}: 20 A/div; time: 4 μs/div).



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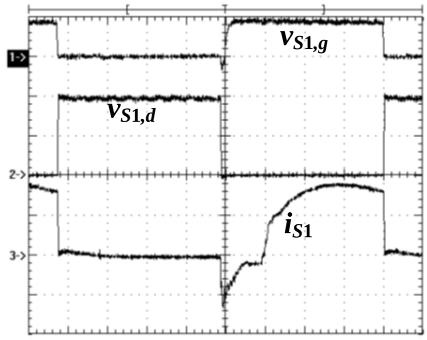
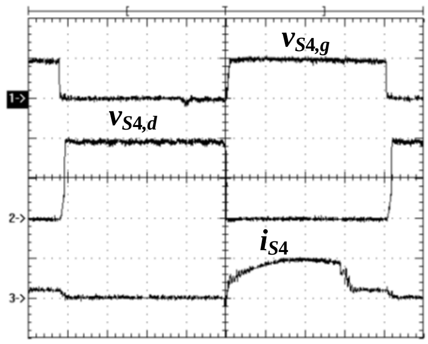


(**b**)

Figure 12. Measured waveforms of the leading-leg switch S_1 at 800 V input (**a**) 20% load ($v_{S1,g}$: 10 V/div; $v_{S1,d}$: 200 V/div; i_{S1}: 1 A/div; time: 2 μs/div) and (**b**) full load ($v_{S1,g}$: 10 V/div; $v_{S1,d}$: 200 V/div; i_{S1}: 2 A/div; time: 2 μs/div).



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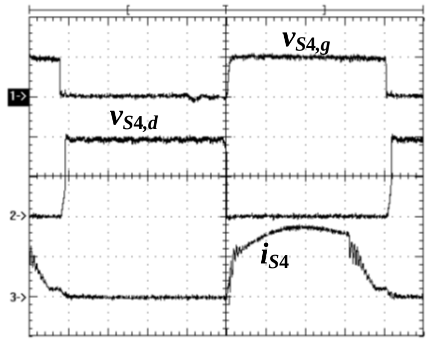

(**b**)

Figure 13. Measured waveforms of the lagging-leg switch S_4 at 800 V input (**a**) 50% load and (**b**) full load ($v_{S4,g}$: 10 V/div; $v_{S4,d}$: 200 V/div; i_{S4}: 2 A/div; time: 2 μs/div).

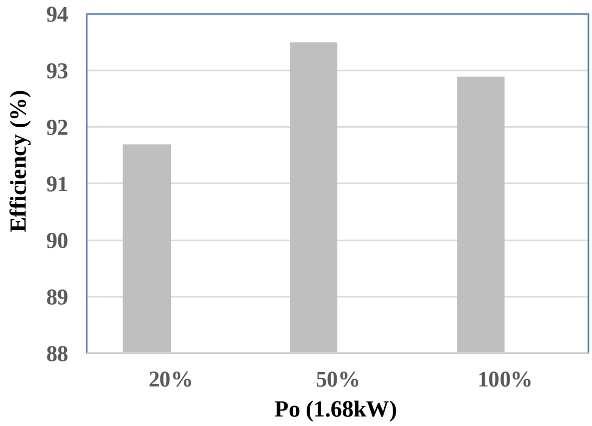

Figure 14. Measured circuit efficiencies of the proposed circuit.

5. Conclusions

A parallel dc/dc converter was proposed and investigated to achieve the main benefits of balanced input split voltages, load current sharing and reduced circulating current loss. Input split voltage balance was realized using a balance capacitor to automatically charge/discharge split capacitors in every switching cycle. The current sharing of two series full bridge circuits was achieved using a magnetic core. Passive circuits were employed on output side to decrease primary circulating current at commutated state. However, the proposed converter was out of work under power switch failure. Therefore, some bypass circuits may be added in the circuit to protect the converter from damage. This protection procedure is the next study case to further improve the circuit reliability. The theoretical analysis was well supported by the test waveforms of a prototype.

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References

1. Cho, I.-H.; Cho, K.-M.; Kim, J.-W.; Moon, G.-W. A New Phase-Shifted Full-Bridge Converter With Maximum Duty Operation for Server Power System. *IEEE Trans. Power Electron.* **2011**, *26*, 3491–3500. [CrossRef]
2. Sun, B.; Burgos, R.; Boroyevich, D. Ultralow Input–Output Capacitance PCB-Embedded Dual-Output Gate-Drive Power Supply for 650 V GaN-Based Half-Bridges. *IEEE Trans. Power Electron.* **2019**, *34*, 1382–1393. [CrossRef]
3. Fu, D.; Lee, F.C.; Qiu, Y.; Wang, F. A Novel High-Power-Density Three-Level LCC Resonant Converter with Constant-Power-Factor-Control for Charging Applications. *IEEE Trans. Power Electron.* **2008**, *23*, 2411–2420. [CrossRef]
4. Song, B.-M.; McDowell, R.; Bushnell, A.; Ennis, J. A Three-Level DC–DC Converter with Wide-Input Voltage Operations for Ship-Electric-Power-Distribution Systems. *IEEE Trans. Plasma Sci.* **2004**, *32*, 1856–1863. [CrossRef]
5. Nejabatkhah, F.; Li, Y.W. Overview of Power Management Strategies of Hybrid AC/DC Microgrid. *IEEE Trans. Power Electron.* **2015**, *30*, 7072–7089. [CrossRef]
6. Dragicevic, T.; Lu, X.; Vasquez, J.C.; Guerrero, J. DC Microgrids—Part I: A Review of Control Strategies and Stabilization Techniques. *IEEE Trans. Power Electron.* **2016**, *31*, 4876–4891. [CrossRef]
7. Dragicevic, T.; Lu, X.; Vasquez, J.C.; Guerrero, J. DC Microgrids—Part II: A Review of Power Architectures, Applications, and Standardization Issues. *IEEE Trans. Power Electron.* **2016**, *31*, 3528–3549. [CrossRef]

8. Chua, T.Z.Y.; Ong, Y.T.; Toh, C.L. Transformerless DC traction power conversion system design for light-rail-transit (LRT). In Proceedings of the IEEE Energy Conversion Conf. (CENCON), Kuala Lumpur, Malaysia, 30–31 November 2017; pp. 38–43.
9. Lin, B.-R. Investigation of a Resonant dc–dc Converter for Light Rail Transportation Applications. *Energies* **2018**, *11*, 1078. [CrossRef]
10. Lin, B.R. Hybrid dc/dc converter based on dual three-level circuit and full circuit. *IET Power Electron.* **2016**, *9*, 817–824. [CrossRef]
11. Lin, B.-R. Soft Switching DC Converter for Medium Voltage Applications. *Electronics* **2018**, *7*, 449. [CrossRef]
12. Ren, R.; Liu, B.; Jones, E.A.; Wang, F.F.; Zhang, Z.; Costinett, D. Capacitor-Clamped, Three-level GaN-Based DC–DC Converter with Dual Voltage Outputs for Battery Charger Applications. *IEEE J. Emerg. Sel. Top. Electron.* **2016**, *4*, 841–853. [CrossRef]
13. Haga, H.; Kurokawa, F. A novel modulation method of the full bridge three-level LLC resonant converter for battery charger of electrical vehicles. In Proceedings of the IEEE ECCE, Montreal, QC, Canada, 20–24 September 2015; pp. 5498–5504.
14. Dusmez, S.; Li, X.; Akin, B. A New Multi-Input Three-Level DC/DC Converter. *IEEE Trans. Power Electron.* **2016**, *31*, 1230–1240. [CrossRef]
15. Choi, H.-S.; Kim, J.-W.; Cho, B.H. Novel zero-voltage and zero-current-switching (ZVZCS) full-bridge PWM converter using coupled output inductor. *IEEE Trans. Power Electron.* **2002**, *17*, 641–648. [CrossRef]
16. Pahlevaninezhad, M.; Das, P.; Drobnik, J.; Jain, P.K.; Bakhshai, A. A Novel ZVZCS Full-Bridge DC/DC Converter Used for Electric Vehicles. *IEEE Trans. Power Electron.* **2012**, *27*, 2752–2769. [CrossRef]
17. Mishima, T.; Akamatsu, K.; Nakaoka, M. A high frequency-link secondary-side phase-shifted full-bridge soft-switching PWM DC-DC converter with ZCS active rectifier for EV battery charger. *IEEE Trans. Power Electron.* **2013**, *28*, 5758–5773. [CrossRef]
18. You, H.; Xu, C. A family of un-isolated modular dc/dc converters. In Proceedings of the IEEE IPEMC, Hefei, China, 22–26 May 2016; pp. 696–702.
19. Shi, J.J.; Liu, T.J.; Cheng, J.; He, X.N. Automatic current sharing of an input-parallel output-parallel (IPOP)-connected DC-DC converter system with chain-connected rectifiers. *IEEE Trans. Power Electron.* **2015**, *30*, 2997–3016. [CrossRef]
20. Liu, C.; Xu, X.; He, D.; Liu, H.; Tian, X.; Guo, Y.; Cai, G.; Ma, C.; Mu, G. Magnetic-coupling current-balancing cells based input-parallel output-parallel LLC resonant converter modules for high-frequency isolation of DC distribution systems. *IEEE Trans. Power Electron.* **2016**, *31*, 6968–6979. [CrossRef]