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Area-Efficient Embedded Resistor-Triggered SCR with High ESD Robustness

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Abstract: The trigger voltage of the direct-connected silicon-controlled rectifier (DCSCR) was effectively reduced for electrostatic discharge (ESD) protection. However, a deep NWELL (DNW) is required to isolate PWELL from P-type substrate (PSUB) in DCSCR, which wastes part of the layout area. An area-efficient embedded resistor-triggered silicon-controlled rectifier (ERTSCR) is proposed in this paper. As verified in a 0.3-μm CMOS process, the proposed ERTSCR exhibits lower triggering voltage due to series diode chains and embedded deep n-well resistor in the trigger path. Additionally, the proposed ERTSCR has a failure current of more than 5 A and a corresponding HBM ESD robustness of more than 8 KV. Furthermore, compared with the traditional DCSCR, to sustain the same ESD protection capability, the proposed ERTSCR will consume 10% less silicon area by fully utilizing the lateral dimension in the deep n-well extension region, while the proposed ERTSCR has a larger top metal width.

Keywords: electrostatic discharge (ESD); silicon-controlled rectifier (SCR); deep n-well resistor; trigger voltage

1. Introduction

The silicon-controlled rectifier (SCR) has been widely used in electrostatic discharge (ESD) protection for a long time due to its significantly high robustness and area efficiency [1]. However, the SCR device still has a higher trigger voltage, which is generally greater than the gate-oxide breakdown voltage of the protected device [2]. Thus, some modified SCR devices and trigger-assist SCR devices have been invented to reduce the trigger voltage of SCR, such as the modified lateral SCR (MLSCR) [3], the low-voltage triggering SCR (LVTSCR) [4,5], the GGNMOS-triggered SCR [6] and the diode chain triggering SCR (DTSCR) [7]. Furthermore, the direct-connected SCR (DCSCR) has been proposed to significantly reduce the trigger voltage to a level that is as low as twice of one diode's turn-on voltage [8–13].

The cross-sectional view and equivalent circuit diagram of the conventional DCSCR are shown in Figure 1a,b. As shown in Figure 1a, the main SCR conduction path of DCSCR (illustrated by a red arrow) is triggered by two direct-connected diodes D1 (P+/NWELL diode) and D2 (PWELL/N+ diode), which are located in the adjacent NWELL and PWELL, respectively (illustrated by a blue arrow named as diode chain path). These two diodes are connected by anode gate (N+ in NWELL) and cathode gate (P+ in PWELL), which are connected together by a metal connection. Unlike the PWELL grounded in the conventional lateral SCR structure, the PWELL in DCSCR is not grounded and thus, a deep NWELL (DNW) is required to isolate PWELL from the P-type substrate (PSUB) [9]. Generally, the minimum extension (L1) of a DNW region beyond a PWELL region is several micrometers according to the layout design rule, which will result in the DCSCR consuming more silicon area compared to the conventional

SCR. To optimize the layout area of DCSCR, an embedded resistor-triggered silicon-controlled rectifier (ERTSCR) is presented in this work. Compared to the conventional DCSCR with a figure of merit (FOM) of 3.30 mA/μm^2, the FOM of proposed ERTSCR is 3.66 mA/μm^2, which is higher by 10.9% compared to that of the conventional DCSCR. Additionally, the proposed ERTSCR has more robustness and a uniform metal connection against the huge ESD current.

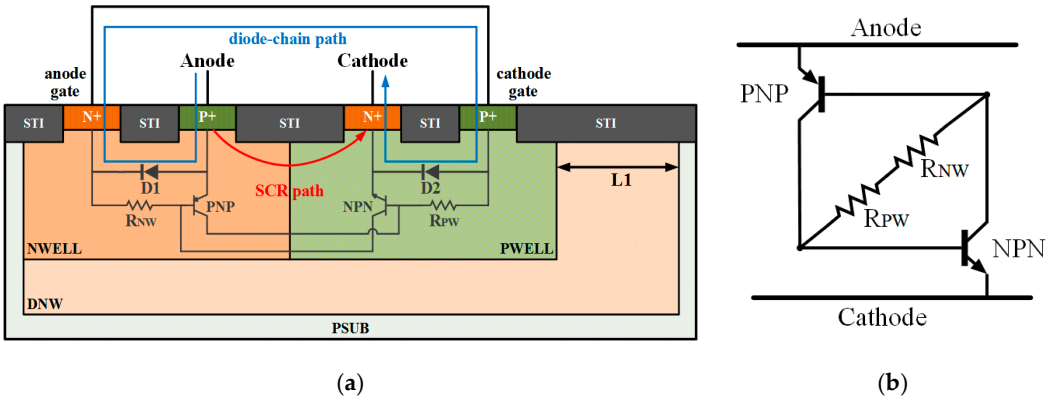


Figure 1. (**a**) Cross-sectional view of conventional DCSCR. The trigger path is illustrated by a blue arrow that is called the diode chain path; (**b**) Equivalent circuit diagram of conventional DCSCR.

2. Proposed ESD Device Structure and Simulation

In the conventional DCSCR, the DNW cannot be fully utilized although it has a sufficient width of L1. Actually, the DNW has the same doping type as NWELL and thus, it can be regarded as an embedded deep well resistor (R_{DNW}), which conduct the surface of DNW region and the NWELL region. Therefore, the N+ active region of the anode gate in the NWELL region can be moved to the surface of DNW region, which will not affect the turning on of D1 and D2. By making use of the conductive DNW, an area-efficient ERTSCR is proposed in this paper. The cross-sectional view and equivalent circuit diagram of proposed ERTSCR are shown in Figure 2a,b. It can be observed that the anode gate in ERTSCR is moved from NWELL to DNW and is connected to the cathode gate in adjacent PWELL by a metal connection. Compared with the DCSCR structure shown in Figure 1a, the lateral dimension of NWELL in ERTSCR will decrease due to the removal of anode gate, while the lateral dimension of DNW is unchanged. Correspondingly, the layout area of ERTSCR is smaller than that of DCSCR, which leads to a smaller layout area cost. From above, the use of R_{DNW} can reduce the device layout area. In the meantime, R_{DNW} plays an important role in the trigger path. Compared with DCSCR, the diode chain path in ERTSCR has one more R_{DNW} in series with D1 and D2. However, R_{DNW} is a conductor in trigger path and thus, the triggering of ERTSCR is still mainly determined by the turning on of two embedded diodes D1 and D2, which is similar to DCSCR.

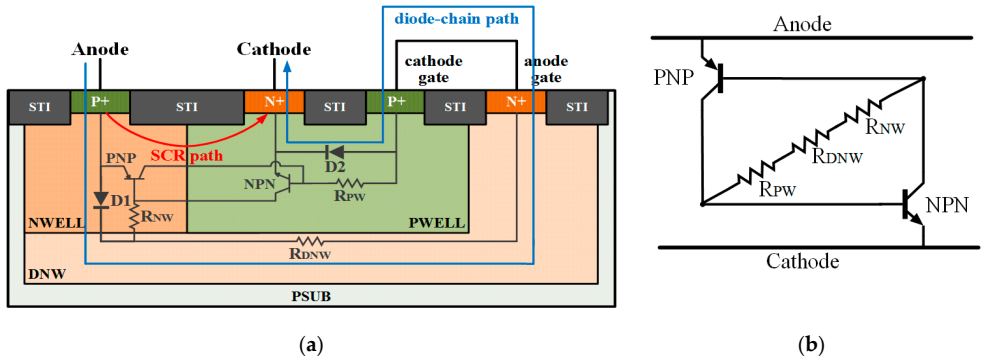


Figure 2. (**a**) Cross-sectional view of proposed ERTSCR. The DNW acts as an embedded well resistor R_{DNW} in the trigger path; (**b**) Equivalent circuit diagram of proposed ERTSCR.

In order to further explore the physics mechanisms of the DCSCR and proposed ERTSCR, a two dimension (2D) Technology Computer-Aided Design (TCAD) simulation was carried out using the Sentaurus tool, where the substrate of the device was regarded as the only heat sink and the ambient temperature was set at 300 K. The current density distributions in the triggering procedures of the DCSCR and proposed ERTSCR are shown in Figures 3 and 4. When the ESD pulse that is applied to the anode of both DCSCR and ERTSCR is more than two times one diode's turn-on voltage, D1 and D2 turn on and the trigger current flows through the diode chain path of each device (as shown in Figures 3a and 4a). As a result, the parasitic lateral NPN transistor and PNP transistor turn on (as shown in Figures 3b and 4b). As the current continues to increase, the current gain of the parasitic NPN transistor (β_{NPN}) and the current gain of the PNP transistor (β_{PNP}) will increase. Consequently, this gives rise to the regeneration between the two parasitic NPN and PNP transistors and thus, SCR paths are triggered (as shown in Figures 3c and 4c). Finally, the SCR paths of both DCSCR and ERTSCR discharge more current than the parallel diode chain paths due to the smaller turn-on resistance (as shown in Figures 3d and 4d). Compared to the current density distributions in DCSCR, the current density distributions in ERTSCR indicate that the DNW acts as an electrical connection between D1 and D2 to conduct the trigger current.

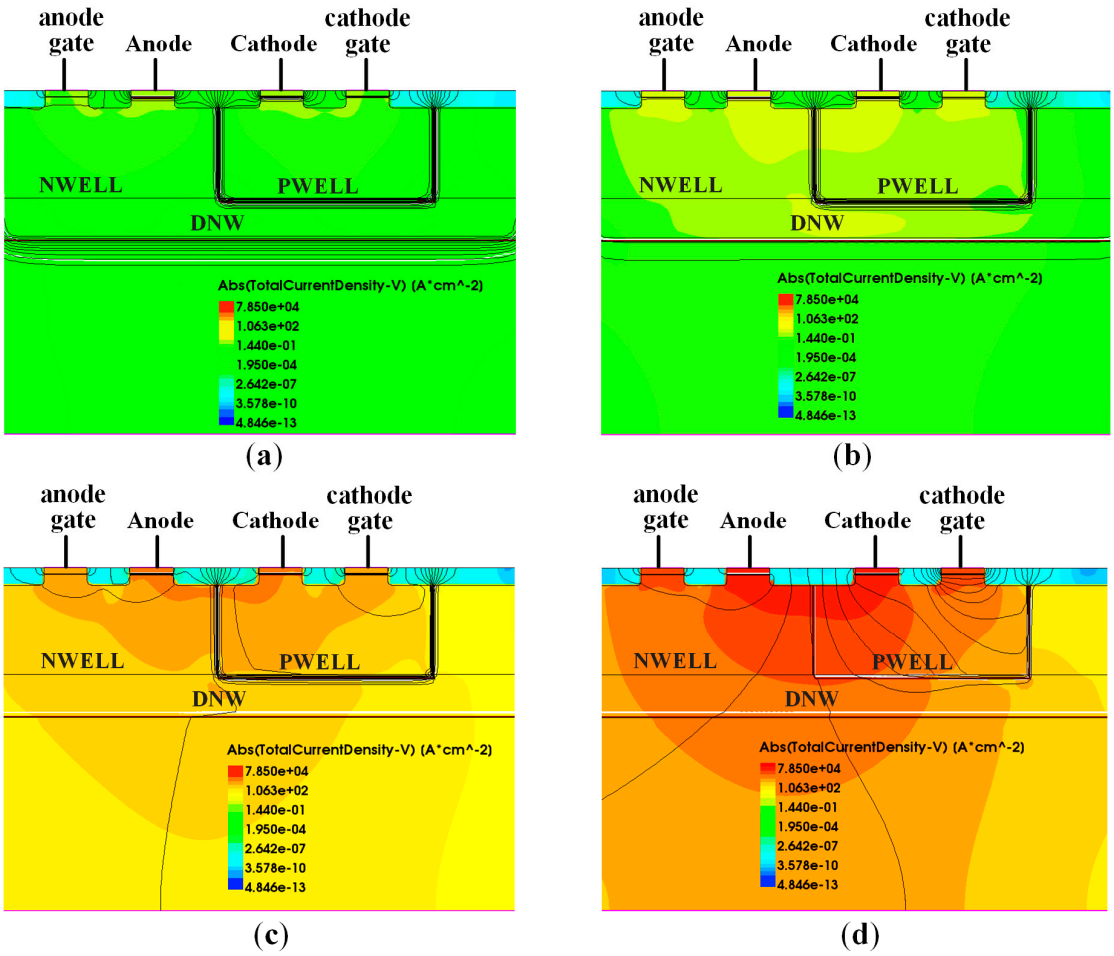


Figure 3. Total current density distributions at different current levels in DCSCR. (**a**) The trigger current flows along diode chain path; (**b**) the parasitic NPN and PNP transistors turn on; (**c**) the SCR path is triggered; and (**d**) the ESD current distribution after holding point.

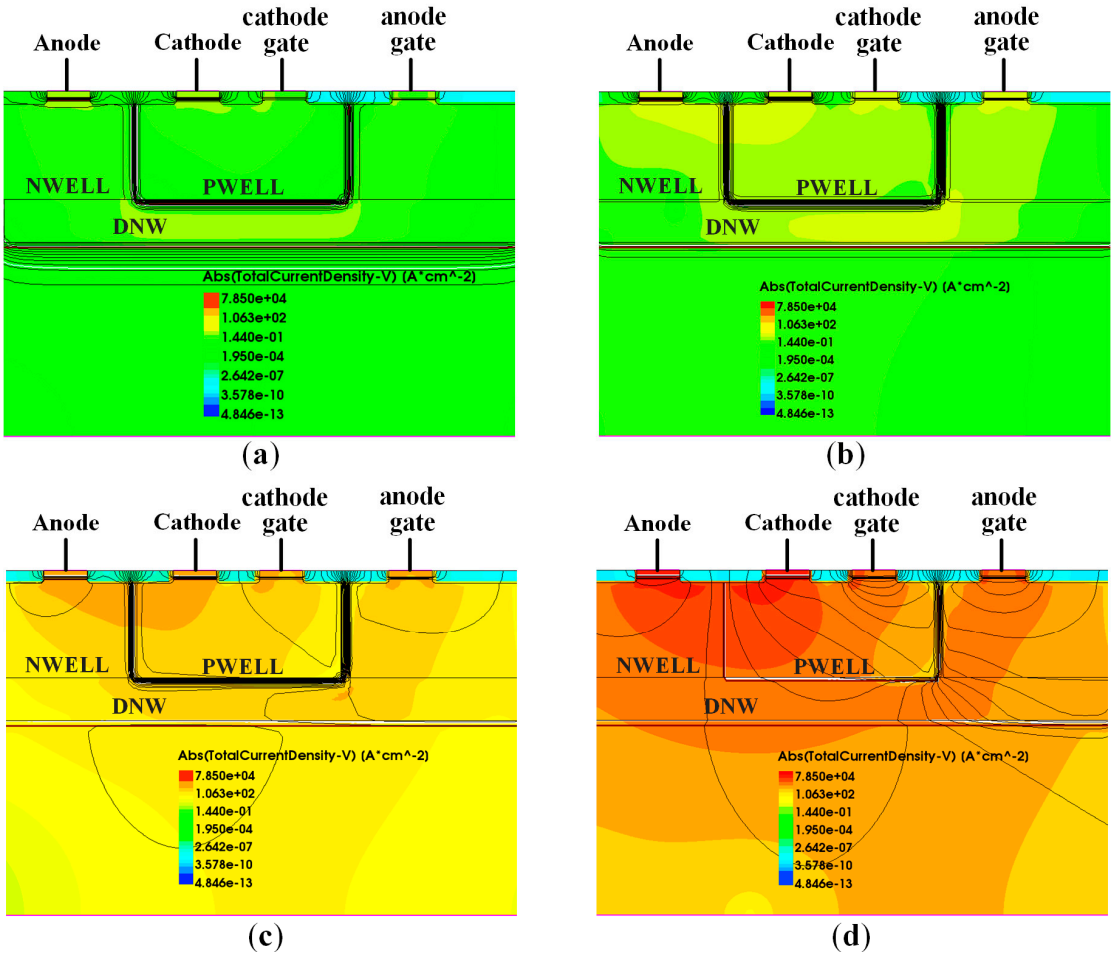


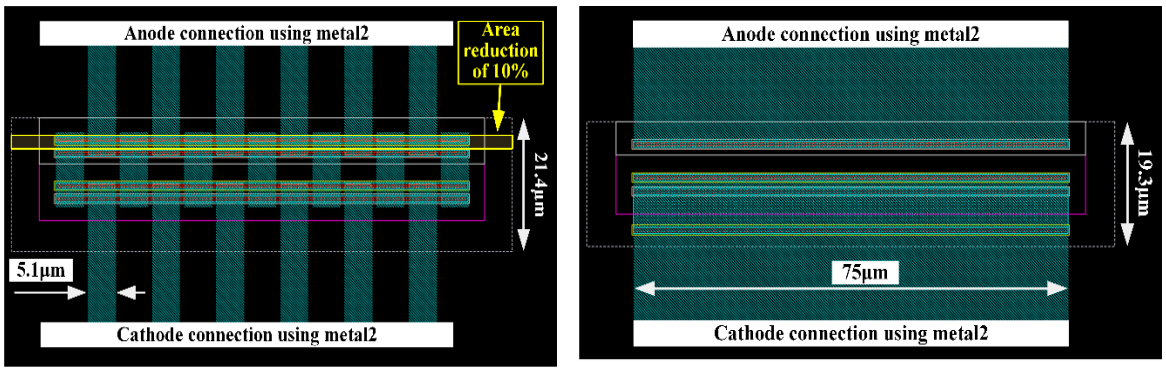
Figure 4. Total current density distributions at different current levels in proposed ERTSCR. (**a**) The trigger current flows along diode chain path; (**b**) the parasitic NPN and PNP transistors turn on; (**c**) the SCR path is triggered; and (**d**) the ESD current distribution after holding point.

3. Layout Design of Proposed ERTSCR

The proposed ERTSCR has been fabricated together with a conventional DCSCR in a 0.3-μm CMOS process. Figure 5a,b illustrate the layout top views of the conventional DCSCR and proposed ERTSCR with the same device width of 75 μm. In accordance with the design rule of this 0.3-μm CMOS process, the conventional DCSCR has a device length of 21.4 μm, while the proposed ERTSCR has a device length of 19.3 μm, with an area reduction of approximately 10% compared with the DCSCR as illustrated by the yellow rectangle in Figure 5a.

For SCR type devices with a smaller turn-on resistance and highest ESD current conduction capability per unit, the robustness of metal connection from the PADs to the anode and cathode of SCR device will be critical in the development of an optimized ESD discharging structure [14–16]. Regarding the conventional DCSCR structure, as shown in Figure 5a, the metal connections of PADs and anode/cathode have been split into six metal fingers by the metal connections between the anode gate and cathode gate since both metal connections used metal2. According to the measurements, the width of each metal finger is only 5.1 μm and thus, the total valid metal connection widths of PADs to anode/cathode will be reduced from 75 μm to 30.6 μm. However, in the proposed ERTSCR structure as shown in Figure 5b, the metal connections between PADs and anode/cathode and the ones between the anode gate and cathode gate can use different metal layers, such as metal2 and metal1, respectively. Thus, the metal connections of PADs to anode/cathode in ERTSCR will spread all over the full device width and their total valid widths will be 75 μm in this design. The larger metal connection width in

ERTSCR results in a smaller metal resistance of device connection and effectively troubleshoots the metal connection bottleneck.



(**a**) (**b**)

Figure 5. Layout top views and device dimensions of (**a**) conventional DCSCR; and (**b**) proposed ERTSCR. Both DCSCR and ERTSCR have a same device width of 75 μm.

4. Experimental Results and Discussion

4.1. TLP and HBM Results

The quasi-static I-V characteristics of the conventional DCSCR and proposed ERTSCR are measured using the transmission line pulse (TLP) HANWA TED-T5000 tester, with a rise time of 10 ns and pulse width of 100 ns. Figure 6 shows the TLP I-V curves of the conventional DCSCR and proposed ERTSCR with the same device width of 75 μm. Firstly, it can be observed that the trigger voltage (V_{t1}) of ERTSCR (1.33 V) is lower than that of DCSCR (1.48 V), which is due to the different trigger current distribution. As shown in Figure 3a, the trigger current of the conventional DCSCR flows sideways along the diode chain conduction path from the anode to anode gate before flowing from the cathode gate to cathode, which deviates from the direction of SCR path. As a result, less carriers will be injected to WELLs to trigger the SCR. However, the trigger current of the proposed ERTSCR flows inwardly along the diode chain conduction path as illustrated in Figure 4a from the anode to deeper DNW in the same direction as SCR path. Therefore, more carriers will be injected to WELLs, which is more convenient for triggering SCR. Secondly, it can also be observed that the holding voltage (V_h) of ERTSCR (1.06 V) is lower than that of DCSCR (1.32 V), which is due to the different current distribution of diode chain conduction path and main SCR conduction path. When DCSCR and ERTSCR have been triggered, the ESD current flows through both the diode chain conduction path and main SCR conduction path. In ERTSCR, the diode chain conduction path and main SCR conduction path overlap in NWELL-DNW. Thus, the holding voltage is mainly determined by the main SCR conduction path, which has a deeper snapback and lower holding voltage. Finally, the second breakdown currents of both conventional DCSCR and proposed ERTSCR are both approximately 5.3 A. Additionally, the human body model (HBM) measurement results show that both the conventional DCSCR and proposed ERTSCR have a HBM ESD robustness of more than 8 KV as measured using HANWA TED-W5000M. That means the proposed ERTSCR with a silicon area that is smaller by 10% has the same ESD robustness and can be regarded as an area efficient structure compared to the conventional DCSCR.

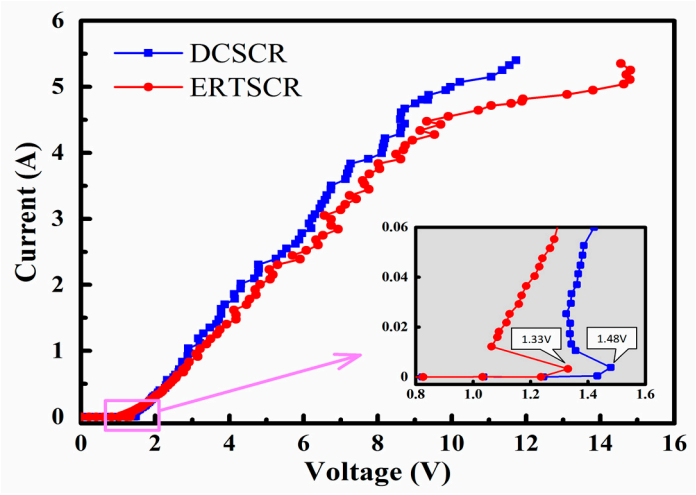


Figure 6. Measured TLP I-V curves of conventional DCSCR and proposed ERTSCR.

4.2. VF-TLP Measurement and Results

Another very fast TLP (VF-TLP) measurement was used to evaluate the turn-on performance of the ESD protection device during the fast ESD stress, such as in the charged device model (CDM). In this paper, the pulse width of VF-TLP pulse is 10 ns and the rise time is 200 ps. Figure 7 shows the measured VF-TLP I-V curves and the transient voltage waveforms in the holding region of the conventional DCSCR and proposed ERTSCR. The measurement results show that the overshoot voltages of DCSCR and ERTSCR at 0.5 A are 4.34 V and 6.15 V, respectively. The overshoot voltage of ERTSCR is slightly higher than that of DCSCR due to the increasing resistance in the trigger path that is introduced using R_{DNW}. However, the overshoot voltage of ERTSCR is low enough to protect the internal circuit from the fast ESD damage even in the nanometer scale process [17].

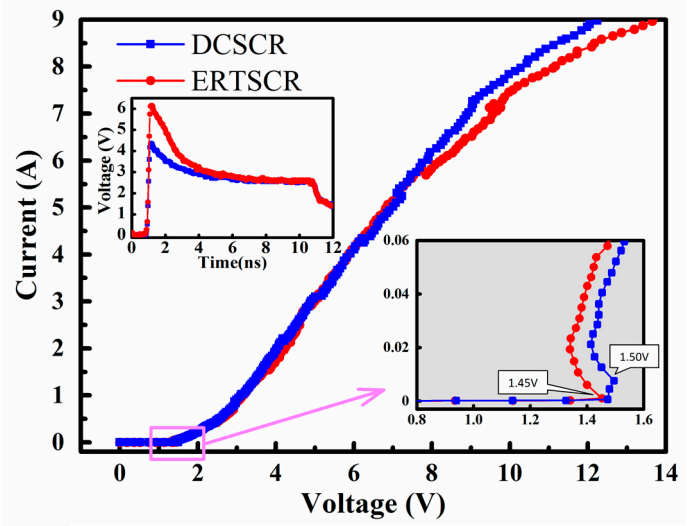


Figure 7. Measured VF-TLP I-V curves and transient voltage waveforms of conventional DCSCR and proposed ERTSCR.

4.3. Leakage Current Characteristics

Leakage current is another critical design metric for the ESD devices [18,19]. Figure 8 shows the measured leakage currents of the conventional DCSCR and proposed ERTSCR, with the anode biased from 0 V to 1.6 V and the cathode grounded. It can be seen that the leakage currents are less than 1 μA when biased below 1.2 V, which shows that both structures are suitable for the ESD protection of the

ICs working at 1.2 V or below [20]. As the biased voltage continuously increases, both the leakage currents quickly increase with the turning on of the two diodes and following SCR.

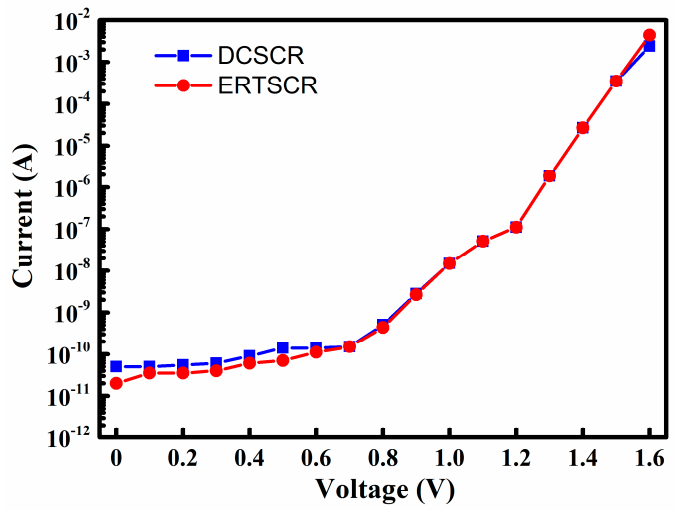


Figure 8. Measured leakage currents of conventional DCSCR and proposed ERTSCR.

5. Conclusions

An ESD protection device is presented in this article as an embedded resistor-triggered SCR. The proposed ERTSCR has a low trigger voltage, high second breakdown currents and acceptable leakage current. With comparable ESD robustness to conventional DCSCR, the proposed ERTSCR has a wider top metal width and an area cost reduction of approximately 10%.

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Conflicts of Interest: The authors declare no conflict of interest.

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