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Shaping SiC MOSFET Voltage and Current Transitions by Intelligent Control for Reduced EMI Generation

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Abstract: In power converters, the fast switching of the power conversion components results in rapid changes in voltage and current, which results in oscillations and high-level electromagnetic interference (EMI), so the power components become a source of internal electromagnetic interference. Taking SiC Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) as an example, an intelligent control method to suppressing interference sources is proposed in this paper. The combination of open-loop and closed-loop methods can simultaneously reduce the electromagnetic interference generated by voltage and current. Firstly, this paper analyzes how to select a reference signal. The relationship between the time domain and the frequency domain of the noise signal is analyzed. The convolution of the trapezoidal signal and the Gaussian signal is selected as the reference signal, which is named S-shaped signal in this paper. The S-shaped signal has continuous infinitely conductive characteristics, so its spectrum has a large attenuation in the high frequency region. Secondly, a new topology is proposed. Based on the closed-loop gate control, a current control signal is added, which can simultaneously shape the output voltage and control the output current slope. Both the simulation results and the experimental results show that the output voltage can follow the reference signal, S-shaped signal, and the slope and overshoot of output current can be changed. Compared with classical gate driver method, the spectrum of output voltage and output current obtained by the method proposed in this paper has a large attenuation, in other words, the electromagnetic interference is significantly reduced.

Keywords: power converters; EMI; intelligent control; classical gate driver; interference sources

1. Induction

Power converters composed of SiC MOSFETs are widely used in home, aerospace, and other fields due to their high operating frequency, high voltage, and high power density. However, due to the high dv/dt and di/dt of SiC MOSFET for high-speed switching, electromagnetic interference (EMI) is generated so that the SiC MOSFET becomes an electromagnetic interference source [1]. High dv/dt may produce common mode interference signals in power electronic circuits, while higher di/dt can cause higher voltage and current overshoot and oscillation due to parasitic factors in the circuit. The EMI signal can easily affect external sensitive components by radiation or conduction. It is common to reduce conducted interference by adding filters in the conduction path and radiated interference by shielding sensitive components. However, these two methods will take up more PCB space and increase the cost greatly. It is a challenge for engineers to balance the suppression effect of electromagnetic interference and costs [2]. Therefore, it is an interseting research direction that is suppressing EMI by controlling the fast switching transient [3]. Changing gate driving current [4], and using a built-in

snubber [5] all have limited effect for suppressing EMI. Active voltage control (AVC) method is applied to control the slope dv/dt of the output voltage, which is effective to control the switching transients of IGBT to reduce the EMI [6]. References [7–9] introduced how to predict the EMI for the defined edges of signal and what the influence of the defined reference signal is for the transients of IGBT, which provided the possibility to shape the Gaussian switching transients to suppress EMI. The active gate drive (AGD) method is an effective method for suppressing electromagnetic interference from the viewpoint of suppressing electromagnetic interference sources. The AGD method mainly includes three methods: controlling the gate current, controlling the gate voltage, and controlling the gate resistance. References [10,11] applied a method of controlling the gate current to control the switching transient. During the turn-off period of SiC MOSFET, a large current is injected into the gate to increase dv/dt to reduce the turn-off time and the turn-off loss is reduced thereby. When the output current drops, the rapidly decreasing gate current reduces the di/dt of the output current and the oscillation of the voltage generated by the inductance and parasitic capacitance is reduced. However, the dv/dt of the output voltage is not adjustable.

Reference [12] proposes a method of controlling the gate current by closed-loop and adding a delay compensation device to control the gate source turn-off voltage slope dv/dt and current slope di/dt, thereby achieving the trade-off between switching losses and electromagnetic interference. However, this method also has its limitations, because it can only control dv/dt and di/dt when MOSFET is closed. A new method of active gate drive method is proposed Reference [13], the principle of which is to increase the gate resistance value during the Miller plateau of the gate voltage during the turn-on and turn-off of the SiC MOSFET. This control method can control di/dt during turn-on and dv/dt during turn-off, respectively, and its switching loss is low. This control method can control di/dt during turn-on and dv/dt during turn-off, respectively, and its switching loss is low but this method cannot control dv/dt during turn-on and di/dt during turn-off. The precondition for this method to work properly is to select the correct switching time of gate resistance and the gate voltage cannot have large fluctuations, however, which is difficult to implement in engineering. In [14], the closed-loop control method is applied and di/dt and dv/dt are measured and then compared with reference signals to get the error. The error is input to the buffer pole through a differential op amp to dynamically adjust the gate voltage. The power semiconductor is turned on by the waveform following the reference signal. However, it is impossible to adjust dv/dt without di/dt restrictions because the same reference and the same gain are used [4]. All of the above methods of controlling a single dv/dt or di/dt have limited suppression of high frequency noise, and fail to achieve simultaneous control of voltage and current turn-on and turn-off. The results of reference [1] indicate that any switching waveform can be expressed in the form of convolution that it is get by an ideal square wave signal and a normalized instantaneous function derivative. From a frequency domain perspective, the switching waveform is the product of the square wave signal spectrum and the instantaneous function derivative spectrum. Reference [15] shows that if the transient function can be derived n times, the high-frequency spectral envelope of the switching waveform will be attenuated by a slope of $-20(n + 1)$ dB/dec. The Gaussian signal has continuous infinitely conductive characteristics, so that the high frequency spectrum of the Gaussian waveform is attenuated faster than the high frequency spectrum of the single slope theoretically. Therefore, in [2], the convolution waveform of the square wave signal and the Gaussian signal as the reference signal is used, and the switching voltage following the reference voltage by the method of closed-loop active voltage control is realized.

This paper proposed an intelligent control method based on the characteristic that voltage and current are not synchronized during SiC MOSFET switching. The intelligent control method that include a closed-loop circuit to shape the output voltage and an open-loop circuit to control the slope of the output current control the switching voltage and current simultaneously.

The article is organized as follows: Theoretical analysis of voltage reference signals and current control signals is discussed in the Section 2. An intelligent control method combining closed-loop and open-loop control methods is proposed in the Section 3. Simulation and experimental verification were

performed based on the proposed method in Sections 4 and 5. The conclusion of the experiment is presented in Section 6.

2. Theoretical Analysis

2.1. Selection of Voltage Reference Signal

In order to make the output voltage have a smooth transient during turn-on and turn-off period, it is a feasible method to select an appropriate reference signal in closed-loop control circuit. Therefore, the paper discussed how to select the reference signals first. Reference [1] discussed the effects of time domain parameters on the frequency domain envelope of the signal. The relationship between the number of derivatives of the transient signal in the time domain and the envelope of the high frequency component of the signal in the frequency domain is discussed in [15] that plays an important role to guide this paper. According to [16], a brief review of how to select the reference signal is shown as follows.

It is assumed that the switching transient waveform is represented by sw(t), and its image is shown in Figure 1a. Its expression is assumed as follow Equation (1)

$$\begin{gathered} t < 0\text{: } sw(t) = 0 \\ 0 < t < \tau\text{: } sw(t) = s(t) \\ \tau < t < t_0\text{: } sw(t) = A \\ t_0 < t < t_0 + \tau\text{: } sw(t) = A - s(t - t_0) \\ t_0 + \tau < t < T\text{: } sw(t) = 0 \end{gathered} \tag{1}$$

where s(t) is the switching transient function, A is the amplitude of the switching signal that is a constant, τ is the rise time and fall time, T is the switching period of the signal, t_0 is the signal width of square wave.

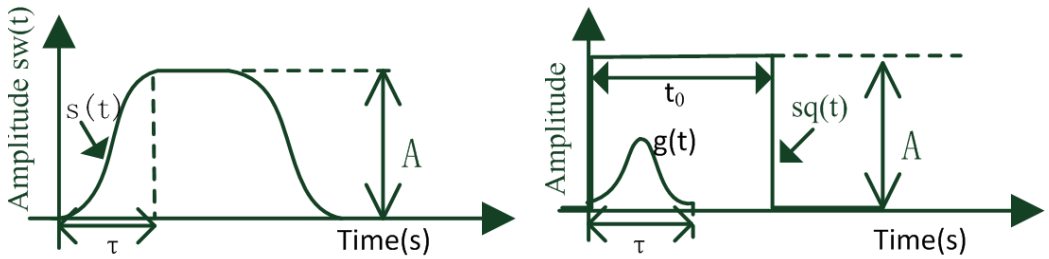

Figure 1. Switching signal (**a**) and structure (**b**).

Figure 1b explains how to get sw(t). The switching signal, sw(t), can be expressed as the convolution of the square wave signal sq(t) with 1/A*ds(t)/dt that is the normalized derivative of the transient function. The equation is

$$sw(t) = sq(t)*(1/A.ds(t)/dt) = sq(t)*g(t) \tag{2}$$

Perform the Fourier transform on Equation (2) and get the following Equation (3)

$$sw(f) = sq(f).g(f) \tag{3}$$

Obviously, it can be seen from Equation (3) that the switching signal sw(f) can be regarded as the product of the Fourier transform of a square wave signal and a shaped smoothing function.

According to [1], in the frequency domain, the slope of the envelope of sw(f) is closely related to the derivative times k of the function in the time domain. It is supposed that $sw^{(k)}(t)$ shows discontinuity and P Dirac pulses will appear in $sw^{(k+1)}(t)$ after the (k + 1) times derivative.

$$sw^{(k+1)}(t) = \sum_{i=1}^{p} A_i \delta(t - \tau_i) \tag{4}$$

τ_i and A_i are the times and amplitudes of the Dirac pulse. The expression of Fourier transform on (4) is

$$F_s{}^{(k+1)}(n) = \sum_{i=1}^{p} A_i e^{-jnw_0\tau_i} \tag{5}$$

where $w_0 = 2\pi/T$, $F_s(n)$ is the coefficient of the Fourier transform of sw(t). The expression of $F_s(n)$ is as Equation (6)

$$F_s(n) = \frac{\sum_{i=1}^{p} A_i e^{-jnw_0\tau_i}}{T(jnw_0)^{k+1}},\ n \neq 0 \tag{6}$$

From Equation (6), high-frequency harmonics coefficients is get as Equation (7) when $n \to \infty$.

$$\lim_{n\to\infty} F_s(n) = \frac{\sum_{i=1}^{p} |A_i|}{T(nw_0)^{k+1}} \tag{7}$$

It can be seen from (7) that for an arbitrary waveform, the high-frequency boundary amplitude is determined by the sum of its derivative times k, P Dirac pulses amplitude and its fundamental frequency $f_0 = w_0/2\pi$ in the frequency domain. The attenuation envelope slope is $-20(k + 1)$ in the high-frequency domain. In order to verify the higher frequency, the derivatives times of the function, the better the high-frequency EMI suppression effect [17], the following examples are used.

We define the zero-order signal to be the square signal $q_0(t)$ and two-order signal to be the symmetrical trapezoidal signal. Infinite-order signal, $sw_\infty(t)$, can be expressed as the convolution of a square wave signal and a Gaussian signal. Their expressions are

$$sw_1(t) = q_0(t) * g_0(t) \tag{8}$$

$$sw_\infty(t) = q_0(t) * gs(t) \tag{9}$$

where $g_0(t)$ is a square signal, $g_S(t) = \frac{1}{\sigma_t\sqrt{2\pi}} e^{-\frac{t^2}{2\sigma_t^2}}$ is a Gaussian signal. The mentioned zero-order signal and two-order signal that we selected both are symmetric signal. The duty cycle is D = 0.5, the switching frequency is 10 kHz, rise time is t_{off} = 1 µs, fall time is t_{fall} = 10 µs, $\sigma_t = \frac{1}{4}t_s = 0.25 \times 10^{-6}$.

The spectrum of $q_0(t)$, $sw_1(t)$ and $sw_\infty(t)$ are shown in Figure 2. It is worth mentioning that only time t is$|t| \to \infty$, the Gaussian function is $g_S(t) \to 0$. In other words, the value of Gaussian function is not strictly equal to 0 in a finite period so there is a theoretical limitation. However, when $|t| \geq 2\sigma_t$, the Gaussian value is close to 0. Therefore, if $\sigma_t = (1/4)t_s$ is taken, the value of Gaussian function can be regarded as 0 at the two endpoints of the finite time.

From Figure 1, it can be seen that the high frequency component of one-order signal (trapezoidal signal) is lower than zero-order signal (square signal) and the high frequency component of infinite-order signal (Gaussian signal) is lower than one-order signal, which is consistent with the theory that the higher the derivative times is, the better the suppression effect on high frequency noise is.

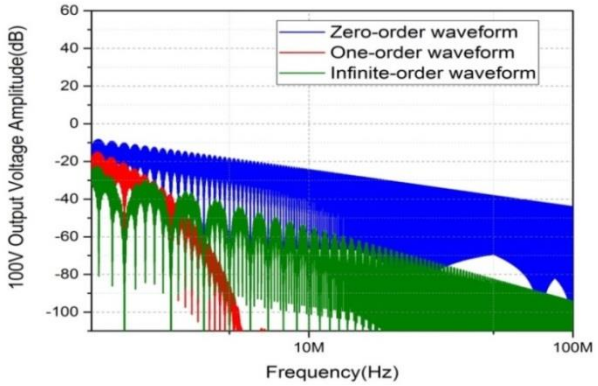

Figure 2. Spectra comparison of zero-order waveform (square signal), one-order waveform (trapezoidal signal) and infinite-order waveform (Gaussian signal).

2.2. Control Principle for Current

According to the literature [18], the derivative of the drain current to time, $\frac{dI_d}{dt}$ is expressed as Equation (10) when the MOSFET is turned on.

$$\frac{dI_d}{dt} = \frac{V_{gg} - \left(\frac{I_d}{g_m} + V_{th} + \frac{L_g C_{iss}}{g_m}\frac{d^2 I_d}{dt^2}\right)}{R_{g,on}\frac{C_{iss}}{g_m} + L_s} \tag{10}$$

where V_{gg} is the gate voltage, Vth is the threshold voltage, L_g is the gate parasitic inductance, $C_{iss} = C_{gs} + C_{gd}$ (C_{gs} gate source parasitic capacitance, C_{gd} gate drain parasitic capacitance), g_m is transconductance, $R_{g,on}$ gate resistance at turn-on and L_s is the source parasitic inductance. The drain reverse recovery current is given by (11) [19].

$$I_{rr} = \sqrt{\frac{2Q_{rr}\frac{dI_d}{dt}\Big|I_d = I_l}{S+1}} \tag{11}$$

where Q_{rr} is the reverse recovery charge and S represents the fast factor. It can be seen from (10) (11) that the reverse recovery current and current overshoot can be controlled by changing the V_{gg}.

During turn-on period for MOSFET, the derivative of the drain current to time is given by (12)

$$\frac{dI_d}{dt} = -\frac{V_{ee} + \frac{I_d}{g_m} + V_{th} + \frac{L_g C_{iss}}{g_m}\frac{d^2 I_d}{dt^2}}{Rg,off\frac{C_{iss}}{g_m} + L_s} \tag{12}$$

where V_{ee} is the gate voltage at turn-off for MOSFET. From (12), the slope of the drain voltage can be controlled by changing the gate voltage V_{ee} during turn-off period.

3. Proposed Intelligent Control Method and Operation Principle

The total circuit diagram used in the proposed intelligent control method for voltage and current is shown in Figure 3. The circuit consists of an open-loop circuit, a closed-loop circuit and a conventional totem pole drive. The drain-source voltage V_{ds} of the SiC MOSFET is shaped by the closed-loop circuit in the upper side. When Logic1 outputs 1, switches S1 and S2 are turned on at the same time, the closed-loop circuit starts to work and the drain voltage is fed back by the drain voltage feedback circuit to the positive terminal of the operational amplifier according to the ratio β. The feedback signal is compared with a reference signal generated by the reference signal generator 1, and the gate of the SiC MOSFET is controlled by a totem pole drive circuit. When Logic2 outputs 1, the switches S3 and S4 are turned on, and the current control signal V_i control the gate voltage by the operational amplifier

2. It is necessary to add a resistor R_g to the gate to connect the gate to prevent the SiC MOSFET from operating outside the safe zone. Another function for the R_g is to reduce the oscillation of voltage and current when turned on and off. The value of R_g can be selected according to the values recommended in the datasheet. In this paper, its value is 5 ohms.

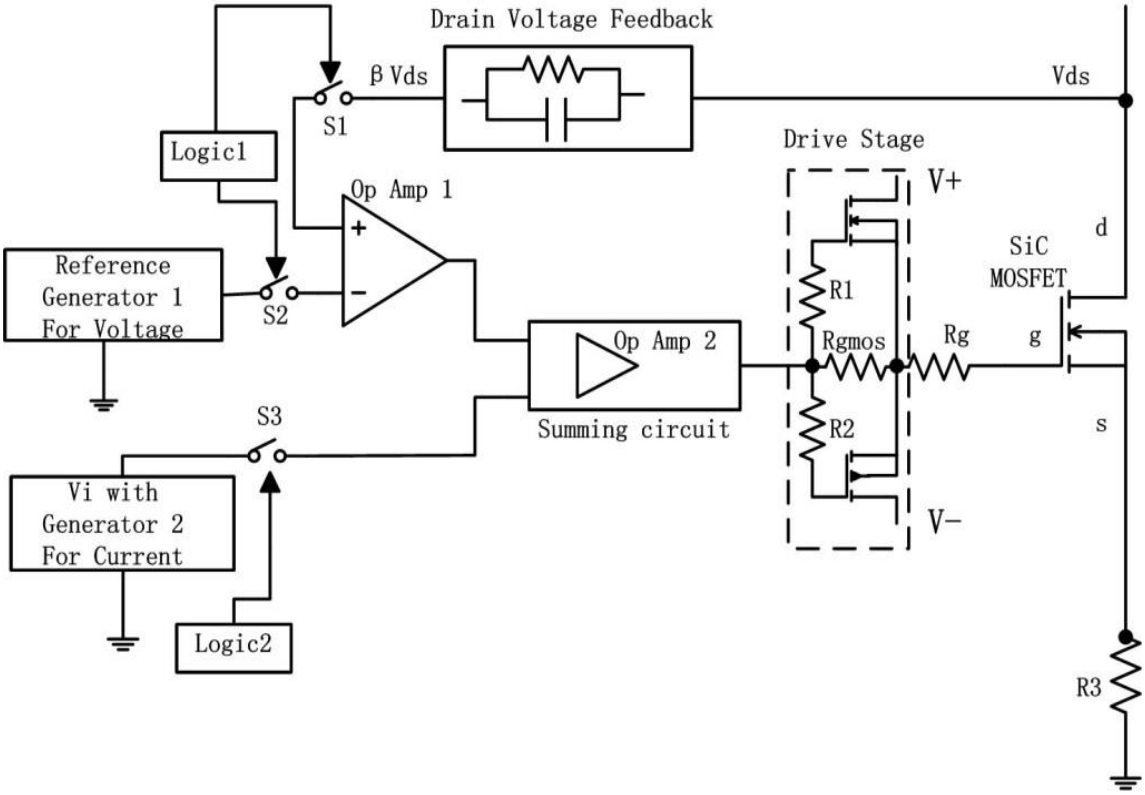

Figure 3. The general scheme of control method for the proposed time division shaped switching transitions.

The control signal selected is the Gaussian signal in this paper, which is generated by arbitrary waveform generator, M3202A, according to Equation (11). The proposed intelligent control method for voltage and current is based on fact that the current and voltage are not synchronized during MOSFET switching period. Figures 4 and 5 show the time domain signal of the SiC MOSFET during turn-on and turn-off period under hard switching conditions respectively. During the period from t2 to t3, the current I_d rises firstly, and the voltage V_d has a small decrease (in order to simplify the analysis, V_d is regarded as unchanged in this paper). At the time t3, the current rises to the maximum, the voltage begins to drop rapidly, and it drops to the lowest moment. During the period from t7 to t8, the voltage V_d rises rapidly, and the current I_d has a small drop (to simplify the analysis, the I_d does not change during this time period). At t8, the voltage V_d (Drain voltage) gets the maximum value. The current I_d drops rapidly after t8 and the current gets the minimum value t9. Therefore, the drain voltage and current of SiC MOSFET are not synchronized during switching period, which provides a possibility for intelligent control.

Time domain diagram of Gaussian control signals for voltage and current is shown in Figure 6. S1(t) and S2(t) are rising edges for drain voltage and current respectively and the falling edge signal is symmetric with the rising edge signal. They can be obtained by Equation (11).

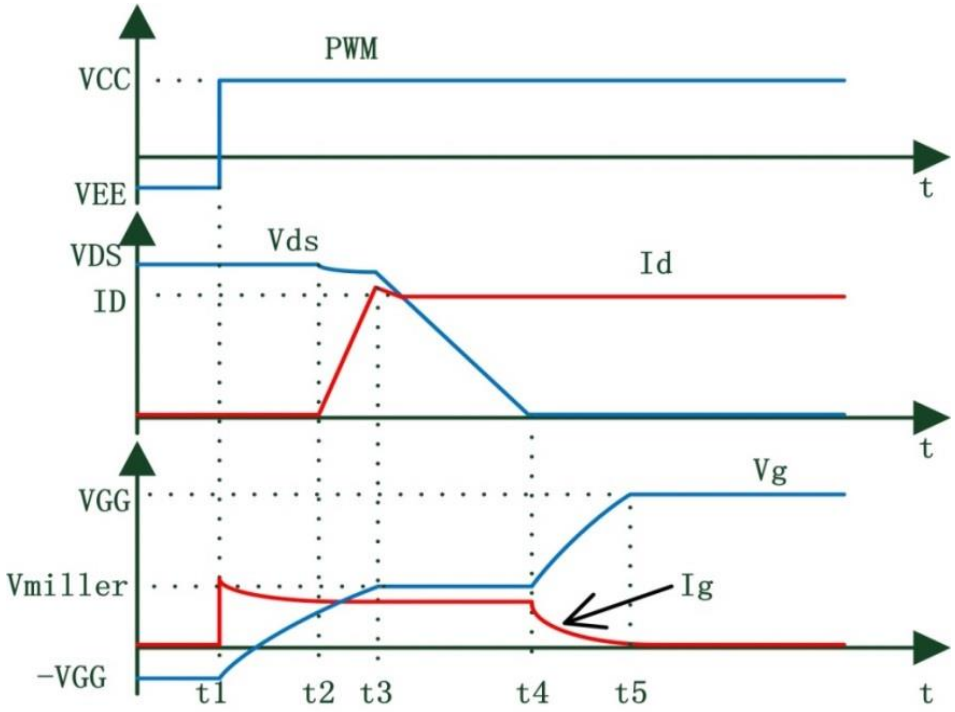

Figure 4. Turn-on voltage and current of SiC MOSFET under hard switching conditions.

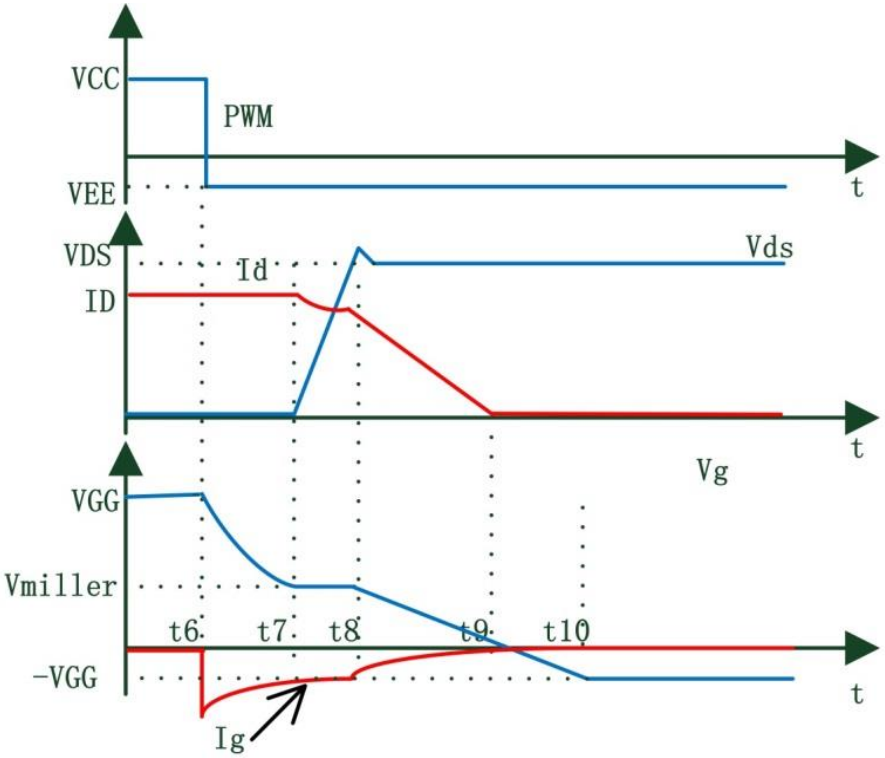

Figure 5. Turn-off voltage and current of SiC MOSFET under hard switching conditions.

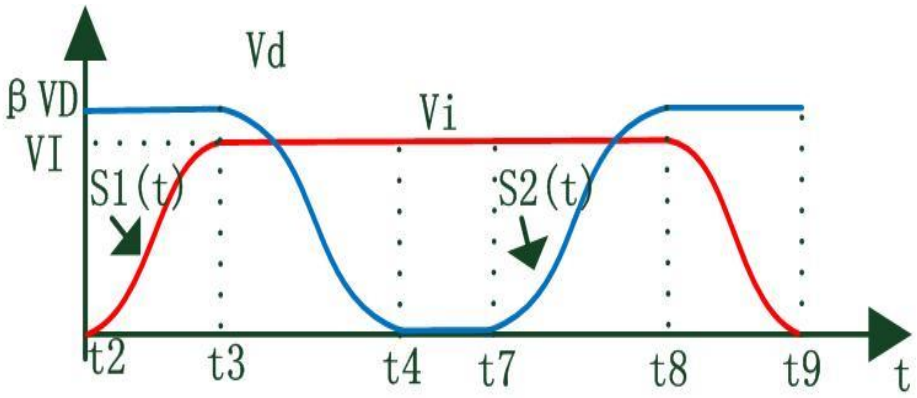

Figure 6. Time domain diagram of Gaussian control signals for voltage and current.

Figures 7 and 8 are the theoretical waveforms of the voltage and current of the proposed intelligent control for turn-on and turn-off, respectively. The switch S3 is turned on and the current control signal is connected to the circuit to control the output current during the 0–t3 period. At time t3, switch S3 is opened and the open-loop circuit stop working. It should be noted that S1 and S2 are closed at time t21 that is before time t3. The delay time for switches S1 and S2 is td1 = t3 − t21. The delay time is caused by MOSFET, operational amplifier, and coupling circuit, which must be taken into account to make the upper part of the circuit achieve the best turn-on transient behavior, when the open-loop stops working. In contrast to the turn-on transient, S1 and S2 are turned on during the t21–t8 period and the voltage closed-loop operates normally. At time t8, S1 and S2 are turned off. However, S3 is turned on at time t_{71} that is before time t8. This is because a delay time td2 = t8 − t71 is required to achieve current control after the switch S3 turned-on. The delay time that we concerned to cause by MOSFET, operational amplifier, and coupling circuit guarantees that MOSFET has an optimal turn-off behavior transient. The values of td1 and td2 can be dynamically adjusted to determine the optimum value, according to the switching voltage and current transients of the MOSFET.

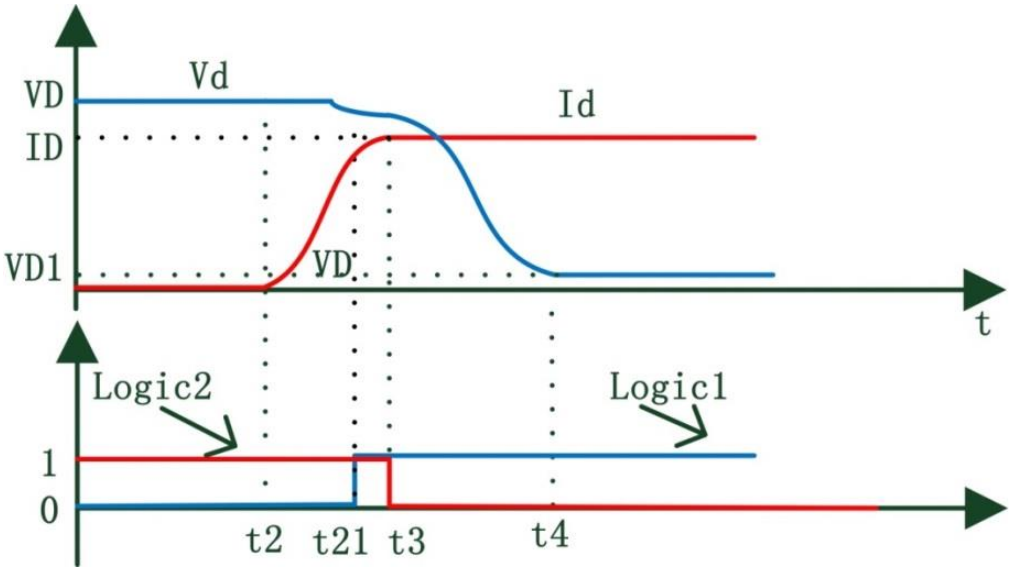

Figure 7. Turn-on voltage and current waveform of SiC MOSFET the in the proposed circuit.

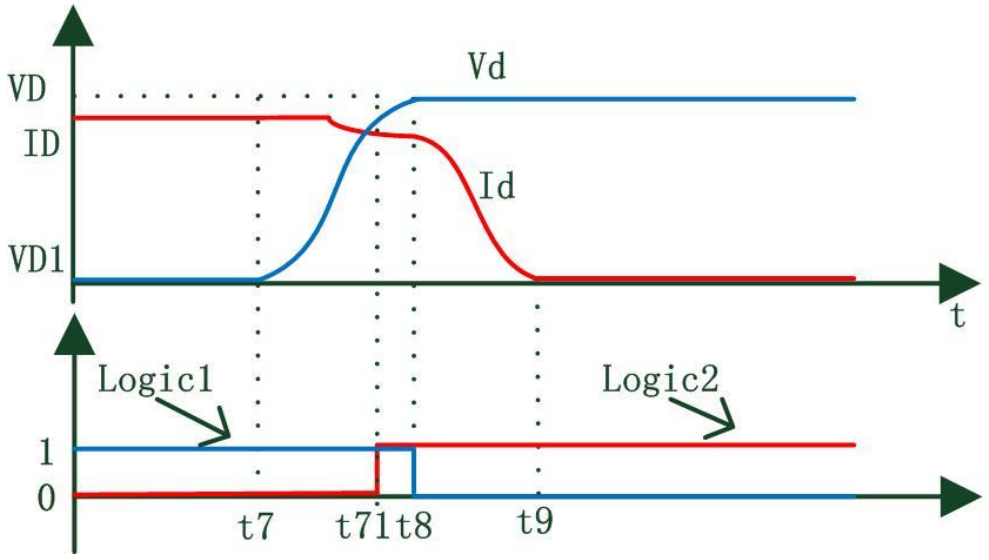

Figure 8. Turn-off voltage and current waveform of SiC MOSFET in the proposed circuit.

4. Circuit Simulation and Discussion

Before the experiment, it is necessary to simulate the proposed circuit, which can improve the experimental guidance and improve the efficiency for the experiment. Pspice is a professional circuit simulation software so it was chosen as the simulation software in this paper. Japan's ROHM semiconductor's SCT2160KE SiC MOSFET was selected and the body manufacturer offered the user a 1200-V/22-A Pspice model of SiC MOSFET. In order to simplify the circuit, the standard chopper unit was selected as the control object with inductive load in this paper. Both the voltage reference signal and the current control signal are Gaussian signals and the rising edge time, 1 μs, is equal to the falling edge time. The amplitudes of the voltage reference signal and the current control signal are 5, 4, respectively. According to Equation (11), the values of the Gaussian signal was calculated by the MATLAB and then imports into Pspice. The period is set to 6 μs and the duty cycle is 2/3. It is worth noting that in the simulation, the Gaussian reference signal is compared with the output signal that is fed back according to a certain ratio, rather than compared with the real output signal. Figures 9 and 10 are simulation diagram for turn-on and turn-off in time domain respectively. The rising edge time and falling edge time of the voltage reference signal are both 1 μs and the rising edge time and falling edge time of the current control signal are also 1 μs in Figures 9 and 10. The rising edge time and the falling edge time of the reference voltage are both 1 us, and the rising edge time rise time and the falling edge time of the current control voltage are both 0.5 μs. Figure 11 has the same working conditions with Figure 12 including the voltage reference signal and the current control signal. Comparing Figures 9–12, it can be seen that the proposed method can not only achieve the output voltage following the reference voltage, but also control the rising and falling edge of the drain current. It is worth mentioning that due to the presence of the on-resistance and the sampling resistor, the minimum value of the output voltage V_{ds} is not zero, and the minimum voltage of V_{ds} is defined as VD1 in this paper.

$$V_{D1} = I_D(R_{in} + R_3), \tag{13}$$

where I_D is the on-state current, R_{in} is on-state resistance and R_3 is the sampling resistor.

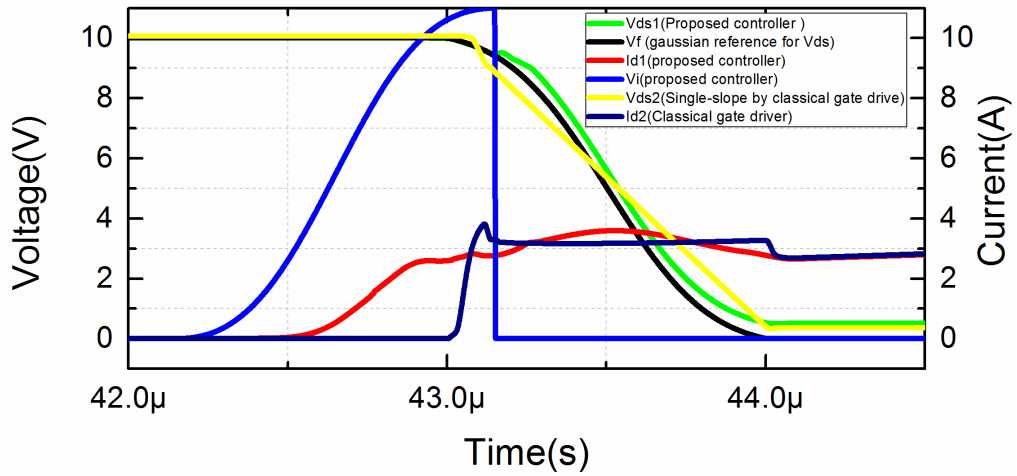

Figure 9. Pspice simulation for SiC MOSFET during turn-on with 1 µs falling edge of V_f (reference voltage) and 1 µs rising edge of V_i (the voltage to control current).

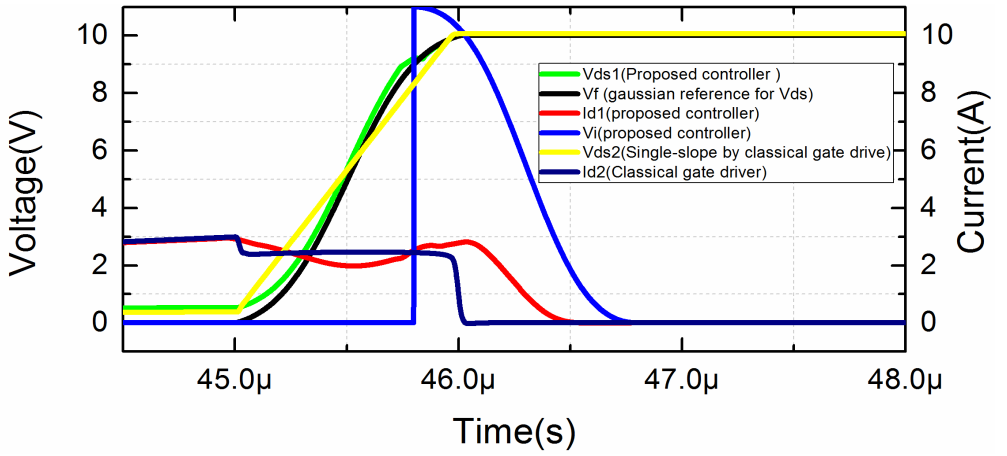

Figure 10. Pspice simulation for SiC MOSFET during turn-off with 1 µs rising edge time of V_f (reference voltage) and 1 µs falling edge time of V_i (the voltage to control current).

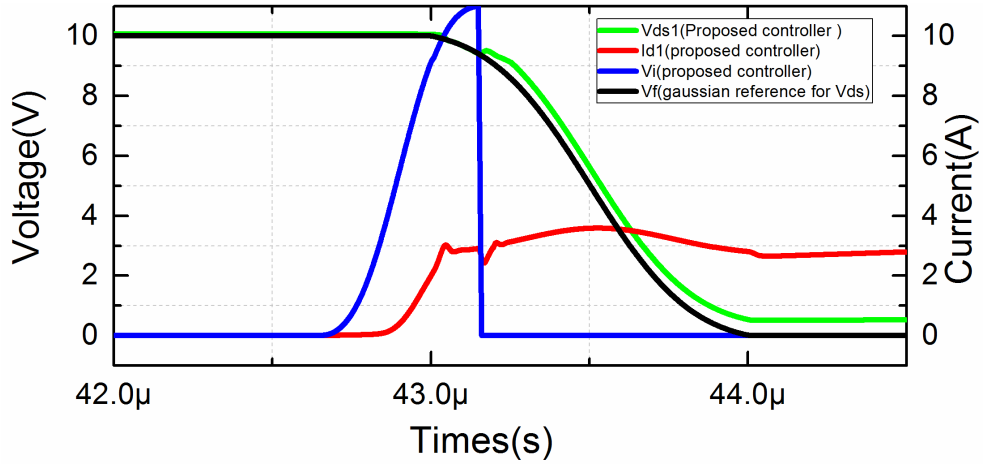

Figure 11. Pspice simulation SiC MOSFET during turn-on with 1 µs falling edge time of V_f (reference voltage) and 0.5 µs rising edge time of V_i (the voltage to control current).

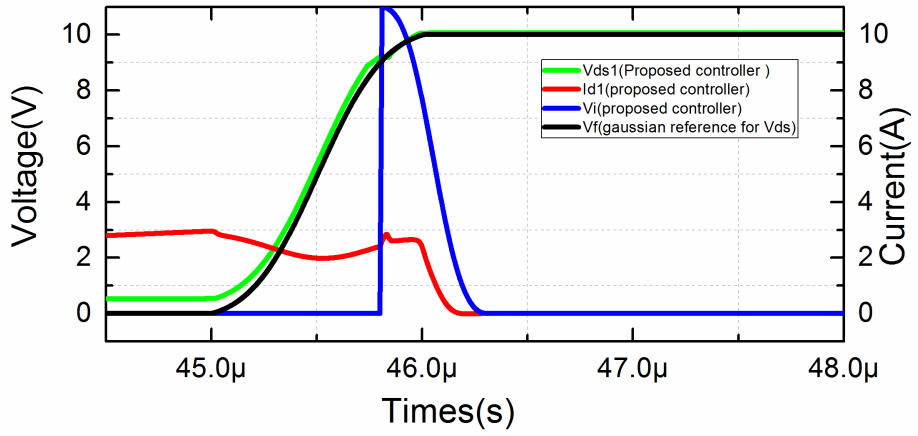

Figure 12. Pspice simulation SiC MOSFET during turn-off with 1 µs decline time of V_f and 0.5 µs rise time of V_i.

It is worth mentioning that the time domain diagrams of the gate-source voltage and gate current of the conventional gate drive method are also shown in Figures 9 and 10. This paper compares the spectrum of the obtained drain voltage and drain current obtained by the conventional gate driving method and the proposed method shown in Figures 13 and 14. Figure 13 shows the spectrum of the drain voltage obtained by the conventional method and the proposed method. It can be seen from Figure 13 that the envelope of the spectrum obtained by the proposed method is lower than the conventional gate driving method in the frequency range of 100 kHz to 70 MHz. However, the proposed method has obvious bumps in the spectrum around 80 M, which may be caused by fluctuations of the drain voltage caused by voltage switching. Figure 14 compared the spectrum of the drain current obtained by the proposed method with the drain current obtained by the conventional method. It can be seen from Figure 14 that when the frequency is less than 200 kHz, their spectral envelopes are basically coincident. When the frequency is higher than 200 kHz, the envelope obtained by the proposed method has a significant attenuation compared with the classical gate driving method and the attenuation is about 30 dB. Therefore, the effect of the proposed control method for suppressing EMI is very obvious.

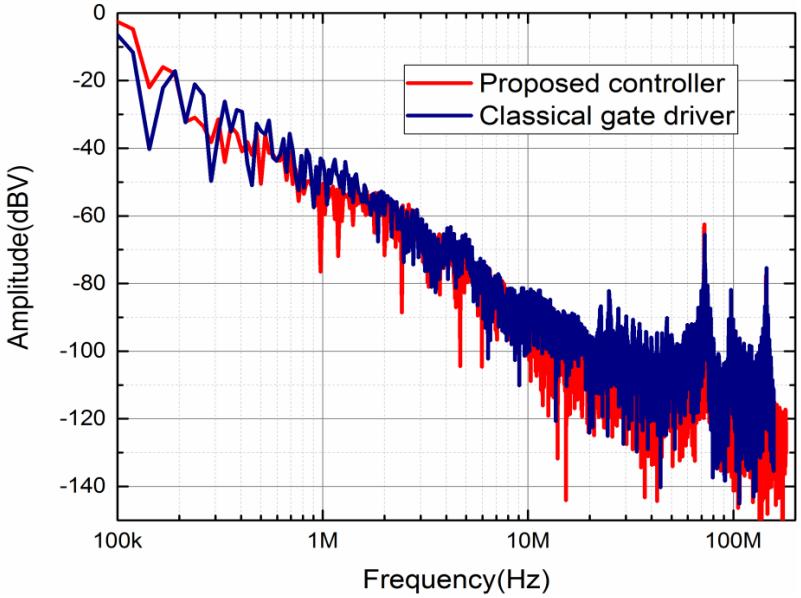

Figure 13. Pspice simulation V_{ds} spectra comparison (t_{off} = t_{fall} = 1.0 µs, purple: classic gate driver, red: proposed controller).

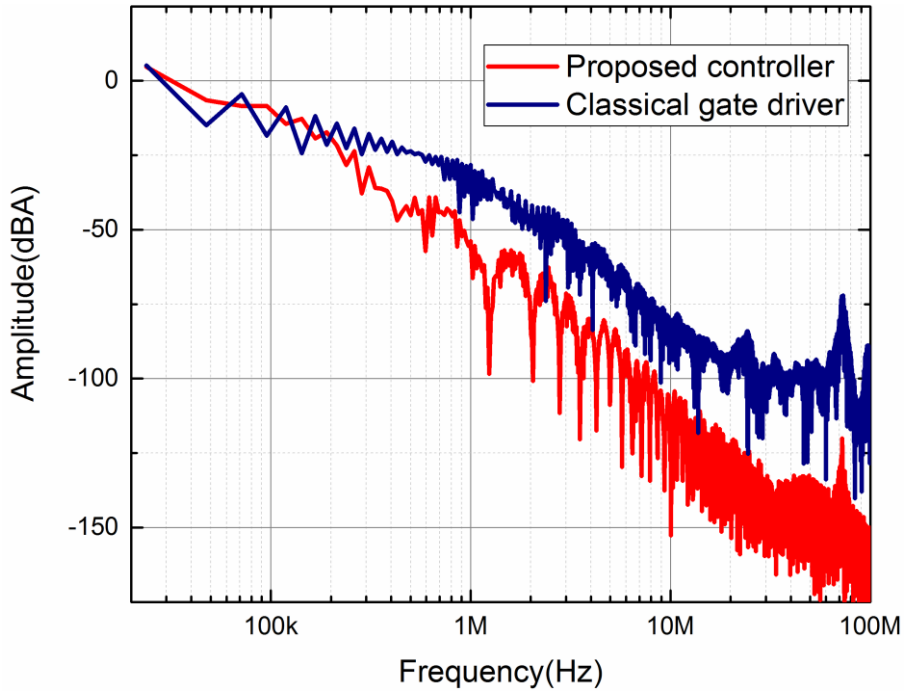

Figure 14. Pspice simulation I_d spectra comparison (t_{off} = t_{fall} = 1.0 µs, purple: classic gate driver, red: proposed controller).

5. Experiment Results of Proposed Method and Classic Method and Discussion

Similar to the simulation, the chopper unit with inductive load was also selected as the experimental circuit for simplicity. The op amp TH3091 that has wide Supply Range ±5 v to ±15 v, low voltage noise 2 nV $\sqrt{\text{Hz}}$ and high band 200 MHz was used in this paper. The specific parameters of the proposed circuit and the classical gate drive circuit are listed in Table 1. The time domain data of the Gaussian signal is obtained by MATLAB and imported into the M3202A that is an arbitrary signal generator. The hardware configuration of the proposed intelligent control method is shown in Table 1. In the first experiment, proposed controller 1 was used, assuming that the rising edge time t_{off} = 1 µs, the falling edge time t_{fall} = 1 µs, cycle T = 6 µs, duty cycle D = 1/3 for the reference signal V_f and the rising edge time t_{r2} = 1 µs, the falling edge time t_{f2} = 1 µs for the control voltage V_i. The time domain relationship between voltage reference signal and current control signal is shown in Figure 6. In the second experiment, the proposed controller 2 was used, in which the setting of the voltage reference signal V_f was the same as the first experiment, but V_i, t_{off} = 0.5 µs, t_{fall} = 0.5 µs, is different with the first experiment.

Table 1. Experiment circuit parameters.

Rg(Ω)	Op Amp	A1 × A2		Driver
Classical gate driver	5	NULL	NULL	MOS
Proposed Intelligent controller	5	THS3091	10 × 1	MOS

In Figure 15, the drain-source voltage V_{ds} for the blue track of the controller 1 and the red track of controller 2 is delayed by 0.1 µs compared with the reference voltage at turn-on. At turn-off the drain-source voltage V_{ds} for the blue track of the controller 1 and the red track of controller 2 follows the reference voltage well. However, for the blue trajectory and the red trajectory, there is a significant fluctuation in the top corner region at turn-on and turn-off, which may be caused by fluctuations in current for switching, parasitic inductance, and sampling resistor parasitic capacitance.

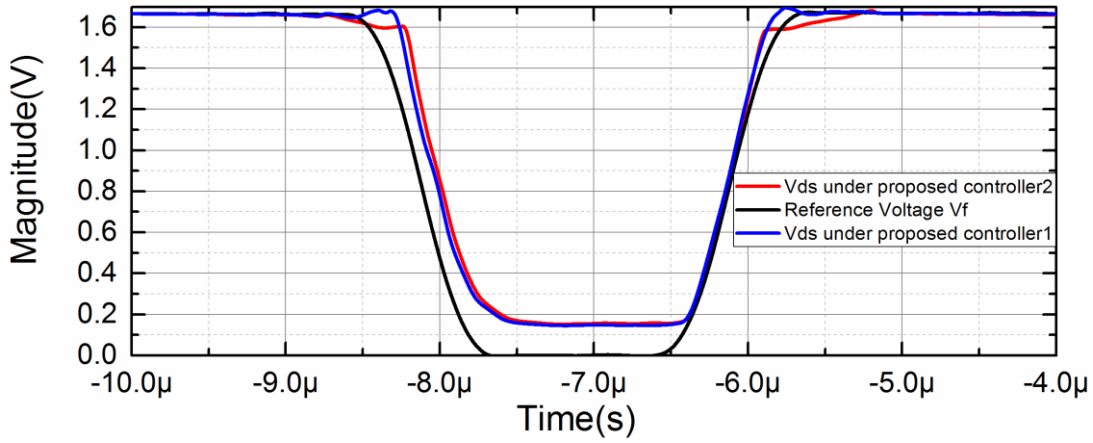

Figure 15. Experiment result that voltage comparison V_{ds} of proposed controller 1 (blue, $t_{off} = t_{fall} = 1$ μs of V_f), proposed controller 2 (red, $t_{off} = t_{fall} = 1$ μs of V_f), and reference voltage V_f (black, $t_{off} = t_{fall} = 1$ μs).

The classic gate driver is also used in the chopper for comparison, in which the hardware configuration is shown in Table 1 and the drive signal is the ideal PWM, the period 6 μs, duty cycle 1/3. The spectrum comparison of the drain-source voltage is shown in Figure 16. As can be seen from Figure 16, the envelopes of the three spectra in the low frequency region are almost coincident. The envelope of the classic gate drive in the 10^6–10^7 Hz range is 20 dB higher than the envelope of the proposed control 1 and control 2. The envelope of the classic gate drive in the range of 10^7–10^8 Hz is 40 dB higher than the proposed envelope of control 1 and control 2. In the analyzed frequency range of 10^5–10^8 Hz, the spectral envelopes of the proposed control 1 and control 2 are almost coincident, which shows that the current control signal V_i has little effect on the drain-source noise when the reference voltage V_f is the same in the proposed circuit.

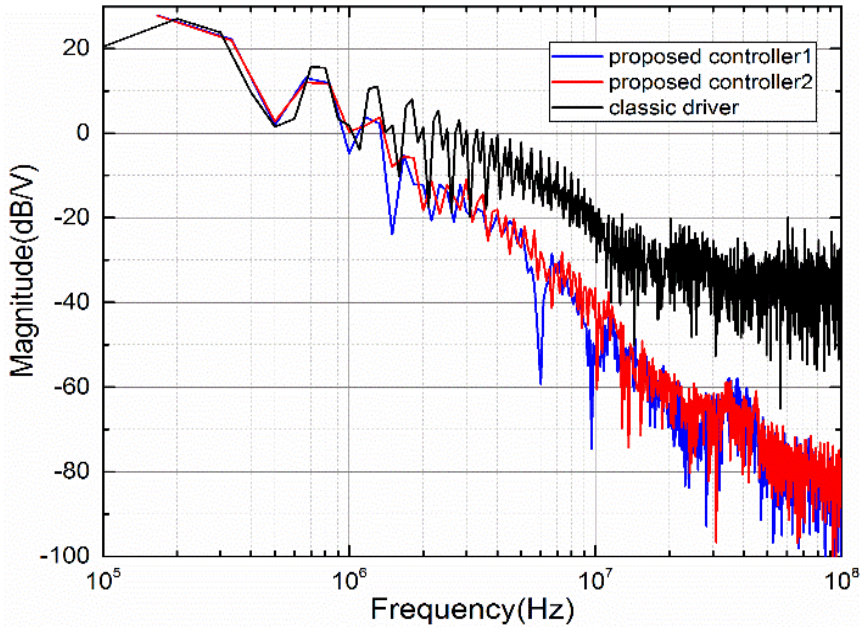

Figure 16. Spectra comparison of V_{ds} between classic gate driver (black), proposed controller 1 (blue) and proposed controller 2 (red). Same reference voltage V_f was used in controller 1 and controller 2.

In Figure 17, the drain current I_d of proposed controller 1 has lower slope di/dt of 2.94 A/us than controller 2 of 6.46 A/us so that the controller 1 reduces the current overshoot 40% at turn-off.

At turn-on, the switching speed di/dt of controller 1 is 4.58 A/us, and the di/dt of controller 2 is 6.87 A/us. Accordingly, the controller 1 reduces the current overshoot about 50%.

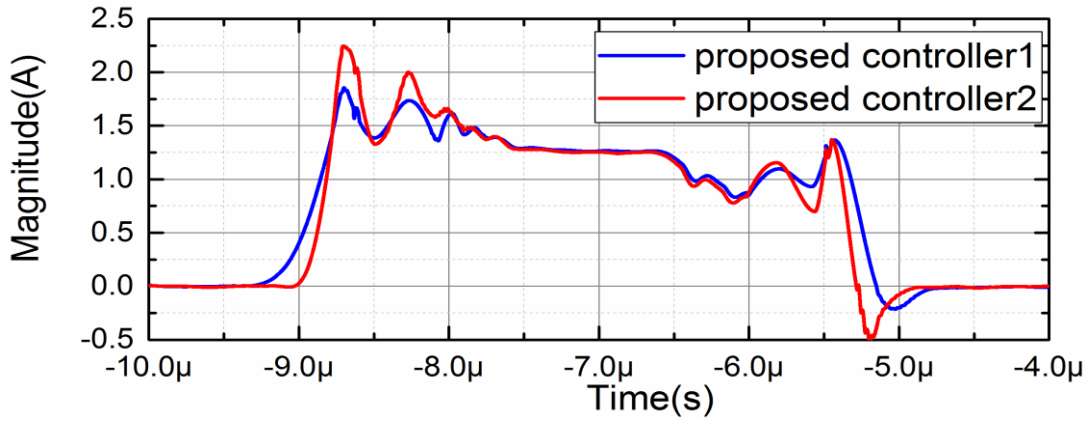

Figure 17. Experiment results of I_d for turn-on and off transition between controller 1 (t_{off} = t_{fall} = 1 μs of V_i) and controller 2 (t_{off} = t_{fall} = 0.5 μs of V_i). Same reference voltage V_f was used in controller 1 and controller 2.

The spectrum comparison of the drain-source current I_d is shown in Figure 18. It can be seen from the Figure 18 that before 3×10^6 Hz, the spectrum of the classical gate driver, the proposed control 1 and control 2 are almost coincident. When the frequency is greater than 3×10^6 Hz, the spectrum envelope of the classical gate driver is 10–40 dB higher than the proposed controller 1 and controller 2. In the frequency range of 10^7–5×10^7 Hz, control 1 is reduced by 5–10 dB compared with controller 2, since the current slope di/dt of controller 1 is smaller than controller 2.

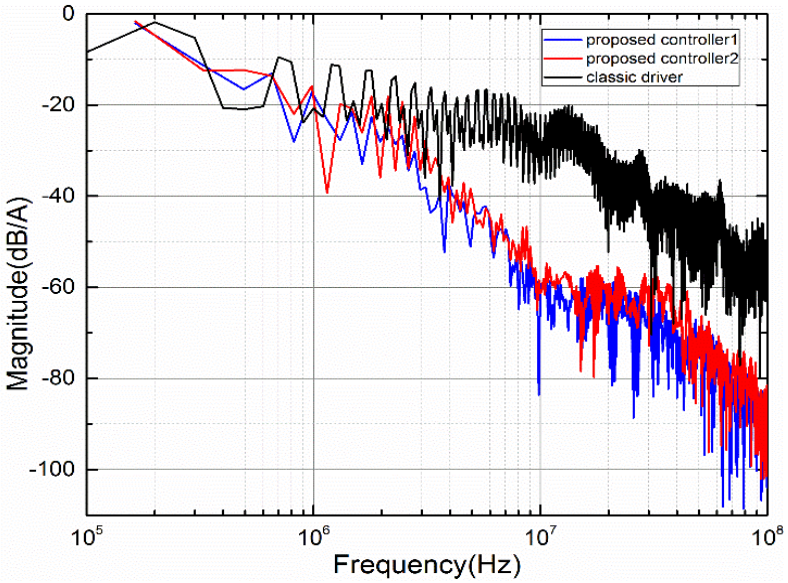

Figure 18. Spectra comparison for I_d between classic gate driver (black), proposed controller 1 (blue) and proposed controller 2 (red).

Switching losses also has been studied in this paper. The switching power of the three experiments are compared in Figure 19. As can be seen from Figure 19, there are mainly two peaks in one cycle. The first power peak is generated when the SiC MOSFET is turned on, and the second power peak is generated when the SiC MOSFET is turned off. The area enclosed by the power curve and the time axis represents the energy of the loss, and the loss at turn-on is higher than it at turn-off significantly.

The typical gate driver switching losses are smaller than the proposed controller 1 and controller 2. Figure 20 shows the curve of switching loss over time in one cycle. It can be seen in Figure 20 that the proposed controller's switching losses are approximately 120% higher than the classic gate drivers at the end of a cycle, since the switching time of the classic gate drive is much shorter than the proposed controller 1 and controller 2. The switching loss of the controller 2 is 6.4% lower than the controller 1, because the current rise and fall time of the controller 2 is shorter than the controller 1. It should be noted that in actual application, we can adjust the parameters to adjust the loss. According to [20], we know that there is compromise between EMI and switching losses. Therefore, we can reduce the switching loss by reducing the rising and falling edge times of the reference voltage within the acceptable EMI range.

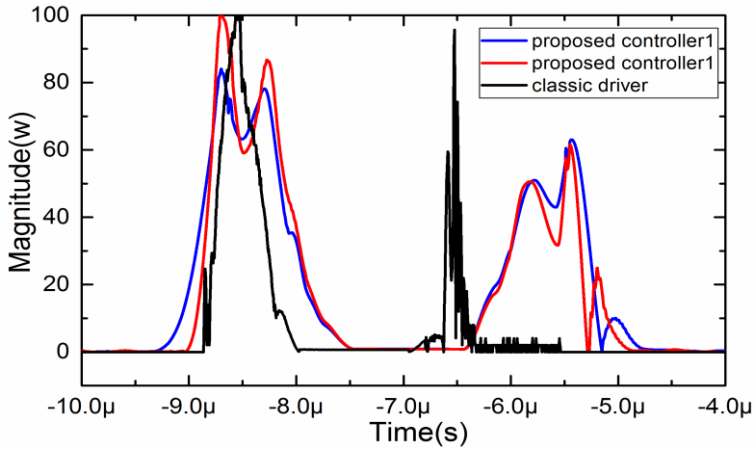

Figure 19. Power comparison between the proposed controller 1, the proposed controller 2, and classical gate driver.

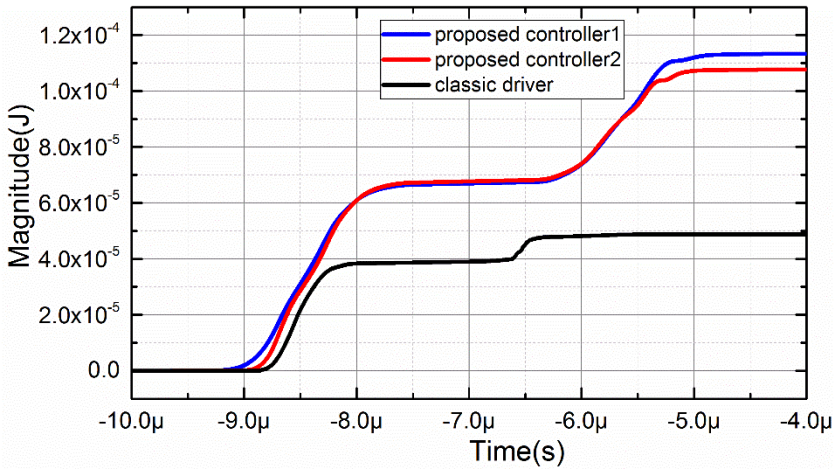

Figure 20. Switching losses comparison between the proposed controller 1, the proposed controller 2, and classical gate driver.

6. Conclusions

The proposed intelligent control method has good EMI suppression for voltage and current compared with the classical gate driving method, the hard switching method. It has been proved that the intelligent control method can shape the SiC MOSFET switching transition effectively. Compared with the common method, it achieves control of drain-source voltage and drain current simultaneously. This method requires a precise fit of the voltage control signal and the current control signal so that a high frequency signal generator is needed. However, the proposed method needs longer switching

time than classic driver so that the proposed method causes more power loss. Therefore, it is needed to tradeoff the EMI and switching loss. According to [20], it is an effective way to adjust the rise and fall switching time to reduce switching loss. Control signals can be obtained by convolution calculations and generated by high frequency multi-channel arbitrary signal generators. However, there are certain limitations, for example, voltage and current oscillations during circuit switching. The future work is to study the finite time stability of the circuit when two circuits work at the same time.

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