electronics

MDPI

Article

A Fast Transient Response Digital LDO with a TDC-Based Signal Converter

Hongda Zhang, Peiyuan Wan *, Jiarong Geng, Zhaozhe Liu and Zhijie Chen

College of Microelectronics, Faculty of Information Technology, Beijing University of Technology, Beijing 100124, China; feall3@emails.bjut.edu.cn (H.Z.); fresh_grapes@126.com (J.G.); dsx_54lzz@sina.com (Z.L.); chenzj@bjut.edu.cn (Z.C.)

* Correspondence: wanpy@bjut.edu.cn; Tel.: +86-(010)-6739-1269

Received: 24 December 2019; Accepted: 8 January 2020; Published: 10 January 2020

Abstract: The digital low drop-out regulator (LDO) has been used widely in digital circuits for its low supply voltage characteristics. However, as the traditional digital LDOs regulate the output voltage code at a rate of 1 bit per clock cycle, the transient response speed is limited. This paper presents a digital LDO to improve transient response speed with a multi-bit conversion technique. The proposed technology uses a voltage sensor and a time-to-digital converter to convert the output voltage to digital codes. Based on a 65-nm CMOS process, the proposed DLDO reduces the settling time from 147.8 ns to 25.2 ns on average and the response speed is improved by about six times.

Keywords: low drop-out regulator; digital control; fast response; embedded power management

1. Introduction

Process scaling causes the continuous reduction in supply voltage. In particular, the application of the Internet of things (IoT) makes the low operating supply voltage more important than ever. In such conditions, dynamic range and bandwidth of integrated circuits are reduced, thus the stability is harder to control. The fine-grained supply voltage management faces a real challenge. In contrast to analog low drop-out regulator (LDO), digital LDOs (DLDO) exhibiting ultra-low operating voltage [1–6]. Hence, the DLDO has been widely used in the low source supply voltage conditions and digital load circuits.

The traditional DLDO employs a barrel shifter, whose output code switches 1 bit in a clock cycle [7]. When there is a large transient, it takes a long time to regulate the output voltage to the target value. Some studies have attempted to enhance the transient performance using adaptive regulation technology [8–13], but the circuit complexity increases obviously and the multiple times regulation is still required. In [14–16], DLDO with a flash analog-to-digital converter (ADC) is proposed. The ADC converts the output voltage to the digital domain and a digital controller provides a multi-bit regulation. Since the comparator offset increases the error of ADC, there may be a deviation in the regulation. In [17–19], a time-to-digital converter (TDC) is employed to replace ADC. To convert the output voltage to digital codes, the TDC alters the buffer-gate's propagation delay by changing the power supply of the buffer-gate. However, the relationship between the power supply and the propagation delay of buffer-gate is nonlinear, and the resolution of TDC is degraded. In this paper, a voltage sensor based on capacitor charging is introduced. Since the proposed TDC operates by changing the time intervals rather than buffer-gate's propagation delay, the linearity is improved. With a digital controller behind TDC, a multi-bit regulation is achieved and the transient response speed is increased.

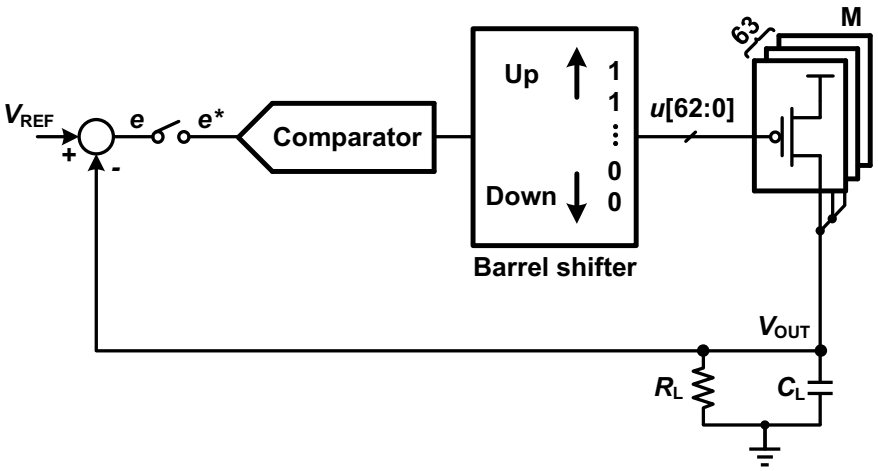
This paper is organized as follows. Inl Section 2, the fast response DLDO is proposed with circuit architecture and system dynamic model. Section 3 discusses the circuit implementation of the proposed

DLDO. In Section 4, the circuit performance is simulated and the simulation results are shown. Finally, conclusions are drawn in Section 5.

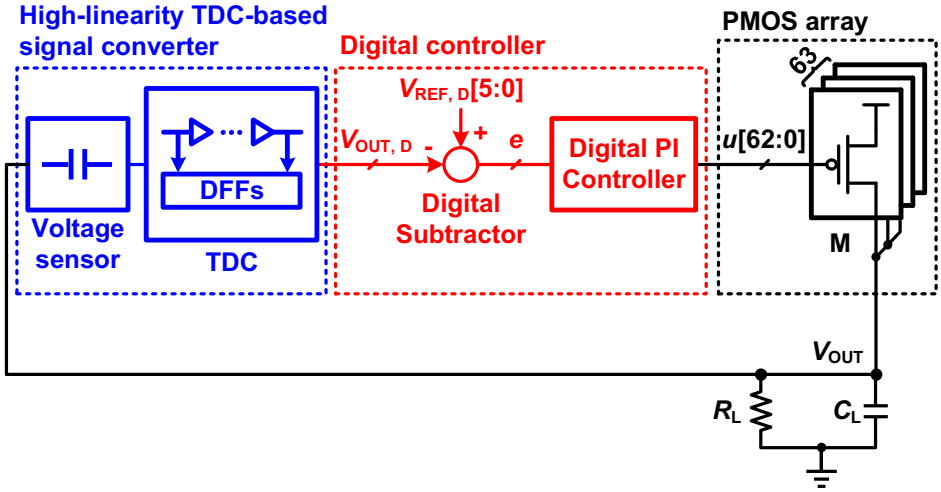
2. System Overview

2.1. The Architecture of the Proposed DLDO

Figure 1 shows circuit diagrams for the baseline DLDO and the proposed DLDO. The proposed DLDO consists of three components. The first component is the TDC-based signal converter, which provides a digital code of the output voltage V_{OUT} to a digital controller. As the second component, the digital controller outputs a regulation code to drive a PMOS array according to the different inputs. Finally, the PMOS array M provides appropriate current to regulate the V_{OUT}.



(a)



(b)

Figure 1. The circuit architecture of (**a**) baseline DLDO and (**b**) proposed DLDO.

In the TDC-based signal converter, a voltage sensor generates a time signal related to V_{OUT} by capturing the charging time of a capacitor. The TDC behind the voltage sensor converts the time signal to a digital code $V_{OUT,D}$. Subtracting $V_{OUT,D}$ from the reference voltage code $V_{REF,D}$, the digital subtractor produces an error value e and drives the digital PI controller to vary the number of turned-on transistors in M. When the error value e is 0, $V_{OUT,D}$ is equal to $V_{REF,D}$ and output voltage V_{OUT} is regulated to the target value.

In contrast to the conventional DLDO, the proposed circuit regulates its output voltage using a digital PI controller rather than a shift register. Hence, the number of turned-on transistors can be switched multi-bits in a clock cycle. A faster response is achieved in the proposed circuit.

2.2. System Hybrid Model

To understand the overall system behavior, a system hybrid model for the proposed DLDO is shown in Figure 2. The relationship between input and output of the TDC-based signal converter is rounding linearly and the TDC-based signal converter is modeled as a cascade between gain K_{TDC} and a rounding function. TDC-based signal converter operates periodically, and the rounding function is followed by a zero-order holder (ZOH). Since the digital PI controller accumulates the previous output of the digital subtractor, it acts as the superposition of a gain K_{p} and an ideal integrator in discrete-time. The power MOSFETs are driven by a digital circuit, and their parasitic gate capacitances affect the settling time. The effect is modeled as a time delay $\mathrm{e}^{-sT_{\mathrm{DEL}}}$, where T_{DEL} is the delay caused by the parasitic gate capacitances. The corresponding transfer function in the z-domain is $z^{-T_{\mathrm{DEL}}}$. The load and power MOSFETs can be approximated as an RC load with gain K_{DC}. The s-domain model of the load and power MOSFETs is

$$P(s) = \frac{K_{\mathrm{DC}}}{1 + \frac{s}{F_{\mathrm{LOAD}}}} \tag{1}$$

where F_{LOAD} is the output pole frequency and can be written as $F_{\mathrm{LOAD}} = 1/(2\pi \cdot R_{\mathrm{LOAD}} \cdot C_{\mathrm{LOAD}})$. The corresponding $P(z)$ in z-domain can be represented as

$$P(z) = \frac{K_{\mathrm{DC}} F_{\mathrm{LOAD}} z}{z - \mathrm{e}^{-F_{\mathrm{LOAD}}/F_{\mathrm{S}}}} \tag{2}$$

where F_{S} is the sampling frequency and $F_{\mathrm{S}} = 1/T$. Thus, the open-loop transfer function between $V_{\mathrm{REF,\,D}}$ and V_{OUT} can be written as

$$G(z) = K \cdot \frac{z^{1-T_{\mathrm{DEL}}} \left(z - \frac{K_{\mathrm{P}} - K_{\mathrm{I}}/F_{\mathrm{S}}}{K_{\mathrm{P}}}\right)}{(z-1)\left(z - \mathrm{e}^{-F_{\mathrm{LOAD}}/F_{\mathrm{S}}}\right)} \tag{3}$$

where the open-loop gain $K = K_{\mathrm{DC}} K_{\mathrm{P}} F_{\mathrm{LOAD}}$. Taking the TDC-based signal converter and the zero-order holder into account, the entire closed-loop transfer function of the proposed DLDO in z-domain is

$$Q(z) = \frac{K \cdot z^{1-T_{DEL}} \left(z - \frac{K_{\mathrm{P}} - K_{\mathrm{I}}/F_{\mathrm{S}}}{K_{\mathrm{P}}}\right)}{z^2 + K_{\mathrm{TDC}} K z^{2-T_{\mathrm{DEL}}} - \left(1 + \mathrm{e}^{-F_{\mathrm{LOAD}}/F_{\mathrm{S}}}\right) z - \left(K_{\mathrm{TDC}} K \frac{K_{\mathrm{P}} - K_{\mathrm{I}}/F_{\mathrm{S}}}{K_{\mathrm{P}}}\right) z^{1-T_{\mathrm{DEL}}} + \mathrm{e}^{-F_{\mathrm{LOAD}}/F_{\mathrm{S}}}} \tag{4}$$

Because T_{DEL} is much smaller than 1, Equation (4) can be approximated to

$$Q(z) = \frac{K \cdot z \left(z - \frac{K_{\mathrm{P}} - K_{\mathrm{I}}/F_{\mathrm{S}}}{K_{\mathrm{P}}}\right)}{(1 + K_{\mathrm{TDC}} K) z^2 - \left(1 + \mathrm{e}^{-F_{\mathrm{LOAD}}/F_{\mathrm{S}}} + K_{\mathrm{TDC}} K \frac{K_{\mathrm{P}} - K_{\mathrm{I}}/F_{\mathrm{S}}}{K_{\mathrm{P}}}\right) z + \mathrm{e}^{-F_{\mathrm{LOAD}}/F_{\mathrm{S}}}} \tag{5}$$

Equation (5) provides insights into the stability of the proposed DLDO. Compared with the transfer function of the traditional DLDO in [20], the PI controller produces an extra zero at $z = (K_{\mathrm{P}} - K_{\mathrm{I}}/F_{\mathrm{S}})/K_{\mathrm{P}}$. The bandwidth and transient response speed of the proposed system are increased.

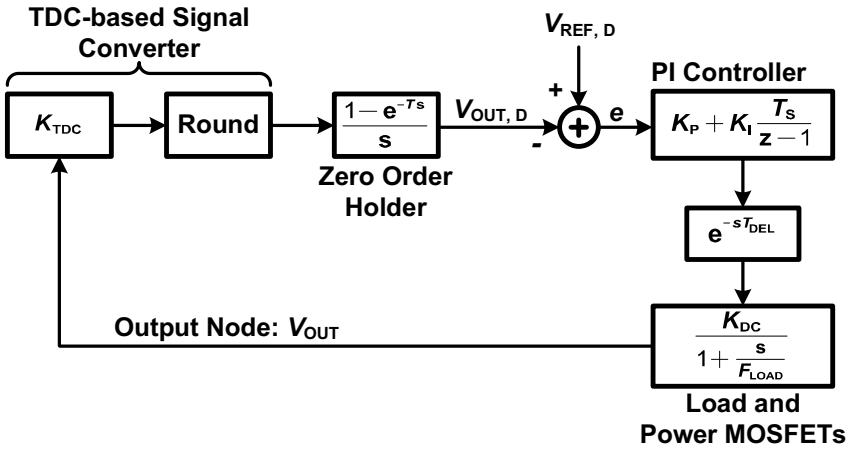
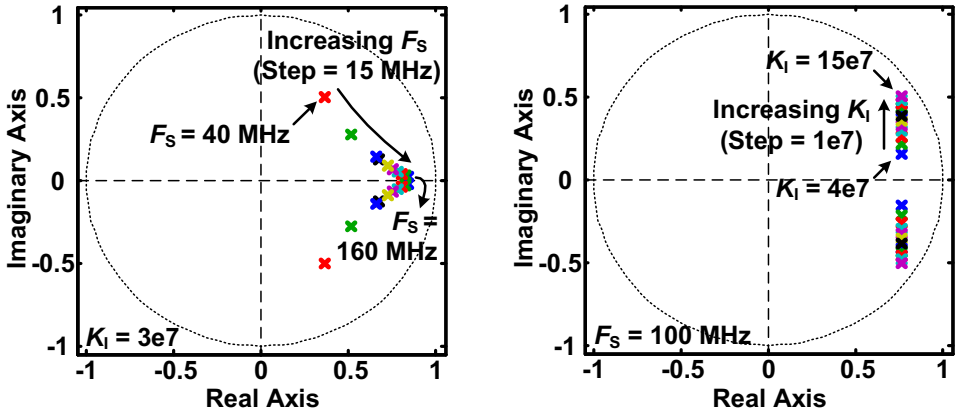


Figure 2. The system hybrid model for the proposed DLDO.

Figure 3 shows the pole plots of the proposed system under different sampling frequency and integration gain conditions. The simulation parameters are listed in Table 1. As illustrated in the plots, a large sampling frequency damages the system stability. In addition, the higher integration gain of the digital PI controller leads to decreasing stability. Hence, large F_S and K_I should be avoided in the selection of parameters. In Figure 4, the pole plots of the proposed system under variable load are shown and the simulation parameters in Table 1 are used. As illustrated in the plots, the increasing load resistance, which results in a lower load current, reduces the stability of the proposed system. Meanwhile, the decreasing load capacitance degrades the system stability as well. When the load capacitance is decreased to 13 pF, the pole is close to the unit circle, and the system is in critical stability.



(a) (b)

Figure 3. The pole plot of the proposed system under: (**a**) variable sampling frequency; and (**b**) variable integration gain.

Table 1. The simulation parameters of the system hybrid model.

K_P	K_{TDC}	K_{DC}	R_{LOAD}	C_{LOAD}	F_{LOAD}	T_{DEL}
1	38	0.02	10 Ω	500 pF	32 MHz	10 ps

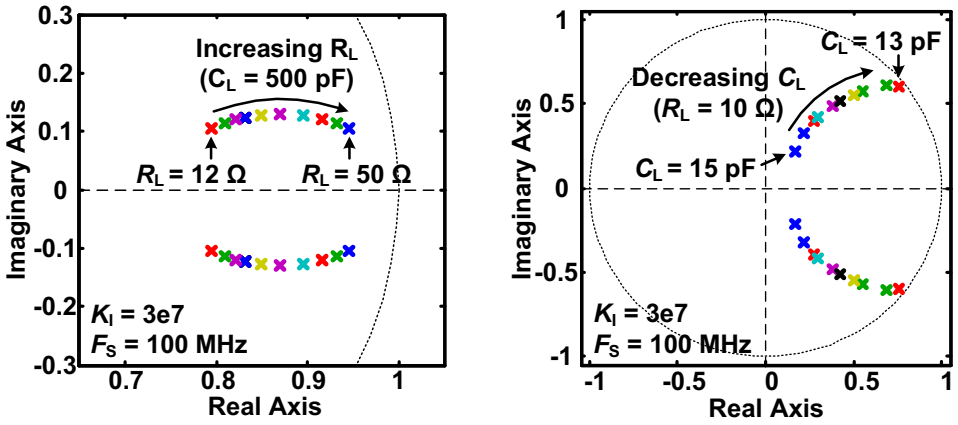


Figure 4. The pole plot of the proposed system under: (**a**) variable load resistance; and (**b**) variable load capacitance.

3. Circuit Implementation

3.1. Voltage Sensor

The transformation of the output voltage from analog to digital is achieved by a TDC-based signal converter, which contains a voltage sensor and a time-to-digital converter. Figure 5 illustrates the circuit scheme of the voltage sensor. During phase ϕ_1, two plates of the charge capacitor C_C are pre-charge to V_{OUT} and V_{IL}, respectively, where V_{IL} is the acceptable high level of the buffer-gate in TDC. After the capacitor is pre-charged, the voltage difference between node A and node B is $(V_{OUT} - V_{IL})$. At the moment the phase is switched, node A is connected to ground. Because the voltage difference between the two plates of a capacitor does not change suddenly, the voltage of node B is $(V_{IL} - V_{OUT})$. During phase ϕ_2, node B is charged by a constant current source I, which is supplied by a PMOS of a current mirror. Since V_{IL} is usually lower than half the supply voltage, the source-drain voltage of the PMOS is large enough and the PMOS operates in the saturation region. Under such a condition, the drain current is slightly affected by the source-drain voltage. Hence, the linearity of the voltage sensor is not greatly affected by the change of the voltage of node B. The charging current I is stable in the range of concern.

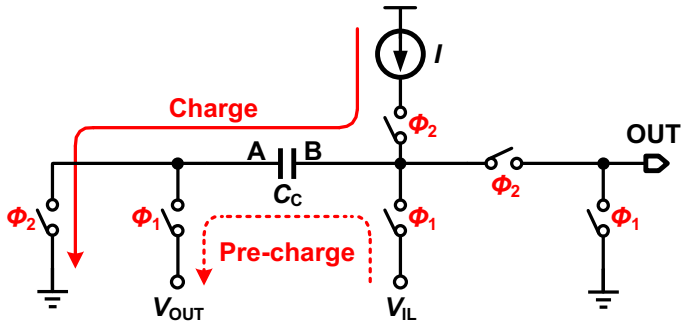


Figure 5. The circuit scheme of the voltage sensor.

When the voltage of node B rises to V_{IL}, the voltage level turns to logic "1" and the TDC is triggered. During the process, the charge variation in C_C can be expressed as

$$\Delta Q_C = I \cdot \Delta t \tag{6}$$

where Δt is the time interval of node B is charged from ($V_{IL} - V_{OUT}$) to V_{IL}. Meanwhile, the voltage variation of node B is [V_{IL}-(V_{IL}-V_{OUT})]. The relationship between ΔQ_C and the voltage change during Δt is

$$\Delta Q_C = C_C \cdot [V_{IL} - (V_{IL} - V_{OUT})] \tag{7}$$

Combining Equations (6) and (7), Δt can be expressed as

$$\Delta t = \frac{C_C}{I} V_{OUT} \tag{8}$$

Hence, the output voltage is converted to a time interval by varying the initial voltage of C_C.

In the voltage sensor, a parasitic capacitance exists in the capacitor C_C, which causes a slight change of about 20–30 fF in C_C. In the proposed circuit, the charging capacitance is 250 fF, which is much larger than the parasitic capacitance. Because the resolution of the proposed 6-bit TDC-based voltage converter is about 25 mV, the circuit response is not modified by the slight fluctuation of C_C.

3.2. Time-to-Digital Converter

The circuit scheme of the time-to-digital converter is shown in Figure 6. As an all digital circuits, TDC is implemented by logical synthesis. The input ports of the TDC are connected to the clock ϕ and the output of the voltage sensor. In the delay line, the propagated time of each buffer is t_d. Figure 7 shows the timing diagram of the TDC-based signal converter. At the beginning of phase ϕ_2, signal "1" is transmitted in the delay line. When the voltage sensor generates a positive edge, the D flip-flops are triggered, and ports D_i (i = 1, 2, $\cdots$, n) output the voltage level of node P_i (i = 1, 2, $\cdots$, n). The number of buffers transmitted by signal "1" is $N = [\Delta t / t_d]$. According to Equation (8),

$$N = \left[\frac{C_C}{I \cdot t_d} V_{OUT} \right] \tag{9}$$

Using the voltage sensor and TDC, the transformation of V_{OUT} from analog to digital can be achieved.

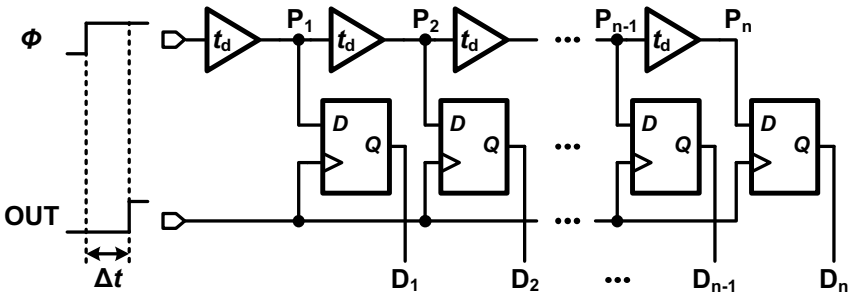


Figure 6. The circuit scheme of the time-to-digital converter.

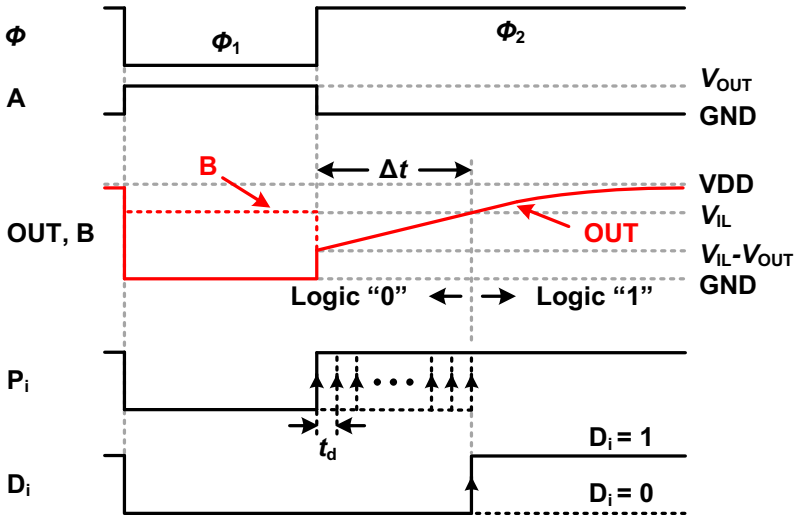


Figure 7. The timing diagram of the TDC-based signal converter.

3.3. Digital Controller

The delay line in TDC outputs a 64-bit thermometer-coded digital signal $V_{\mathrm{OUT,D}}$. The digital subtractor subtracts the temperature code from the reference voltage $V_{\mathrm{REF,D}}$ and outputs an error value e. Driven by the error value, the output of the digital PI controller at kth clock cycle can be expressed as

$$u(k) = K_{\mathrm{P}} e(k) + K_{\mathrm{I}} \sum_{j=0}^{k} e(j) \tag{10}$$

When there is a steady-state error, $V_{\mathrm{OUT,D}}$ is not equal to the $V_{\mathrm{REF,D}}$ and the output of digital subtractor is non-zero. Under such a condition, the accumulative component of Equation (10) causes the PI to output a variable value. The digital code $V_{\mathrm{OUT,D}}$ is forced to approach the $V_{\mathrm{REF,D}}$ until steady-state error is eliminated. When the circuit is stable, $V_{\mathrm{OUT,D}}$ is equal to the $V_{\mathrm{REF,D}}$ and the output of the digital subtractor is 0. Since the accumulative component of the digital PI controller no longer changes, a stable voltage is outputted continuously.

4. Simulation and Results

4.1. TDC-Based Signal Converter

The proposed fast response DLDO was realized in a 65-nm TSMC technology. It occupies an active area of 0.017 mm^2 and the layout is shown in Figure 8. The current injection of the switches in the TDC-based voltage converter introduces the voltage errors to the output voltage of switches. To describe the effect, the voltage errors were measured and the results are shown in Figure 9. In the circuit, the charging capacitor is 250 fF and the charging current I is 120 µA. According to the results, the current injection causes the positive errors at node A and node B under different V_{OUT} conditions. The resolution of the proposed TDC-based voltage converter is about 25 mV, which is larger than the maximum voltage error. Hence, the current injection will not affect the accuracy of the proposed circuit. Figure 10 shows the comparison of linearity between the conventional TDC and the proposed TDC. The test points are fitted into a quadratic function. According to the fitting results, the coefficients of the quadratic term of the conventional TDC and the proposed TDC are -47.1 and -2.8×10^{-14}, respectively. Relative to the conventional TDC, the performance of linearity is improved in the proposed design.

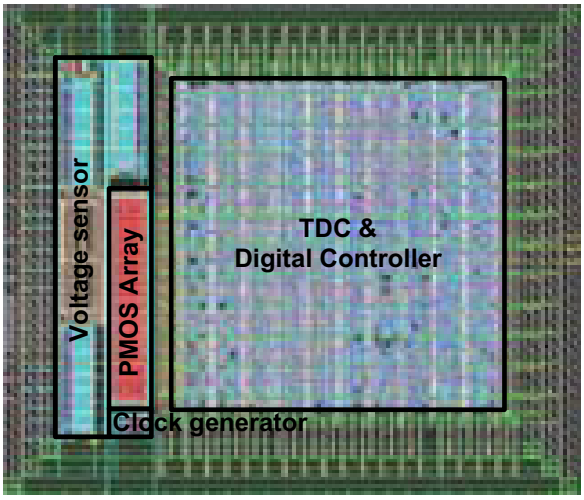


Figure 8. The layout of the proposed fast response DLDO.

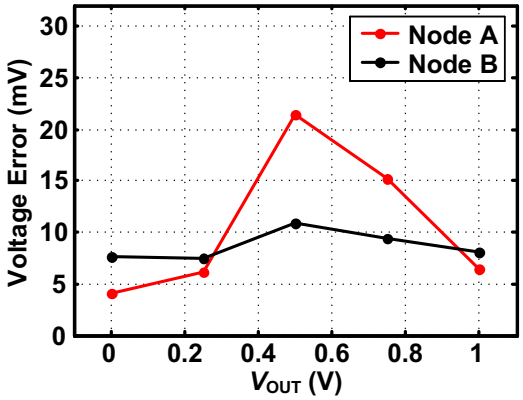
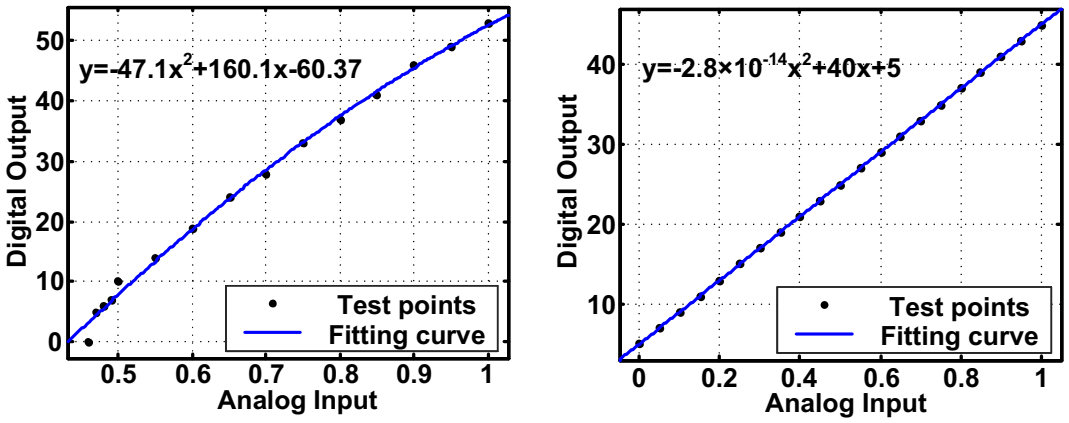


Figure 9. The voltage error caused by the current inject of switches.



(a) (b)

Figure 10. The comparison of linearity for: (**a**) conventional TDC; and (**b**) proposed TDC.

4.2. Proposed DLDO

To describe the transient response speed of the proposed circuit, the settling time T_S with variable load was simulated. The settling time is defined as the time of the output voltage recovers to 90% of

the droop voltage. As shown in Figure 11, the proposed DLDO reduces the settling time under each condition. The settling time is decreased to only 17.1% of the baseline design of DLDO (from 147.8 ns to 25.2 ns) on average. In other words, the proposed circuit improves the response speed by about six times. Under the variations of sampling frequency and load current, the settling time was evaluated as well. In Figure 12, the increasing sampling frequency results in a shorter T_S. The settling time when f_S = 100 MHz is about half that of f_S = 50 MHz. Compared with the heavy load condition, settling time is shorter in the light load condition under each frequency.

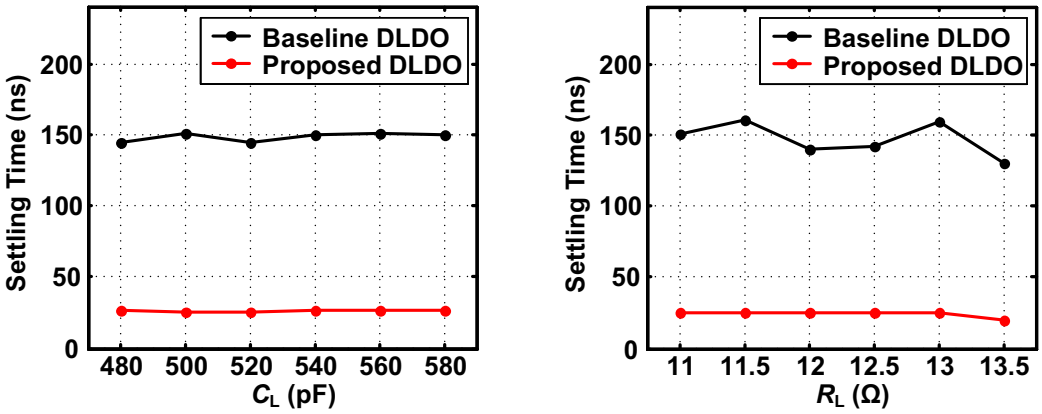


Figure 11. The settling time when: (**a**) load resistance is 11 Ω; and (**b**) load capacitance is 500 pF.

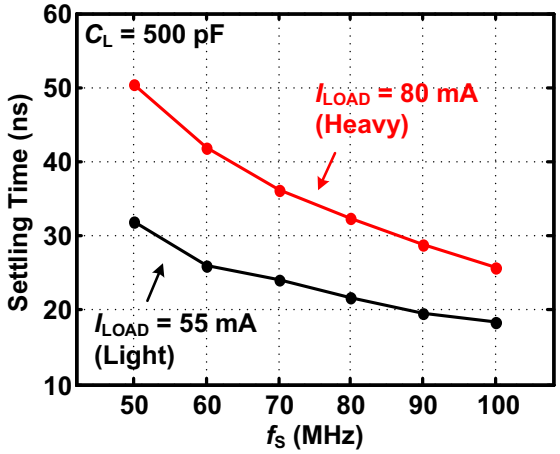


Figure 12. The settling time under the variations of sampling frequency and load current.

Figure 13 shows the measured transient responses of the baseline DLDO and the proposed DLDO with a load step of 80 mA. With V_{IN} = 1 V, V_{OUT} = 0.85 V (step up) or V_{OUT} = 0.65 V (step down), f_S = 100 MHz and C_L = 500 pF, we measured a 25 ns (step up) or 64 ns (step down) settling time. Compared with the baseline case, the proposed DLDO shows a significantly faster settling time. The output voltage is measured for a target voltage of from 0.95 to 0.65 V with V_{IN} ranging from 0.7 to 1.1 V. As shown in Figure 14, the effect of the line voltage on the output voltage is slight. A line regulation of 15 mV/V is achieved. The output voltage with a load current range from 55 to 85 mA is measured. As shown in Figure 15, the circuit regulates the output voltage from 0.95 to 0.65 V, and a load regulation of <0.8 mV/mA is achieved. A performance comparison with published DLDO is given in Table 2, which includes both the ALDO and DLDO. In comparison to those prior designs in Table 2, this paper achieves the shortest response time, the best figure of merit (FOM) of speed [21], and competitive current efficiency.

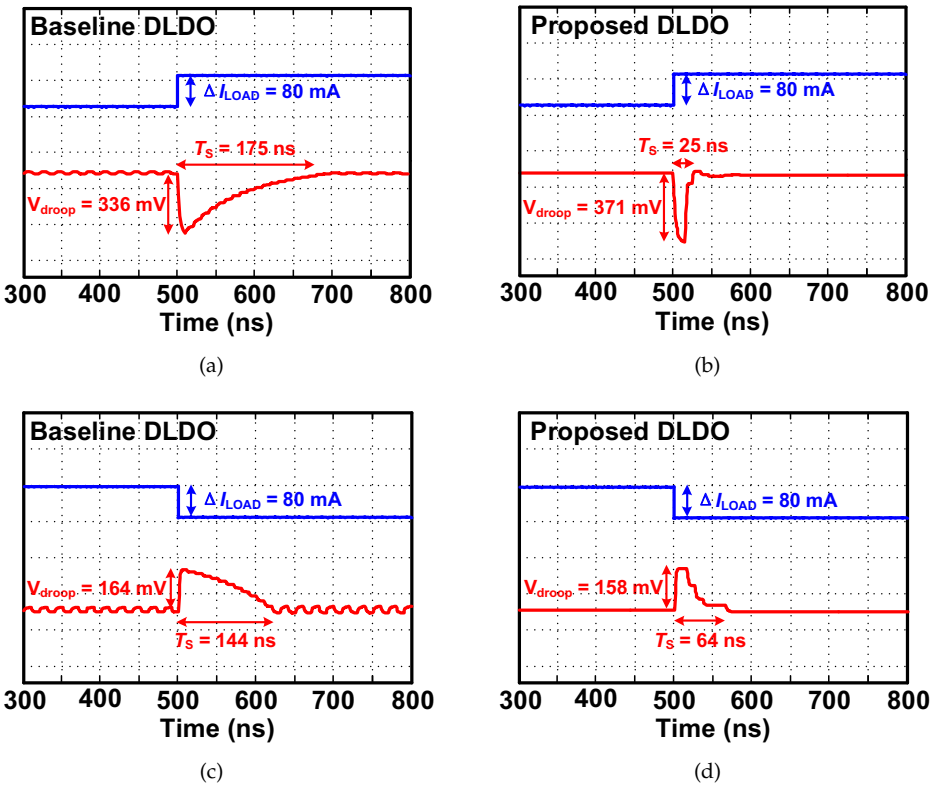


Figure 13. The measured transient responses of the baseline DLDO and the proposed DLDO for a load: step up (**a**,**b**); and step down (**c**,**d**).

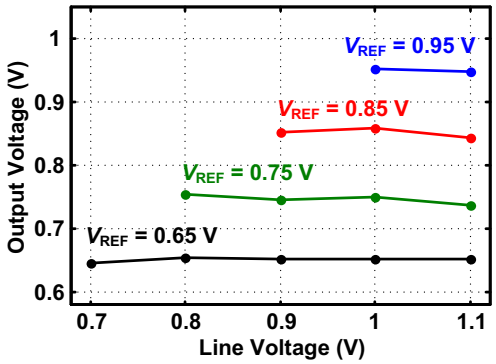


Figure 14. The output voltage under the variations of line voltage.

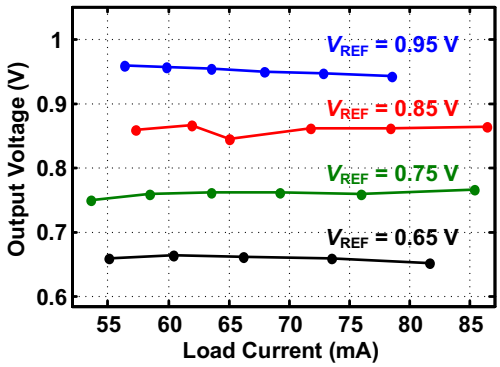


Figure 15. The output voltage under the variations of load current.

Table 2. Comparison with published LDO designs.

Paper	2015 [22]	2018 [23]	2019 [24]	2018 [25]	This Work
Type	Analog	Digital	Analog	Digital	Digital
Process	180 nm	65 nm	55 nm	65 nm	65 nm
Active area [mm^2]	0.021	NA	0.042	0.012	0.017
V_{IN} [V]	1.3–1.8	0.8–1	<0.8	0.5–1	0.7–1.1
V_{OUT} [V]	1.2	0.75–0.95	0.6	0.35–0.95	0.65–1.05
Quiescent I_Q [μA]	10	24	0.016	45.2	495
I_{MAX} [mA]	25	13	10	2.8	120
Peak current efficiency η [%]	99.9	99.8	99.8	98.4	99.6
Line regulation [mV/V]	0.5	NA	0.5	NA	15
Load regulation [mV/mA]	0.14	NA	1.05	NA	0.6
Load capacitor C_L [nF]	4700	0.2	1000	0.1	0.5
Max voltage droop [mV] @	2 @	100 @	70 @	46 @	371 @
Load step	25 mA	6 mA	10 mA	1.76 mA	80 mA
Response time T_R * [ns]	376	3.3	7000	2.63	2.1
FOM ** [ps]	150	13.3	11.4	67.1	8.7

* $T_R = C_L * V_{droop}/I_{MAX}$; ** FOM = $T_R * I_Q/I_{MAX}$.

5. Conclusions

This paper presents a fast response DLDO with a TDC-based signal converter for decreasing the settling time. The voltage sensor and TDC convert the output voltage from analog to digital. The digital controller provides a multi-bit regulation and improves transient response performance. The simulation results show that the proposed fast response DLDO can decrease the settling time to 17.1% of the baseline design of DLDO on average, and a FOM of 8.7 ps is achieved.

Author Contributions: Conceptualization, H.Z., J.G., and Z.C.; Data curation, P.W. and Z.L; Investigation, J.G. and Z.L.; Methodology, H.Z. and J.G.; Resources, P.W. and Z.C.; Writing—original draft, H.Z.; and Writing—review and editing, P. W. and Z.C. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by Beijing Natural Science Foundation Project No.4184083, and National Natural Science Foundation of China, Key Project No.61731019.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Ma, X.; Lu, Y.; Martins, R.P.; Li, Q. A 0.4 V 430nA quiescent current NMOS digital LDO with NAND-based analog-assisted loop in 28 nm CMOS. In Proceedings of the 2018 IEEE International Solid-State Circuits Conference-(ISSCC), San Francisco, CA, USA, 11–15 February 2018; pp. 306–308.
2. Oh, T.J.; Hwang, I.C. A 110-nm CMOS 0.7-V input transient-enhanced digital low-dropout regulator with 99.98% current efficiency at 80-mA load. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2014**, *23*, 1281–1286. [CrossRef]
3. Li, Y.; Zhang, X.; Zhang, Z.; Lian, Y. A 0.45-to-1.2-V fully digital low-dropout voltage regulator with fast-transient controller for near/subthreshold circuits. *IEEE Trans. Power Electron.* **2015**, *31*, 6341–6350. [CrossRef]
4. Yang, F.; Mok, P.K. A nanosecond-transient fine-grained digital LDO with multi-step switching scheme and asynchronous adaptive pipeline control. *IEEE J. Solid-State Circuits* **2017**, *52*, 2463–2474. [CrossRef]
5. Huang, M.; Lu, Y.; Seng-Pan, U.; Martins, R.P. An output-capacitor-free analog-assisted digital low-dropout regulator with tri-loop control. In Proceedings of the 2017 IEEE International Solid-State Circuits Conference-(ISSCC), San Francisco, CA, USA, 5–9 February 2017; pp. 342–343.
6. Salem, L.G.; Warchall, J.; Mercier, P.P. A 100 nA-to-2 mA successive-approximation digital LDO with PD compensation and sub-LSB duty control achieving a 15.1 ns response time at 0.5 V. In Proceedings of the 2017 IEEE International Solid-State Circuits Conference-(ISSCC), San Francisco, CA, USA, 5–9 February 2017; pp. 340–341.

7. Okuma, Y.; Ishida, K.; Ryu, Y.; Zhang, X.; Chen, P. H.; Watanabe, K.; Sakurai, T. 0.5-V input digital LDO with 98.7% current efficiency and 2.7-μA quiescent current in 65nm CMOS. In Proceedings of the IEEE Custom Integrated Circuits Conference, San Jose, CA, USA, 19–22 September 2010; pp. 1–4.
8. Lee, J.; Bang, J.; Lim, Y.; Choi, J. A 0.5 VV IN, 0.29 ps-Transient-FOM, and Sub-2mV-Accuracy Adaptive-Sampling Digital LDO Using Single-VCO-Based Edge-Racing Time Quantizer. In Proceedings of the 2019 Symposium on VLSI Circuits, Kyoto, Japan, 9–14 June 2019; pp. C130–C131.
9. Nasir, S.B.; Gangopadhyay, S.; Raychowdhury, A. A 0.13 μm fully digital low-dropout regulator with adaptive control and reduced dynamic stability for ultra-wide dynamic range. In Proceedings of the 2015 IEEE International Solid-State Circuits Conference-(ISSCC), San Francisco, CA, USA, 22–26 February 2015; pp. 1–3.
10. Kundu, S.; Liu, M.; Wong, R.; Wen, S.J.; Kim, C.H. A fully integrated 40 pF output capacitor beat-frequency-quantizer-based digital LDO with built-in adaptive sampling and active voltage positioning. In Proceedings of the 2018 IEEE International Solid-State Circuits Conference-(ISSCC), San Francisco, CA, USA, 11–15 February 2018; pp. 308–310.
11. Nasir, S.B.; Sen, S.; Raychowdhury, A. Switched-mode-control based hybrid LDO for fine-grain power management of digital load circuits. *IEEE J. Solid-State Circuits* **2017**, *53*, 569–581. [CrossRef]
12. Tsou, W.J.; Yang, W.H.; Lin, J.H.; Chen, H.; Chen, K.H.; Wey, C.L.; Tsai, T.Y. Digital low-dropout regulator with anti PVT-variation technique for dynamic voltage scaling and adaptive voltage scaling multicore processor. In Proceedings of the 2017 IEEE International Solid-State Circuits Conference-(ISSCC), San Francisco, CA, USA, 5–9 February 2017; pp. 338–339.
13. Kundu, S.; Liu, M.; Wen, S.J.; Wong, R.; Kim, C.H. A Fully Integrated Digital LDO With Built-In Adaptive Sampling and Active Voltage Positioning Using a Beat-Frequency Quantizer. *IEEE J. Solid-State Circuits* **2018**, *54*, 109–120. [CrossRef]
14. Kim, D.; Seok, M. A fully integrated digital low-dropout regulator based on event-driven explicit time-coding architecture. *IEEE J. Solid-State Circuits* **2017**, *52*, 3071–3080. [CrossRef]
15. Kim, D.; Kim, J.; Ham, H.; Seok, M. A 0.5 VV IN 1.44 mA-class event-driven digital LDO with a fully integrated 100 pF output capacitor. In Proceedings of the 2017 IEEE International Solid-State Circuits Conference-(ISSCC), San Francisco, CA, USA, 5–9 February 2017; pp. 346–347.
16. Ding, Z.; Xu, X.; Song, H.; Rhee, W.; Wang, Z. Flash ADC-based digital LDO with non-linear decoder and exponential-ratio array. *Electron. Lett.* **2019**, *55*, 585–587. [CrossRef]
17. Lim, C.; Mandal, D.; Bakkaloglu, B.; Kiaei, S. A 50-mA 99.2% peak current efficiency, 250-ns settling time digital low-dropout regulator with transient enhanced PI controller. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2017**, *25*, 2360–2370. [CrossRef]
18. Otsuga, K.; Onouchi, M.; Igarashi, Y.; Ikeya, T.; Morita, S.; Ishibashi, K.; Yanagisawa, K. An on-chip 250 mA 40 nm CMOS digital LDO using dynamic sampling clock frequency scaling with offset-free TDC-based voltage sensor. In Proceedings of the 2012 IEEE International SOC Conference, Falls, NY, USA, 12–14 September 2012; pp. 11–14.
19. Ojima, N.; Nakura, T.; Iizuka, T.; Asada, K. A synthesizable digital low-dropout regulator based on voltage-to-time conversion. In Proceedings of the 2018 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), Verona, Italy, 8–10 October 2018; pp. 55–58.
20. Nasir, S.B.; Gangopadhyay, S.; Raychowdhury, A. All-digital low-dropout regulator with adaptive control and reduced dynamic stability for digital load circuits. *IEEE Trans. Power Electron.* **2016**, *31*, 8293–8302. [CrossRef]
21. Hazucha, P.; Karnik, T.; Bloechel, B.A.; Parsons, C.; Finan, D.; Borkar, S. Area-efficient linear regulator with ultra-fast load regulation. *IEEE J. Solid-State Circuits* **2005**, *40*, 933–940. [CrossRef]
22. Chen, L.; Cheng, Q.; Guo, J.; Chen, M. High-PSR CMOS LDO with embedded ripple feedforward and energy-efficient bandwidth extension. In Proceedings of the 2015 28th IEEE International System-on-Chip Conference (SOCC), Beijing, China, 8–11 September 2015; pp. 384–389.
23. Ding, Z.; Rhee, W.; Wang, Z. A VCO-dedicated digital LDO with multi-comparator coarse loop and 1-bit ΔΣ fine loop for robust frequency generation. In Proceedings of the 2018 IEEE MTT-S International Wireless Symposium (IWS), Chengdu, China, 6–10 May 2018; pp. 1–4.

24. Adorni, N.; Stanzione, S.; Boni, A. A 10-mA LDO With 16-nA IQ and Operating From 800-mV Supply. *IEEE J. Solid-State Circuits* **2019**, 1–10. [CrossRef]
25. Kim, S. J.; Kim, D.; Ham, H.; Kim, J.; Seok, M. A 67.1-ps FOM, 0.5-V-hybrid digital LDO with asynchronous feedforward control via slope detection and synchronous PI with state-based hysteresis clock switching. *IEEE Solid-State Circuits Lett.* **2018**, *1*, 130–133. [CrossRef]

© 2020 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/).