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A Non-Dissipative Equalizer with Fast Energy Transfer Based on Adaptive Balancing Current Control †

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Abstract: In this study, an active inductive equalizer with fast energy transfer based on adaptive balancing current control is proposed to rapidly equilibrate lithium-ion battery packs. A multiphase structure of equalizer formed by many specific parallel converter legs (PCLs) with bidirectional energy conversion serves as the power transfer stage to make the charge shuttle back and forth between the cell and sub-pack or sub-pack and sub-pack more flexible and efficient. This article focuses on dealing with the problem of slow balancing rate, which inherently arises from the reduction of balancing current as the voltage difference between the cells or sub-packs decreases, especially in the later period of equalization. An adaptive varied-duty-cycle (AVDC) algorithm is put forward here to accelerate the balance process. The devised method has taken the battery nonlinear behavior and the nonideality of circuit component into consideration and can adaptively modulate the duty cycle with the change of voltage differences to maintain balancing current nearly constant in the whole equilibrating procedure. Test results derived from simulations and experiments are provided to demonstrate the validity and effectiveness of the equalizer prototype constructed. Comparing with the conventional fixed duty cycle (FDC) method, the improvements of 68.3% and 8.3% in terms of balance time and efficiency have been achieved.

Keywords: bidirectional energy transfer; equalizer; lithium-ion battery; varied-duty-cycle method

1. Introduction

Groups of battery cells arranged in connection of series and/or parallel to constitute a battery energy storage system (BESS) have been widely used in many emerging industrial applications, such as all kinds of renewable energy generation systems and various types of electric vehicles (EVs), in which there is a need to fill the requirements for high power and/or high voltage [1–4]. A modern BESS must be equipped with a reliable and effective battery management system (BMS) to ensure that the BESS itself and its powered loads can work normally and safely [5,6]. Functionalities like cell protection, charge control, state of charge (SOC)/state of health (SOH) determination, cell equalization, and communications, etc., must be involved in a BMS to achieve the main objectives, e.g., protect the battery from destruction, retain the battery in meeting the requirements of application specified, and extend the lifetime of the battery [7,8]. Among them, battery balance dominates the battery

lifespan and cost-effectiveness in particular. The strict battery screening process [9] is usually done by manufacturers to sort cells with similar SOCs by the test of open circuit voltage (OCV) when making multi-cell packs. However, there exists a subtle discrepancy in electrochemical characteristics among different cells in a string owing to the manufacturing and environment variance, self-discharge rates, and inhomogeneous degradation with aging [10–12]. Battery inconsistencies usually reveal a mismatch in internal resistance, voltage, or capacity imbalances after charging and discharging cycles [12,13]. These mismatches will severely lose the energy supply efficacy and reliability, available longevity, safety of the battery pack, and greatly raise the cost of investment and maintenance as well [13,14].

Weak cells, i.e., cells with lower capacity or higher internal impedance, become overstressed during charging, which causes them to be weakened further by continuous overcharge cycles until they eventually fail to result in premature failure of the battery pack. Similarly, during discharging, the weak cells will hit the limit of the cell under-voltage protection earlier while the pack is still sufficient to power the load, thus the pack capacity cannot be fully utilized. Cell equalization is an effective way of compensating for weak cells and providing safer pack solutions to extend battery run time and lifespan as well. In the last decade, considerable balancing architectures with various balancing strategies have been proposed in the literature [15–21] to solve the problem of cell imbalance. Based on the energy transfer manner, the equalizer is divided into passive and active types [22–24]. The passive type, also known as "resistor bleeding balancing," achieves equalization using shunt resistors to dissipate surplus energies stored in cells with high voltage. It is simple in structure and easy to control. Nevertheless, the large energy consumption leads to heat dissipation, making the passive method inefficient and inapplicable to use during discharge. In addition, based on the energy transfer mode, the realizable ways for active equalizers include capacitive, inductive, and transformer-isolated types [25,26]. Namely, it can be subdivided into switched-capacitor (SC)-based [27,28], converter-based [16–19], and transformer- or inductor-based [20,21,29,30] solutions. Active balancers reach cell equilibrium by transferring energy from higher voltage cell(s) to the lower one(s), which can obtain fast and efficient balance compared with passive counterparts at the expense of bulky size as well as high control complexity and cost. The SC equalizer achieves the charge shuttle between cells using regular switching operation. Its structure is simple and control complexity is low, however, the connection between cells and the SC equalizer is not flexible, and the charge can only be shuttled between two adjacent cells, resulting in the significant increase in balance time required. Equalizers based on isolated or non-isolated switching converters transfer energy from a cell or group of cells to another cell or group of cells via the inductor or transformer. This type of balancer can perform the energy transfer through the converter, which owns more efficient equilibrium as compared with the passive one, but the whole architecture and control mechanism of this type of balancer is also more complicated and expensive. Enhancement of efficiency in the inductor-based equalizer with zero-voltage and/or zero-current switching has been proposed in References [31,32]. The topology of the inductor-based equalizer is simplified by minimizing the number of inductances and switches to save the space and cost of the transformer used in converter-based balancers [33]. The transformer-isolated equalizer is further classified into multi-transformer [29] and multi-secondary winding structures [34], which can equalize multiple cells in the same balancing period. However, the transformer or winding number is proportional to the number of the cell in series, which makes the entire size of the transformer-based equalizer too bulky and the complexities are also too high to equilibrate the battery pack with numerous cells connected in series. Even though the active type of equalizers can achieve more efficacy and faster equilibrium, the sophistication of the hardware configuration and control strategy will significantly increase as the number of cells in series massively increases. Hence, the concept of modularization balance has been addressed to tackle the balancing problem for battery stacks with a long string of cells [35–37]. On the other hand, the proper balancing strategy is also indispensable to control balance operation and address diverse situations during the entire equalization cycle regardless of the equalizer topology. The manipulation of balance can be formulated as optimization problems to make the desired pack performances best through the control of appropriate balancing algorithms. Thus, a new classified

way based on the output indices of equalization, objective functions to be optimized, and control approaches to reach balance quality factors has been proposed in Reference [38].

Consequently, the active balancing ways are suitable for most modern BESSs because its balance mechanism is not related to the chemistries and characteristics of the battery employed. However, as the equalization progresses, the balancing current will decrease as the voltage difference (ΔV_{diff}) between cells becomes smaller. This will induce the problem of slow balance rate in the later duration of the balancing cycle that has always been a challenging issue in the study of balancers. Accordingly, a non-dissipative active equalizer with fast energy transfer based on adaptive balancing current control is proposed in this paper to rapidly equilibrate lithium-ion battery packs. To make the charge shuttle back and forth between the cell and sub-pack or sub-pack and sub-pack more efficient and flexible, a multiphase architecture of equalizer, constructed by many parallel converter legs (PCLs) with bidirectional energy conversion via inductors, serves as the energy transfer power stage. This paper focuses on solving the problem of slow balancing speed induced by the diminution in balancing current owing to the gradual decrease in voltage difference between cells or sub-packs during the later period of equilibration in particular. In order to speed up the balance process and shorten the balance time needed, an adaptive varied-duty-cycle (AVDC) algorithm is presented in this study, which has taken the battery nonlinear characteristics and circuit parameter nonideality into account, to precisely calculate and adaptively modulate the duty cycle in real time with the change of the voltage difference between cells or sub-packs to keep the balancing current almost unchanged in the entire duration of the equilibration process.

Recently, the research on improvements in battery balancers mainly focused on the proposal of new balance control strategies or new balancer circuit architectures. However, there is often a situation where benefits of the hardware and software solutions cannot be achieved at the same time. That is, although a simple balancer topology presented can reduce requirements for space, cost, and reliability, it often needs to coordinate with sophisticated balance strategies which are realized on MCUs with high computational capability, thus the effectiveness of the balancer circuit adopted can be strengthened; conversely, simple and easy balance strategies often need to combine with high-complexity balancer architectures, thus the power and flexibility of the control strategies can be embodied. In order to bridge the gap, this paper devises a non-dissipative active equalizer with simple circuit topology and adaptive balancing current control to shorten the balance time. All PCLs used are connected to the same pack bus, this makes the monolithic or mixed integration of all power switches with gate drivers and auxiliary supplies possible. The topology features generalization and flexibility in the structure, as well as has the advantages of ease of expansion and modularization. As a result, the main contributions of this paper are that the proposed balancer is constructed by uncomplicated and reliable converters based on the control of a low-cost MCU with minimum computational effort, which avoids the need for more powerful and costly hardware or performance degradation due to the extra complexity and computation. Moreover, the adaptive varied-duty-cycle (AVDC) algorithm is presented to deal with the problem of the component non-ideality and nonlinearity. Thus, accurate battery and circuit models are not needed. Besides, an MCU with cost attraction can be selected to implement the devised scheme. This means the equalizer has good cost competitiveness, expandability, and modularity to equalize a battery string with more cells in series.

The rest of the paper is organized as follows. Section 2 introduces the topology and operating principle of the equalizer power stage. The system architecture studied is illustrated and the balancing control strategy proposed is derived in Section 3. In Section 4, the setup for experiment and measurement is specified, simulation and experimental results are shown to verify the proposed equalizer, and then comparisons with the conventional counterparts are also made to demonstrate the effectiveness and performance improvement of the proposed scheme. Finally, the conclusions of this paper are included in Section 5.

2. Operating Principle and Design of Equalizer Power Stage

2.1. Topology of the Power Stage Studied

Figure 1 shows the architecture of the studied equalizer power stage and its wiring scheme for a battery string with N cells in series. The equalizer power stage consists of $(N-1)$ parallel converter legs (PCLs). V_{pack} is the total voltage available across the battery string. This architecture enables the access to all available energy in the battery pack if the capacities stored in the cells are not identical. Due to the parallel nature of the topology, energies in a cell or sub-pack with high SOC can be transferred to any sub-pack or cell with low SOC under operations of charging, discharging, or idling the battery string. As shown in Figure 2a,b, each PCL is formed by a modified buck–boost converter with the operation mode of bidirectional continuous current, which deriving from replacing the diode and load resistor in the traditional buck–boost converter with an active switch and another cell or sub-pack voltage, serves as a basic converter leg unit of the adopted equalizer to make the charge shuttle back and forth between the cell and sub-pack or sub-pack and sub-pack realizable. The input voltage of each PCL may come from the voltage source of a certain cell or sub-pack in the battery string being balanced, and its output voltage may be the voltage source of the remaining certain cell or sub-pack of the battery string. Based on the topology of bidirectional buck–boost converters in parallel, it can be seen from Figure 1 that each phase PCL is connected at the potential available between two adjacent cells through an inductor, and the potential can be stably maintained and regulated to a fraction of the V_{pack}.

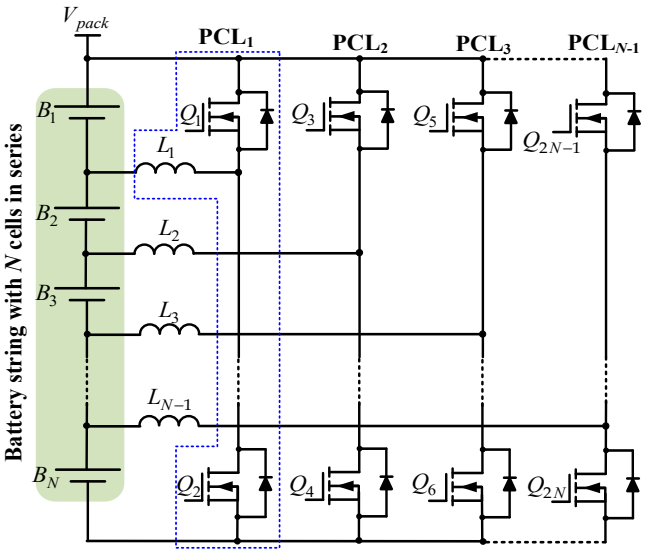


Figure 1. Architecture of the studied equalizer power stage with $(N-1)$ converter legs in parallel.

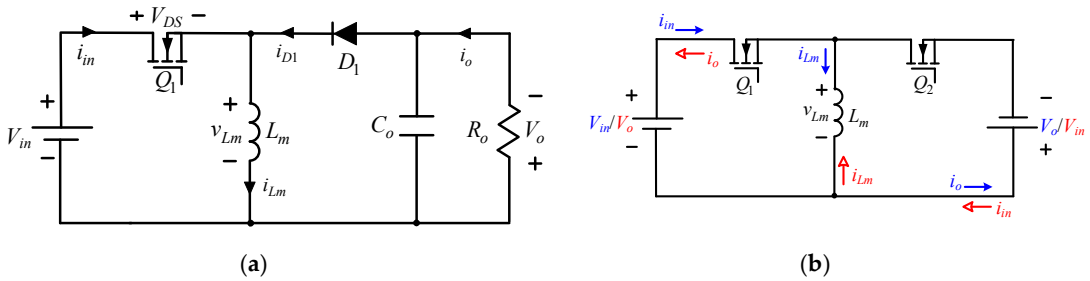


Figure 2. Development of the parallel converter leg (PCL): (**a**) Conventional buck–boost converter and (**b**) modified buck–boost converter with bidirectional energy transfer.

The equalizer topology is adapted to any battery pack as the number of the PCLs is $N-1$, where N is the number of the series-connected cells in a pack. For the configuration of multiple PCLs depicted in Figure 1, in the case of natural balancing control (or called a technique of fixed duty cycle (FDC) control balance), the high-side and low-side MOSFETs in each PCL_i ($i = 1, 2, \ldots, N-1$) are driven in complementary mode with a fixed duty cycle which is related to the input and output voltages applied to the leg, i.e., in a certain PCL, if the duty cycle of the high-side switch is D_{HQi}, then the duty cycle for the low-side switch, D_{LQi}, is $1 - D_{HQi}$, and vice versa. On one side of the inductor, a switching pattern with a fixed duty cycle will generate an average voltage equal to a fraction of the V_{pack}. If all cells are in equilibrium, the average voltage on the other side of the inductor is the same. If this is not the case, the inductor will have current flowing to balance the voltage between the cells on both sides. If there are m cells on the input side of a PCL, from Figure 2b, based on the principle that the inductor operation must maintain a volt-second balance, the duty cycle of the PCL can be derived as

$$D_m = \frac{V_{o-m}}{V_{in-m} + V_{o-m}} \tag{1}$$

in which D_m is the duty cycle of each PCL, and V_{o-m} and V_{in-m} are the input and output voltages of the PCL, which are specified respectively by

$$V_{in-m} = \sum_{j=1}^{m} V_{cell-j} \tag{2}$$

$$V_{o-m} = \sum_{j=m+1}^{N} V_{cell-j} \tag{3}$$

where m is the number of cells on the input side of PCL, $m \in \text{int}\,[1, N-1]$, and V_{cell-j} is the corresponding cell voltage. Under the FDC balancing control technique, in order to retain all cell voltages equal, Equations (2) and (3) can be substituted into Equation (1) to obtain the duty cycle value required for different input cell numbers, which can be expressed as

$$D_m = \frac{N-m}{N}. \tag{4}$$

2.2. Operating Principle

As per the aforementioned description, the equalizer employed here can achieve the balance of cell-to-sub-pack (C2SP) or sub-pack-to-cell (SP2C) and sub-pack-to-sub-pack (SP2SP) through the bidirectional energy transfer operated by the PCLs. Take the balancer for a battery string with four cells ($N = 4$) as an example: three PCLs are needed in this case to constitute the power stage of the equalizer. The specific balance strategy studied will be described in detail later. The operation principle under different balance modes is described as follows:

- C2SP or SP2C mode: From Figure 1, it can be observed that cell B_1 and sub-pack B_2-B_3-B_4 can transfer energy to each other bidirectionally to achieve the C2SP or SP2C balancing mode through the PCL_1, which is formed by the Q_1, Q_2, and L_1. When the average voltage of the sub-pack B_2-B_3-B_4 is less than the voltage of cell B_1, C2SP mode is activated. The PCL_1 is operated in boost mode to step up the cell voltage for output voltage regulation and releases its energy to charge the sub-pack through the inductor L_1. Figure 3a shows the equivalent circuit (EC) operated in subinterval 1, the switch Q_1 is turned on, Q_2 is turned off, and the B_1 energizes the L_1. In subinterval 2, the Q_2 is turned on and Q_1 is turned off, and the EC is shown in Figure 3b. At this time, the energy stored in L_1 in the former subinterval is transferred to the sub-pack. This C2SP mode mainly modulates the duty cycle of Q_1, the duty cycle of Q_2 is complementary to Q_1 and a proper dead time must be added to promise correct operation and avoid failure. On the other

hand, when the average voltage of the sub-pack is more than the B_1 voltage, the SP2C mode is actuated and the PCL_1 is operated in buck mode to step down the sub-pack voltage for output voltage regulation and releases its energy to charge the cell B_1. The operation flow of SP2C balance mode is opposite to C2SP mode, i.e., when in subinterval 1 operation, the switch Q_2 is turned on and Q_1 is turned off, and the sub-pack energizes L_1. The EC, as shown in Figure 5a, illustrates the energy flowing in this subinterval. Figure 5b shows the EC operated in subinterval 2, the switch Q_2 is turned off and Q_1 is turned on. At this time, the energy stored in L_1 in the previous subinterval is released to charge B_1 to complete the energy conversion. In SP2C mode, the duty cycle of Q_2 is modulated dominantly to maintain the correct process. The duty cycle of Q_1 is complementary to Q_2, and an appropriate dead time should also be inserted to avoid breakdown. Similarly, in this four-cell example, the SP2C or C2SP balance mode can also be done by the PCL_3, which is constituted by the Q_5, Q_6, and L_3, to transfer energy to each other bidirectionally between the sub-pack B_1-B_2-B_3 and cell B_4. The operating principle and analysis method are the same as that described above, so it will not be repeated.

- SP2SP mode: The energy stored in sub-pack B_1-B_2 or sub-pack B_3-B_4 can be transferred to each other through the bidirectional PCL_2 constructed by the Q_3, Q_4, and L_2 to achieve the SP2SP balance mode. When the average voltage of sub-pack B_3-B_4 is more than that of sub-pack B_1-B_2, SP2SP mode is triggered and the sub-pack B_3-B_4 releases its energy, through the inductor L_2 for energy exchange, to charge the other side sub-pack B_1-B_2. Figure 4a shows the EC operated in subinterval 1 in SP2SP mode, the switch Q_4 is turned on and Q_3 is turned off, and the B_3-B_4 energizes the inductor L_2. In subinterval 2, the switch Q_3 is turned on and Q_4 is turned off, and the EC is shown in Figure 4b. At this time, the energy stored in L_2 in the previous subinterval is released to charge the sub-pack B_1-B_2. In this SP2SP mode, the duty cycle of Q_4 is modulated mainly to dominate the energy conversion exactly. The duty cycle of Q_3 is regulated complementarily with Q_4, and a good dead time should be added to the switching period to achieve correct circuit operation and avoid malfunction. On the other hand, in the situation that the average voltage of the sub-pack B_3-B_4 is less than that of the sub-pack B_1-B_2, the SP2SP mode is still asserted, but in turn, the sub-pack B_1-B_2 discharges to energize the other side sub-pack B_3-B_4 through the control of PCL_2. Basically, the operating principles and analysis manners of these two balance modes are exactly the same as those mentioned above, except for the interchange of the input and output voltages and the main switch of regulating the duty cycle of the PCL_2, so it will not be described again.

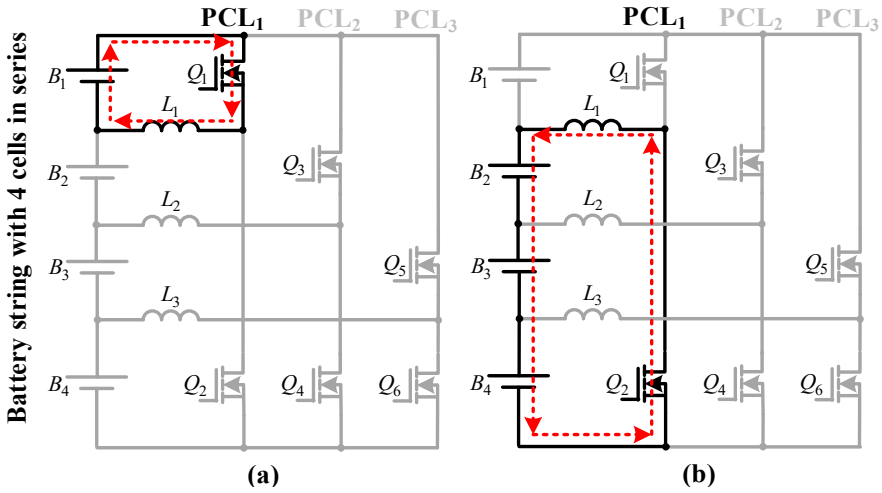


Figure 3. Operation of cell-to-sub-pack (C2SP) mode: (**a**) equivalent circuit (EC) of subinterval 1, (**b**) EC of subinterval 2.

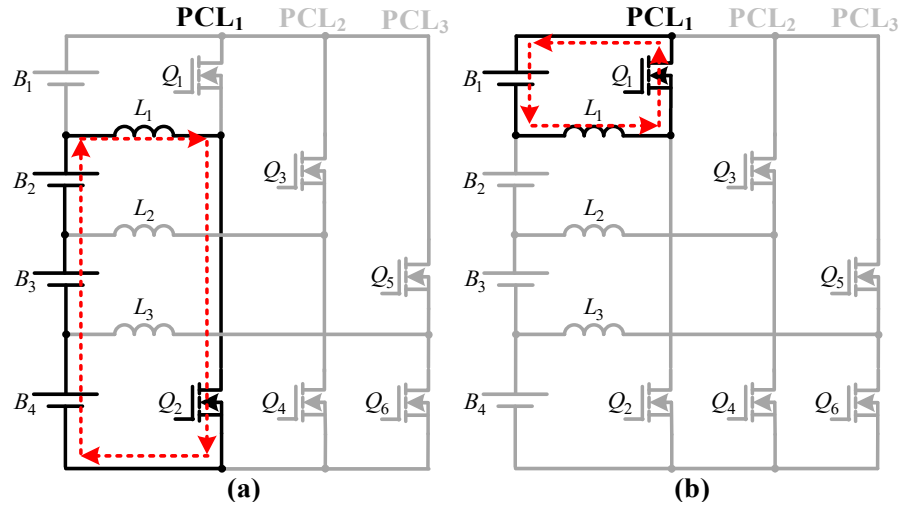


Figure 4. Operation of sub-pack-to-sub-pack (SP2SP) mode: (**a**) EC of subinterval 1, (**b**) EC of subinterval 2.

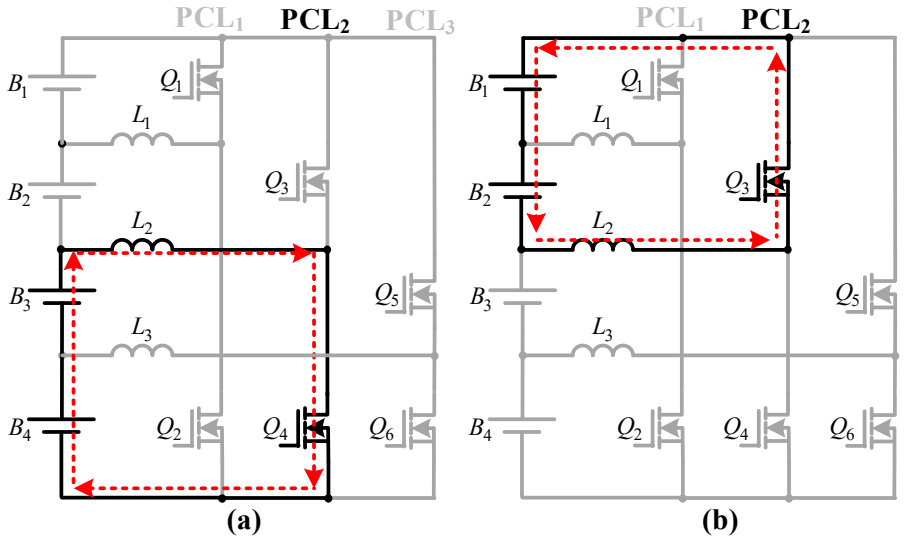


Figure 5. Operation of sub-pack-to-cell (SP2C) mode: (**a**) EC of subinterval 1, (**b**) EC of subinterval 2.

2.3. Parameter Design of Key Components

This subsection specifies the design consideration of the inductor and power switch. From Figure 2a, for continuous current mode (CCM), the following assumptions are made before circuit analysis: (1) The circuit can operate in the steady state and the inductor current is continuous, (2) the filter capacitor (C_o) is large enough to assume a constant output voltage, (3) all components are ideal, and (4) the MOSFET (Q_1) has the on time of DT_s and off time of $(1-D)T_s$. Where, D and T_s are the duty cycle and switching period of the switch, respectively. According to the basis of volt-second balance, conservation of energy, and the average voltage across an inductor over one cycle is zero, the relationship between the average input/output voltages and input/output currents, the average, maximum, as well as minimum inductor currents can be respectively derived as

$$\frac{V_o}{V_{in}} = \frac{D}{1-D} = \frac{I_{in}}{I_o} \tag{5}$$

$$I_{Lm} = \frac{V_{in}D}{R(1-D)^2} \tag{6}$$

$$I_{Lm,\max} = \frac{V_{in}D}{R(1-D)^2} + \frac{V_{in}DT_s}{2L_m} \tag{7}$$

$$I_{Lm,\min} = \frac{V_{in}D}{R(1-D)^2} - \frac{V_{in}DT_s}{2L_m} \tag{8}$$

where V_{in}, V_o, I_{in}, and I_o are the average input/output voltages and currents, I_{Lm}, $I_{Lm,\max}$, and $I_{Lm,\min}$, are the average, maximum, and minimum inductor currents, and R is the load resistor which is equal to V_o/I_o. Let the $I_{Lm,\min}$ of Equation (8) be zero, the boundary between continuous and discontinuous current operation can be found, then the minimum inductance ($L_{m,\min}$) required for continuous current operation can be calculated as

$$L_{m,\min} = \frac{(1-D)^2 V_o}{2f_s I_o} \tag{9}$$

where f_s is the switching frequency. Accordingly, by substituting sub-pack voltage, balance current of setting, switching frequency, and duty cycle into Equation (9), the $L_{m,\min}$ needed to be applied to the studied PCL can be determined. However, in practical circuit application, the inductance must be designed more than $L_{m,\min}$ to ensure CCM operation can be confirmed.

When choosing an active switch, the specifications of allowable current and voltage for the switch must be considered. For each PCL, when the switch is turned off, the voltage across the drain and source (V_{DS}) is equal to the input voltage V_{in}, but a three-fold voltage rating is adopted here to consider the impact of voltage surges. In addition, the selection of current rating needs to reflect the magnitude of the average current and peak current flowing through the switch when the switch is turned on; here, add about 20% margin to allow safe operation. Besides, the equivalent on resistance, $R_{DS(\text{on})}$, and output capacitance (C_{OSS}) of the MOSFET must also be contemplated to reduce the conduction loss and switching loss of the switch during balance operation.

3. Equalizer System Configuration and Balance Strategy

3.1. System Configuration

Figure 6 illustrates the schematic configuration of the studied equalizer system applied to the four-cell string example, as shown in Figure 3. It consists of the equalizer power circuit which is constructed by $(N-1)$ bidirectional PCLs in parallel, differential voltage sensing circuit, data acquisition (DAQ) card, digital signal processor (DSP), and a personal computer (PC) with graphic user interface (GUI). Where the DSP TMS320F28335 from Texas Instruments Incorporated serves as the system controller to manipulate all processes and protections during the balance cycle. The voltage of each cell sensed is transmitted to the DSP and quantized via the analog to digital converter (ADC) imbedded in the DSP. The noises mixed with the digitized data are filtered by the firmware-based finite impulse response (FIR) filter and then its output is sent to the balance strategy controller, which is also realized by firmware. The switch gating signals with the desired duty cycles are derived from the computation of the proposed balance algorithm and generated by the pulse width modulation (PWM) module inside the DSP. The PWM gating signals drive the main switches inside the PCLs to regulate the balance current at a preset value throughout the balance process. In addition, the voltage data of each cell are also read by the DAQ card and routed to the PC equipped with a friendly GUI developed on the LabVIEW platform from National Instruments Corp. to execute data monitor, log, and store in real time. If an over-temperature protection or over-voltage protection event occurs, a corresponding interrupt command will be sent to the DSP to stop the equalization procedure and protect the system from damage immediately. In practical application, the data acquisition and recording, as well as the protection mechanism, are integrated into the BMS with a good communication protocol to make certain these functionalities and manipulations can be carried out safely.

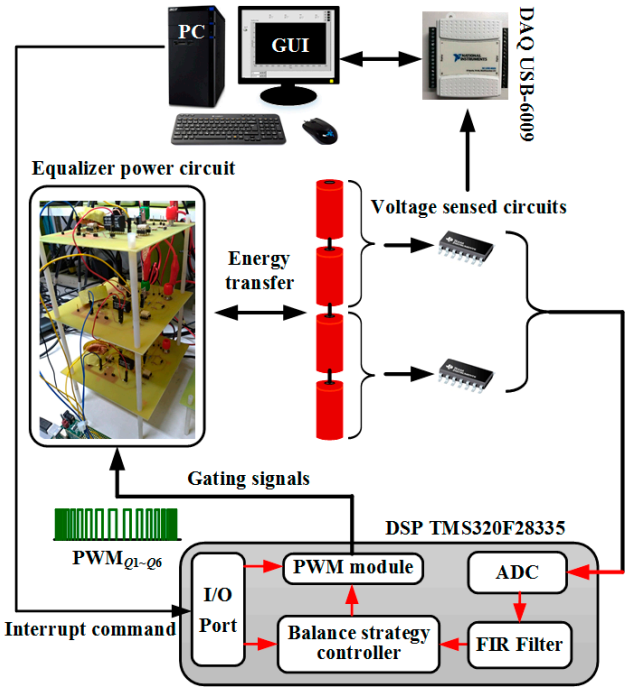


Figure 6. Schematic configuration of the proposed equalizer system applied to a four-cell string case.

3.2. Derivation of Balance Strategy

The balance control strategy studied in this article includes the fixed duty cycle (FDC) and varied duty cycle (AVDC) methods. Based on the same equalizer architecture shown in Figure 6, two different control algorithms are implemented with firmware into the balance strategy controller (BSC) inside the DSP. The general control mechanisms of the two methods need to find out which PCL path in the equalizer has the maximum average voltage difference ($\Delta V_{diff,\max}$) between the cell and sub-pack connected on both sides of the inductor and make the PCL circuit unit of this path actuate preferentially for balancing, while the PCL circuit units of the other two paths are disabled. The entire balancing process repeats the following steps of judging which PCL path has the maximum voltage difference between the cell or sub-pack, selecting the corresponding balance path, and performing equalization, until the maximum voltage difference is reduced to a preset value (which is set to 100 mV in this paper), it is considered that the battery pack has reached equilibrium. In the FDC method, the power switches of high-side and low-side in the PCL have corresponding and fixed duty cycles for control, and voltage variation in individual cell in the pack does not change the duty cycles of the two switches. However, the disadvantage of this method is that, during the balancing process, the balancing current will decrease due to the voltage difference between the cells or sub-packs becomes smaller and result in a slower balance. On the other hand, to resolve the problem of the FDC method, the AVDC method calculates the duty cycle of the corresponding PCL switch according to the voltages of the cells or sub-packs to be balanced, and dynamically modulates the duty cycle with the voltage changes to maintain the inductor current constant during the balance process and thus shorten the balance time. The following introduces the control principle, derivation of duty cycle, and operation flowchart of the two balancing methods studied in this paper.

3.2.1. Balance Strategy for the FDC Method

From Figure 1, in the FDC equalization, each power switch in each PCL$_i$ (i = 1, 2, ... , N − 1) has a fixed duty cycle specified based on the knowledge of previous operating experience. For example, if the duty cycle of the high-side switch (Q_{2i-1}) is denoted by D_{HQi}, then the duty cycle of the low-side

switch (Q_{2i}), D_{LQi}, on the same leg is $1 - D_{HQi}$, and vice versa. Where D_{HQi} and D_{LQi} can be expressed empirically by

$$D_{HQi} = \frac{N-i}{N},\ i = 1, 2, \cdots, N-1 \tag{10}$$

$$D_{LQi} = 1 - D_{HQi} = \frac{i}{N},\ i = 1, 2, \cdots, N-1 \tag{11}$$

As mentioned above, for the example of the four-cell string ($N = 4$) shown in Figure 3, the duty cycles D_{HQ1}~D_{LQ6} of the switches Q_1~Q_6 are specified respectively as (PCL_1: $D_{HQ1} = 3/4 = 0.75$, $D_{LQ2} = 1/4 = 0.25$), (PCL_2: D_{HQ3} 2/4 = 0.5, D_{LQ4} = 2/4 = 0.5), and (PCL_3: D_{HQ5} = 1/4 = 0.25, $D_{LQ6} = 3/4 = 0.75$), which meet the complementary operations of gate drive signals for the high-side and low-side switches on the same leg. Moreover, for instance, in the natural balance mode of C2SP or SP2C run in PCL_1, this type of duty cycle assignment enables the DSP that controls the PCL_1 to operate in boost mode naturally when the cell (B_1) voltage is more than the average voltage of the sub-pack (B_2-B_3-B_4), which boosts the cell voltage to transfer its stored energy to the sub-pack. Otherwise, if the cell voltage is less than the average voltage of the sub-pack, the DSP dominates the PCL_1 to operate in buck mode naturally, which steps down the sub-pack voltage to transmit its stored energy to the cell. Similarly, the above fixed duty assignment and operation mechanism are also applicable to PCL2 and PCL3 paths worked in SP2SP and SP2C balance modes.

3.2.2. Balance Strategy for the AVDC Method

To deal with the problem of the balance current decrease as the voltage difference between the cells or sub-pack becomes smaller leading to the prolongation of the balance time in the later phase especially, a forced balancing technique, the AVDC approach, is addressed to figure out the required duty cycle of each power switch in each PCL. With the variation in voltage difference, the AVDC strategy forces the PCL to modulate the duty cycle dynamically to make constant balancing current achievable throughout the balance cycle to speed up the equilibrium. The circuit operation principles and control mechanisms of the AVDC strategy under various balance modes have been introduced in the previous Section 2.2. The derivation of the duty cycle needed to sustain the fixed balance current is described as follows.

Figure 7 shows the equivalent circuit of the used bidirectional PCL_1 with consideration to nonideal component parameters, including cell internal resistances $R_{BG1\&2}$, switch on resistances $R_{Q1\&2}$, and the inductor resistance R_L. Based on the rule of volt-second balance of the inductor L_m, the average voltage across the inductance equals zero in one switching cycle and can be expressed by Equation (12).

$$[V_{BG_1} - I_{Lm} \cdot (R_L + R_{BG_1} + R_{Q_1})] \cdot D_{HQ_1} + [-V_{BG_2} - I_{Lm} \cdot (R_L + R_{BG_2} + R_{Q_2})] \cdot (D_\alpha - D_{HQ_1}) = 0 \tag{12}$$

where V_{BG1}, V_{BG2}, and D_{HQ1} are the average voltages of sub-pack BG_1 and BG_2, the duty cycle of the Q_1, respectively. D_α is the duty cycle which subtracts the duty cycle occupied by the dead time between the gating signals of Q_1 and Q_2 from the original duty cycle. In practical application, D_α is very close to 1 and can be denoted by

$$D_\alpha = \frac{t_{on} - t_{dt}}{T_s} = D - D_{dt} \tag{13}$$

where t_{on} and t_{dt} are the on time of Q_1 and dead time added, respectively. D and D_{dt} are the original duty cycle of Q_1 and that in the dead time, respectively. From Equation (12), the average inductor current I_{Lm} can be derived as

$$I_{Lm} = \frac{D_{HQ_1} V_{BG_1} - (D_\alpha - D_{HQ_1}) V_{BG_2}}{D_{HQ_1}(R_{BG_1} + R_{Q_1} + R_L) + (D_\alpha - D_{HQ_1})(R_{BG_2} + R_{Q_2} + R_L)} \tag{14}$$

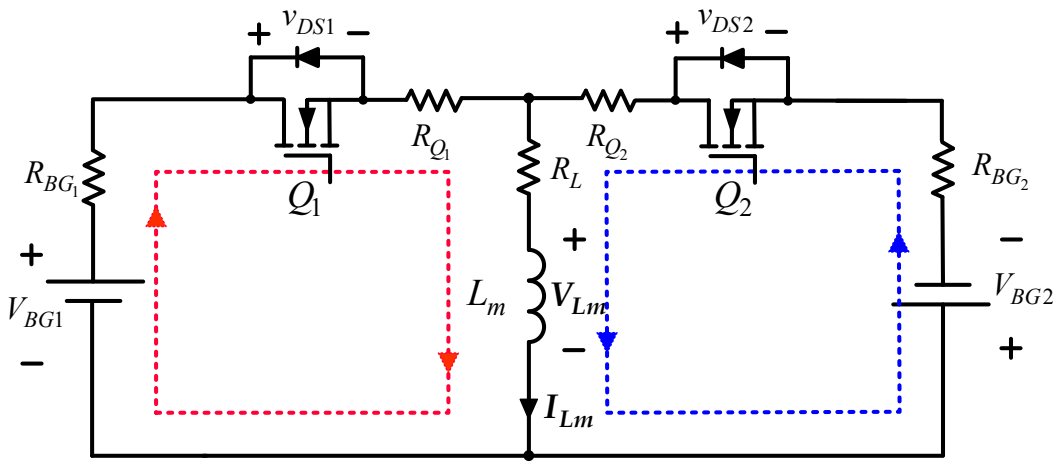


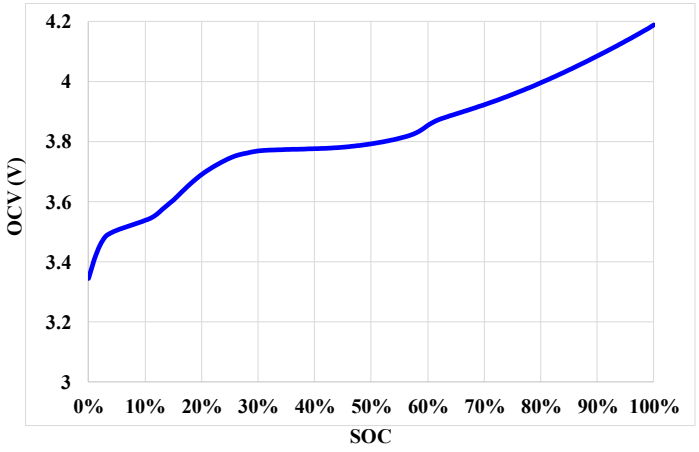
Figure 7. Equivalent circuit of a PCL with nonideal component parameters.

If the target value of the balance current in Equation (14) has been specified, then the duty cycles of the high-side and low-side switches, D_{HQ1} and D_{LQ2}, in the bidirectional PCL_1 needed to generate the desired current can be respectively figured out by

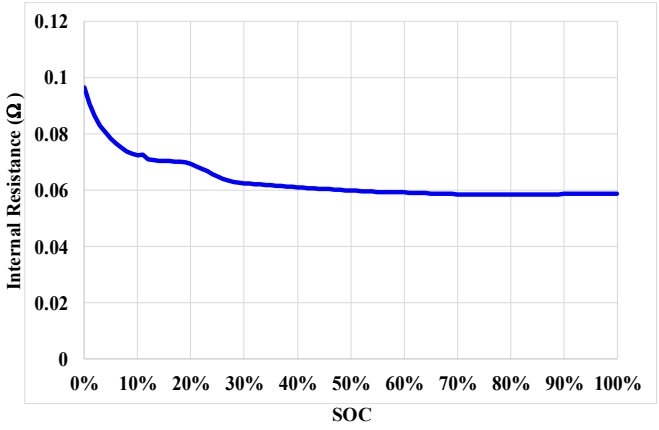
$$D_{HQ_1} = \frac{D_\alpha V_{BG_2} + D_\alpha I_{Lm}(R_{BG_2} + R_{Q_2} + R_L)}{V_{BG_1} + V_{BG_2} - I_{Lm}(R_{BG_1} - R_{BG_2} + R_{Q_1} - R_{Q_2})} \tag{15}$$

$$D_{LQ_2} = D_\alpha - D_{HQ_1} \tag{16}$$

From Equation (15), the known parameters include the sub-pack voltage V_{BG1}, V_{BG2} which can be obtained from the voltage sensing circuit, D_α whose value can be determined by the dead time known, R_{Q1} and R_{Q2} which can be obtained from the datasheet provided by the component vendor, R_L which can also be obtained by measuring, I_{Lm} whose value is specified by the designer, and it is set to 0.5 A here based on the comprehensive considerations to battery specifications, safety, and expected balance time. Thus, the non-ideal characteristics (such as R_L and $R_{Q1\&2}$) of the components adopted have been involved in the circuit model for calculation. Besides, in order to also take the battery nonlinear behavior into consideration for the circuit model, the screening and testing items, including OCV test, internal resistance measurement, and capacity test, are conducted using potentiostat VSP with EC-Lab software from BioLogic Corp. When the battery is fully charged after a proper rest period to ensure that the electrochemical reaction has stabilized, the next step is to discharge with 0.01 C current for one hour each time (releasing capacity with a step of 1%). In each test cycle, the value of OCV and internal resistance is recorded until the end of 100 discharging cycles. Hence, the OCV and internal resistance versus SOC, as illustrated in Figure 8a,b respectively, can be obtained to involve the nonlinear characteristics ($R_{BG1\&2}$) of the battery in the equalization analysis.



(**a**)



(**b**)

Figure 8. Battery characteristic curve test: (**a**) Curve of OCV vs. SOC, (**b**) curve of internal resistance vs. SOC.

3.2.3. Operating Flowchart of Balance Algorithm

Based on the same hardware architecture, both balance strategies have the identical control process, but the mechanism of the duty cycle determined is very different. For the example of the four-cell string taken in this article, Figure 9a,b describe the operating flowchart of the main program and subroutine to specify or calculate the duty cycle for the FDC and AVDC balance strategies studied. Beginning the balance procedure, the program reads each cell's voltage and calculates the average and maximum voltage difference (ΔV_{diff} and $\Delta V_{diff,max}$) between cells or sub-packs to determine whether the battery pack has reached equilibrium or not. If the $\Delta V_{diff,max}$ is more than 100 mV, then the controller needs to find out which PCL path must be activated first to run equalization, that is, the PCL leg with the largest average voltage difference between the cells or sub-packs has the top priority balance order. Next, the procedure enters a subroutine to determine or calculate the duty cycle required for each switch of the PCL to generate or regulate the balance current. In the FDC method, the duty cycle of each switch is constant and has been specified in advance as mentioned above in Section 3.2.1. In the AVDC method, the duty cycle of each switch can be obtained via the calculation of Equations (15) and (16). Descriptions about the duty cycle derivation in AVDC have also been introduced in the previous Section 3.2.2. The balance cycle is done consecutively until the predefined criterion for balance termination is met ($\Delta V_{diff,max} \leq 100$ mV) or the default balance time is out.

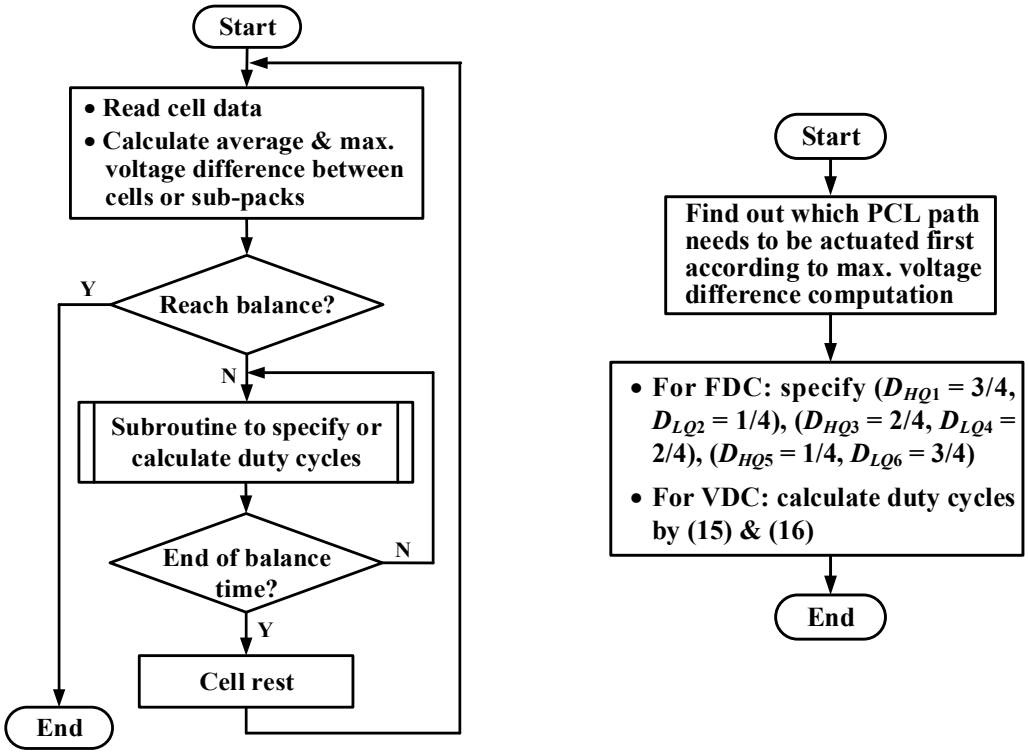


Figure 9. Operating flowchart of the balance strategy: (**a**) Main program, (**b**) subroutine to determine or calculate the duty cycle.

4. Experimental Results and Comparisons

In this section, the setup of the experimental system and parameter is specified at first. The results of the simulation and practical test are offered to confirm the validity and feasibility of the balance strategies studied in this paper, and the comparison of the results obtained by running the FDC and AVDC strategies on the same test platform is included to distinguish the performance enhancement. This article particularly focuses on improving the problem of slow balancing rate, caused by the reduction of balancing current due to the voltage difference between the cells or sub-packs which decreases in the later period of equalization. Lithium-ion battery UR18650ZY from SANYO Energy (U.S.A.) Corp. is used for experimental tests in this paper, and the specifications of key parameters are listed in Table 1. The component parameters designed for the PCL circuit are tabulated in Table 2. Figure 10 shows a photograph of the equalizer prototype constructed in the laboratory for experimental tests and performance verification.

Table 1. Specifications of UR18650ZY key parameters.

Items	Value
Nominal capacity (25 °C)	2600 mAh
Nominal voltage	3.7 V
Maximum continuous discharge current/Discharge cut-off voltage	2.5 A/3.0 V
Energy density	Volumetric: 535 Wh/L Gravimetric: 193 Wh/kg
Temperature	Charge: 0 to +45 °C Discharge: −20 to +60 °C

Table 2. Component parameters designed for the PCL unit.

Items	Value/Part Number
Inductance (L_m)	16 μH
MOSFET-related parameters	IPP030N10N
On resistance ($R_{DS(on)}/R_{Qi}$)	3 mΩ
Output capacitance (C_{OSS})	1210 pF
Switching frequency (f_s)	50 kHz
Dead time	1 μs

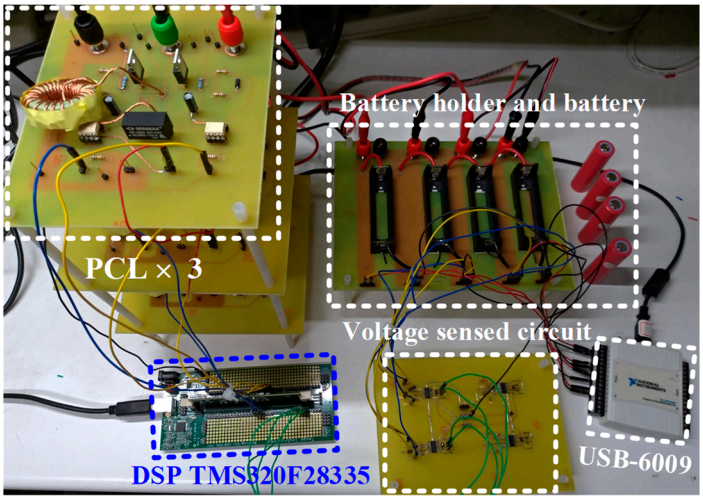


Figure 10. Photograph of the equalizer prototype implemented for a four-cell string.

4.1. Simulation Results

The PSIM from PowerSim Corp. is employed to perform the simulation of the four-cell string equalization. For the simulation, the equivalent *RC* model is used, and the battery is replaced with a capacitor of 0.2 F to reduce the simulation time. The equivalent average internal resistance is 0.063 Ω according to the test results of Figure 8b. The initial voltages of four cells (V_{B1}, V_{B2}, V_{B3}, V_{B4}) before balancing are 3.89, 3.76, 3.74, and 3.46 V, respectively. The relevant component parameters of the PCL circuit are available from Table 2, where the criterion of stopping balance simulation is that the maximum voltage difference ($\Delta V_{diff,\max}$) between the maximum and minimum voltages ($V_{\max}$, $V_{\min}$) of the cell is less than 10 mV. Figure 11a,b show the cell voltage balance curves simulated by the FDC and AVDC methods, respectively. From Figure 11, it can be observed that both control strategies can reduce the ΔV_{diff} within 10 mV and effectively achieve equalization. Table 3 summarizes the comparison of simulation results. In Table 3, in terms of improving balance time, the AVDC method is 21.4% shorter than that of the FDC method. It can be verified that the proposed balance approach can modulate the duty cycle adaptively with the change of voltage difference to maintain a nearly constant balance current, thus the processing speed is boosted in the later stage of balance.

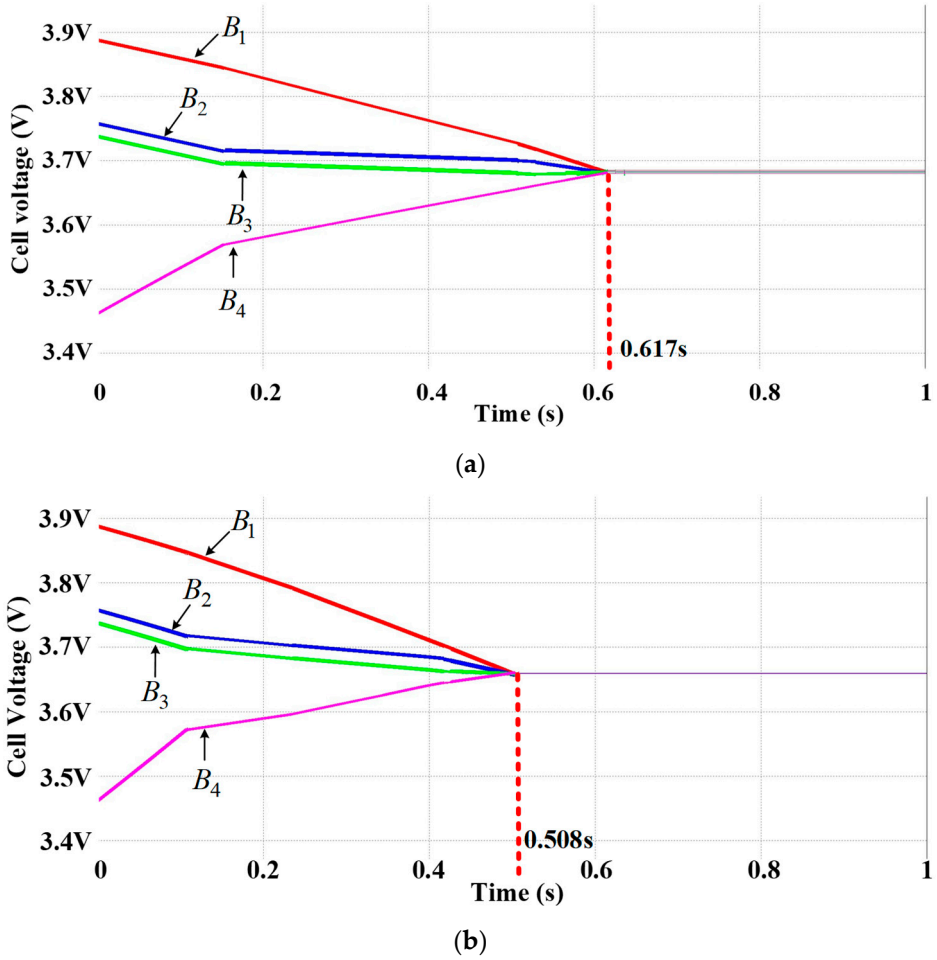


Figure 11. Battery voltage balance simulation curve run by: (**a**) the FDC method and (**b**) the AVDC method.

Table 3. Comparison of balance simulation results.

Item / Method	Before Balance			After Balance			Balance Time
	V_{max}	V_{min}	$\Delta V_{diff,max}$	V_{max}	V_{min}	ΔV_{diff}	
FDC	3.89 V	3.46 V	430 mV	3.68 V	3.67 V	10 mV	0.617 s
AVDC	3.89 V	3.46 V	430 mV	3.66 V	3.65 V	10 mV	0.508 s

4.2. Experimental Results

In order to test and demonstrate the effectiveness of the balance strategy presented, a prototype of the equalizer has been constructed and realized with firmware. The setup of experimental parameters is the same as the simulation, except that the cell voltage is dependent on its own actual capacity, the measuring errors and uncertainties, and the component non-ideal factors have been considered. The benchmark preset in the practical experiment for terminating balance is that the voltage difference (ΔV_{diff}) between V_{max} and V_{min} is less than 100 mV. Besides, the initial voltage of the four cells before balancing should be as similar as possible for fair comparison of different methods. However, there still exists slight discrepancies that are difficult to avoid caused by the deviations of charge/discharge and measurement, yet these tiny mismatches have only a very small influence on the result. First, key operating waveforms of the three PCLs manipulated by the FDC and AVDC methods are measured to validate the correctness of the circuit function. Figures 12a, 13a and 14a respectively show the gating signal (V_{GS}) and voltage across the drain and source (V_{DS}) of the high-side MOSFET (Q_1, Q_3,

Q_5) in each PCL operated in a certain balance status using the FDC method. The initial voltages of the four cells before balancing are 3.89, 3.76, 3.74, and 3.46 V, respectively. Waveforms of inductor currents (i_{L1}, i_{L2}, i_{L3}) in three PCLs corresponding to the previous operating conditions are shown in Figures 12b, 13b and 14b, respectively. Similarly, in the AVDC operation with the initial voltages of 3.90, 3.76, 3.75, and 3.46 V before balancing, the waveforms of the switches and corresponding inductor currents are respectively illustrated in Figures 15–17. From the measured waveforms operated in the FDC method, it can be seen that excluding the duty cycle of dead time, the measured duty cycle values of the Q_1, Q_3, and Q_5 comply with the aforementioned designation rule, and the average value of each inductor current measured cannot be kept unchanged; especially, when the ΔV_{diff} becomes lower during the later phase of balance, the inductor current will decrease significantly. On the other hand, for waveforms measured in the AVDC operation, duty cycle values of the Q_1, Q_3, and Q_5 are designed to be modulated dynamically with the variation of the ΔV_{diff} to maintain a target balance current under different battery voltages. Evidently, the average value of each measured inductor current flowing through the three PCL paths has a significant increase and is close to the target inductor current of 0.5 A, which proves the effectiveness of the proposed AVDC method.

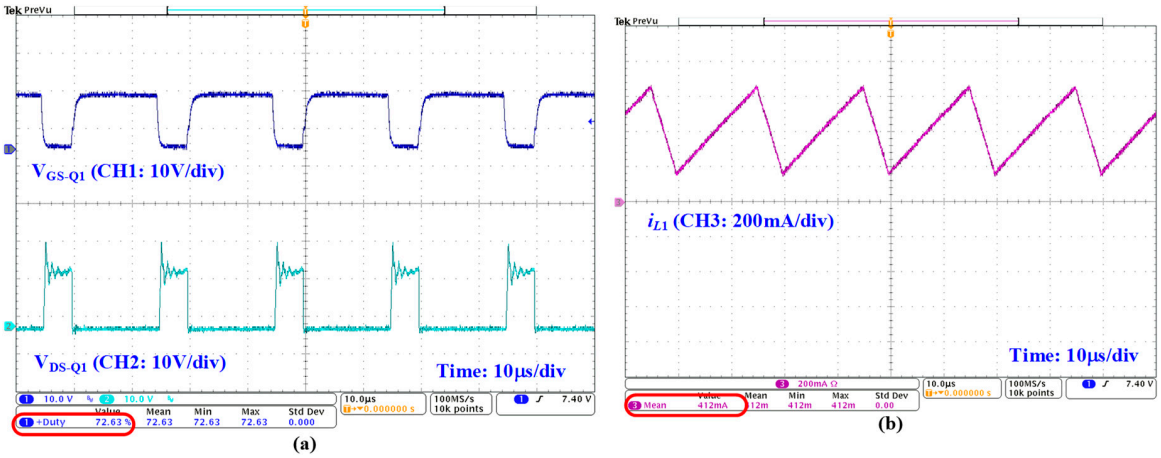


Figure 12. Measured waveforms of PCL_1 with the FDC method: (**a**) switch voltages of $V_{GS\text{-}Q1}$ and $V_{DS\text{-}Q1}$, (**b**) inductor current of i_{L1}.

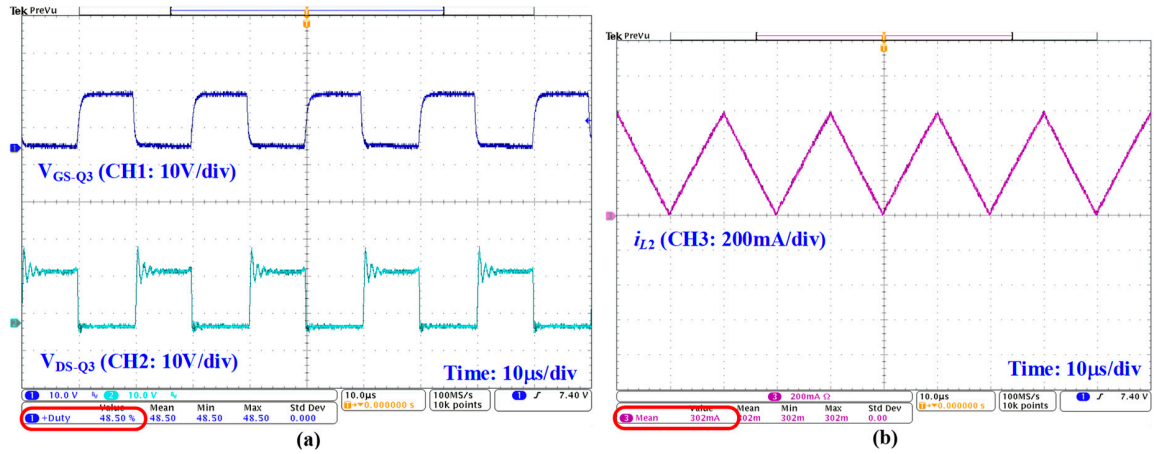


Figure 13. Measured waveforms of PCL_2 with the FDC method: (**a**) switch voltages of $V_{GS\text{-}Q3}$ and $V_{DS\text{-}Q3}$, (**b**) inductor current of i_{L2}.

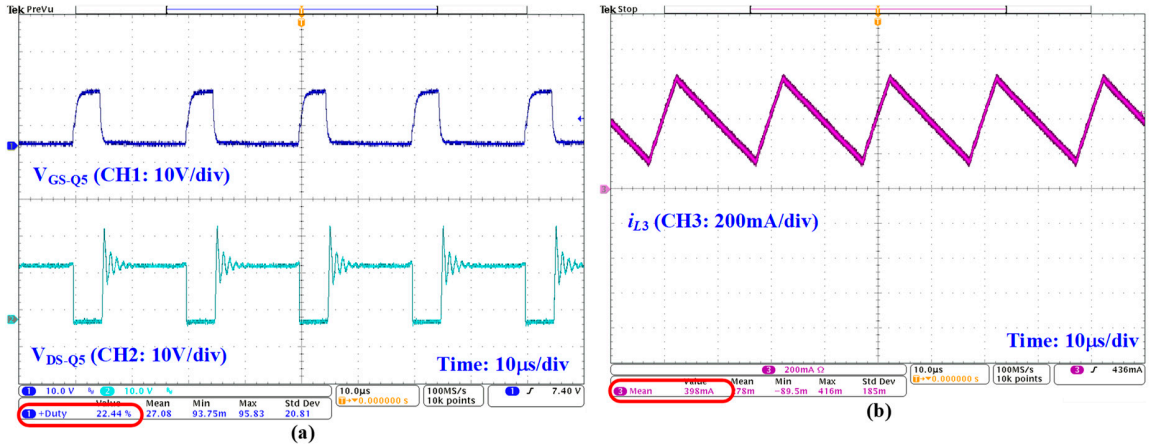


Figure 14. Measured waveforms of PCL_3 with the FDC method: (**a**) switch voltages of $V_{GS\text{-}Q5}$ and $V_{DS\text{-}Q5}$, (**b**) inductor current of i_{L3}.

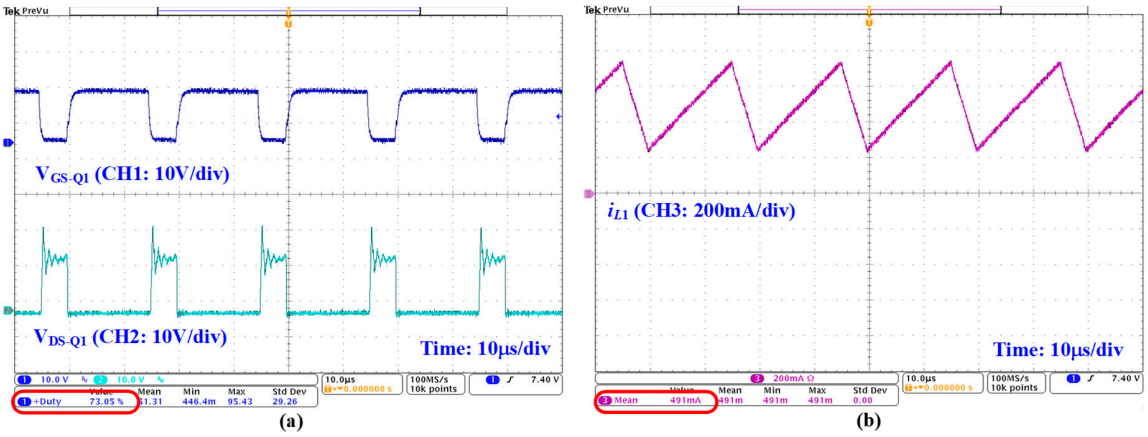


Figure 15. Measured waveforms of PCL_1 with the AVDC method: (**a**) switch voltages of $V_{GS\text{-}Q1}$ and $V_{DS\text{-}Q1}$, (**b**) inductor current of i_{L1}.

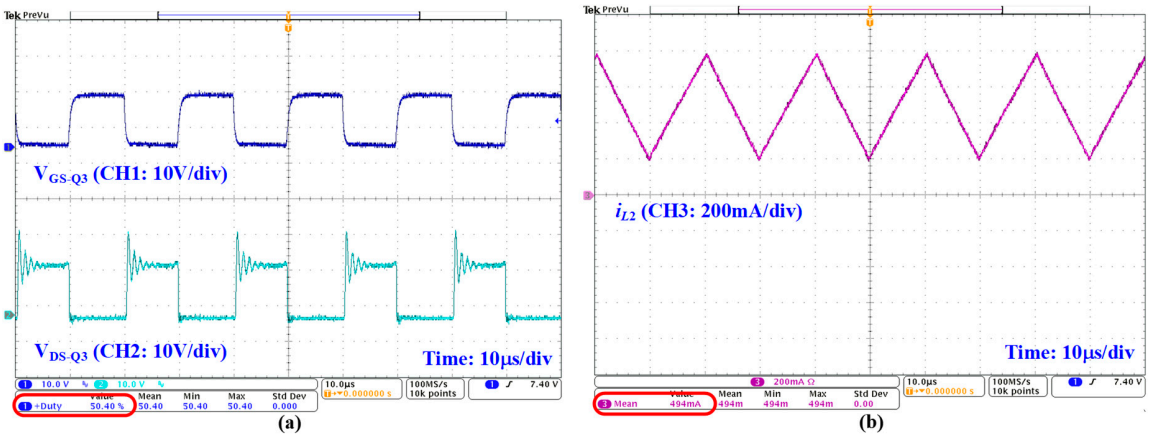


Figure 16. Measured waveforms of PCL_2 with the AVDC method: (**a**) switch voltages of $V_{GS\text{-}Q3}$ and $V_{DS\text{-}Q3}$, (**b**) inductor current of i_{L2}.

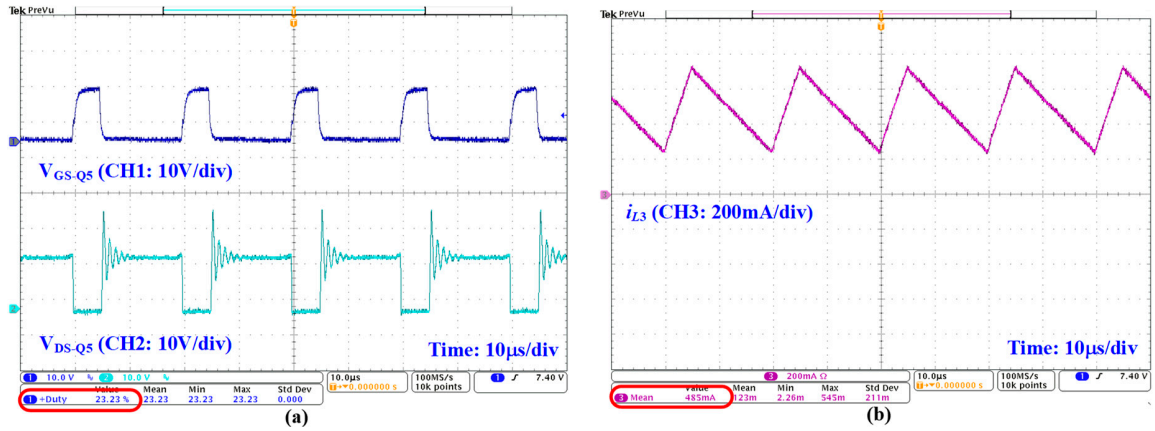


Figure 17. Measured waveforms of PCL_3 with the AVDC method: (**a**) switch voltages of $V_{GS\text{-}Q5}$ and $V_{DS\text{-}Q5}$, (**b**) inductor current of i_{L3}.

Figures 18 and 19 show the balance voltage change curve of each cell during the entire balance process using FDC and AVDC methods, respectively. From Figures 18 and 19, we can see that, for the two balance algorithms, all cell voltages finally converge to approximately the same value, and the maximum voltage difference ($\Delta V_{diff,\max}$) has been reduced to less than 100 mV to actuate the criterion of stopping equalization. Figure 20 plots the change curve of the $\Delta V_{diff,\max}$ operated by the two methods during the balancing process. It can be seen from Figure 20 that the FDC method takes 234 min to perform balance to reduce the $\Delta V_{diff,\max}$ from 430 to 100 mV, while the AVDC method only requires 139 min, i.e., the equilibration time needed for FDC and AVDC methods is 234 min and 139 min, respectively. Obviously, the proposed AVDC method has a significant effect on the improvement of equilibrium time.

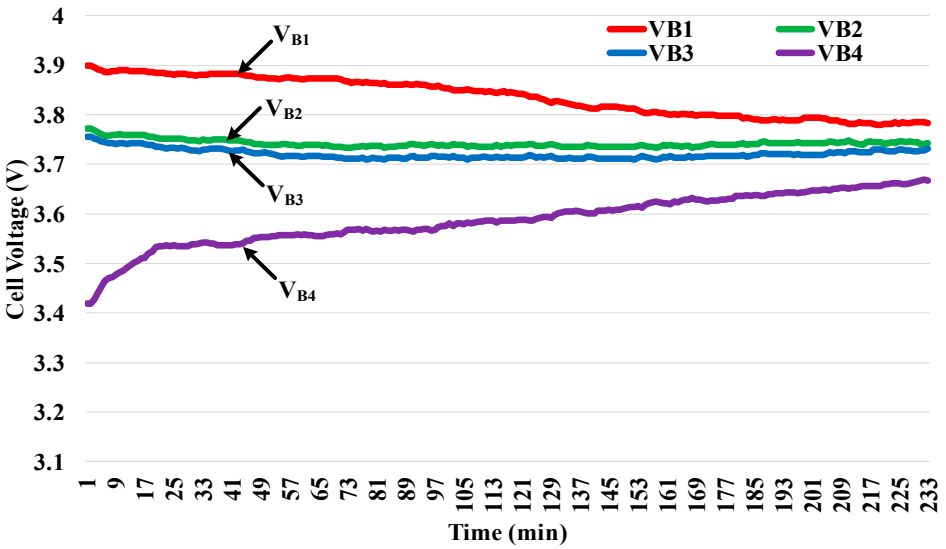


Figure 18. Voltage balance curve operated by the FDC method.

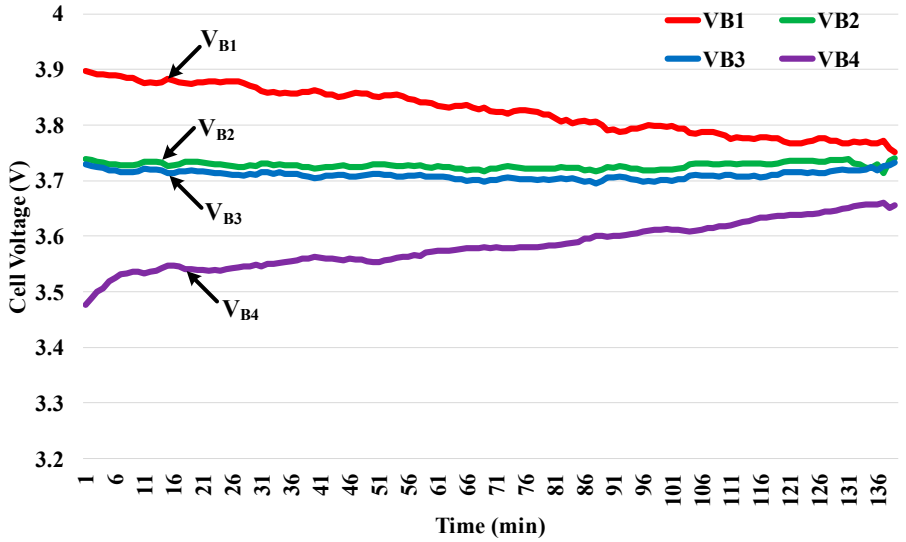


Figure 19. Voltage balance curve operated by the AVDC method.

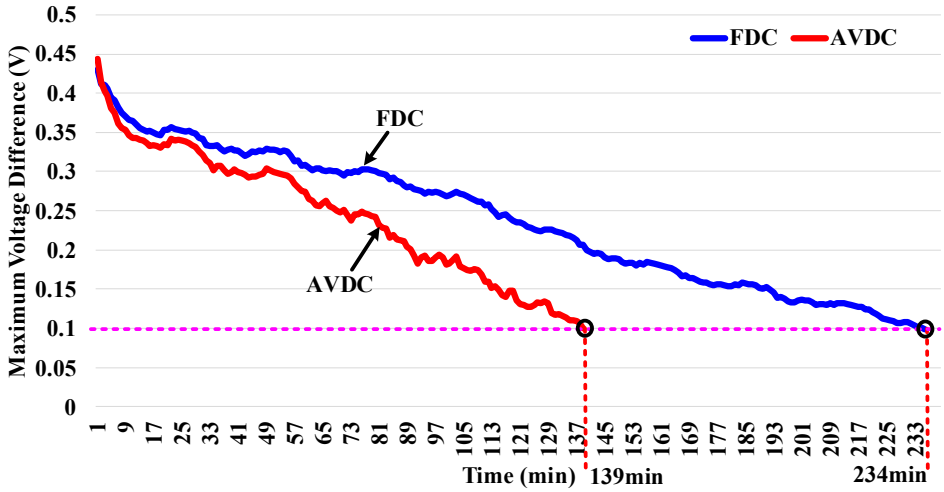


Figure 20. Curve of the $\Delta V_{diff,\max}$ variation operated by the two methods.

4.3. Cpmparison and Discussion on Experimental Results

Test results obtained by the two balancing methods are compared and discussed to stress the performance enhancement of the proposed method. The main performance indices compared include the balance time and the balance efficiency. The cell voltages and SOCs measured before and after equalization are listed in Tables 4 and 5, respectively. From Table 4, the cell voltages are unequal before equalization and there exists a large voltage difference, but these cell voltages converge to nearly the same value after equalization. In Table 5, the SOC value of each cell is determined by looking up the SOC versus OCV curve, as shown in Figure 8a, of the utilized Li-ion battery, and the OCV is measured by resting the battery after equalization. From Table 5, the average SOC obtained by the proposed AVDC method after equalization is higher than that of the FDC method. As a result, the balance efficiency (91.4%) of the AVDC method is better than that (83.1%) of the FDC one. In other words, the proposed method can reduce the power consumption of circuit operation by effectively shortening the balance time and obtain a more efficient balance process and efficacy.

Table 4. Cell voltages before and after balancing.

Item / Method	Before Balance				After Balance			
	V_{B1}	V_{B2}	V_{B3}	V_{B4}	V_{B1}	V_{B2}	V_{B3}	V_{B4}
FDC	3.89 V	3.76 V	3.74 V	3.46 V	3.77 V	3.74 V	3.73 V	3.67 V
AVDC	3.90 V	3.76 V	3.75 V	3.46 V	3.77 V	3.71 V	3.73 V	3.68 V

Table 5. Cell SOCs before and after balancing.

Item / Method	Before Balance				After Balance			
	SOC_1	SOC_2	SOC_3	SOC_4	SOC_1	SOC_2	SOC_3	SOC_4
FDC	70%	33%	31%	8%	37%	27%	29%	25%
AVDC	69%	33%	30%	7%	44%	30%	29%	24%

Table 6 summarizes the experimental results, where SOC_1 to SOC_4 are the state of charge stored in cell B_1 to B_4 individually before and after balancing, T_{rb} is balancing time required, SOC_{total_bb} and SOC_{total_ab} are the total SOC before and after balancing respectively, and the balancing efficiency $\eta_{balance}$ is defined as the percentage of the SOC_{total_ab} divided by SOC_{total_bb}. From Table 6, the proposed AVDC has better performance in terms of balance speed and balance efficiency than that of the FDC method. Comparing with FDC and AVDC methods, the proposed AVDC method can improve the balance time by 68.3%. On the other hand, the proposed method has taken the battery nonlinear characteristics and circuit parameter nonideality into account, to precisely calculate and adaptively modulate the duty cycle in real time to maintain the balancing current, so the balance speed is faster than that of the FDC method. For balancing efficiency, the proposed method has an improvement of 8.3% as compared with the FDC method.

Table 6. Comparison of balance simulation results.

Item / Method	Before Balance		After Balance		Balance Efficiency ($\eta_{balance} = SOC_{total\_ab}/SOC_{total\_bb}$)
	$\Delta V_{diff,max}$	SOC_{total_bb}	T_{rb}	SOC_{total_ab}	
FDC	0.43 V	142%	234 min	118%	83.1%
AVDC	0.44 V	139%	139 min	127%	91.4%

5. Conclusions

A non-dissipative equalizer with fast energy transfer based on adaptive balancing current control has been proposed and developed in this paper to rapidly equilibrate lithium-ion battery packs. The studied multiphase of equalizer formed by many specific parallel converter legs (PCLs) with bidirectional energy conversion serves as the power transfer stage to make the charge shuttle back and forth between the cell and sub-pack or sub-pack and sub-pack more flexible and efficient. The architecture is capable of transferring energy between cells or sub-packs bidirectionally. It has advantages of structural and simple topology, fast balancing speed, and ease of implementation with low-cost micro-controllers. This paper focuses on improving the problem of poor balance speed, and the proposed balance strategy has achieved a very significant improvement in balance time. For the experimental verification, as compared with the conventional FDC method, the improvements of 68.3% and 8.3% in terms of balance time and efficiency have been reached. Therefore, the main contributions of this paper are that the proposed equalizer can control and maintain the balancing current adaptively throughout the balancing process to accelerate the equalization speed. Moreover, the derivation of the adaptive duty cycle modulation has taken the battery nonlinear characteristics and circuit parameter nonideality into consideration. Hence, an accurate battery and circuit model is not needed. In addition, a low-cost MCU can be utilized to implement the devised equalizer and its ease of extension and modularization to equalize a long battery string.

On the other hand, the limitations of the proposed multiphase parallel converter legs solution are that the equalization of cell to cell and cell to pack or vice versa cannot be achieved under the premise of simplifying the balancer structure and reducing the number of two-way switch sets used. Accordingly, based on the proposed multiphase PCL architecture, to accomplish the energy transfer from any cell(s) to any cell(s) and highly integrate converter topology to downsize the balancer volume, future research will be directed towards the development of an interleaved topology with coupled inductor. This type of balancer can significantly reduce the number of passive and magnetic components and further slim down the size and cost of the balance system with compact integration and reconstruction of circuit topology. Besides, future work also needs to perform long-term life testing of battery string to validate that the proposed equalizer features a positive impact on the extension of battery pack lifespan.

Author Contributions: This research article has three authors. S.-C.W. and Y.-H.L. conceived the research method and designed the control strategy. C.-Y.L. constructed the prototyping circuits and performed the experiments. S.-C.W. and Y.-H.L. analyzed the resulting data and wrote the manuscript. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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