

Article

High-PSRR Wide-Range Supply-Independent CMOS Voltage Reference for Retinal Prosthetic Systems

Ruhaifi Bin Abdullah Zawawi ¹, Hojong Choi ^{2,*} and Jung Suk Kim ^{3,*} 

¹ Department of Health Science and Technology, Gachon Advanced Institute for Health Sciences & Technology, Incheon 21999, Korea; ruhaifi@bme.gachon.ac.kr

² Department of Medical IT Convergence Engineering, Kumoh National Institute of Technology, 350-27, Gum-daero, Gumi 39253, Korea

³ Department of Biomedical Engineering, Gachon University, 191, Hambakmoe-ro, Incheon 21936, Korea

* Correspondence: hojongch@kumoh.ac.kr (H.C.); jungsuk@bme.gachon.ac.kr (J.K.)

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Abstract: This paper presents a fully integrated voltage-reference circuit for implantable devices such as retinal implants. The recently developed retinal prostheses require a stable supply voltage to drive a high-density stimulator array. Accordingly, a voltage-reference circuit plays a critical role in generating a constant reference voltage, which is provided to a low-voltage-drop regulator (LDO), and filtering out the AC ripples in a power-supply rail after rectification. For this purpose, we use a beta-multiplier voltage-reference architecture to which a nonlinear current sink circuit is added, to improve the supply-independent performance drastically. The proposed reference circuit is fabricated using the standard 0.35 μm technology, along with an LDO that adopts an output ringing compensation circuit. The novel reference circuit generates a reference voltage of 1.37 V with a line regulation of 3.45 mV/V and maximum power-supply rejection ratio (PSRR) of -93 dB.

Keywords: reference circuit; inductive link; implantable device; line regulation; wireless power telemetry; supply independence

1. Introduction

Short-distance wireless communication for retinal prosthetic systems plays a critical role in delivering a radio-frequency (RF) power carrier and data from the external world to an implant inside the eyeball. Communication techniques based on inductively coupled coils have been widely used, owing to their high power-transfer efficiency and hardware simplicity [1–4]. The recent advances in submicron complementary metal oxide semiconductor (CMOS) technologies have also facilitated the reduction of the size of the implanted hardware such as an inductive coil receiver, digital controller, or high-density stimulator array. As a result, the device can be implanted above the ganglion cells in the case of epiretinal prostheses [5,6] or below the bipolar cells in subretinal prostheses [7–9].

Figure 1 shows a retinal prosthetic system architecture wherein a dual half-wave rectifier is used to recover dual-rail DC power from a received RF power carrier, through inductively coupled coils. The external device is composed of a commercial class-E power amplifier, an amplitude-shift-keying (ASK) modulator circuit, and a current-sense circuit for back-telemetry data recovery. The implanted device consists of a rectifier, regulator, over-voltage-protection circuit, demodulator, reverse telemetry controller, global digital controller, and stimulator array. The class-E amplifier is driven by an RF carrier signal of 13.56 MHz, which is allowed for industry, science, and medical purposes, containing command data of 1.356 Mbps, which is transmitted to the implanted device through inductively coupled coils. The RF signals received in the implanted device are rectified and fed to the regulator to generate dual-rail DC supply voltages, $+V_{1,2}$ and $-V_{1,2}$. The connection of reference circuits (+REF, –REF)

is shown in Figure 1, where +REF and −REF, respectively generate positive and negative reference voltages for internal LDO. LDO1 and LDO2 supply constant voltages to analog and digital circuits in the implanted devices respectively. The command data modulated on the RF carrier are recovered using the demodulator and sent to the global digital controller that decodes the demodulated data in order to activate the stimulator array. Here, a single-pixel stimulator, which is composed of a photosensor, current amplifier, and pulse shaper [10], generates a biphasic current pulse, which is delivered to the bipolar cells through a microelectrode. Back telemetry is utilized to observe the operating status of the implanted device. A load-shift keying (LSK) technique is used for back telemetry, which is fully controlled by the reverse telemetry controller in the retinal prosthesis. The over-voltage-protection circuit in the implanted device is activated when the rectified signal exceeds the allowable voltage limit. This circuit allows to shift the reactance of the implanted secondary coil and capacitor away from its resonance, and as a result, the received signal is attenuated to a safe voltage level.

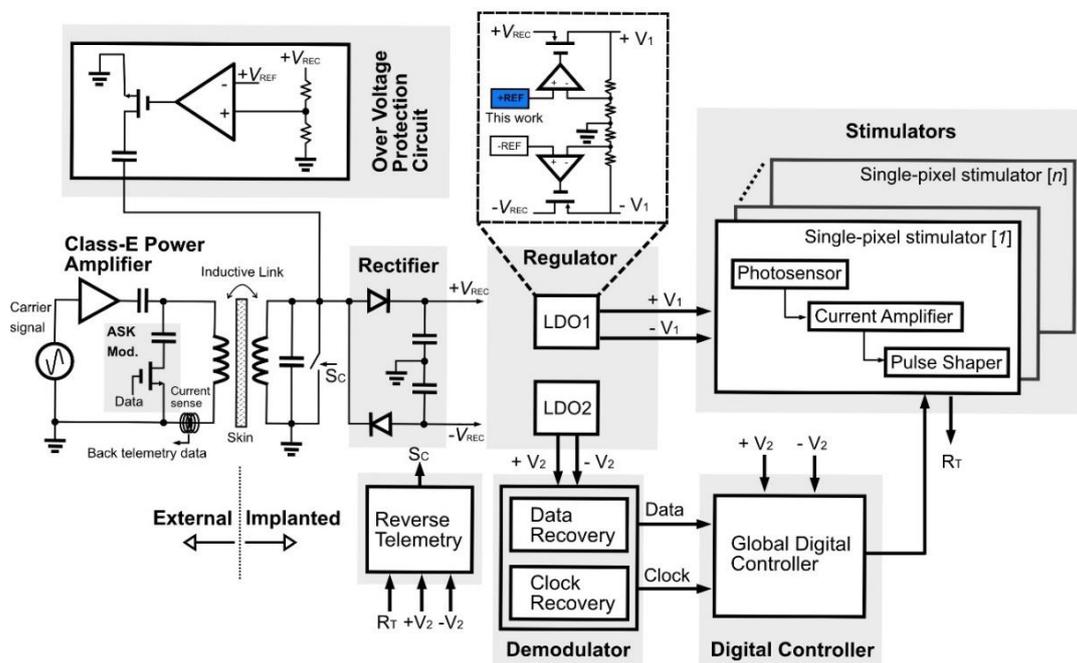


Figure 1. Retinal prosthetic system architecture.

In this retinal prosthetic implant, it is important to provide stable DC voltages to each functional block such as the demodulator, digital controller, and stimulator array. If the DC voltage level varies during stimulation, it will affect the biphasic pulse amplitude, resulting in more or less charge injection to the bipolar cells. However, the amplitude of the rectified DC voltage that determines the regulated DC supply voltage level often fluctuates for the following two reasons. First, natural eye rolling may cause axial and/or lateral misalignment of the implanted coil. This angular misalignment decreases the coupling coefficient, leading to low power-transfer efficiency and DC supply voltage drop [11]. Second, a high-modulation-index waveform of the received RF carrier, based on the ASK scheme, causes a deep ripple in the rectified voltage. This is because the on-chip small capacitor for the rectifier is not sufficient to eliminate the rapid change in charging and discharging. Therefore, it is indispensable for the reference circuit to provide a stable DC voltage to the regulator, regardless of the deep ripple variation after rectification.

For a retinal implant, the reference circuit must meet three design requirements. First, the reference circuit requires a wide-range supply-independent reference voltage. As mentioned above, eye rolling affects the rectified voltage level shift, and can vary the reference voltage output. This also causes a regulator output biasing drop. Second, a high-power supply rejection ratio (PSRR) is necessary for the reference circuit to lessen the deleterious effect of the deep AC ripple. An abrupt change in the

ripple after rectification produces a high-frequency noise that can affect the output voltage. Finally, the reference circuit for the implantable device should be fully integrated on a single chip to reduce the active area. Because the eyeball is not large enough to accept external components, all components should be miniaturized on a single chip. Motivated by this, in this paper, we propose an integrated reference circuit that has a nonlinear current sink circuit (NSC) to improve the supply dependency and ripple rejection performances. This novel circuit is designed, fabricated using an SK Hynix 0.35- μm CMOS technology, and demonstrated on a benchtop.

The current paper is an extension of our previous work in [12]. Our last work utilizes the temperature compensation technique, which had been proven to reduce the variation of the reference voltage at higher temperatures. However, the proposed temperature circuit limits the line regulation performance as the biasing voltage of the compensation circuit varies proportionally to the supply changes. As a result, some current from the output path sinks out through the compensation circuit, which eventually deteriorates the output reference voltage. Besides that, the performance of the operational amplifier drops as the power supply increases because the input voltage of the amplifier exceeding the allowable input common-mode range, set for the current source of the amplifier to be kept in the saturation region. Consequently, the amplifier becomes unstable, which leads to the poor performances of line regulation and PSRR. The new architecture of the reference circuit resolves this issue to fulfil all requirements highlighted in this paper. With the proposed circuit, the improvements have been made in terms of its supply rejection and wide-range supply independent performance. The proposed circuit was also evaluated in the full-path retinal prosthetic system shown in Section 3. This system includes on-chip digital controller and stimulator, which is not implemented in [12].

2. Methods

2.1. Static Analysis

The newly proposed circuit and its small-signal equivalent circuit are illustrated in Figure 2a,b respectively. The proposed circuit is based on a V_{GS} reference supply independent current-reference circuit [13]. The loop around M_{N1} and M_{N2} has negative feedback; consequently, the output voltage at node V_{REF} is unchanged even when the voltage across the resistor R_1 varies. However, the nonlinear current I_1 in the current mirror, produced by the square-law behavior of the transistor and channel length modulation that results in a nonzero slope for I_D/V_{DS} , deteriorates the DC level of the reference voltage. The second-order factor in the reference voltage due to the nonlinear current can be eliminated if a linear current flows into M_{P3} . Therefore, the NSC formed by transistors M_{P4} and M_{N3} is proposed in Figure 2a, whereby a linear current can be produced in the output path. The slope of the output voltage with respect to V_{DD} is also controlled by the NSC. As a result, improvements have been made in terms of its supply dependency and ripple rejection performance.

If I_4 and V_{REF} are constant, the gate–source voltages of M_{N1} and M_{N2} will also be constant. V_{REF} can be expressed as follows:

$$V_{REF} = V_{GS,N1} + V_{GS,N2}. \quad (1)$$

A supply-independent reference voltage can be achieved if:

$$\frac{\partial V_{REF}}{\partial V_{DD}} = 0 \quad (2)$$

or

$$\frac{\partial V_{GS,N1}}{\partial V_{DD}} + \frac{\partial V_{GS,N2}}{\partial V_{DD}} = 0 \quad (3)$$

The gate–source voltage of M_{N1} can be obtained by first allowing the current in M_{N1} to saturate; hence,

$$I_4 = \frac{1}{2}k_{n,N1}(V_{GS,N1} - V_{TH,N1})^2(1 + \lambda_{N1}V_{DS,N1}). \quad (4)$$

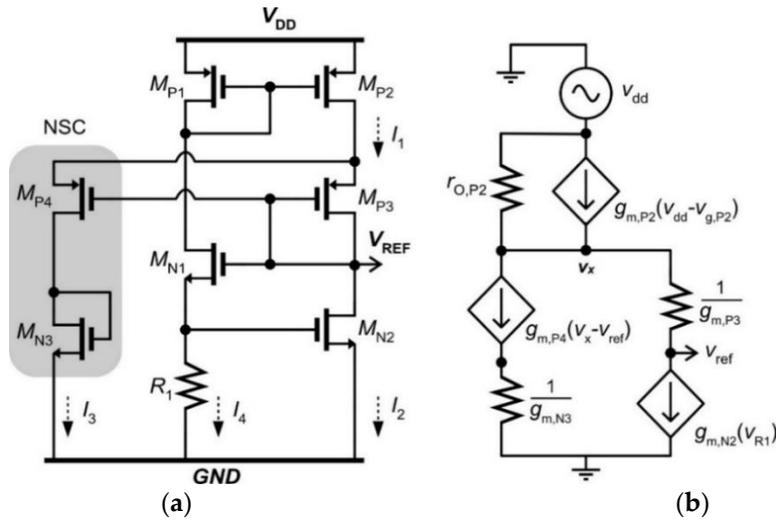


Figure 2. (a) Proposed reference circuit and (b) its small-signal equivalent circuit.

Rearranging Equation (4) gives:

$$V_{GS,N1} = \sqrt{\frac{2I_4}{K_{n,N1}}} \cdot \frac{1}{(1 + \lambda_{N1}V_{DS,N1})^{\frac{1}{2}}} + V_{TH,N1} \quad (5)$$

and taking the derivative of $V_{GS,N1}$ with respect to $V_{DS,N1}$ results in:

$$\frac{\partial V_{GS,N1}}{\partial V_{DS,N1}} = -\sqrt{\frac{2I_4}{K_{n,N1}}} \cdot \frac{\lambda_{N1}}{2(1 + \lambda_{N1}V_{DS,N1})}. \quad (6)$$

By approximating $\frac{\partial V_{DS,N1}}{\partial V_{DD}} = 1$, we obtain, from Equation (6),

$$\frac{\partial V_{GS,N1}}{\partial V_{DS,N1}} = \frac{\partial V_{GS,N1}}{\partial V_{DD}} \quad (7)$$

From Figure 2a, we know that:

$$I_2 = I_1 - I_3. \quad (8)$$

The NSC senses the voltage variation at the source terminals of M_{P3} and M_{P4} by assuming that V_{REF} is constant and that the nonlinear current in I_1 sinks into M_{P4} leaving a linear current in M_{P3} . By assuming that I_1 and I_3 grow linearly with respect to V_{DD} , we can rewrite I_2 in Equation (8) as follows:

$$\begin{aligned} I_2 &= m_1V_{DD} + C_1 - (m_3V_{DD} + C_3) \\ &= V_{DD}(m_1 - m_3) + (C_1 - C_3), \end{aligned} \quad (9)$$

where m_1 and m_3 are the slopes of I_1 and I_3 , respectively, and C_1 and C_3 are constant values. I_2 can also be written as:

$$I_2 = \frac{1}{2}k_{n,N2}(V_{GS,N2} - V_{TH,N2})^2. \quad (10)$$

By substituting Equation (9) into (10), Equation (10) becomes:

$$V_{DD}(m_1 - m_3) + (C_1 - C_3) = \frac{1}{2}k_{n,N2}(V_{GS,N2} - V_{TH,N2})^2. \quad (11)$$

Rearranging Equation (11) for $V_{GS,N2}$ gives:

$$V_{GS,N2} = \sqrt{\frac{2}{K_{n,N2}}} \cdot \sqrt{(m_1 - m_3)V_{DD} + (C_1 - C_3) + V_{TH,N2}} \quad (12)$$

and taking the derivative of $V_{GS,N2}$ with respect to V_{DD} results in:

$$\frac{\partial V_{GS,N2}}{\partial V_{DD}} = \sqrt{\frac{2}{K_{n,N2}}} \cdot \frac{(m_1 - m_3)}{2\sqrt{(m_1 - m_3)V_{DD} + (C_1 - C_3)}}. \quad (13)$$

Substituting Equations (6) and (13) into (3) produces:

$$-\sqrt{\frac{2I_4}{K_{n,N1}}} \cdot \frac{\lambda_{N1}}{2(1 + \lambda_{N1}V_{DS,N1})} + \sqrt{\frac{2}{K_{n,N2}}} \cdot \frac{(m_1 - m_3)}{2\sqrt{(m_1 - m_3)V_{DD} + (C_1 - C_3)}} = 0. \quad (14)$$

A key parameter of interest in Equation (14) is m_3 . To satisfy the condition in Equation (2), m_3 in Equation (14) can be controlled by adjusting the size of transistor M_{P4} . The slope of m_3 should be less than m_1 , so that the first term of Equation (14) can be subtracted to zero. Trimming the transistor's width and length can be performed by the Cadence Spectre simulation to optimize the output voltage variation.

2.2. Dynamic Analysis

The dynamic behavior of the proposed circuit can be determined by analyzing the equivalent circuit shown in Figure 2b. M_{N1} and R_1 form a source follower. For simplifying the design equations, we presume that $g_{m,N1}R_1 \gg 1$; as a result, v_{R1} is close to v_{ref} and $v_{g,p2}$ can be approximately equal to v_{dd} . From Figure 2b, by applying Kirchhoff's current law at node v_x , we can derive the following equation:

$$\frac{v_{dd} - v_x}{r_{o,P2}} = g_{m,P4}v_x + v_{ref}(g_{m,N2} - g_{m,P4}). \quad (15)$$

v_x can be derived from the circuit given as:

$$v_x = v_{ref} \left(\frac{g_{m,N2} + g_{m,P3}}{g_{m,P3}} \right) \quad (16)$$

By substituting Equation (16) into (15), the ratio of v_{ref} to v_{dd} can be obtained as follows:

$$\frac{v_{ref}}{v_{dd}} \approx \frac{g_{m,P3}}{r_{o,P2}(g_{m,N2} \times g_{m,P4} + g_{m,N2} \times g_{m,P3})} \quad (17)$$

Accordingly, Equation (17) shows that v_{ref} becomes decoupled from small variations in v_{dd} when the output resistance of $r_{o,P2}$ is sufficiently high. The NSC produces the $g_{m,P4}$ in the denominator of Equation (17), which can help improve the PSRR performance.

Table 1 shows all the parameters used in the proposed reference circuit in Figure 2b.

Table 1. Component parameters.

Component	Parameter	Component	Parameter
M_{P1}, M_{P2}	$W = 4 \mu\text{m}, L = 1 \mu\text{m}, m = 50$	M_{N2}	$W = 25 \mu\text{m}, L = 3 \mu\text{m}, m = 4$
M_{P3}	$W = 1.15 \mu\text{m}, L = 1 \mu\text{m}, m = 1$	M_{N3}	$W = 4 \mu\text{m}, L = 1 \mu\text{m}, m = 20$
M_{P4}	$W = 4 \mu\text{m}, L = 1 \mu\text{m}, m = 9$	R_1	70 k Ω
M_{N1}	$W = 4 \mu\text{m}, L = 1 \mu\text{m}, m = 10$		

3. Simulation and Measurement Results

The proposed supply independent voltage reference circuit was fabricated using SK Hynix 0.35 μm CMOS technology. The micrograph of the proposed reference circuit is displayed in Figure 3a, and it occupies an active area of 0.0131 mm^2 . Figure 3b illustrates the transient response of the output voltage V_{REF} when V_{DD} is ramped from 0 to 5 V. When the current starts flowing in the circuit, the self-biasing reference circuit drives itself towards the desired stable state, according to the measurement, the output voltage starts settling at 1.37 V when V_{DD} reaches over 2 V.

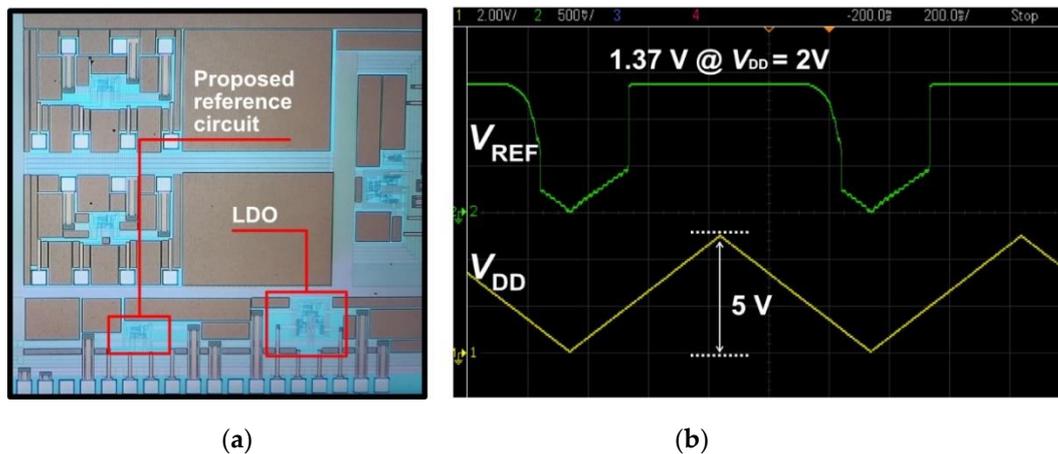


Figure 3. (a) Micrograph of the proposed reference circuit, (b) measured transient response.

The measured output voltage variation with respect to V_{DD} is plotted in Figure 4a. The inset graphs show the measured and simulated results when V_{DD} varies from 2 V to 5 V and 0 to 30 V, respectively. The observed output voltage increases linearly by 10 mV for V_{DD} variation from 2.1 V to 5 V. This results in a line regulation of 3.45 mV/V. This dependency can be further optimized by adjusting M_{P4} , as indicated in Equation (14). The simulation shows a stable reference voltage even when V_{DD} reaches up to 30 V. However, the measurement was stopped by the breakdown voltage of ~ 6 V for transistors. The variation of V_{REF} between 2.4 V to 30 V for V_{DD} is only 11 mV, which results in a line regulation of 0.4 mV/V. The measured and simulated PSRR of the proposed reference circuit is displayed in Figure 4b, where we obtain the simulated PSRR of -67 dB without the NSC block and -112 dB with one, respectively. This shows that the nonlinear current sink circuit we proposed in this work works as expected. In reality, however, a maximum PSRR of -93 dB is observed for frequencies lower than 1 kHz. The difference of -19 dB between the simulation and measurement is probably due to the parasitic capacitance that arises from the metal lines and pads in the fabricated chip, where our proposed reference circuit shares the power supply rails of other test blocks.

Figure 5a illustrates 500 Monte Carlo simulation results of the reference voltage. The average reference voltage, μ , and the standard deviation, σ , are 1.3955 V and 66.15 m, respectively. The line regulation results in different corners are shown in Figure 5b. The results indicate that the effectiveness of NSC produces stable reference voltage in all corners. The worst case occurs in SS condition in which the line regulation of 34.4 mV/V is obtained for V_{DD} variation from 2.1 V to 5 V.

The overall electrical performance of the CMOS reference circuit designed in this work is summarized in Table 2, where it is also compared with the performances of the prior designs presented in [14–17].

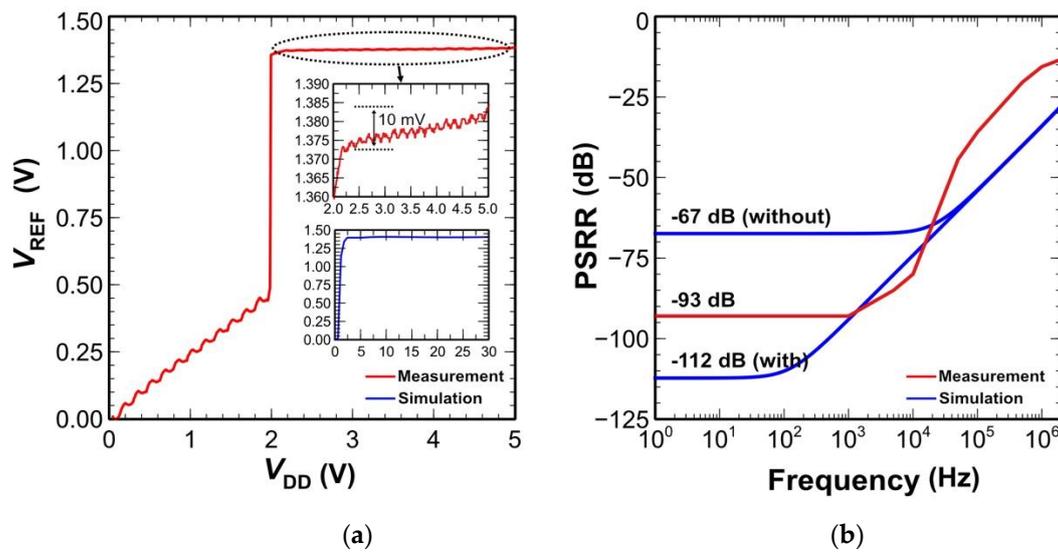


Figure 4. Measured results of (a) line regulation and (b) power supply rejection ratio (PSRR).

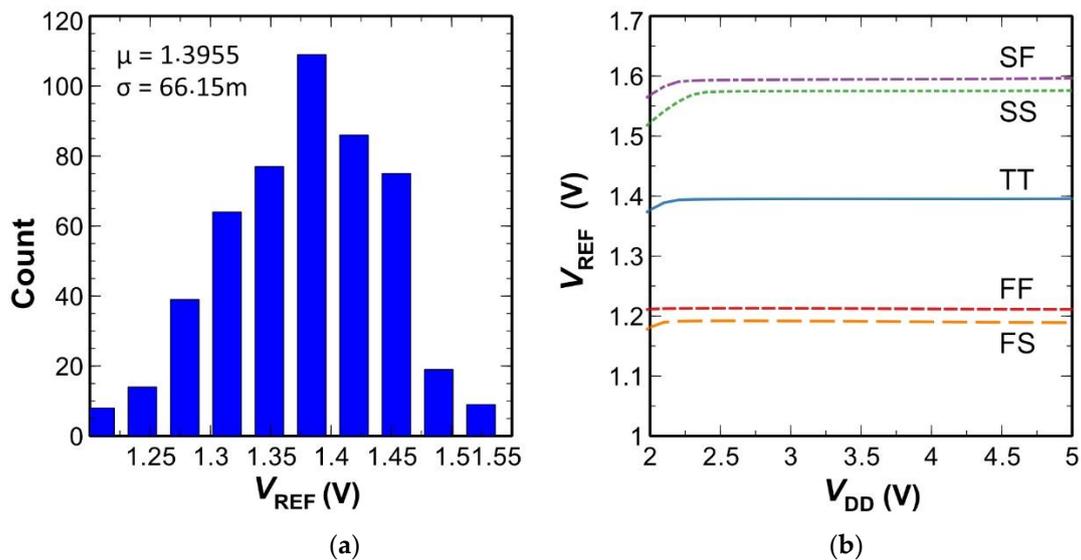


Figure 5. (a) 500 Monte Carlo simulation results at 3.3 V supply, 27 °C; (b) line regulation results in different corners.

Table 2. Electrical performance summary and comparison of reference circuit with previous designs.

Parameter	[14]	[15]	[16]	[17]	This Work
Supply voltage range (V)	2 to 5	0.5 to 1	1.3 to 1.8	2.6 to 12 (2.4 to 20) *	2.1 to 5 (2.4 to 30) *
Reference output voltage (V)	1.14055	0.495	1.17	1.6	1.37
Line regulation (mV/V)	2	3.2	0.35	0.957 (0.511) *	3.45 (0.39) *
PSRR (dB)	-61	-50	-52	-60 (-59.2) *	-93 (-112) *
Chip Area (mm ²)	0.0396	0.0522	0.082	-	0.0131
Technology (μm)	0.35	0.065	0.18	1.6	0.35

* Simulation result.

To verify the real performance of the proposed reference circuit, we applied it to the low-voltage-drop regulator (LDO) circuit plotted in Figure 6a. This LDO circuit that utilizes an output ringing compensation circuit was fabricated in the same chip displayed in Figure 3a. The output

of the LDO provides a positive supply voltage to 64 pixels stimulator circuit which requires maximum current of 10 mA. This requirement is based on our previous work which can be found in [10]. In the experimental setup to evaluate the line-transient responses of LDO, a 100 Ω resistor was chosen as a load for the LDO output terminal so that the load current is larger than 10 mA. When we applied a ramp voltage varying from 0 to 5 V, the LDO still output a constant voltage of 1.62 V, as shown in Figure 6b, while the reference circuit output 1.37 V. While maintaining a load current of 16.2 mA, the LDO output variation was observed as 17.6 mV in the supply range from 2.5 V to 5 V. The overshoot and undershoot voltages were 80 mV and 100 mV, respectively, as illustrated in Figure 6c. This LDO also had a fast recovery time of 240 ns, corresponding to the rapid change of V_{DD} from 5 V to 5.2 V in 20 ns. Presently, we evaluated the full-path system using separate chips for LDO, digital controller and stimulator shown in Figure 7.

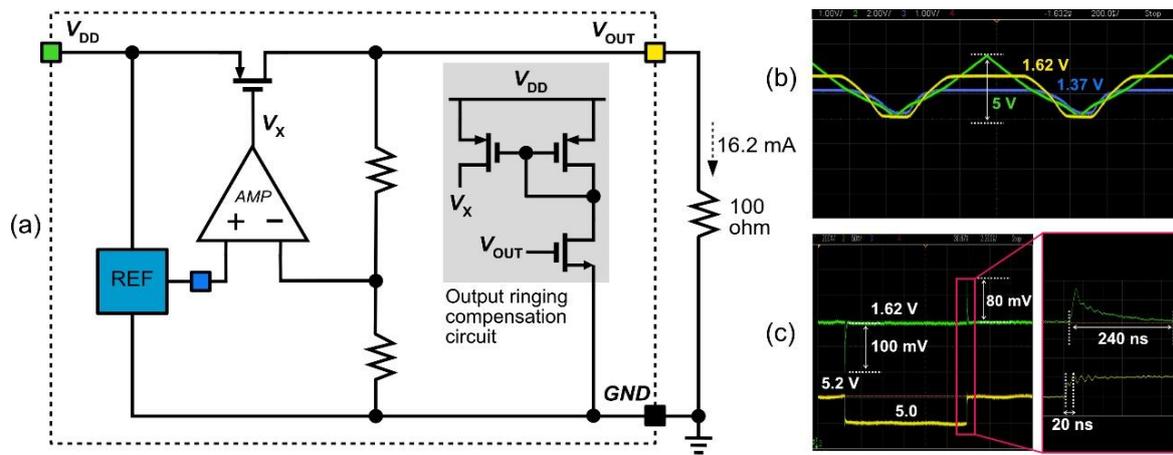


Figure 6. (a) Low-voltage-drop regulator (LDO) circuit incorporating the proposed reference circuit; (b) measured line-transient responses; and (c) measured overshoot and undershoot voltages.

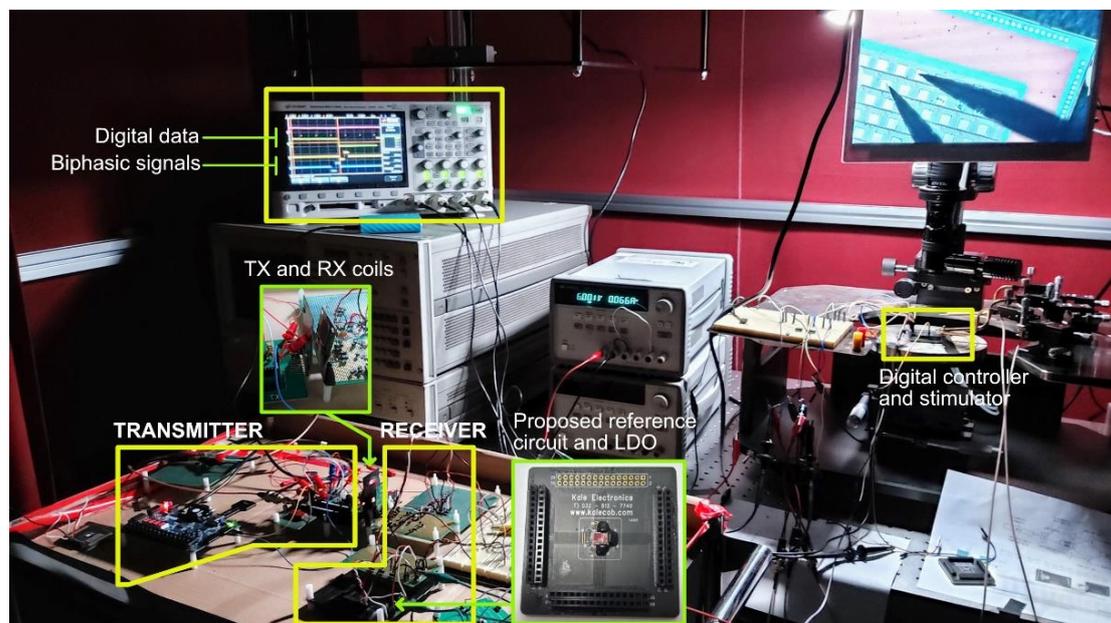


Figure 7. Full-path prosthetic system experimental setup.

In the near future, the proposed voltage-reference circuit working with the LDO can be applied to fully integrated retinal prosthetic systems. Our proved concept prototype system could be further miniaturized and potentially transformed into stretchable devices which is beyond the flatland constrain

of the traditional wafer-based system. Currently, we have developed a stretchable receiving coil and are progressively working on flexible microelectrode arrays.

4. Conclusions

In this paper, a novel CMOS voltage-reference circuit with high PSRR and wide-range supply independence was proposed and designed for a subretinal prosthetic system. The proposed NSC reduced the supply ripples significantly and sank out undesired signals in the reference voltage. Experimental results exhibited good agreement with the proposed concept and demonstrated better performance in supply independence and PSRR, when compared to the previous works. The proposed circuit provided a constant output voltage of 1.37 V and exhibited 10 mV variations over the supply range from 2.1 V to 5 V, resulting in a line regulation of 3.45 mV/V. The maximum PSRR was observed to be -93 dB for frequencies below 1 kHz. The current proof-of-concept prototype was implemented on a single chip with the LDO circuit, using a standard $0.35\ \mu\text{m}$ CMOS process. The proposed reference design occupied an active area of $0.0131\ \text{mm}^2$. Considering the high precision and small size design, this novel reference circuit can be used for implantable devices such as retinal prostheses and cochlear implants. As a future work, we will integrate the proposed reference circuit and LDO onto a single chip along with other functional blocks such as a demodulator, digital control, and high-density stimulator array.

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