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Investigation of Inhibited Channel Potential of 3D NAND Flash Memory According to Word-Line Location

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Abstract: Natural local self-boosting (NLSB) was analyzed according to the location of a selected word-line (WL) where potential boosting occurs. When the same pattern occurred, it was found that the top cells (WL11 through WL15) and bottom cells (WL0 through WL4) have identically symmetrical potential boosting. In addition, in the region of the middle cells (WL6 through WL10), a slight change in the potential boosting was also almost the same. In the 3D NAND, where there was a dummy WL (DWL), the NLSB for the edge WL changed as the pattern of the DWL changed. The DWL did not affect the NLSB of the main cell, regardless of the pattern. Therefore, the high potential of the edge WL could reduce the potential difference between the main cell and the edge WL using the DWL.

Keywords: 3D NAND flash memory; word-line (WL); natural local self-boosting (NLSB); dummy word line (DWL)

1. Introduction

In many major markets, NAND flash memory is widely used in electronics that require high density and low power storage and demand is growing. However, the 2D NAND development environment faces device scaling issues such as intercell interference and lithography limitations [1–4]. Therefore, 2D NAND flash memory technology was replaced by 3D NAND flash memory technology with a vertical stacked structure. This 3D NAND flash memory is solved by increasing the capacity by stacking cells vertically. The structure of 3D NAND flash memory is based on an ultra-thin body (UTB) structure in which the channel of the main cell is not connected to the body, and body bias is not applicable to the channel of the main cell. This can cause the channel to float, resulting in the down coupling phenomenon (DCP) and natural local self-boosting (NLSB) phenomena [5–8]. When program voltage (V_{PGM}) is applied to selected word-line (WL) of 3D NAND flash memory, program operation should not be performed on the selected WL of inhibit string. In this case, the channel potential is decreased due to the NLSB effect in selected cells of inhibited string. The development of current technology is a situation whereby the stack of 3D NAND is increasing. The uniform occurrence of program disturbances in each WL is one of the very important focuses for NAND Flash reliability. In order to control such program disturbance, it is necessary to further study the NLSB generated for each WL. Moreover, the maximum potential boosting of NLSB at an edge WL can cause secondary problems such as hot carrier injection (HCI) [9]. Previous studies analyzed how the NLSB phenomenon occurs when the bias applied to the selected WL or the pattern of adjacent cells changes [10–13]. In this study,

the top cells (WL11 through WL15), middle cells (WL6 through WL10) and bottom cells (WL0 through WL4) were divided and the NLSB generated by the WL was analyzed [14–16]. Therefore, it is necessary to explain the different potential boosting phenomena occurring at each WL. We also analyzed the change in potential boosting when adding a dummy WL (DWL) [17–19]. This phenomenon was analyzed using a technical computer aided design (TCAD) simulation (ATLAS Silvaco) [20].

2. Structure and Simulations

Figure 1a shows the structure of 3D NAND with 16 WL, select string line (SSL), and ground string line (GSL). To see the NLSB for each WL according to the pattern, the value of each pattern E, P1, P2, and P3 represents the threshold voltage (V_T) of WL, and E = −1 V, P1 = 1 V, P2 = 2 V, and P3 = 3 V. When the V_{PASS} is applied to the adjacent WL (P3 pattern) of WL 8 (E pattern), which drops from 6 V, the phenomenon of channel floating occurs in which the body bias is not applied to the channel when the V_{PASS} does not exceed the V_T of the adjacent WL. At this time, the transistor is turned OFF and the channel of selected WL is floating, as shown in Figure 1b. Here, DCP occurs as much as V_T of cell when the voltage of the adjacent WL is further reduced to 0 V. After that, the floating state is maintained and V_{PASS} is applied to all WLs so that the channel potential is increased by capacitive coupling. After the V_{PGM} is applied to the selected WL and the voltage is increased to 18 V, electrons of the channel are collected into the selected WL channel by the potential difference of the WL. This results in a sharp increase in the potential in the selected WL channel. This phenomenon is called NLSB and the timing diagram where these events occurred is shown in Figure 1c.

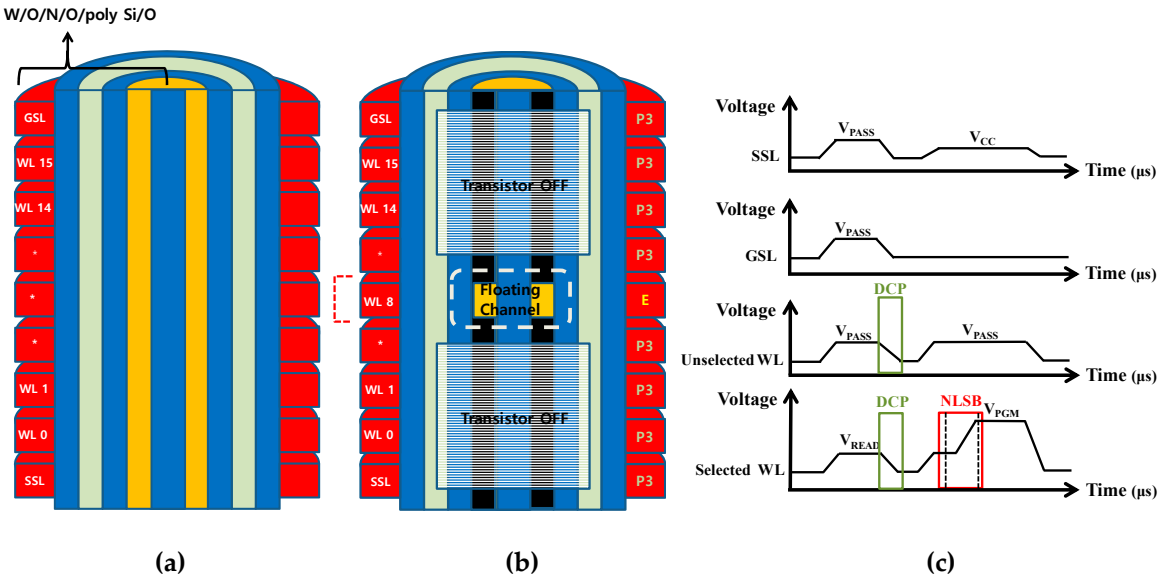


Figure 1. (**a**) Structure of 3D NAND with 16WL, select string line (SSL) and ground string line (GSL) transistors; (**b**) the explanation of channel floating behavior; (**c**) bias timing diagram when NLSB occurs.

In this paper, TCAD simulation was performed to observe NLSB for each WL in 3D NAND Flash memory. The parameters were used based on the simulation data validated in the previous study, and Table 1 lists the parameters used in the TCAD simulation [7,8]. In addition, 16 WL, GSL, and SSL composed the entire 3D NAND string and the internal structure is the same as in the previous research.

Table 1. Three-dimensional NAND device parameters, bias condition.

Device Parameter	Value
V_{CC}	2.4 V
V_{PASS}	6 V
V_{PGM}	18 V
Gate length (WL)	40 nm
Gate length (transistor)	150 nm
Channel hole diameter	80 nm
Poly Si Channel	10 nm
Oxide/Nitride/Oxide	4/8/8 nm

For 3D NAND, the analysis of NLSB by WL in Figure 2a shows that the potential decreases gradually toward the main cell with the largest potential at edge WL. In Figure 2a, the selected WL is patterned with E and the unselected WL is patterned with P3. Comparing Figure 2a,b, the top and bottom cells symmetrically produced the same channel potential according to the WL. The channel of the edge WL is adjacent to the doped region; therefore, when the NLSB occurs, the carrier of the doped region is over, causing more boosting. The phenomenon gradually decreases toward the main cell WL8.

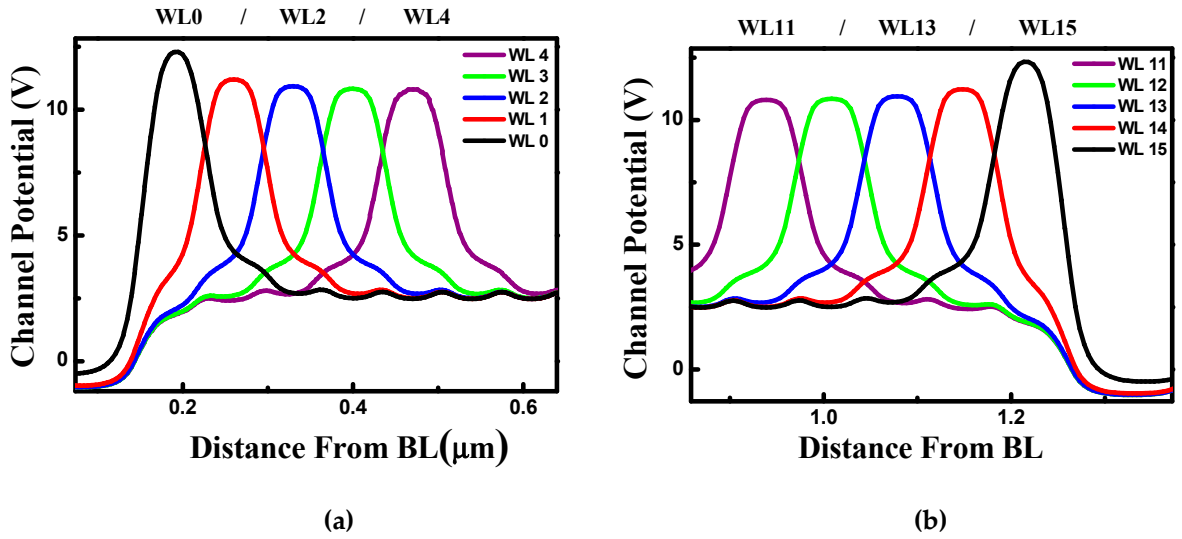


Figure 2. NLSB in WL (**a**) NLSB occurring in the bottom cells (WL0 through WL4), and (**b**) NLSB occurring in the top cells (WL11 through WL15).

Figure 3 shows the potential boosting of each WL in the middle cell section. The selected WL is patterned with E and the unselected WL is patterned with P3. Unlike the top and bottom cells, there was no difference in potential boosting for each WL and the same channel potential of 10.8 V.

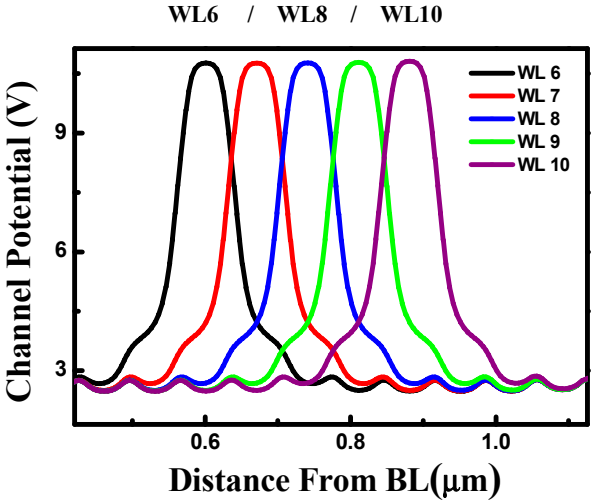
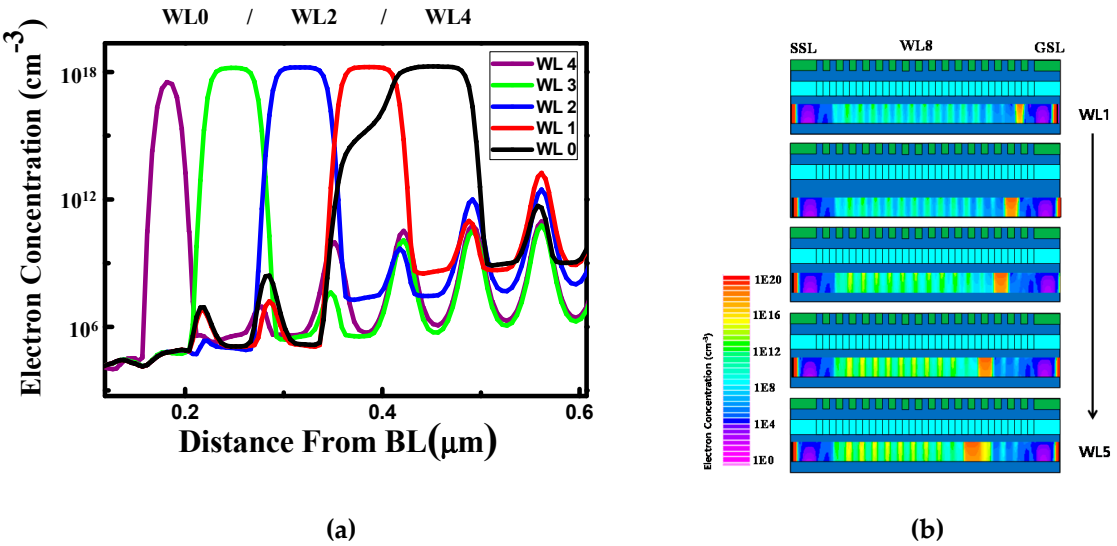


Figure 3. NLSB that occurs for each WL generated in the middle cell (WL11 through WL15).

The electron concentration in Figure 4a is the channel concentration at *t1* in Figure 1b. In this case, electrons are not trapped in the channel to the floating gate, so the electron concentration in the channel is high. Figure 4b shows that the electron concentration is more widely distributed in the channel toward the main cell than the edge WL. This is because the channel concentrates electrons from the adjacent WL with the V_{PASS} to the selected WL with the V_{PGM}. At this time, the closer to WL8 from WL0 through WL8, the more widely distributed the electron concentration. This is because as the number of adjacent WLs increases, more electrons can be collected in the selected WL.

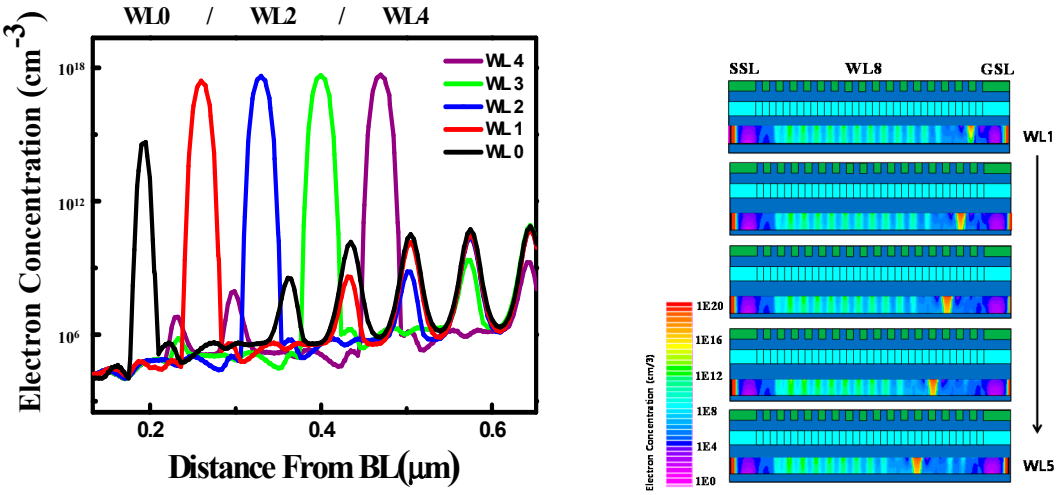


(a) **(b)**

Figure 4. Electron concentration of the 3D NAND when the V_{PGM} reaches 7.8V (**a**) electron concentration of each WL and (**b**) electron concentration profile of the channel in the real simulation device.

Figure 5a shows the electron concentration of the channel at point *t2* in Figure 1b. When the V_{PGM} is 18 V, the electrons in the channel trap to the floating gate a lot and the electrons in the channel is smaller than in Figure 4 [17]. Figure 5b shows the electron concentration in the channel in the simulation device. The figure shows that the channel of WL0 has considerably fewer electrons than in Figure 4. The potential boosting by NLSB occurs, and it is lower than the maximum concentration of 10^{18} compared with other WLs. This means that the concentration of electrons is lower because the number of adjacent WLs is fewer than the number of main cells, so if the electrons are trapped in the floating gate because of V_{PGM} as other WLs are, the concentration of WL0 is lower. Figure 1 also

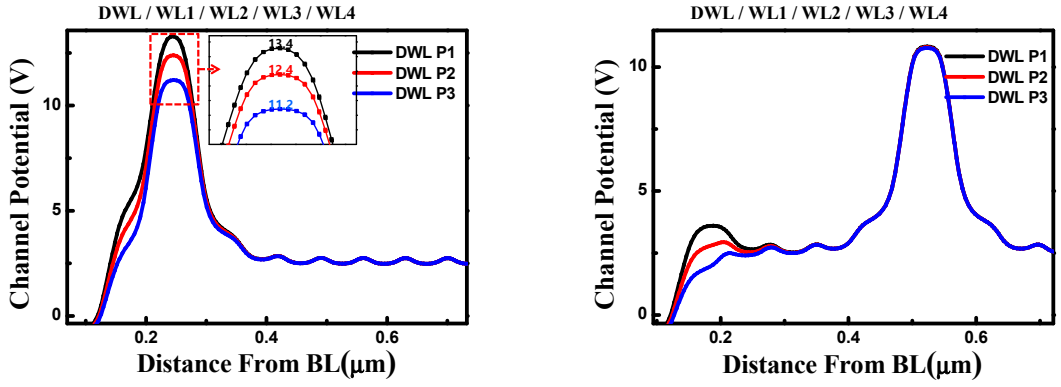
shows that the boosting potential of WL0 is the largest, which leads to a further drop in the electron concentration of WL0, which is relatively less than that of the other WL. Therefore, the high boosting potential of edge WL resulted in the HCI phenomenon, which reduced the electron concentration [9].



(a) (b)

Figure 5. Electron concentration of the 3D NAND channel when V_{PGM} reaches 18V (**a**) electron concentration of each WL and (**b**) electron concentration profile of the channel in the real simulation device.

Figure 6 shows the analysis of NLSB by WL when DWL is present in 3D NAND. Figure 6a shows the boosting potential at edge WL while the pattern at the DWL changes. Under these conditions, the NLSB of WL0 had the highest potential in the NAND channel with the DWL of the P1 pattern. This is because the NAND of the P3 pattern started at a low channel potential because of the DCP. Therefore, the NAND channel with a P3 pattern DWL had a low potential. In addition, Figure 6b shows the boosting potential of WL4 under the same conditions as in Figure 6a. The figure shows no change in potential rise. Because the pattern of the DWL is far from the main cell, the DWL cannot affect the main cell. As a result, the high edge potential can be controlled by using the DWL.



(a) (b)

Figure 6. Three-dimensional NAND environment where a DWL exists, and where the NLSB is analyzed changing the pattern of the DWL (**a**) NLSB for the pattern of DWL at edge WL and (**b**) NLSB for the pattern of DWL in WL4 close to the main cell.

3. Conclusions

NLSBs occurring in 3D NAND flash memory were investigated. Such phenomena and characteristics as NLSB were analyzed in a TCAD simulation. When all WLs had the same pattern, they had the largest boosting potential at the edge WL and appeared to decrease gradually as they approached the main cell. The lowest electron concentration was seen at the edge WL after the V_{PGM} was applied. This is because HCI occurred because of the highest potential boosting at the edge WL. If the DWL is present, one can adjust the potential boosting of the edge WL without affecting the main WL potential. Therefore, using the DWL reduces the potential difference between the main WL and edge WL. This reduces the HCI phenomenon and creates uniform potential boosting in the overall WL.

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