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A 28 GHz Highly Linear Up-Conversion Mixer for 5G Cellular Communications

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Abstract: In this paper, we present a highly linear direct in-phase/quadrature (I/Q) up-conversion mixer for 5G millimeter-wave applications. To enhance the linearity of the mixer, we propose a complementary derivative superposition technique with pre-distortion. The proposed up-conversion mixer consists of a quadrature generator, LO buffer amplifiers, and an I/Q up-conversion mixer core and achieves an output third-order intercept point of 15.7 dBm and an output 1 dB compression point of 2 dBm at 27.6 GHz, while it consumes 15 mW at a supply voltage of 1 V. The conversion gain is 11.4 dB and the LO leakage and image rejection ratio are −56 dBc and 61 dB, respectively, in the measurement. The proposed I/Q up-conversion mixer is suitable for 5G cellular communication systems.

Keywords: 5G; 28 GHz; 1 dB compression point; CMOS; cellular communication; complementary derivative superposition; image-rejection; linearity; LO leakage; third-order intercept point

1. Introduction

Recently, millimeter-wave (mm-wave) transceivers have been intensively researched for multi-Gb/s data transfer with low-latency and high reliability [1–8]. For fifth-generation (5G) cellular communications, n260 (37~40 GHz) and n257 (26.5~29.5 GHz) mm-wave bands are allocated for 5G applications [9–11]. Transceiver systems [1–8] have successfully demonstrated 5G cellular communications using mm-wave bands. The transceivers for mm-wave 5G cellular communications use phased arrays to enhance communication distance and coverage to non-line-of-sight propagation [5–8].

The direct conversion transceiver is popular since it reduces the power consumption and chip area. In the transmitter, one of the most important key blocks is the in-phase/quadrature (I/Q) direct up-conversion mixer. Local oscillator (LO) leakage and I/Q mismatch of the mixer severely degrade the error vector magnitude (EVM) performance. Moreover, a high linearity mixer is required for the minimum stages of the power amplifier to provide a small chip area and low DC power consumption.

Linearity enhancement techniques with a dual-gate mixer, an adaptive biasing circuit, inductive degeneration, and LO boosting linearization have been reported for a higher 1-dB compression point (P1dB) [12–15]; however, these techniques are limited by an output P1dB (OP1dB) of less than 0 dBm and hence limited by the third-order intercept point (IP3). To enhance IP3 performance of the up-conversion mixer, second-order intermodulation (IM2) injection and single stack transistor are used [16,17]. However, the IM2 injection degrades the conversion gain (CG) and the single-stack transistor consumes a huge amount of DC power from a large LO signal. Furthermore, the output IP3 (OIP3) is than 11 dBm. To suppress the LO leakage and enhance the CG and image rejection ratio (IRR), transformers and high-precision polyphase filters are used [18,19]. These up-conversion mixers provide high LO leakage and IRR, but the linearity performance is limited.

This paper presents a highly linear direct I/Q up-conversion mixer designed for 5G applications operating in the 28 GHz frequency band. The proposed mixer utilizes a symmetric layout for the mixer core and complementary derivative superposition (DS)

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technique with pre-distortion to improve IRR, LO leakage, and linearity. The proposed mixer was implemented in 65 nm CMOS. The mixer achieves an OP1dB of 2 dBm and an OIP3 of 15.7 dBm at 27.6 GHz with a DC power consumption of 15 mW from a supply voltage of 1 V. The CG is 11.4 dB and the IRR and LO leakage are 61 dB and −56 dBc, respectively. This article is an extended version of [20], with an in-depth analysis.

2. Design of I/Q Up-Conversion Mixer

Figure 1 shows the block diagram of the direct up-conversion mm-wave transmitter. This architecture is widely adopted due to the low DC power consumption and small chip area compared to the heterodyne architecture [21]. One of the most important building blocks in the transmitter is the I/Q up-conversion mixer. Figure 2 presents the simplified block diagram of the proposed up-conversion mixer. The proposed mixer consists of a quadrature generator, mixer core, and two LO amplifiers. The quadrature generator is integrated to provide 0°/90°/180°/270° signals to the LO inputs of the mixer. The gain and phase mismatches of the quadrature generator and mixer core cause I/Q imbalance and EVM degradation. EVM due to I/Q imbalance can be expressed as

$$\mathrm{EVM_{I/Q}(dB)} = 10\log 10\left(\frac{\epsilon^2}{4} + \frac{\theta^2}{4}\right), \tag{1}$$

where ϵ is the gain error and θ is the phase error.

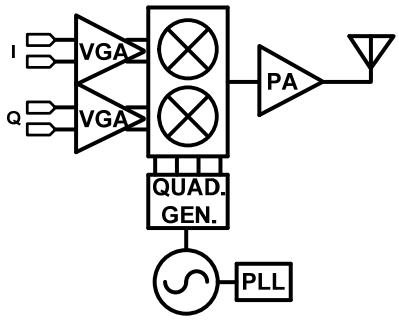

Figure 1. Block diagram of a direct up-conversion mm-wave transmitter.

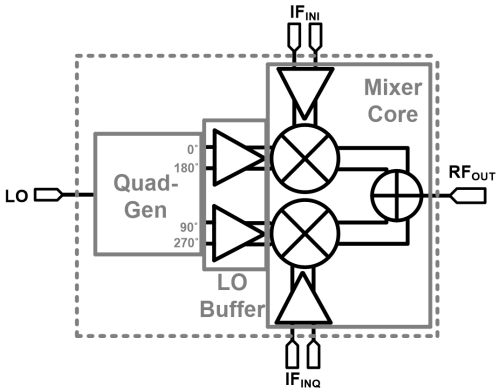

Figure 2. Block diagram of the fabricated I/Q up-conversion mixer.

Figure 3 shows the quadrature generator, which consists of a 90° phase generator and two active baluns. The resistive power divider splits the power equally without gain and phase errors in a small chip area at the cost of a 3 dB loss. A high-pass/low-pass structure gives 90° phase difference. Active baluns generate differential signals and reduce amplitude and phase errors. Even though the resistive power divider, 90° phase generator and the active balun provide acute I/Q signal generation in the simulation, temperature and process variations limit the signal quality. To overcome this issue, phase tuning and amplitude

tuning are introduced at the 90° phase generator and the active balun, respectively. In the 90° phase generator, a shunt capacitor bank and a varactor are used for coarse and fine tuning of the phase in the I-path, respectively, which provides continuous phase control of 18°. An active balun provides 6 dB gain control with 4 bit DAC. The active balun and the LO buffer amplifiers use differential common source amplifiers with inductive degeneration to provide fully differential outputs. The quadrature signals are generated at the quadrature generator and amplified by the LO buffer amplifiers to provide a 500 mVp-p voltage swing at the LO input port of the mixer from a −13 dBm LO input power.

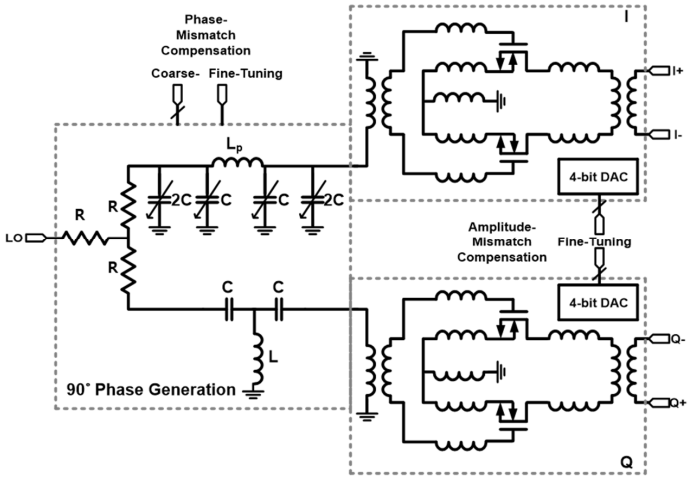

Figure 3. Schematic of a quadrature generator.

Figure 4 depicts the schematic of a mixer core and its intermodulation components in a two-tone test. To simultaneously achieve small LO leakage and high IRR, the mixer adopts the Gilbert-cell architecture. Unwanted mismatch of the layout degrades IRR and LO leakage performances. To minimize the LO leakage and IRR, the mixer core layout is set out in a symmetric way. Figure 5 shows the 2D and 3D layout for the switching stage of the mixer. The IF input is applied to the left and right sides with the two bottom metals and is isolated from the RF and LO signal lines using a ground middle metal. The output of the mixer core, RF, is obtained at the drain, on the top side, with the two top metals. LO inputs are connected to the gate of the switching stage, on the bottom side, with the top metal. As a result, the RF, LO, and IF signal lines are symmetric and they do not interfere each other, which enhances IRR and LO leakage performance.

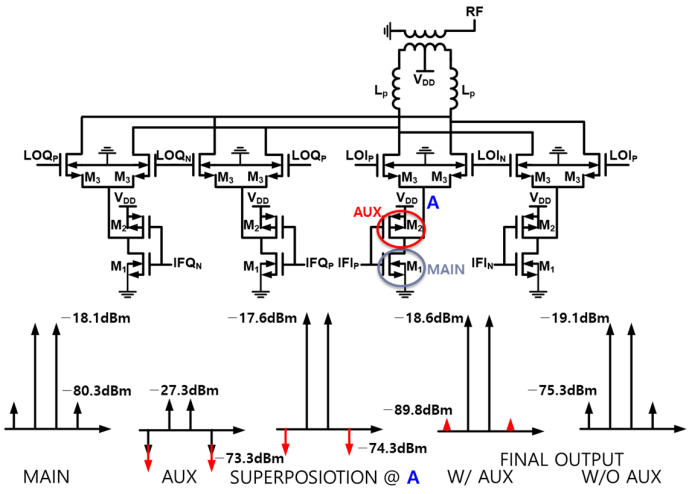

Figure 4. Schematic of mixer core and intermodulation components in the two-tone test.

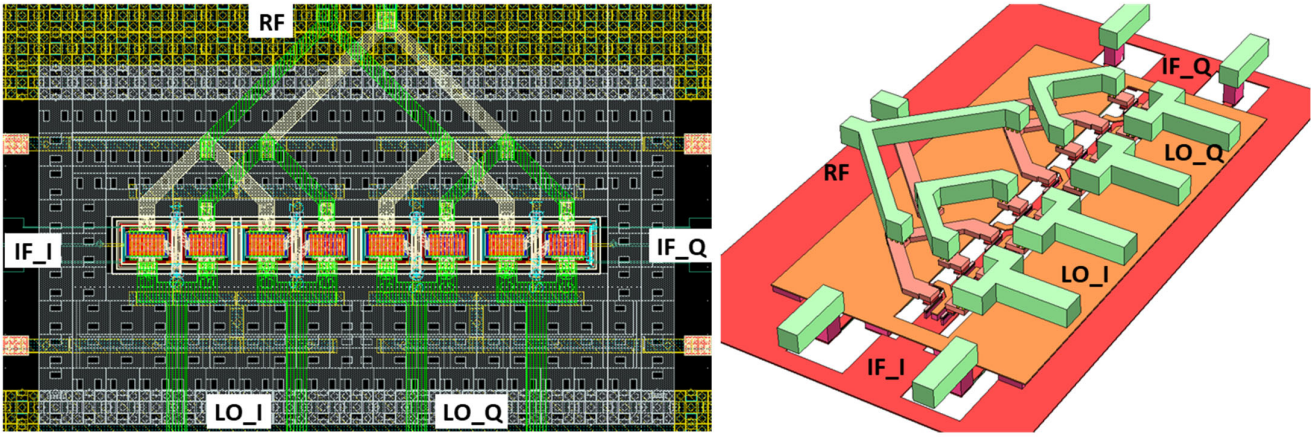

Figure 5. Two- and three-dimensional layout of switching stage.

In the transmitter, we need a high-linearity mixer to reduce the power consumption and the chip area by using fewer power amplifier stages. The switching stage is the main source of non-linearity in the Gilbert-cell mixer. To enhance linearity, we employ a complementary DS technique with pre-distortion. We add an auxiliary (aux) transistor M2 to the main transistor M1. The complementary DS technique [22] removes the third-order derivatives, gm3, of the current at the drain depending on the input voltage of both transistors, resulting in high OIP3 performance. Unlike the low noise amplifier in [22], we use M2 to cancel out the gm3 of not only M1 but also M3 in Figure 4. Without additional current, M2 also pre-distorts gm3 to enhance the linearity by minimizing the gm3 of M3. Moreover, M2 adds a power gain of 0.5 dB and reduces output third-order intermodulation distortion from −75.3 to −89.8 dBm at the input of −30 dBm, as shown in Figure 4.

The proposed I/Q up-conversion mixer is designed for a center frequency of 28 GHz and employs inductors and transformers in the matching network for low loss and compact design. All inductors, transformers, and interconnections are designed and optimized with electromagnetic simulation. The proposed up-conversion mixer uses the complementary DS technique to improve the linearity, resulting in 4 dB higher OP1dB and 8 dB higher OIP3 than the mixer without M2 in Figure 4. The simulation results show that the mixer achieves a CG of 11.4 dB, a 3 dB bandwidth of 2.7 GHz, an OP1dB of 2 dBm and an OIP3 of 17 dBm.

3. Fabrication and Measurement

The proposed mixer was designed and implemented in 65 nm CMOS technology. Figure 6 depicts a microphotograph of the proposed up-conversion mixer. The core area of the mixer, including the pads, was 1.232 mm^2. The up-conversion mixer core consumed 15 mW from a supply voltage of 1 V. The S-parameter, CG, P1dB, and OIP3 were measured on-wafer using ground–signal–ground and ground–signal–signal–ground probes. For the S-parameter measurement, the Keysight E8361A Vector Network Analyzer was used. As shown in Figure 7, CG, P1dB and OIP3 were measured with a signal generator, an arbitrary waveform generator (AWG) and a spectrum analyzer. In the measurement results, all losses of cables and probes were de-embedded.

Figure 8 depicts the simulated and measured CG gain versus IF frequency of the proposed mixer. An input frequency of 28 GHz and an input power of −30 dBm were applied to LO and IF, respectively. A measured CG of 11.4 dB was achieved with −13 dBm LO input power and 400 MHz IF frequency. A 3 dB bandwidth of 2.2 GHz was measured. Output and input return losses higher than 10 dB were achieved for LO and RF frequencies of 26–30 GHz and an IF frequency of 0.1–3 GHz, respectively.

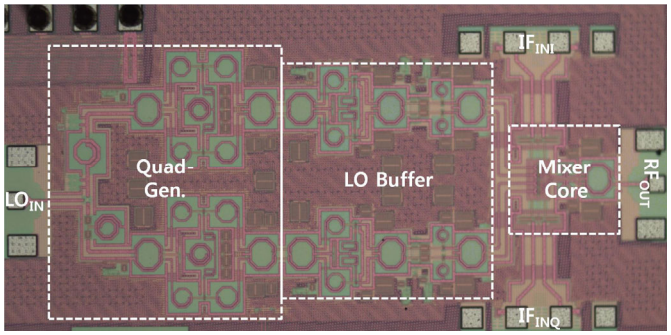

Figure 6. Chip microphotograph of proposed up-conversion mixer.

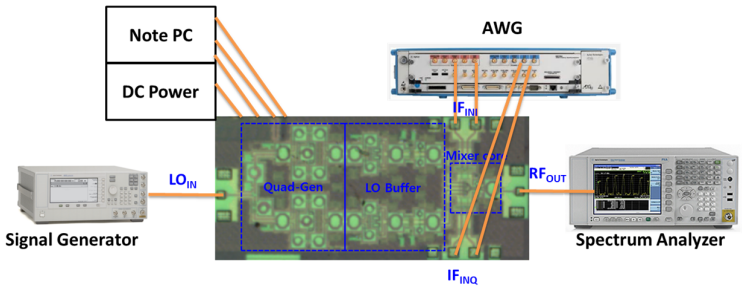

Figure 7. Measurement setup for CG, P1dB and OIP3.

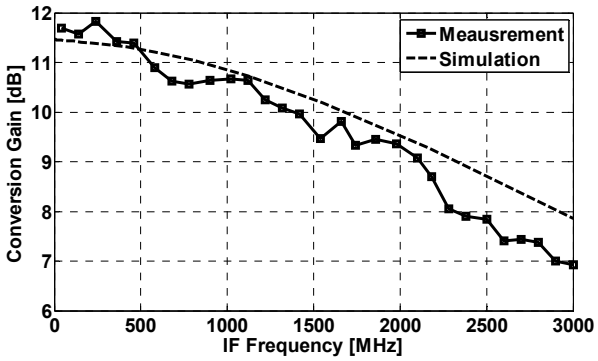

Figure 8. Simulated and measured mixer conversion gain versus IF frequency: f_{LO} = 28 GHz; P_{LO} = −13 dBm; P_{IF} = −30 dBm.

Figure 9 illustrates the measured and simulated CG of the proposed mixer with LO input power. The LO and IF frequencies were 28 GHz and 400 MHz, respectively, and an input power of −30 dBm was applied. A CG of 11.4 dB was measured at −13 dBm LO input power. Figure 10 shows the simulated and measured CG of the mixer with IF input power. The LO and IF frequencies were 28 GHz and 400 MHz, respectively. The measured OP1dB of the mixer was 2 dBm at −13 dBm LO input power.

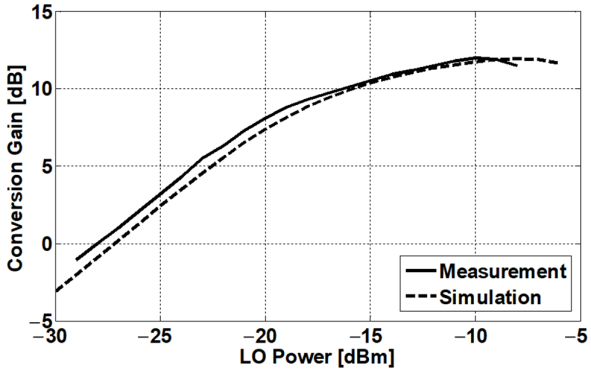

Figure 9. Measured and simulated conversion gain of mixer with respect to LO power: f_{LO} = 28 GHz; f_{IF} = 400 MHz; P_{IF} = −30 dBm.

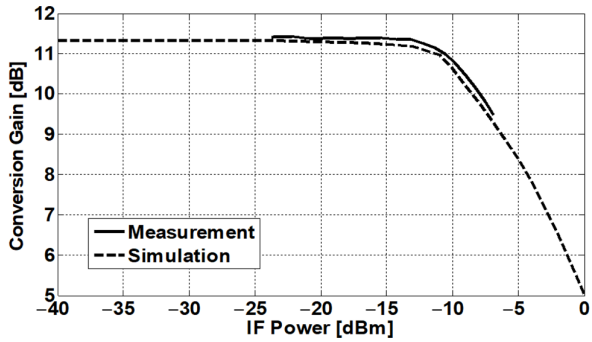

Figure 10. Measured and simulated conversion gain of mixer with respect to IF power: f_{LO} = 28 GHz; f_{IF} = 400 MHz; P_{LO} = −13 dBm.

Figure 11 shows the simulated and measured OIP3 with the input gate voltage and LO input power. Figure 12 depicts the measured output spectrum. The IF input gates of the mixer were biased at 0.53 V. An input power of −13 dBm with a frequency of 28 GHz was applied to LO and frequencies of 390 MHz and 400 MHz were selected for IF. An OIP3 of 15.7 dBm was measured. Figure 13 shows the measured output spectrum for the LO leakage and IRR test with 10 MHz IF frequency. The LO input power is −13 dBm at 28 GHz. The mixer achieved 61 dB IRR and −56 dBc LO leakage from a symmetrical-layout and accurate quadrature generator.

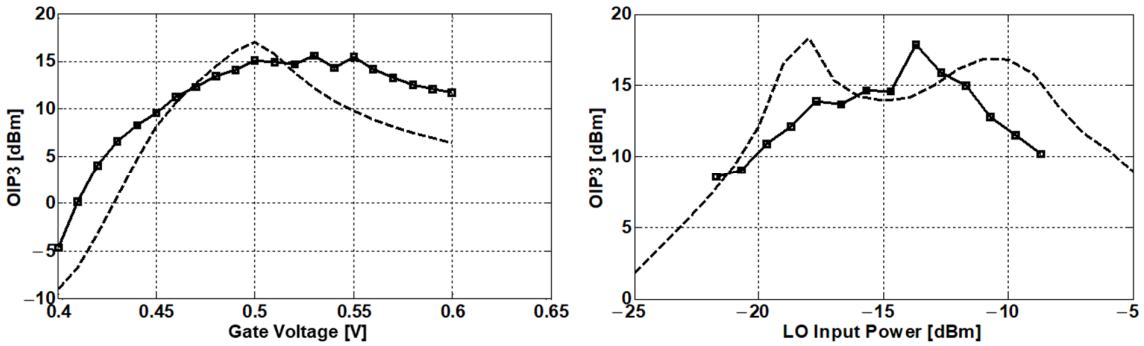

Figure 11. Simulated and measured OIP3 of mixer.

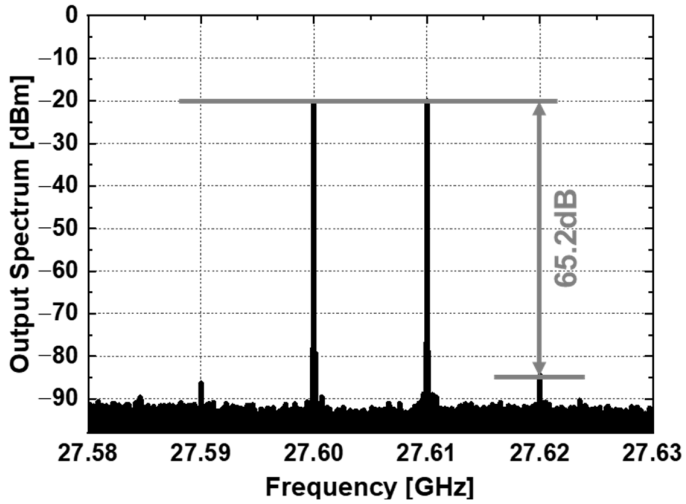

Figure 12. Measured output spectrum for OIP3: f_{LO} = 28 GHz; f_{IF1} = 390 MHz; f_{IF1} = 400 MHz.

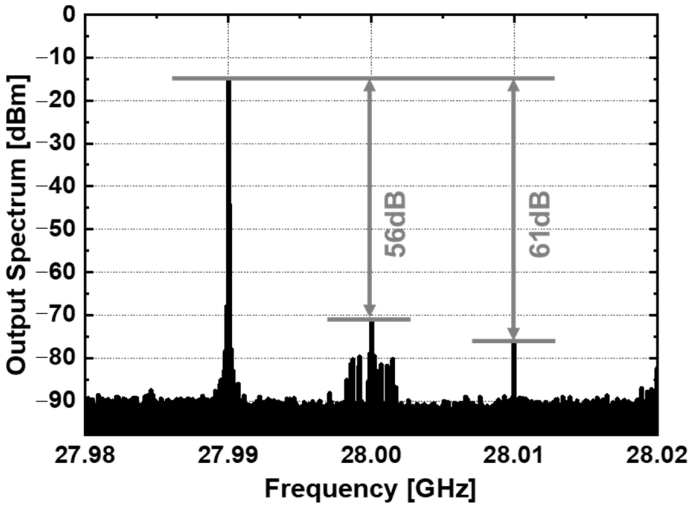

Figure 13. Measured output spectrum for LO leakage and IRR: f_{LO} = 28 GHz; f_{IF} = 10 MHz; P_{LO} = −13 dBm.

Table 1 compares the performance of several K-/Ka-band up-conversion mixers. To compare the overall performance of the mixers in Table 1, a figure of merit (FoM) [18], defined as

$$\mathrm{FoM} = 10\log\left(\frac{\mathrm{Gain(linear)}\cdot\mathrm{OP1dB(linear)}\cdot\mathrm{frequency(GHz)}}{\mathrm{P_{DC}(mW)}}\right), \quad (2)$$

was employed.

The proposed mixer, which uses the pre-distorted complementary DS technique, symmetric layout, and phase/amplitude control, achieved a higher OIP3 of 15.7 dBm, a higher OP1dB of 2 dBm, a higher CG of 11.4 dB, a lower LO leakage of −56 dBc, and a higher IRR of 61 dB than other works. As a result, the proposed mixer achieved higher FoM compared with other works in Table 1. The measurement results show that this work is suitable for 5G cellular communications.

Table 1. Performance comparisons of the state-of-the-art K-/Ka-band CMOS mixers.

	This Work	[12]	[13]	[14]	[15]	[16]	[17]	[18]	[19]
Process	**65 nm CMOS**	**130 nm CMOS**	**130 nm CMOS**	**65 nm CMOS**	**65 nm CMOS**	**28 nm CMOS**	**40 nm CMOS**	**65 nm CMOS**	**55 nm CMOS**
Topology	Pre-distorted complementary DS Gilbert-cell	Dual gate	Gilbert-cell	Gilbert-cell	Sub-harmonic dual ring	Gilbert-cell with IM2 Injection	Single-stack core Gm-boosting	Gilbert-cell	Gilbert-cell
Frequency (GHz)	28	18–28	23.4–29.2	28–35	27–44	17–29	24.2–29.5	26.5–29.5	20–42
CG (dB)	11.4	−2–0.7	−1.9	0.9–3.5	−10.5	−6.4	4.2–5.3	>22.2 *	1.2
OP1dB (dBm)	2	−5.2	0.3	−6.3	−9	−2.2	0.3	−5	−2.57
OIP3 (dBm)	15.7	5.8	-	1.93	-	10.2	10.8	4.6	-
LO Power (dBm)	−13	3	0	10	9	2	−10	−8	12
LO Leakage (dBc)	−56	-	-	-	-	-	-	−35 ##	-
LO-RF Isolation (dB)	56	>30	28.9	31.2	>45 #	-	-	-	>35
IRR (dB)	61	-	-	-	-	-	-	-	>30
P_{DC} (mW)	15	8	22.8	9.6	0	19	24.3	27.1	24
Area (mm^2)	1.23	0.47	0.86	0.77	0.33	0.48	0.59	1.09	0.58
FoM	9.68	6.72	3.27	8.13	-	1.82	5.02	9.33	3.88

* Including IF amplifier; # 2LO-RF isolation; ## 2LO leakage.

4. Conclusions

In this paper, we present a highly linear direct I/Q up-converter that was implemented in 65 nm CMOS technology. The proposed mixer utilizes a pre-distorted complementary DS technique, symmetric layout, and phase/amplitude control to enhance the linearity, LO leakage, and IRR performances. With this architecture, the proposed I/Q up-converter achieved a low LO leakage of −56 dBc, a high OIP3 of 15.7 dBm, and a high IRR of 61 dB at a DC power consumption of 15 mW, which proves that this work is suitable for 5G cellular communications.

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