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Finite Control Set Model Predictive Control (FCS-MPC) for Enhancing the Performance of a Single-Phase Inverter in a Renewable Energy System (RES)

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Abstract: A single-phase five-level T-type topology has been investigated in this article. This topology has emerged as a viable option for renewable energy systems (RES) due to its inherent benefits. The finite control set model predictive control (FCS-MPC) strategy has been implemented to this topology in order to improve the performance and overall reliability of the system. This control strategy empowers the inverter to predict future behavior based on a discrete set of control signals, enabling precise modulation and high-speed response to system dynamics. In the realm of RES, integration of FCS-MPC with multilevel inverters (MLIs) holds great potential to enhance energy conversion efficiency, grid integration, and overall system reliability. The article is structured to present an overview of the evolving landscape of power electronic systems, and the advantages of FCS-MPC. This paper provides a comprehensive analysis of the FCS-MPC control strategy applied to the single-phase five-level T-type topology. The study covers various aspects including the theoretical framework, hardware development, and experimental evaluation. It is obvious from the analysis that this inverter topology is reliable. Several redundant states make it fault-tolerant which helps in maintaining the output voltage at the same level even in the fault conditions. Additionally, the results show that the output load voltage is maintained at the same level irrespective of load change. Also, output load voltage has maintained the high-quality sinusoidal characteristics as the total harmonic distortion (THD) is very low. With all these features, this system is suitable within the framework of RES.

Keywords: renewable energy systems (RES); model predictive control (MPC); finite control set-MPC (FCS-MPC); multilevel inverter (MLI); T-type topology; deadband

MSC: 93B52; 94C11; 93B45

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1. Introduction

The escalating demands for energy production, distribution, and storage have triggered unprecedented advancements and research in power electronic systems. Increasingly, developments such as cheaper and more powerful microcontrollers, battery energy storage technologies, and wide-bandgap devices have made this technologically and economically feasible. Nevertheless, recent concerns about energy conservation, environmental protection, and achieving net zero emissions have further propelled this momentum. The emergence of renewable energy systems and enormous gains in demands of transportation electrification have also added to it [1]. This facilitates the need for more efficient, feasible,

and reliable power electronic converters, of which voltage source inverters (VSI) serve a key role. The applications encompass motor drives, power supplies, static compensators (STATCOMs), fast-charging, high-voltage direct current (HVDC) transmissions, and flexible AC transmission systems (FACTS) ranging from medium to high power (1 kW to several gigawatts) and medium-voltage to high-voltage levels (several hundred volts to several kVs) with continued advancements for even higher levels [2–4].

The applications of multilevel inverters (MLI) are depicted in Figure 1. MLIs are used in diverse domains such as electric vehicle (EV) and aircraft systems, railway transportation, renewable energy systems, and HVDC systems [5]. In these contexts, multilevel configurations have emerged as the favored architectures, supplanting conventional two-level structures. The first development of MLI was the Cascaded H-bridge (CHB) topology which was configured using multiple H-bridges to produce a multilevel output. Subsequently, Neutral-Point Clamped (NPC) and Flying Capacitor (FC) MLI followed in their wake [6–8]. Since then, a multitude of topologies that are either derived from these three structures or novel ones have been ventured. A wide range of MLI topologies have been proposed with varying quantities of semiconductor device count, levels, DC sources, and passive components. A comprehensive analysis of these topologies is necessary to evaluate the feasibility of these topologies for multiple applications. These topologies can be divided into multiple categories conforming to their structure. Topologies employing multiple independent DC sources are inherently complex to implement due to the necessity of isolation transformers and balancing complexities. Consequently, topologies with a single DC-link shared for all levels and across all three or five phases can more easily be realized for commercial applications. These topologies can be described as common DC-link topologies. The higher-frequency operation, switching losses, power density, ratings, and robustness of IGBTs and MOSFETs are immensely improved with wide bandgap semiconductor devices. The cost of wide-bandgap devices is significantly higher than conventional devices [9]. Therefore, topologies with a limited number of levels to find an optimal balance between level count and complexity are ideal.

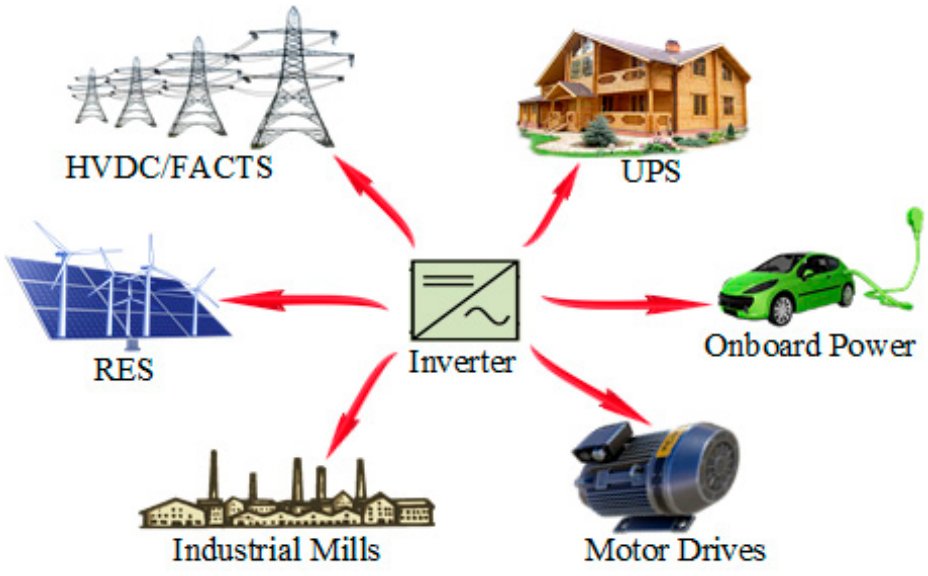

Figure 1. Applications of multilevel inverters.

The count of semiconductor components such as switches and diodes with their ratings, as well as capacitor requirements and boosting factors, are evaluated as quantitative factors. The performance of topology is optimized between application voltage and power levels, size and cost, control complexity, loss distribution, reliability, and modularity. Topologies with large peak switch blocking voltages are limited in high-voltage applications whereas a significantly high total standing voltage (TSV) exacerbates its cost. The number of drivers and snubbers requirements are increased with the increase in switch count, as

well as increased modulation algorithm complexity, higher failure rates, and increased computational times. Additionally, it also has the effect of elevated switching losses, particularly in high-frequency applications and it complicates thermal management design. However, imposing constraints on the switch count may lead to a decrease in redundant states that would otherwise help to achieve balanced FC voltages, distribute losses, and enable post-failure reconfiguration. Converters that can be easily built using pre-existing modules are more suitable for industrial applications. Likewise, the increased number of FCs leads to an increase in the number of voltage sensors and the complexity of the voltage balancing algorithms [10–12]. Nevertheless, the rapid growth in the availability of increasingly capable, fast, and low-cost microcontrollers might offset these limitations as well as facilitate the implementation of complex and non-linear control algorithms such as model predictive control. Inverters possessing inherent voltage balancing capabilities greatly reduce the complication of voltage balancing algorithms and computational load. The physical volume and weight of the inverter are considerably affected by the presence of FCs. This leads to reduced power density and increased failure rates which is undesirable in renewable energy systems (RES) and electric transportation. Similar problems can be caused by using more than two DC-link capacitors. On the contrary, a greater value of the DC-link utilization factor offers benefits including enhanced efficiency and easier cable management, and is especially beneficial in traction applications. Higher voltages can also hasten the charging of on-board battery storage systems.

Among the plethora of power electronic solutions, MLIs have emerged as an attractive and versatile option for RES. These inverters offer several advantages, including improved voltage quality, lower harmonic distortion, and enhanced power handling capabilities. Consequently, these can be suitably used in various applications such as grid integration, motor drives, and energy storage. However, the optimal utilization of MLIs in RES and EV requires sophisticated control strategies to address the challenges of power quality, efficiency, and system stability [13]. Model Predictive Control (MPC) is a dynamic and predictive control methodology that has gained considerable attention in recent years for its ability to optimize complex systems and address non-linearities and uncertainties [14–17]. Among its variants, Finite Control Set Model Predictive Control (FCS-MPC) has garnered significant attention for controlling MLIs with superior performance, robustness, and accuracy. This approach enables the inverter to predict future behavior based on a discrete set of control signals and enables a precise modulation and high-speed response to system dynamics [18–24]. In the renewable energy sector, integrating FCS-MPC with MLIs holds significant potential to boost energy conversion efficiency, grid integration, and overall system reliability. Table 1 presents a comprehensive comparison of five similar works of literature with the proposed work. The control strategy used in the proposed work is easy, and the addition of switching frequency control is possible. The presented topology can also generate more output voltage levels with fewer switches. Consequently, the size of the filter requirement is reduced. Hence, the proposed work can effectively be employed in practical applications.

This research article aims to develop and implement the advanced FCS-MPC control strategy on a single-phase five-level T-type topology for RES. The objective is to capitalize on the benefits of MLIs while leveraging the predictive and control capabilities of FCS-MPC to achieve optimal energy harvesting, seamless grid interaction, and superior power quality. This article has been drafted into different sections. The first section introduces the article. The subsequent sections of this article are described as given. Section 2 illustrates the modulation techniques to control the switching of semiconductor devices in the MLIs. Conventional control techniques as well as the MPC technique have been explained. A single-phase five-level T-type topology which has been used in this paper is elaborated in Section 3. This also includes the different switching states of this topology. The Implementation of FCS-MPC on single phase five-level T-type topology has been discussed in Section 4. Section 5 demonstrates the prototype of the topology developed in the laboratory and FCS-MPC implementation on this inverter. This section elaborates the essential components

used in hardware designing and system test bench. The hardware results are also included in this section. The conclusion of the paper is presented in Section 6 followed with the future work in the last section.

Table 1. Comparison of several similar literatures with proposed work.

Description	[25]	[26]	[27]	[28]	[29]	Proposed
Topology	T-type double H-bridge	Transformerless T--Type NPC	Full-bridge	NPC	T-type	T-type
Control Approach	NLC	Combined SVM and hysteresis current control	Dead-beat based FCS-MPC	Artificial neural network-based FCS-MPC	Hybrid ZVS boundary condition mode	FCS-MPC
Number of Switch Count	9	4	4	4	6	6
Number of DC Sources	3	1	1	1	1	1
Number of Output Level	15	3	3	3	3	5
Complexity	Depends on the output level	Difficult	Difficult	Complex	Complex	Easy
Switching Frequency Control	Fixed switching frequency	Fixed switching frequency	Fixed switching frequency	Switching frequency control varies over time and is uncontrollable	Switching frequency control can be added	Switching frequency control can be added

2. Control Strategies for Multilevel Inverter

2.1. Conventional Modulation Strategies

Modulation strategies are techniques used to control the switching of the semiconductor devices within the MLIs to generate desired output voltage waveform. These strategies ensure that the output waveform resembles a sinusoidal waveform with reduced harmonic distortion [3,4]. Some of the commonly used modulation strategies for MLIs and their categorization are depicted in Figure 2.

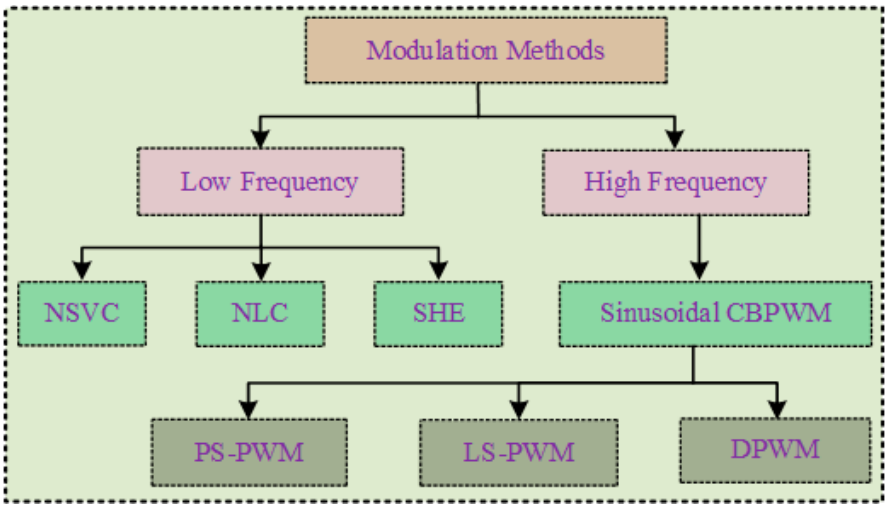

Figure 2. Modulation schemes for multilevel inverters.

Based on switching frequency, conventional modulation strategies for MLIs are categorized as low-frequency modulation (LFM) and high-frequency modulation (HFM) methods. LFMs operate near the fundamental grid frequency and thus have lower switching losses and dv/dt and di/dt issues. LFMs include nearest space vector control (NSVC), nearest level control (NLC), and selective harmonic elimination (SHE) schemes [3,4]. Determining the appropriate space vector is a challenging process in NSVC and it requires a significant amount of time. The NLC scheme is not worthy enough at a low modulation index for

the low number of output levels as it produces ample harmonic distortion. NLC uses a stepped quasi-sinusoidal carrier to approximate a sinusoidal output. SHE involves calculating the firing angles through the solution of an optimization problem through numerical methods or AI-based algorithms. NLC offers faster response and lower computational load while SHE can retain a better and flexible harmonic profile [8]. LFMs are more befitting for high-voltage, high-power applications while HFMs have a wider application range. HFMs achieve better harmonic performance as their harmonic content is concentrated at higher frequencies which can be conveniently eliminated through a low-pass filter. However, HFMs suffer from harmonic deterioration and require a substantial level count or filter design.

The adoption of wide-bandgap semiconductors has significantly mitigated the switching losses and led to the practical applicability of HFMs for high-power and high-voltage applications [9]. Sinusoidal CB (carrier-based) PWM are the most ubiquitous modulation techniques with a wide range of applications, mature technology, and straightforward implementation through look-up tables (LUTs) by comparison of sampled sinusoidal references and triangular carriers. A substantial quantity of research works has explored the performance enhancement in CBPWM to address control, delay, and capacitor balancing issues across several converters. PS (phase-shift) and LS (level shift)—PWM are continuous variants of CBPWM while DPWM (discontinuous) clamps the modulating signal to either polarity of the rail voltage for a certain time interval for each phase. Finally, SVM (state vector modulation) has also been widely implemented for multilevel inverters, with much research work performed to address the complexities associated with a large number of voltage sectors of the converter [30]. SVM is a quasi-hybrid of continuous and discontinuous techniques aimed toward optimizing harmonic performance and switching losses.

2.2. Model Predictive Control

Traditional control techniques encounter several critical concerns including poor dynamic response, challenges in dealing with the nonlinearities and multiple variables, need for the modulators, and difficulty in tuning gains. Thus, advanced and nonlinear control approaches such as Slide Mode Control (SMC), Fuzzy Logic Control (FLC), and Model Predictive Control (MPC) have been developed to address the aforementioned limitations. MPC has emerged as a leading-edge control technique for power converters due to its several distinct advantages such as fast dynamic response, dead-time compensation ability, and capability to manage multiple control objectives using a well-designed cost function and constraints [14,16]. The easy inclusion of non-linearities in the system model offers the flexibility to handle diverse scenarios. Furthermore, the continuous advancement of digital implementation platforms has paved the way for MPC applications in power converters for RES, active power filter (APF), medium-voltage (MV) grid-connected applications, and electrical drives. In general, MPC uses the controlled system model to predict its behavior within a defined prediction horizon. Subsequently, the cost function that defines the system objectives is used to determine the control by minimizing the differences between the predicted and reference values. In each control cycle, just the first action is applied [17].

According to the method of pulse generation, the MPC can be categorized as continuous, deadbeat, and finite control set MPC (FCS-MPC) [21]. The FCS-MPC is the predominant MPC scheme utilized in applications involving MLIs. The FCS-MPC framework possesses the capability to effectively leverage the distinct characteristics inherent in power converters. The optimal control action can be achieved by assessing the finite converter states inside a cost function that incorporates the control objectives. FCS-MPC can address the control problem easily and effectively, even with multiple control objectives and system constraints. Nevertheless, the online calculations required for variable prediction and cost function minimization increase computational burden, especially for high-level MLIs [22]. Moreover, variable switching frequency, tuning of weighting factors (WFs), and extended horizon implementation are also regarded as obstacles in FCS-MPC. The switches can only be toggled between two states—on and off—and their combinations create a

limited state. This inherent property makes it feasible to explain the switching model of the inverter straightforwardly, and succinctly summarize the prediction for the specified constraint. The mathematical model of the system and the fixed cost function forms the backbone of this control strategy. Figure 3 is the block diagram of the standard FCS-MPC approach with a short prediction horizon of only one step (Np = 1). In this configuration, the system's state variables $x(k)$ are measured or estimated and are used as the starting point for making predictions. These predictions produce n expected values $x(k + 1)$, corresponding to the n possible switching states of the converter. The switching state S, which minimizes the cost function, is selected and applied. The design and operating principles can be summed up in the following three steps: (i) developing a discrete-time prediction model; (ii) formulating a cost function including the control objectives and constraints; and (iii) defining and implementing the optimal vector with a minimal cost function using optimization technique.

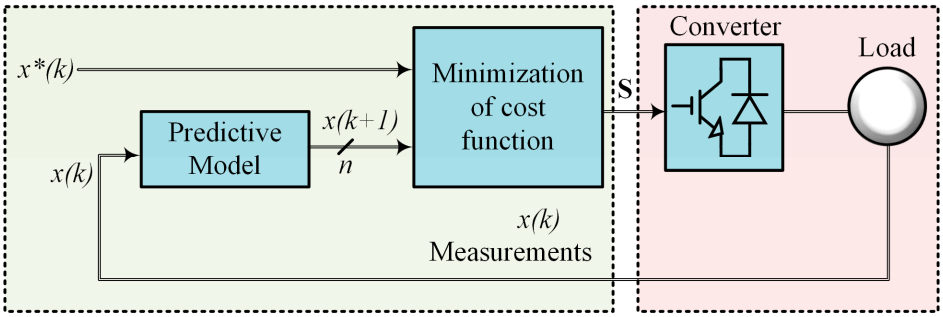

Figure 3. Block diagram of an FCS-MPC [21].

The initial stage involves the identification of all permissible switching states of an MLI by examining the power circuit of the inverter. The identification serves as a valuable tool for the effective management of information. The aforementioned data is afterwards organized and presented in Table 2. This table shows switching states based on inverter output voltage and capacitor voltages. In the subsequent stage, the capacitor voltages and currents are expressed in terms of the load current i_0 and input voltage V_{dc}, as these variables are the only parameters that can be measured. The consideration of measurements and switching states is of utmost importance when formulating equations. The mathematical and logical treatment of the latter can be accomplished within the framework of discrete time S. The model of the MLI is contingent upon the input DC-link voltage, capacitor voltages, and switching states. Once the prediction model is determined, it can be incorporated as the cost function [23]. The incorporation of weighting elements is crucial in the formulation of the cost function. The design of these entities is heuristically determined by analyzing the behavior of the goal variables. Additionally, the incorporation of additional control objectives, such as the reduction of switching frequency can be considered. Lastly, the FCS-MPC scheme is used to select and implement the best switching state for the inverter which is determined by the optimal cost function [24].

Table 2. Switching table of the topology.

Amplitude	S_1	S_2	S_3	S_4	S_5	S_6	C_{dc1}	C_{dc2}	State
V_{dc}	on	off	off	on	off	off	no effect	no effect	T_1
0.5 V_{dc}	on	off	off	off	off	on	↑	↓	T_2
	off	off	off	on	on	off	↓	↑	T_3
Zero	off	off	off	off	on	on	no effect	no effect	T_4
	off	on	off	on	off	off	no effect	no effect	T_5
	on	off	on	off	off	off	no effect	no effect	T_6

Table 2. *Cont.*

Amplitude	S_1	S_2	S_3	S_4	S_5	S_6	C_{dc1}	C_{dc2}	State
$-0.5\ V_{dc}$	off	off	on	off	on	off	↓	↑	T_7
	off	on	off	off	off	on	↑	↓	T_8
$-V_{dc}$	off	on	on	off	off	off	no effect	no effect	T_9

3. Single Phase Five-Level T-Type Topology

The single-phase five-level T-type topology is a derivation of the three-phase T-type topology. The topology encompasses a split DC-link supplied by one DC source V_{dc}, six switches S_1–S_6, and two bidirectional switches. An LC filter consisting of L_f and C_f is connected at the output terminal of the inverter to improve the output quality. The current flowing through the load R is i_g. The structure of the T-type topology is given in the below Figure 4. The topology can produce five levels with a peak equal to the DC source magnitude. The switches S_1, S_2, S_3, and S_4 block the voltage V_{dc}, and the bidirectional switches S_5 and S_6 block $2 \times 0.5V_{dc} = V_{dc}$ each. The upper and lower DC-link capacitors are designated as C_{dc1} and C_{dc2}. The topology can be extended to three or five phases with a common DC-link and similar operating principle. The switching states of the topology are given in Table 2 and visualized in Figure 5. The capacitors are charged and discharged and the states given in the table are represented by ↑ (charging) or ↓ (discharging). This affects the balance of the DC-link neutral point and must be considered in modulation, otherwise output and switch stresses will be drastically affected.

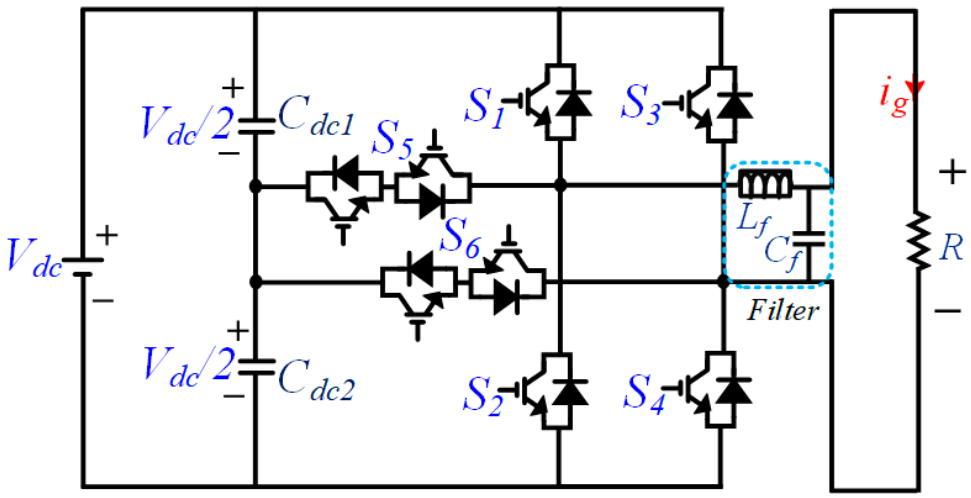

Figure 4. Single-phase five-level T-type topology structure.

All these switching states can also be represented as waveform which is depicted in Figure 6. It is obvious from the waveform that the only two switches are in ON condition for every available state. Moreover, each switch is turned ON thrice to generate a commutative of nine states. The T-type topology is considered for this work as it is suitable for medium voltage, high-power applications with an acceptable compromise on level count, complexity, redundancy, and issues elaborated on. With the advent of ultra-wide bandgap devices, MLI topologies with a greater number of levels can be less cost-effective than MLI topologies with lower levels. However, the traditional two-level and three-level inverters offer little redundancy, thus making MLI topologies with low level counts attractive. Moreover, the T-type topology lacks any switched capacitors and consequently their associated disadvantages.

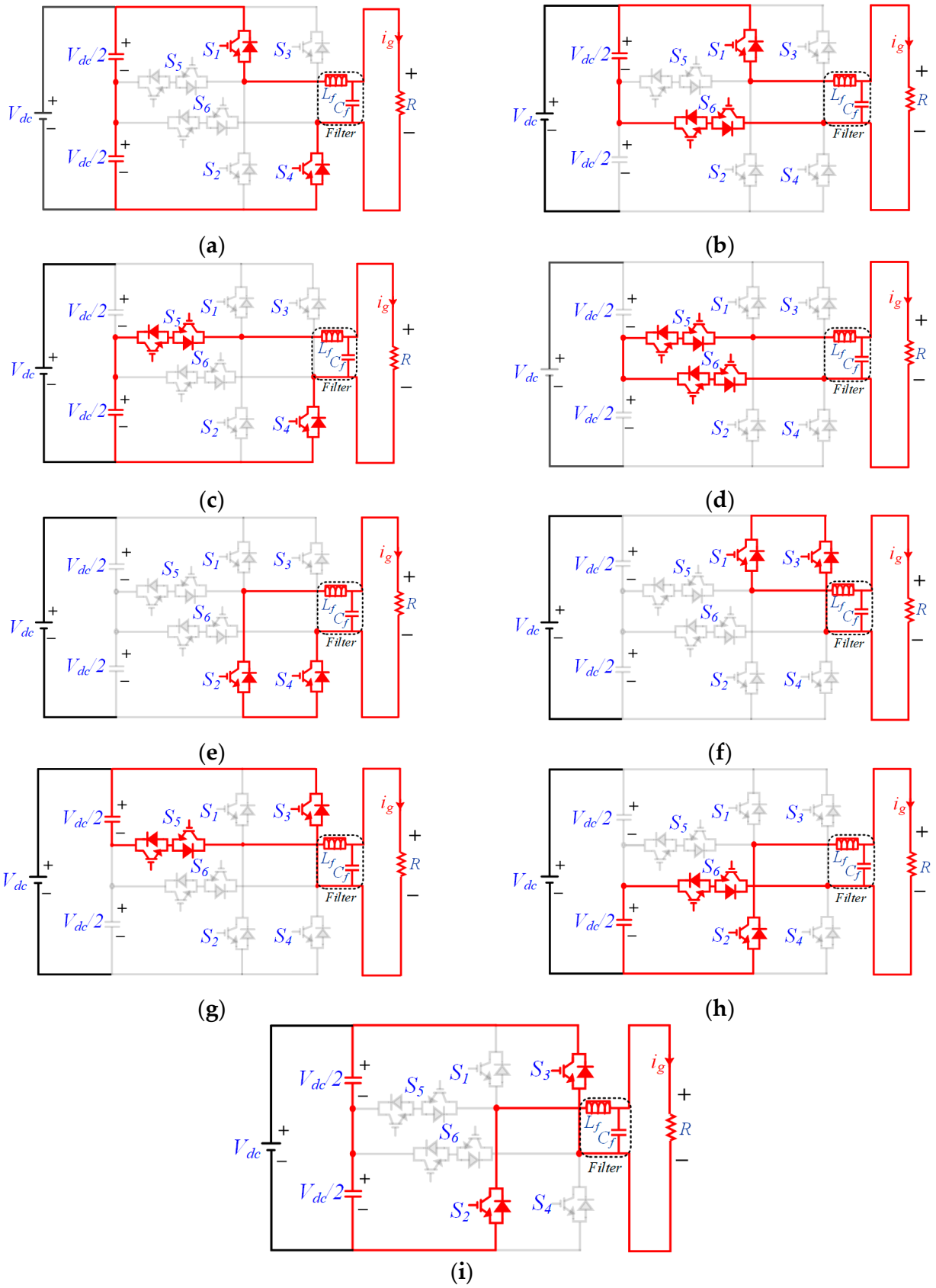

Figure 5. Different switching states of the topology. (**a**) T_1; (**b**) T_2; (**c**) T_3; (**d**) T_4; (**e**) T_5; (**f**) T_6; (**g**) T_7; (**h**) T_8; (**i**) T_9.

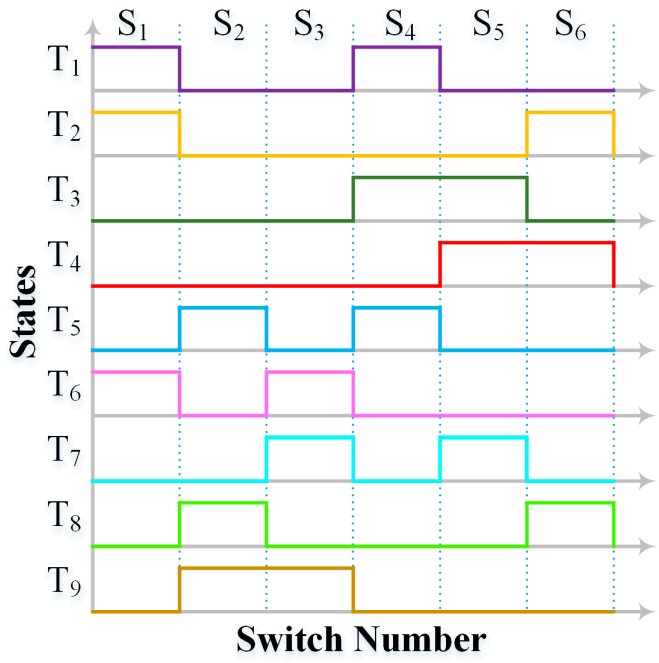

Figure 6. Visualization of switching states as waveforms.

4. Implementation of FCS-MPC on Single Phase Five-Level T-Type Topology

4.1. Implementation of FCS-MPC

The objective of FCS-MPC for inverter operation could be the matching grid connection, motor torque, flux, speed control, capacitor voltage balancing, or loss balancing. A dynamic model of the inverter is derived based on the inverter, load, and filter terminal voltages and currents. The dynamic model of the LC filter can be given as:

$$i_{c1,2} = C_{1,2}\frac{dv_{c1,2}}{dt} \tag{1}$$

where $i_{c1,2}$ is the capacitor current, $C_{1,2}$ are the DC-link capacitance magnitudes, and $v_{c1,2}$ are the DC-link capacitor voltages. Now the filter inductor current i_f can be represented as:

$$i_f = C_f\frac{dv_{Cf}}{dt} + i_o \tag{2}$$

where C_f, v_{cf}, and i_o are the filter capacitor magnitude, filter capacitor voltage, and load current, respectively. Now the filter inductor current can be derived using the following relation:

$$v_i = L_f\frac{di_f}{dt} + v_{Cf} \tag{3}$$

where v_i and L_f are the inverter terminal voltage and filter inductor magnitude respectively. The above equations need to be discretized using Euler's forward transform to facilitate digital controller operation. Therefore, the sampling time needs to be selected in accordance with the digital controller's capabilities and performance requirements. Similarly, the static switching model of the inverter structure can be formulated with the positive load terminal voltage v_a as:

$$v_a = \frac{V_{dc}}{2} * S_1(1-S_2)(1-S_5) - \frac{V_{dc}}{2} * S_2(1-S_1)(1-S_5) + 0 * S_1(1-S_5)(1-S_2) \tag{4}$$

and the negative load terminal voltage v_b as:

$$v_b = \frac{V_{dc}}{2} * S_3(1-S_6)(1-S_4) - \frac{V_{dc}}{2} * S_4(1-S_3)(1-S_6) + 0 * S_6(1-S_3)(1-S_4) \quad (5)$$

where S_1 through S_6 represent the switching functions of the six switches under all conditions, and the cost function needs to be determined. By careful selection of states, neutral-point balancing is ensured without the need for real-time balancing control in the FCS-MPC algorithm [13]. The system block diagram is depicted in Figure 7.

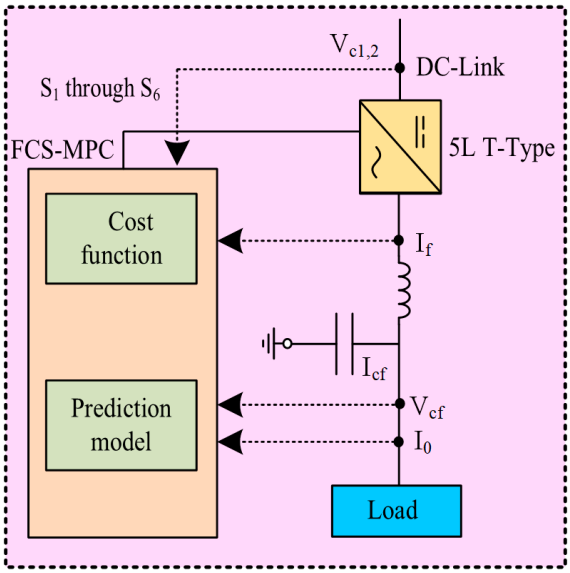

Figure 7. FCS-MPC and T-type system.

4.2. Cost Function and Flowchart

The objective of FCS-MPC is to predict the cost function magnitude for potential switching states and select the optimal state that minimizes the cost. The cost function is based on performance criteria, including voltage reference, current reference, motor torque, flux, losses, switching frequency, etc. Since FCS-MPC has a variable switching frequency dependent on the sampling time, a significantly high switching frequency can have an advert effect on converter efficiency and reliability. To alleviate this, frequency constraints must be included in the cost function. Redundant states can be used to reduce the switching state transitions, hence reducing the average switching frequency and losses. The cost function g can be determined as:

$$\begin{aligned} g = |V_c^* - V_c| + \quad & w * (|S_1 - S_1(k-1)| + |S_2 - S_2(k-1)| + |S_3 - S_3(k-1)| + |S_4 - S_4(k-1)| \\ & + |S_5 - S_5(k-1)| + |S_6 - S_6(k-1)|) \end{aligned} \quad (6)$$

where V_c^* is reference capacitor voltage, V_c is the measured capacitor voltage and w is the weighing factor. The cost function can be described as the objective of optimizing the error between the reference capacitor voltage and the measured capacitor voltage. In the case of an L-filter, only the inverter current could be controlled, albeit with a lower computational load for the FCS-MPC as the L-filter and inverter form a first-order system [15]. This would be sufficient for motor applications, but unsuitable for grid-connected and UPS applications as the voltage harmonics will be uncontrollable. The addition of an LC filter forms a second-order system with increased computational load for the FCS-MPC. However, the filter capacitor allows load voltage control, thus effectively eliminating voltage harmonics. In traditional carrier-based modulation methods, the switching frequency is constant, while in FCS-MPC the switching frequency is flexible and needs to be regulated. The second to seventh terms of the cost function achieve this by setting a penalty on the switching transitions per cycle. The weighting factor w tunes the balance between the two objectives

of voltage error and switching frequency reduction and can be manipulated according to the application and performance constraints. The maximum switching frequency achievable is twice the sampling frequency of the algorithm. The average switching frequency for a five-level inverter can be evaluated using below equation:

$$f_{swa} = \frac{\sum_{i=1}^{N} st(i)}{5 \cdot N \cdot T_s} \tag{7}$$

where the number of time periods for the calculation is N, the sampling time is T_s and st is the switching transition which is given by

$$st(i) = \sum_{j=1,\ldots 6} \left| S_{j,k+1} - S_{j,k} \right| \tag{8}$$

where $S_{j,k+1}$ and $S_{j,k}$ are the candidate states for the jth switch for the kth sampling time. The overall control flow is depicted in Figure 8.

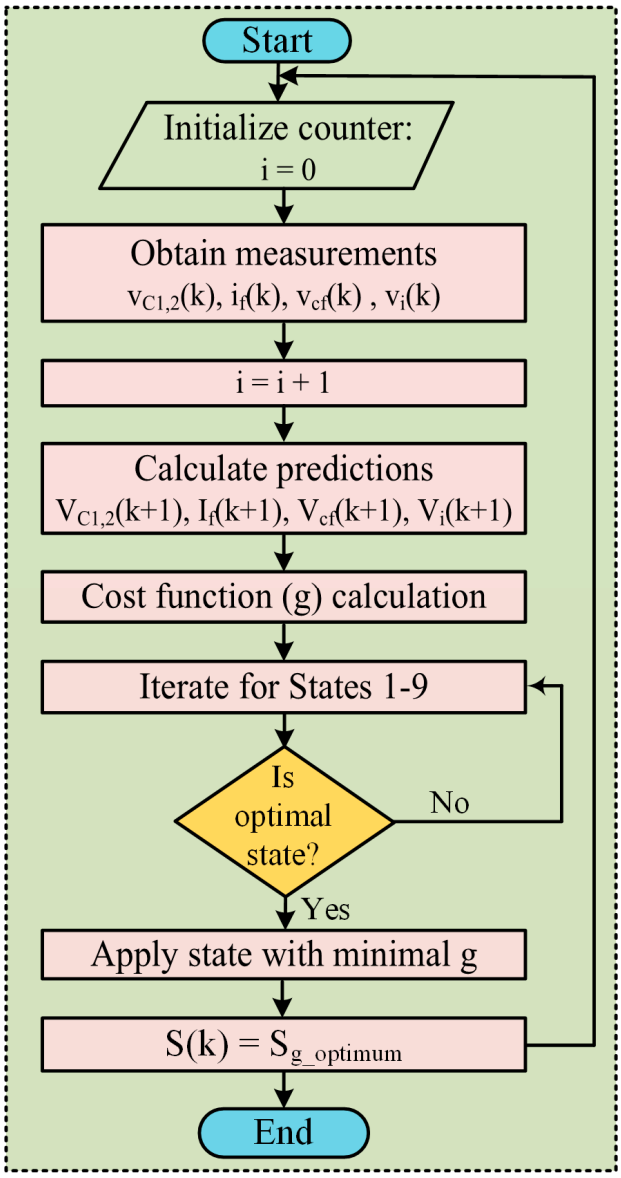

Figure 8. Flowchart of the FCS-MPC algorithm.

The control Algorithm 1 for implementing the cost function can be summarized as follows:

Algorithm 1 Algorithm for implementing the cost function.

Start
1. Initialize counter i = 0
2. Continuously measure the $v_{c1,2}$, i_f, v_{cf} and v_i
3. Compute Equations (4) and (5)
4. Evaluate Equation (6) to compute the cost function g based on the values of Vc^* and Vc.
5. Use optimization techniques to find the optimal switching state that minimizes g.
6. Iterate for switching states T_1–T_9 and check whether the optimal state is obtained or not.
7. If yes, continue with step 7; else repeat step 6.
8. Apply switching state with minimum g.
9. S (k) = $S_{g\_optimum}$

End

Simulations are performed to evaluate the converter loss distribution under high-power conditions without frequency penalization. MATLAB/Simulink environment has been used to perform the simulation of the system. The simulation parameters are given in Table 3. The switching loss distribution in Watts for switches S_1–S_6 is depicted in Figure 9. The figure indicates that S_5 and S_6 have substantially lower switching losses than other switches. Therefore, the frequency penalization weighing factor w is to be applied only on switches S_1 through S_4. Previously, several works have investigated weighing factor tuning against varied objectives. Auto-tuning and factor elimination of weighing factors have been observed in works such as [15]. Optimal weighing factor determination can be solved online or offline.

Table 3. Simulation parameters for evaluating the converter loss distribution.

Specification	Value
Sampling Time	10 µs
Load R	60 Ω
LC Filter L_f C_f	3 mH, 15 µF
DC Source V_{dc}	700 V
Fundamental frequency	60 Hz
MOSFET	C2M0025120D
Ambient temperature	55 °C

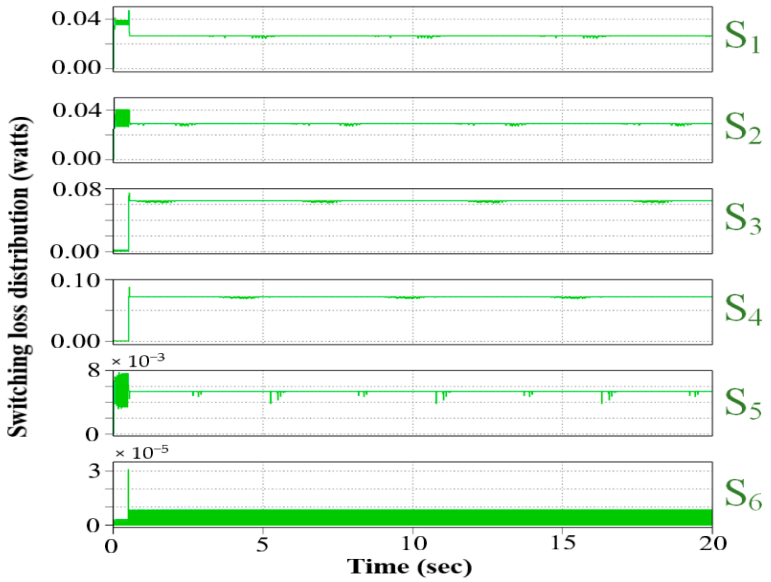

Figure 9. Switching loss distribution without penalization.

Since the frequency penalization weighing factor needs to be applied to switches S_1–S_4 only, the computational load is reduced. Figure 10 shows the transient response of FCS-MPC without weighing factor with a 100% variation of reference voltage. Then, a frequency penalization factor of 0.5 per unit is employed. The resulting loss distribution and dynamic response are given in Figure 11 and Figure 12, respectively. Evidently, the average losses are reduced for S_1 to S_6.

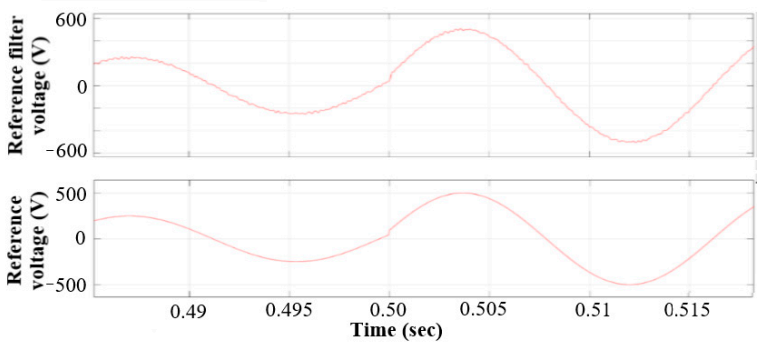

Figure 10. Dynamic response of FCS-MPC without weighing factor.

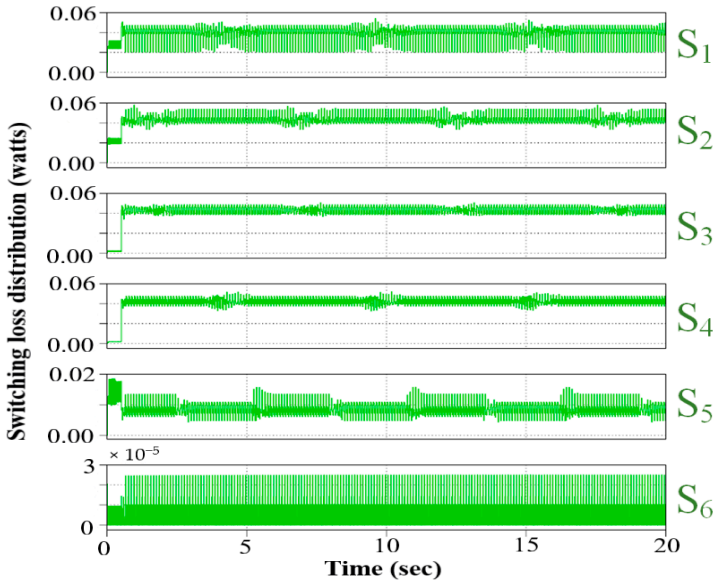

Figure 11. Switching loss distribution under frequency penalization.

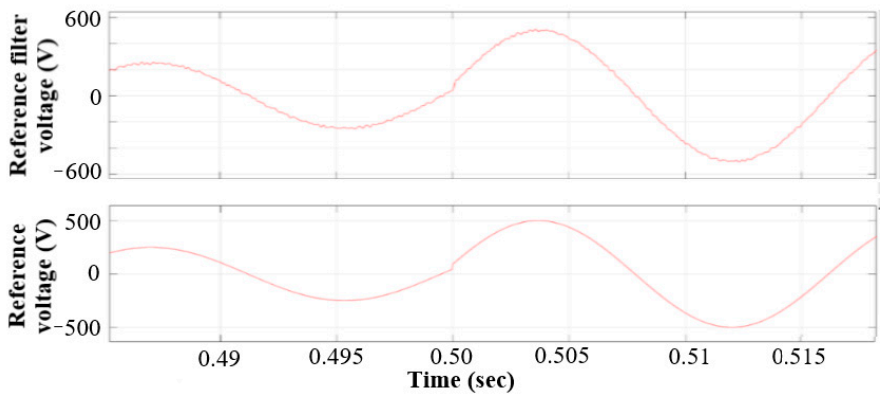

Figure 12. Dynamic response of FCS-MPC under frequency penalization.

The effect of load variation has been illustrated in Figure 13. Three different loading conditions were considered, namely uniform load, dynamic loading with load changing from half load to full load, and dynamic loading with load changing from full load to half load. It is obvious from Figure 13a–c that load voltage is unaffected irrespective of load change and maintained at the same voltage level. Figure 13d depicts the harmonic profile of the output load voltage. It is evident from this figure that output load voltage has maintained the high-quality sinusoidal characteristics as the total harmonic distortion (THD) is merely 1.36%.

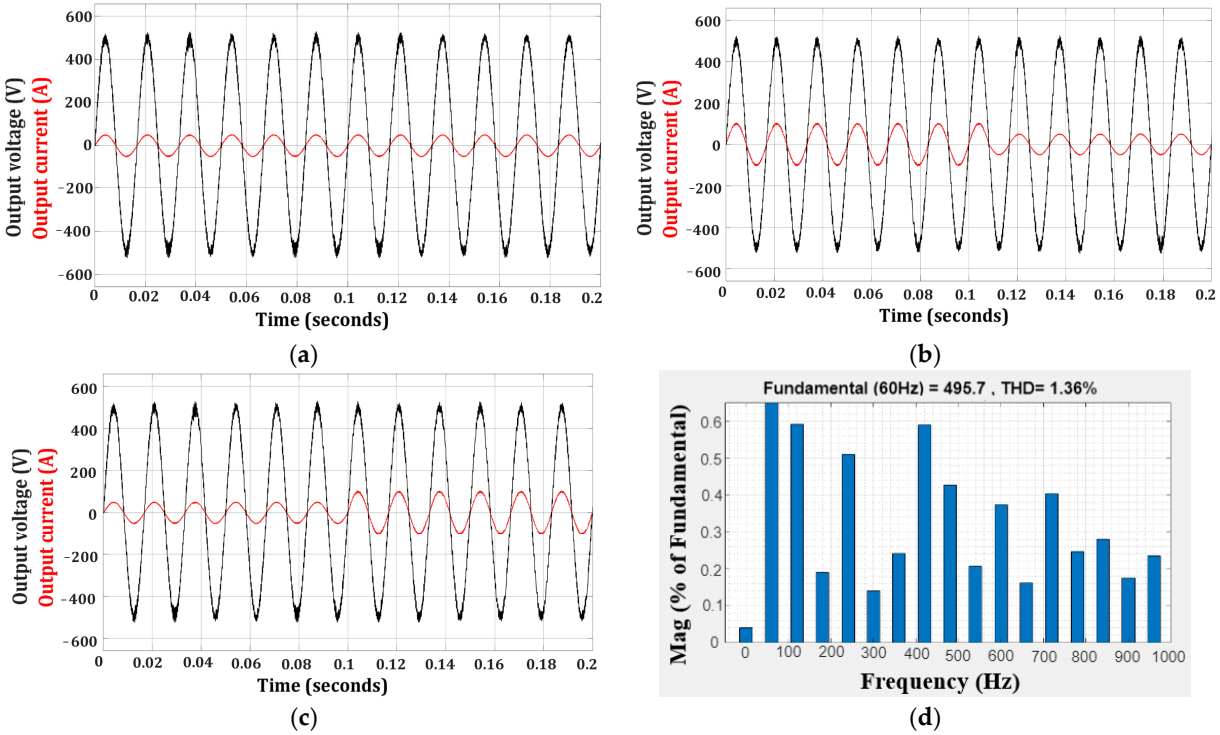

Figure 13. Load voltage under different loading conditions. (**a**) Uniform load; (**b**) dynamic loading with load changing from R/2 to R; (**c**) dynamic loading with load changing from R to R/2; (**d**) harmonic profile of the output load voltage.

5. Hardware Implementation

A prototype of the single-phase five-level T-type topology has been developed in the laboratory and FCS-MPC has been implemented on this inverter to examine the system performance in real-time and investigate hardware development issues.

5.1. Components Used

The important components used in the development of the prototype are described below:

1. Embedded Controller: A 32-bit digital signal processor TI-C2000-F28379D has been used here as it can work at a sample time appropriate for real-time FCS-MPC computation on the prototype. The controller can be programmed through Code-Composer Studio© or through code generation. For rapid development and verification, code generation is applied in this work using MATLAB R2022b-Simulink Embedded Coder. The code generation process involves a dynamic model of the system using compatible blocks in Simulink. The code generation process allows real-time tuning in external mode as well as calibration of sensor modules to allow shorter development durations. Since FCS-MPC works without a modulator, the PWM modules of the controller cannot be employed for the gating signals. GPIO pins are used for the gating signals which do not have an inherent deadband feature unlike the epwm module, hence hardware deadband through gate drivers has been provided;

2. Gate Driver Unit: Gate drivers based on the TLP250 optocoupler and isolated power supply IC (integrated circuit) are provided to drive the gate of the MOSFET used in the prototype. These drivers can amplify the 3.3 V signals provided by the controller as well as provide isolation. A special configuration with resistor $R_1 = 100\ \Omega$, $R_2 = 5\ \Omega$ has been used to provide the hardware deadband which prevents the shoot-through of complementary MOSFET pairs. Since the MOSFET switching time decreases with increasing gate resistance, a fast-switching diode D_1 (1N914) which can pass the switching signals with low propagation delay has been incorporated in the circuit as shown in Figure 14a. This configuration provides increased turn-on time and decreased turn-off time, hence preventing the overlap between the higher and lower side MOSFETs as shown in Figure 14b. The prototype of the gate driver unit used in this experiment is shown in Figure 14c. Six such gate driver units are used in the inverter and one MCWI03-48S15 isolated power ICs are employed in each unit;
3. DC-link capacitors: Two DC-link capacitors are used in the converter for the purpose of dc-bus. The capacitors facilitate the energy storage to allow DC power from the DC source to be converted to pulsating AC power. The capacitor needs to transmit only a fraction of the load current. The capacitors used are of magnitude 1000 µF and rated 250 V;
4. Output Filter: For the five-level inverter, the filter inductor sizing can be performed as

$$L_f \geq \frac{V_{DC}}{16 \times f_{sw} \times \Delta I_{p-p}} \tag{9}$$

where the variables V_{DC}, f_{sw}, and $\Delta I_{(p-p)}$ are the dc-bus voltage, switching frequency, and allowed peak-to-peak current ripple respectively. Considering a bus voltage of 400 V, average switching frequency of 10 kHz, and current ripple of 1 A, the minimum inductance is 2.5 mH. A 2.8 mH inductor is chosen to meet the design criterion.

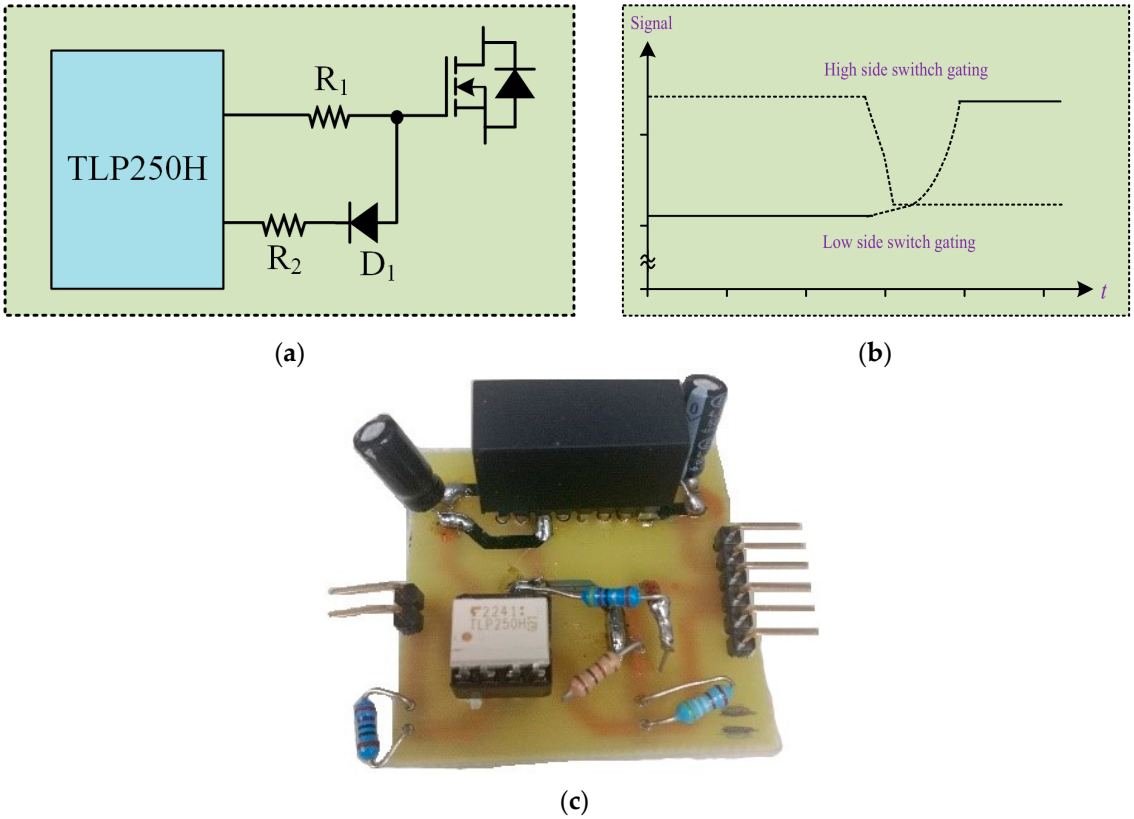

Figure 14. Hardware deadband implementation: (**a**) Block diagram representation; (**b**) deadband realization; (**c**) hardware of the gate driver unit.

Likewise, the output filter capacitor can be sized using the below result based on the inductor-capacitor cut-off frequency and the effective switching frequency:

$$C_f > \left(\frac{1}{2 \times \pi \times f_{crss}}\right)^2 \times \frac{1}{L_f} \tag{10}$$

Selecting the capacitor with a crossover frequency f_{crss} of 2000 Hz, we obtain a minimal capacitance of 2.26 µF. However, a capacitor valued at 3.3 µF of Bipolar film type has been selected.

5. Bleeder resistor selection: To initiate the converter operation, the DC-link capacitors are charged by a single regulated DC power supply. The regulation of the power supply eliminates the need for any pre-charging resistors. However, once the converter operation is terminated, the dc-bus capacitances must be discharged for safety concerns. Bleeder resistors are placed in parallel with the capacitors C_{dc1} and C_{dc2};
6. to facilitate their discharging. The magnitudes of these resistors are 510 kΩ each. Six resistors, in parallel combinations of three series resistors are each placed in parallel with each dc-bus capacitor;
7. Current and Voltage Sensors: The converter needs two current sensors to measure the filter and load current, as well as three voltage sensors for the measurement of filter, load, and capacitor voltages. The current sensors are designed using the ACS712 hall-effect current sensor IC. The filter capacitor for the current sense is chosen as 100 nF. For the voltage sensor, non-inverting operational amplifiers (OP-AMPs) are employed to provide step-down gain, offset and isolation. It has three stages namely, the gain stage, the positive offset stage, and the isolation stage. General-purpose Op-Amps are used for designing the voltage sensors which are powered by a ±15 V supply. The gain stage steps the high voltage to a range between 0–1.65 V. The offset stage adds a positive bias such that the reading is positive for even the negative values for measured voltage. The final isolation stage facilitates galvanic isolation between the MCU ground and the measurement ground through an isolation amplifier. Thus, a value from −300 V to +300 V is scaled to 0 to 3.3 V for data acquisition by the MCU;
8. EMI capacitors: EMI (electromagnetic interference) capacitors are needed to alleviate high-frequency noise due to the dv/dt and di/dt transitions which can affect converter output and the gating signals. The capacitors are placed across every leg. Six 150 nF 630V-rated, Film Bipolar capacitors are employed for this purpose;
9. MOSFET: K2371 MOSFET is used as the switching device for the power stage. The MOSFET can block a voltage of 500 V and transmit a current up to 25 A.

5.2. Hardware Setup

All the above-mentioned components were deployed and fabricated on a PCB for designing the T-type inverter. Figure 15 demonstrates the layout of the power and converter stage on a two-layer PCB. The architecture diagram of the overall T-type inverter is displayed in Figure 16. Hardware implementation of the prototype of the single-phase five-level T-type inverter has been developed in the laboratory to validate the FCS-MPC technique. The components mentioned earlier are arranged according to the circuit shown in the layout. The developed hardware prototype was used in this experiment and is displayed in Figure 17. C2000-F28379D DSP generates the controlling pulses for the gate of MOSFETs. These pulses control the switching time of the MOSFETs by regulating the pulse width of the signal. These controlling pulses have been generated using the FCS-MPC strategy. A load is connected at the output terminal to perform the testing and to evaluate the effectiveness of the control strategy used in this paper. A digital storage oscilloscope is used for measuring the output voltage and current. The specification of the experimental setup is mentioned in Table 4.

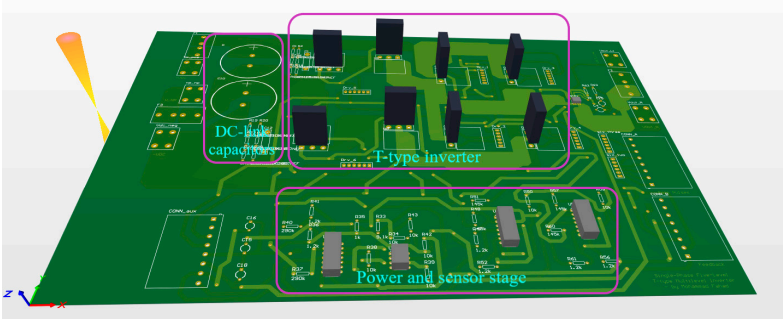

Figure 15. Power and sensor stage layout.

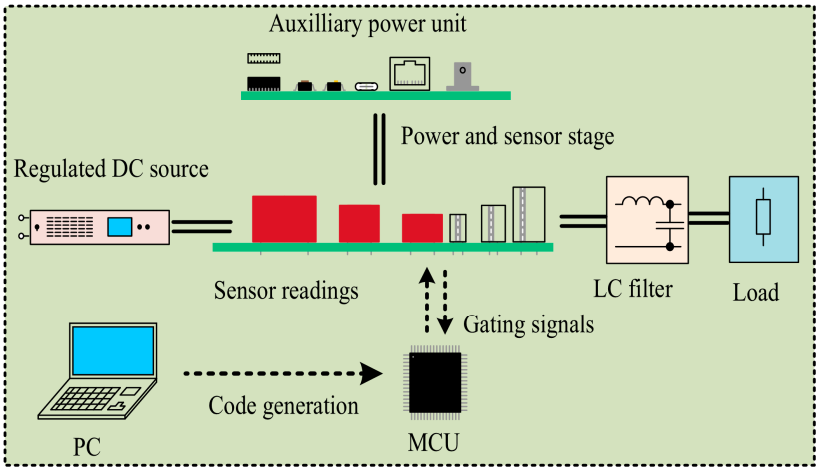

Figure 16. Architecture diagram of the overall system.

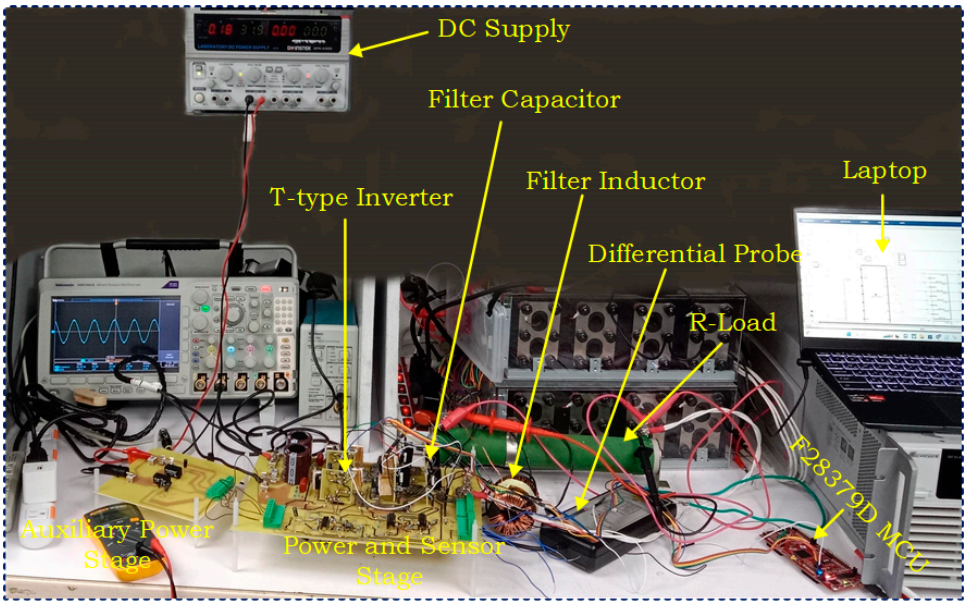

Figure 17. System test bench.

Table 4. Specifications of the laboratory hardware setup.

Equipment/Components	Quantity	Specification
Digital Signal Processor	1	TI, 32-bit, C2000-F28379D
Gate Driver unit	6	TLP 250H, MCWI03-48S15

Table 4. *Cont.*

Equipment/Components	Quantity	Specification
Oscilloscope	1	Tektronix MDO3024
DC Link Capacitor C_{dc1} and C_{dc2}	2	1000 µF, 250 V
Output Filter (Inductor) L_f	1	2.8 mH
Output Filter (Capacitor) C_f	1	3.3 µF, Bipolar film-type
Voltage sensor unit	3	Op-Amp
Current sensor unit	2	ACS712-IC
Laptop	1	HP, Victus
DC power supply	1	GWINSTEK, GPS-4303
DC power supply	1	CHROMA, 62100H
MOSFET	8	K2371

5.3. Hardware Result

The parameters used during the prototype testing are mentioned in Table 5. These parameters have been used in the hardware development as shown in Figure 17. As mentioned earlier, a specific configuration has been used in the gate driver unit to provide the hardware deadband, and the generated deadband is shown in Figure 18. The rise time of the gate signal is 1.502 µs, while the fall time is 77.79 ns. This will prevent the overlap as the first switch will be already turned off well in advance of the other switch's turn-on transition.

Table 5. Prototype parameter description.

Parameters	Specification
Fundamental frequency	60 Hz
DC Bus voltage	155 V (Chroma 62100H)
Load R	60 Ω
Load voltage objective	110 V rms
Sample Time	10 µS
Weighing factor w	0.1

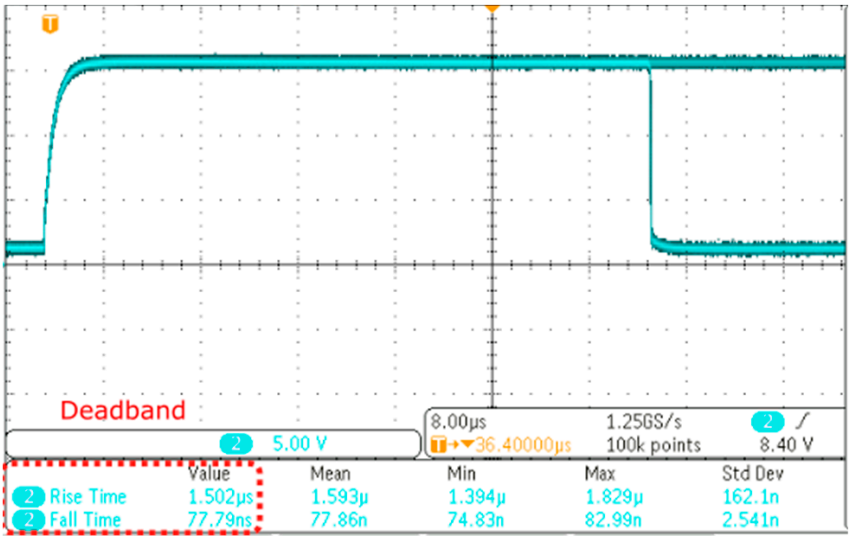

Figure 18. Practical realization of the deadband.

The switch signals of all the switches, i.e., S_1, S_2, S_3, S_4, S_5 and S_6 are given in Figure 19. Note that the inclusion of the switching constraint limits the switching frequency below 10 kHz. The pulse peak is 15 V. The waveform has been recorded on the digital storage oscilloscope. The inverter has been tested with and without the output filter. The inverter

output voltage without the LC filter is shown in Figure 20, having a peak voltage of 150 V. The lack of an LC filter gives rise to a pulsed waveform with significant ripples as visible in Figure 20a with its zoomed view in Figure 20b. The switch S_1 undergoes an open circuit fault, but the converter recovers the output although with reduced peak voltage. Fault-tolerant operation is given in Figure 20c. To improve the quality of the output voltage, an LC filter has been connected to the output terminal. The load voltage with the inclusion of an LC filter is shown in Figure 21a,b. Evidently, the load voltage is close to 110 V rms and 60 Hz, thus the standard operation of the inverter is achieved. The FFT window and spectrum of the inverter with LC filter are given in Figure 21c. The THD is 3.92% which meets IEEE-519 standards [31]. Figure 21d lists the harmonic content distribution. Visibly, the concentration of harmonic content is equally distributed across all frequencies, which is the expected result in FCS-MPC unlike SPWM, in which the harmonic magnitudes are concentrated across particular frequencies.

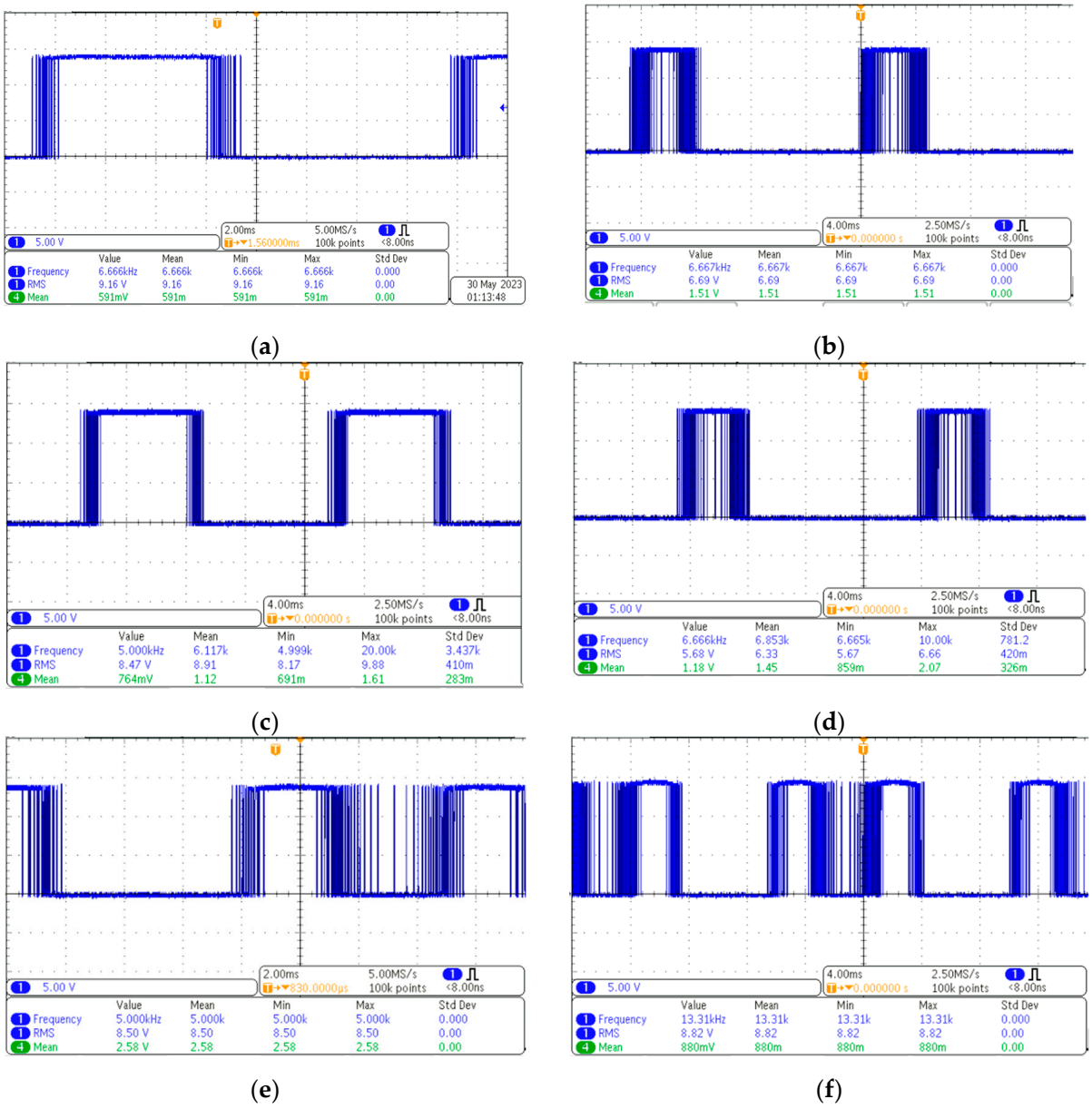

Figure 19. Switching signals to all the switches: (**a**) S_1 gating; (**b**) S_2 gating; (**c**) S_3 gating; (**d**) S_4 gating; (**e**) S_5 gating; (**f**) S_6 gating.

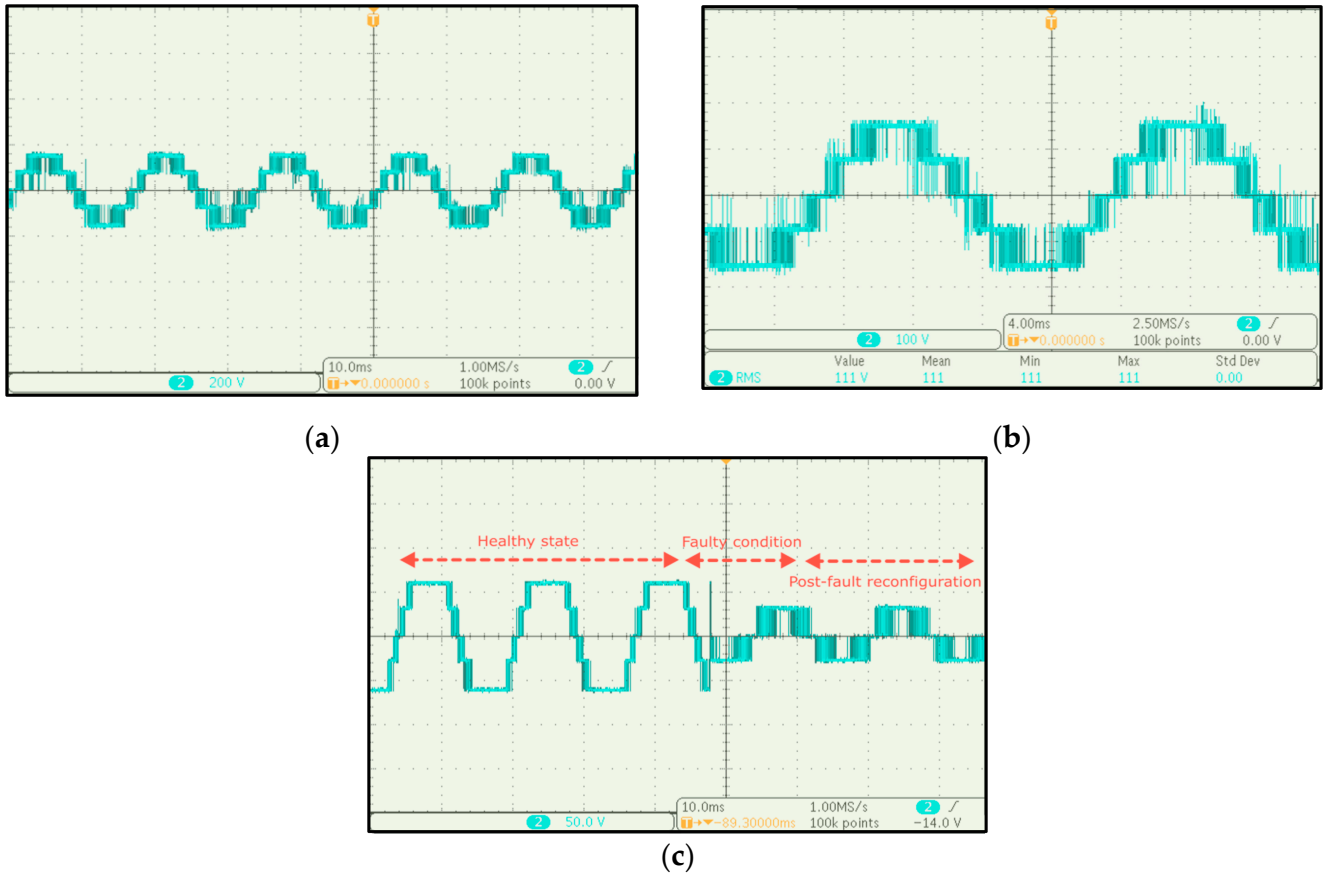

Figure 20. Inverter output voltage. (**a**) Without LC filter; (**b**) without LC filter (zoomed view); (**c**) post-fault transition.

The inverter was tested under three different loading conditions: uniform load, dynamic loading with load changing from R/2 to R, dynamic loading with load changing from half to full load, and dynamic loading with load changing from R to R/2. The effect of load variation on the output load voltage has been illustrated in Figure 22. It is apparent from the figure that load voltage is unaffected by the load change and maintained at the same voltage level. The result outcomes are summarized in Table 6. Thus, a stabilized output voltage can be maintained at the load terminal by implementing the control strategy used in this paper.

Table 6. The summary of result outcomes.

Parameters	Value
Load R	60 Ω
Loading conditions.	Uniform load Dynamic load (R/2-R, R-R/2)
Inverter output voltage	150 V (peak voltage)
Load voltage	110 V (constant), 60 Hz
THD	3.92%

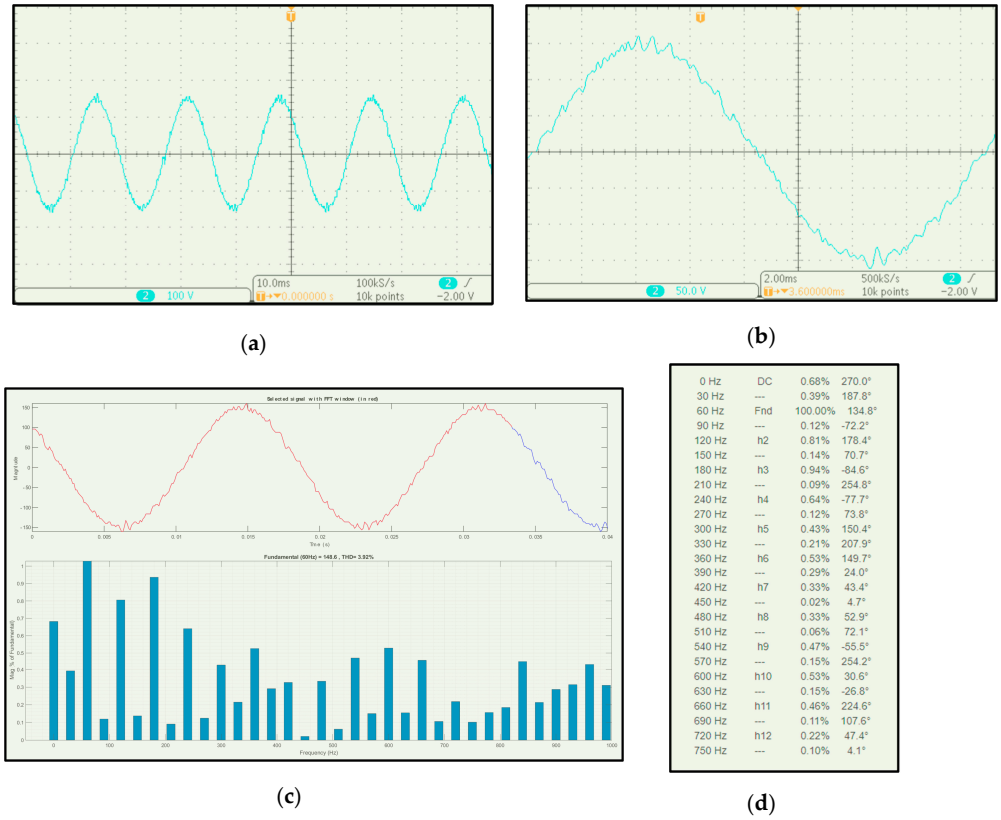

Figure 21. Load voltage. (**a**) With LC filter; (**b**) with LC filter (zoomed view); (**c**) with FFT spectrum; (**d**) harmonic content.

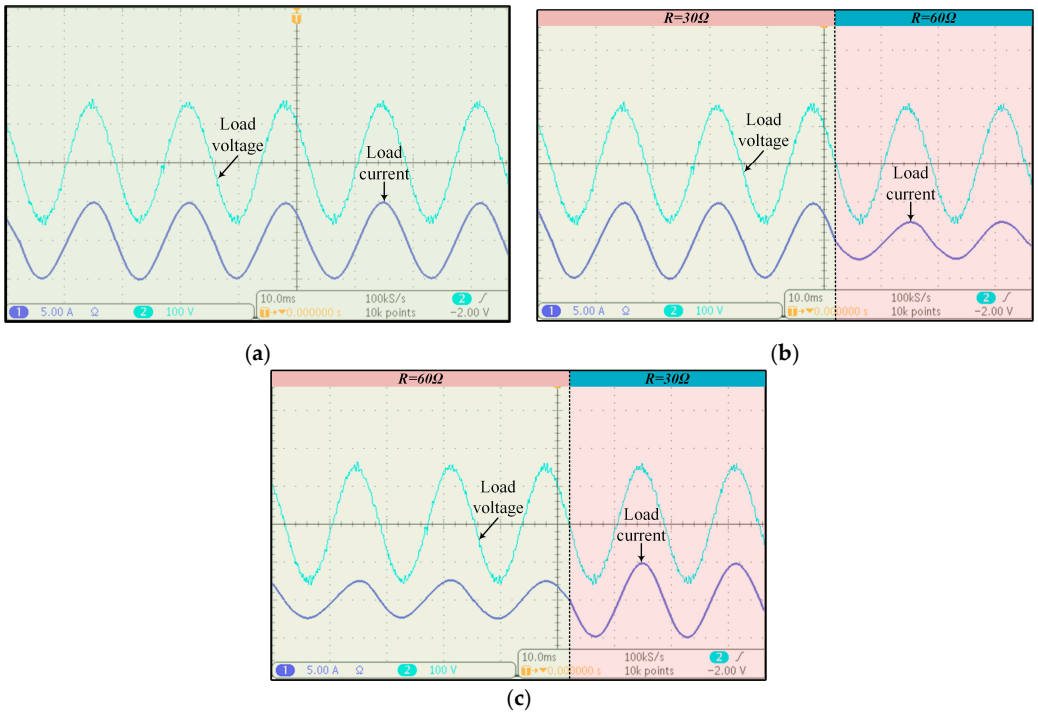

Figure 22. Output load voltage under dynamic loading conditions. Load voltage under different loading conditions. (**a**) Uniform load; (**b**) dynamic loading with load changing from R/2 to R; (**c**) dynamic loading with load changing from R to R/2.

6. Conclusions

Implementation of FCS-MPC for control of a single-phase five-level T-type multilevel inverter has been explored in this work. Operation and switching states of the topology are described and the cost-function, fault-tolerance, and capacitor balancing mechanisms are also presented. A Hardware prototype synthesis of the MPC-MLI system is not only elaborated but also fabricated to evaluate the effectiveness of the control strategy. The system can be developed through code generation on a C2000 DSP with sufficient execution accuracy. As demonstrated, the choice of weighing factor can be decisive in switching loss deduction and performance. A gate driver unit is also made pertaining to the gating pulse requirements with inherent deadband. The results indicate the applicability of FCS-MPC to MLIs for control purposes. The inverter output voltage and load voltage waveforms are presented to verify FCS-MPC operation. The THD content of 3.92% is <5% appropriate for IEEE-519-2014 standards [31]. The results indicate that FCS-MPC has been effectively applied on the single-phase five-level T-type topology, with the resulting system being applicable for a wide range of applications in terms of harmonic performance, loss distribution, reliability and maintaining a high-quality output load voltage at the prescribed voltage level irrespective of load variations. The inverter can seamlessly be integrated with RES applications, including photovoltaic (PV) systems, wind energy systems, and energy storage, and can provide enhanced grid support, load balancing, and energy management.

7. Future Work

This study indicates that FCS-MPC can be implemented across a wide range of converters and applications in a multitude of power electronic systems to come. Further research is warranted for the following:

- Optimizing the sample time, switching frequency, and dynamic response through an application-centric approach and varied mission profiles;
- More precise reliability computation methods while incorporating failure mechanisms and destructive tests under emulated real-environment conditions;
- Real-time optimization of weighing factors and novel optimization algorithms to solve the non-linear problem of state selection;
- Integration with wide-bandgap components and faster processors;
- Design of gate drivers and deadband compensation considering wide-bandgap and FCS-MPC.

Author Contributions: Conceptualization, S.A.F., M.F. and C.-H.L.; Formal analysis, S.A.F., M.F. and C.-H.L.; Investigation, S.A.F., M.F. and C.-H.L.; Software, S.A.F. and M.F.; Methodology, S.A.F. and M.F.; Data curation, S.A.F. and M.F.; Visualization, S.A.F., M.F. and C.-H.L.; Funding acquisition, C.-H.L.; Supervision, C.-H.L.; Writing—original draft, S.A.F. and M.F.; Writing–review & editing, S.A.F., M.F., C.-H.L., H.-D.L. and J.-J.H. All authors have read and agreed to the published version of the manuscript.

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References

1. Farooqui, S.A.; Lin, C.-H.; Lu, S.-D.; Liu, H.-D.; Sarwar, A.; Huang, L.-Y. Exponential Curve-Based Control Strategy for Auxiliary Equipment Power Supply Systems in Railways. *Processes* **2023**, *11*, 1285. [CrossRef]
2. Wang, H.; Iannuzzo, F.; Bahman, A.S.; Zhang, K.; Xue, P.; Zhang, Y.; Yao, B.; Shen, Z.; Sangwongwanich, A.; Vernica, I.; et al. Application-Oriented Reliability Testing of Power Electronic Components and Converters. *IEEE Power Electron. Mag.* **2022**, *9*, 22–31. [CrossRef]
3. Sarwar, M.I.; Sarwar, A.; Farooqui, S.A.; Tariq, M.; Fahad, M.; Beig, A.R.; Alamri, B. A Hybrid Nearest Level Combined with PWM Control Strategy: Analysis and Implementation on Cascaded H-Bridge Multilevel Inverter and its Fault Tolerant Topology. *IEEE Access* **2021**, *9*, 44266–44282. [CrossRef]

4. Khan, R.A.; Farooqui, S.A.; Sarwar, M.I.; Ahmad, S.; Tariq, M.; Sarwar, A.; Zaid, M.; Ahmad, S.; Mohamed, A.S.N. Archimedes optimization algorithm based selective harmonic elimination in a cascaded h-bridge multilevel inverter. *Sustainability* **2022**, *14*, 310. [CrossRef]
5. Guo, F.; Yang, T.; Diab, A.M.; Yeoh, S.S.; Bozhko, S.; Wheeler, P. An Enhanced Virtual Space Vector Modulation Scheme of Three-Level NPC Converters for More-Electric-Aircraft Applications. *IEEE Trans. Ind. Appl.* **2021**, *57*, 5239–5251. [CrossRef]
6. Rodriguez, J.; Lai, J.-S.; Peng, F.Z. Multilevel inverters: A survey of topologies, controls, and applications. *IEEE Trans. Ind. Electron.* **2002**, *49*, 724–738. [CrossRef]
7. Bahrami, A.; Narimani, M. A New Five-Level T-Type Nested Neutral Point Clamped (T-NNPC) Converter. *IEEE Trans. Power Electron.* **2019**, *34*, 10534–10545. [CrossRef]
8. Farooqui, S.A.; Shees, M.M.; Alsharekh, M.F.; Alyahya, S.; Khan, R.A.; Sarwar, A.; Islam, M.; Khan, S. Crystal structure algorithm (Crystal) based selective harmonic elimination modulation in a cascaded h-bridge multilevel inverter. *Electronics* **2021**, *10*, 3070. [CrossRef]
9. Millinger, J.; Wallmark, O.; Soulard, J. Possibilities and Limitations of Wide Bandgap Transistors in High-Speed Electric Drives. In Proceedings of the 2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe), Genova, Italy, 2–6 September 2019; IEEE: Piscataway, NJ, USA, 2019; pp. P.1–P.10. [CrossRef]
10. Yu, H.; Chen, B.; Yao, W.; Lu, Z. Hybrid Seven-Level Converter Based on T-Type Converter and H-Bridge Cascaded under SPWM and SVM. *IEEE Trans. Power Electron.* **2018**, *33*, 689–702. [CrossRef]
11. Xu, S.; Zhang, J.; Hu, X. Model Predictive Control for a Hybrid Multilevel Converter with Different Voltage Ratios. *IEEE J. Emerg. Sel. Top. Power Electron.* **2019**, *7*, 922–935. [CrossRef]
12. Rodriguez, J.; Cortes, P. *Predictive Control of Power Converters and Electrical Drives*; John Wiley & Sons, Ltd.: West Sussex, UK, 2012. [CrossRef]
13. Aly, M.; Ahmed, E.M.; Orabi, M.; Shoyama, M. An enhanced PWM method for loss balancing of five level T-type inverter in PV systems. In Proceedings of the 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, USA, 4–8 March 2018; IEEE: Piscataway, NJ, USA, 2018; pp. 2530–2535. [CrossRef]
14. Harbi, I.; Abdelrahem, M.; Ahmed, M.; Kennel, R. Reduced-Complexity Model Predictive Control with Online Parameter Assessment for a Grid-Connected Single-Phase Multilevel Inverter. *Sustainability* **2020**, *12*, 7997. [CrossRef]
15. Aly, M.; Carnielutti, F.; Shawky, A.; Ahmed, E.M.; Norambuena, M.; Kouro, S.; Rodriguez, J. Weighting Factorless Sequential Model Predictive Control Method with Fixed Switching Frequency for Five-Level T-type Photovoltaic Inverters. In Proceedings of the IECON 2021—47th Annual Conference of the IEEE Industrial Electronics Society, Toronto, ON, Canada, 13–16 October 2021; IEEE: Piscataway, NJ, USA, 2021; pp. 1–6. [CrossRef]
16. Zheng, C.; Dragicevic, T.; Zhang, Z.; Rodriguez, J.; Blaabjerg, F. Model Predictive Control of LC-Filtered Voltage Source Inverters with Optimal Switching Sequence. *IEEE Trans. Power Electron.* **2021**, *36*, 3422–3436. [CrossRef]
17. Harbi, I.; Rodriguez, J.; Liegmann, E.; Makhamreh, H.; Heldwein, M.L.; Novak, M.; Rossi, M.; Abdelrahem, M.; Trabelsi, M.; Ahmed, M.; et al. Model-Predictive Control of Multilevel Inverters: Challenges, Recent Advances, and Trends. *IEEE Trans. Power Electron.* **2023**, *38*, 10845–10868. [CrossRef]
18. Xie, H.; Novak, M.; Wang, F.; Dragicevic, T.; Rodríguez, J.; Blaabjerg, F.; Kennel, R.; Heldwein, M.L. Cooperative Decision-making Approach for Multi-objective Finite Control Set Model Predictive Control without Weighting Parameters. *IEEE Trans. Ind. Electron.* **2023**, 1–11. [CrossRef]
19. Harbi, I.; Abdelrahem, M.; Ahmed, M.; Kennel, R.; Rodriguez, J. Finite Set Model Predictive Control for Split-Capacitor Active-Neutral-Point-Clamped Inverter with Different Voltage Levels Operating Modes. In Proceedings of the 2021 IEEE International Conference on Predictive Control of Electrical Drives and Power Electronics (PRECEDE), Jinan, China, 18–20 September 2021; IEEE: Piscataway, NJ, USA, 2021; pp. 167–172. [CrossRef]
20. Harbi, I.; Ahmed, M.; Rodriguez, J.; Kennel, R.; Abdelrahem, M. Low-Complexity Finite Set Model Predictive Control for Split-Capacitor ANPC Inverter with Different Levels Modes and Online Model Update. *IEEE J. Emerg. Sel. Top. Power Electron.* **2023**, *11*, 506–522. [CrossRef]
21. Abdelrahem, M.; Harbi, I.; Ahmed, M.; Bin Arif, M.S.; Kennel, R.; Rodriguez, J. Finite-Set Model Predictive Control for 17-Level Inverter with Reduced Number of Iterations in Photovoltaic Applications. In Proceedings of the 2023 IEEE International Conference on Predictive Control of Electrical Drives and Power Electronics (PRECEDE), Wuhan, China, 16–19 June 2023; IEEE: Piscataway, NJ, USA, 2023; pp. 1–6. [CrossRef]
22. Wu, W.; Qiu, L.; Rodriguez, J.; Liu, X.; Ma, J.; Fang, Y. Data-Driven Finite Control-Set Model Predictive Control for Modular Multilevel Converter. *IEEE J. Emerg. Sel. Top. Power Electron.* **2023**, *11*, 523–531. [CrossRef]
23. Khosravi, M.; Khaburi, D.A.; Rodriguez, J. Simple two-stage weighting factor design for finite control set model predictive control of modular multilevel converters. *Int. J. Numer. Model. Electron. Netw. Devices Fields* **2022**, *35*, e2938. [CrossRef]
24. Cortes, P.; Kazmierkowski, M.P.; Kennel, R.M.; Quevedo, D.E.; Rodriguez, J. Predictive Control in Power Electronics and Drives. *IEEE Trans. Ind. Electron.* **2008**, *55*, 4312–4324. [CrossRef]
25. Rawa, M.; Siddique, M.D.; Mekhilef, S.; Shah, N.M.; Bassi, H.; Seyedmahmoudian, M.; Horan, B.; Stojcevski, A. Design and Implementation of a Hybrid Single T-Type Double H-Bridge Multilevel Inverter (STDH-MLI) Topology. *Energies* **2019**, *12*, 1810. [CrossRef]

26. Madasamy, P.; Suresh Kumar, V.; Sanjeevikumar, P.; Holm-Nielsen, J.B.; Hosain, E.; Bharatiraja, C. A Three-Phase Transformerless T-Type- NPC-MLI for Grid Connected PV Systems with Common-Mode Leakage Current Mitigation. *Energies* **2019**, *12*, 2434. [CrossRef]
27. Lei, Y.; Du, G.; Zhang, Y.; Li, T. Fixed switching frequency strategy for finite-control-set model predictive control based on cost function reconstruction. *J. Power Electron.* **2021**, *21*, 853–864. [CrossRef]
28. Yang, X.; Wang, K.; Kim, J.; Park, K.-B. Artificial neural network-based FCS-MPC for three-level inverters. *J. Power Electron.* **2022**, *22*, 2158–2165. [CrossRef]
29. Zhang, Z.; Zhang, J.; Wu, X. A single phase T-type inverter operating in boundary conduction mode. In Proceedings of the 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, USA, 18–22 September 2016; IEEE: Piscataway, NJ, USA, 2016; pp. 1–6. [CrossRef]
30. Liu, X.; Zhang, C.; Xing, X.; Zhang, R.; Liu, T.; Ren, Q. A Carrier-Based Low Total Current Ripple Modulation Strategy for Parallel Converters with Leakage Current Attenuation. *IEEE Trans. Ind. Electron.* **2023**, *70*, 3751–3761. [CrossRef]
31. *IEEE Std 519-2022 (Revision of IEEE Std 519-2014)*; IEEE Standard for Harmonic Control in Electric Power Systems. IEEE: Piscataway, NJ, USA, 2022; pp. 1–31. [CrossRef]