Proceedings

Linear Integrated Interface for Automatic Differential Capacitive Sensing †

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Abstract: In this work, the authors introduce a new full-analog front-end for differential capacitance sensors which provides a DC output voltage, directly proportional to the measurand variations. The readout circuit architecture is based on a De Sauty bridge as core of the capacitive sensing whereas the feedback circuitry performs the bridge autobalancing operation by means of changes in a multiplier output. The circuit is designed in a standard CMOS technology (AMS 0.35 μm) so is suitable for portable systems. Simulated results have shown a good agreement with the theoretical model being the percentage relative error less than 2.5%. Interface sensitivity is constant and values around 0.055 V/mm for the considered application.

Keywords: differential capacitance sensors; bridge-based circuits; CMOS technology; sensor interfaces

1. Introduction

In the last decade, capacitive transducers have been gaining popularity, in particular in sensor applications [1]. Capacitive sensors are able to sense and evaluate changes in physical or chemical quantities of interest through the detection of capacitance variations related to modifications of the sensor geometry or in the dielectric material [2]. Capacitive sensor values can span over several decades depending on the application, even if in the recent past the large adoption of MEMS systems lowered the useful range from hundreds of picofarads to fractions of picofarads [3,4]. This kind of sensing is typically performed by an indirect measurement through suitable interface electronic circuits. In this sense, owing to the reduced size of the sensors, the need of a simple and easily integrable interface is of a fundamental importance. In addition, capacitive sensors do not have intrinsic power consumption, thus they can be used with relatively LP circuit techniques, giving them a wide variety of possible applications [5].

A differential capacitive sensor can be represented by a three-plate system (see Figure 1) as the series of two capacitors C_1 and C_2. The two capacitors change their value in a differential way under the action of the measurand [6], which usually is the linear position of the middle plate with respect to the rest central position in displacement sensors.

The measurand variation estimated by the dimensionless variable x can be expressed as follows:

$$x = \frac{C_1 - C_2}{C_1 + C_2} \quad (1)$$

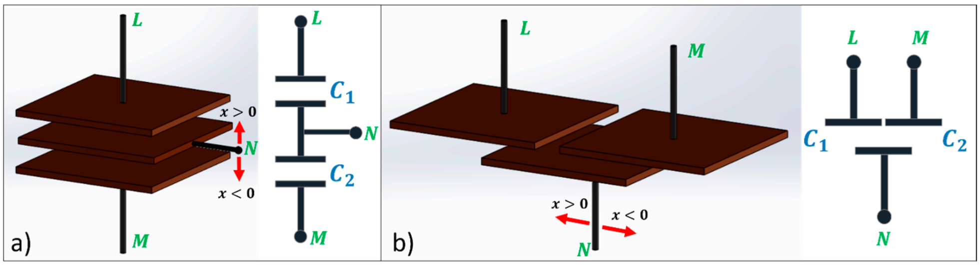

Figure 1. Differential capacitive sensor structure: (**a**) when the measurand influences the distance between plates; (**b**) when the measurand influences the overlapping area of plates.

This behavior makes such a sensor suitable for many applications like displacement and acceleration detection, position measurement, etc. [7–10].

The presented interface results in a deep upgrade with respect to [11,12]. The architecture core still relies on a De Sauty bridge; however, thanks to a redesign of the feedback circuitry, two major improvements have been achieved: Input-Output linearization, and full range autobalancing region. Moreover, with respect to what presented in [12], a fully integrated low-voltage low-power design using a standard CMOS technology has been implemented.

2. The Proposed Interface

The proposed interface is shown in Figure 2. Each block has been designed at transistor level, in a standard CMOS technology. The performed measurement technique consists of a capacitance-to-voltage conversion. The structure hosting the differential sensor is a simple De Sauty bridge, where the left branch is the differential capacitive sensor, whilst the right one is composed by a mechanism which emulates a voltage divider with a VCR (Voltage Controlled Resistor) replacing one resistor of the divider. Generally speaking, an autobalancing strategy can be considered as a negative feedback-based system whose aim is to minimize or null a certain error signal, e.g., the bridge unbalance. In the proposed solution, the feedback circuitry maintains the bridge balance by adjusting the Modulator multiplier output, to produce a signal Va which tends to follow Vb, hence forcing the error signal $\Delta V = Va - Vb$ to zero. The feedback signal V_{ctrl} is obtained by extracting the DC component of the error signal ΔV. This is achieved by synchronously demodulating ΔV performed with the Demodulator multiplier followed by a second order Sallen-Key filter, which removes the residual ripple and ensures a good dynamic response.

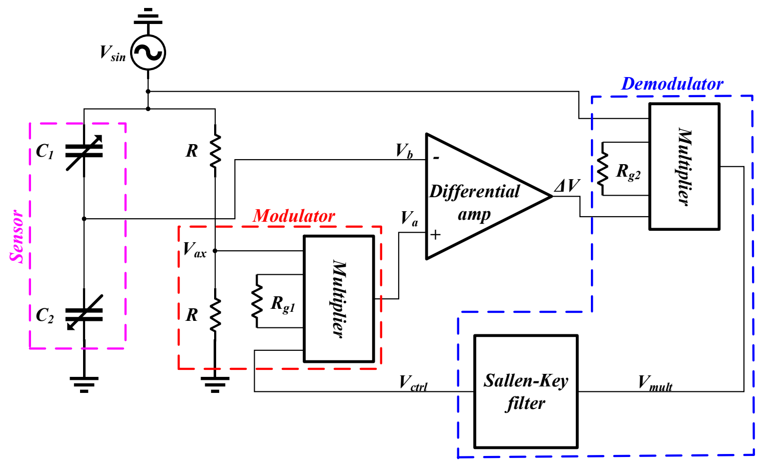

Figure 2. The block scheme of the proposed readout circuit.

A straightforward analysis brings to the following analytical linear relation between the measurand x (defined as in Equation (1)) and the voltage V_{ctrl}:

$$x = G_{mult} k V_{ctrl} - 1 \quad (2)$$

where G_{mult} is the total gain of the multipliers (that can be set varying the value of the two resistors *Rg*1 and *Rg*2) and *k* is a constant depending on both the multiplier design and on the used CMOS technology.

Figure 3a shows the Input-Output static characteristic of the interface. The product between G_{mult} and *k* has been set to $G_{mult}k = 18$, so obtaining a reduced punctual percentage relative error (<2.5%, see Figure 3b) of the simulated data with respect to the theoretical calculations. The curve in Figure 3a is widely contained within the supply voltage (output swing is limited by the multiplier linearity range), this means that no saturation is reached hence a complete ±100% autobalancing range is achieved.

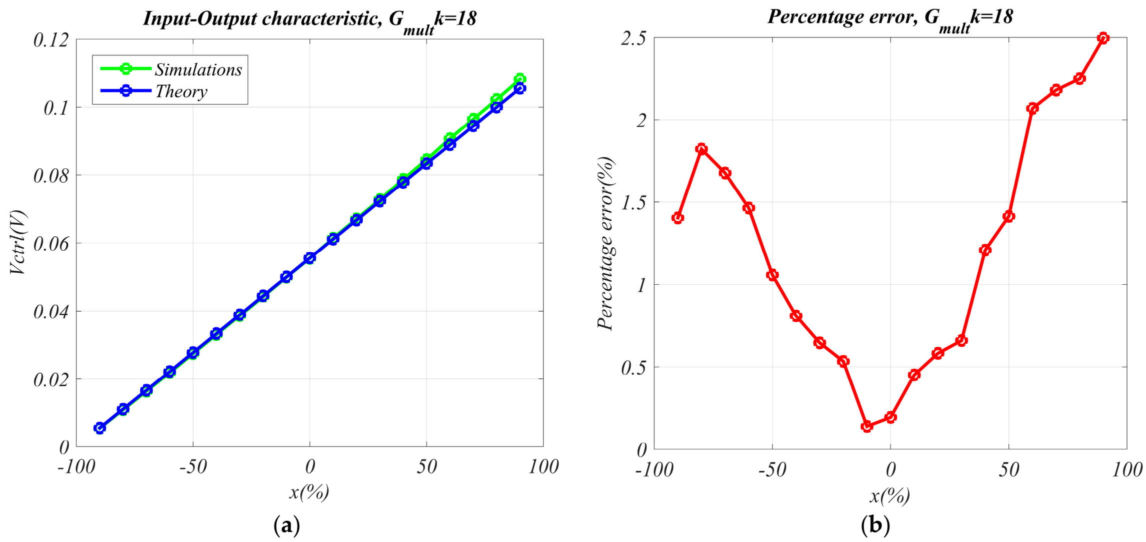

Figure 3. (**a**) Interface Input (x%)—Output (V_{ctrl}) response; (**b**) % percentage relative error between theory and simulation.

Sensitivity analysis has been performed in a displacement measurement application, where a typical baseline value (which corresponds to $x = 0$) has been set to 1 mm in Figure 4. Sensitivity is ideally constant (roughly 0.055 V/mm) and it slightly fluctuates around 0.058 V/mm in simulated results.

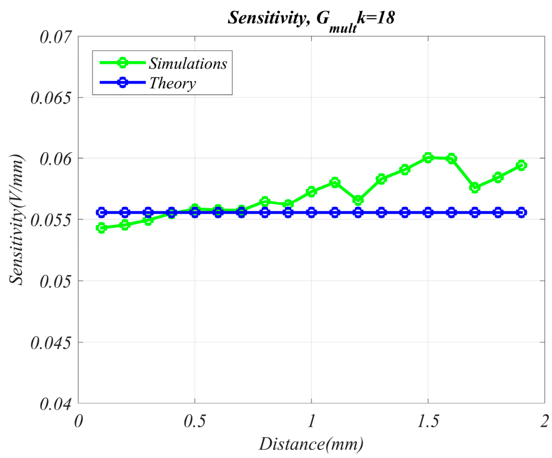

Figure 4. Interface sensitivity vs. distance.

3. Conclusions

A fully integrated low-voltage low-power design using a standard CMOS technology is presented, showing a good agreement with theoretical and simulation results. This work overcomes the main issue of a previous similar solution, i.e., a non-linear relation between the output response and the measurand, providing a direct simple relationship between measurand variations and output voltage. Theoretical and simulated considerations have demonstrated the effectiveness of the proposed approach, confirming the circuit capability to allow a full estimation range.

Conflicts of Interest: The authors declare no conflict of interest.

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