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Advances in Ultra-High-Speed Transceiver IC

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Message from the Guest Editors

Dear Colleagues,

The explosive growth of internet traffic and computing power drives the increasing demand for wireline transceiver data rates. In recent years, various transceiver architectures have been proposed to optimize the link performance in emerging applications. DSP-based transceivers demonstrate robust PAM-4 data transmission on high-loss channels, while the analog counterparts achieve better energy efficiency and lower latency. Although differential signaling provides better signal integrity, single-ended signaling achieves higher bandwidth density in memory interfaces and in-package communications.

This Special Issue of *Electronics* aims to report recent advances in ultra-high-speed transceiver IC, including wireline transceivers achieving outstanding performance, circuit innovations, and new design methodology. The topics of interest include, but are not limited to, the following:

- Backplane transceivers
- High-speed memory interfaces
- In-package communications
- Die-to-die chiplet transceivers
- Optical links
- Plastic waveguide links
- Advanced clock and data recovery
- Building blocks for transceivers
- Equalization techniques

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Message from the Editor-in-Chief

Electronics is a multidisciplinary journal designed to appeal to a diverse audience of research scientists, practitioners, and developers in academia and industry. The journal is devoted to fast publication of latest technological breakthroughs, cutting-edge developments, and timely reviews of current and emerging technologies related to the broad field of electronics. Experimental and theoretical results are published as regular peer-reviewed articles or as articles within Special Issues guestedited by leading experts in selected topics of interest.

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