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Emerging Interconnection Networks Across Scales

Guest Editor:

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Deadline for manuscript submissions: closed (15 December 2018)

Message from the Guest Editor

To advance and capture the recent and future innovations in interconnection technology at multiple scales, such as on-chip networks, chip-to-chip interconnections and data center networks, the proposed Special Issue of JLPEA will be dedicated towards innovative ways of interconnecting electronic devices. The readers of this Special Issue will be able to familiarize themselves with the recent advances in these technology paradigms, while also discovering the common and disparate issues about these interconnections at these various scales. Original contributions from the following non-exhaustive list of topics are solicited:

- Power efficiency in Network-on-Chip
- Chip-to-chip interconnections
- Interconnections for heterogeneous systems
- Dynamic interconnection networks
- Data center networks
- 3D NoC
- Photonic/optical interconnects
- RF interconnections
- Wireless interconnects
- Millimeter-wave wireless communication for computing platforms
- THz band communications for computing systems
- Security and Privacy in NoC
- Data center network security and privacy
- Congruence of interconnection networks with IoT





mdpi.com/si/14573





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Editor-in-Chief

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Message from the Editor-in-Chief

Journal of Low Power Electronics and Applications (ISSN 2079-9268) is an open access journal which provides an advanced forum for the studies of electronics for low power applications. A special emphasize is made on ultralow power bio-medical applications. It publishes reviews, regular research papers and short communications.

Our aim is to encourage scientists to publish their experimental and theoretical results in as much detail as possible. There is no restriction on the length of the papers. Full experimental and/or methodical details must be provided.

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