



Low Power in FD-SOI Technology

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Message from the Guest Editors

Due to its unique inherent properties, fully depleted silicon-on-insulator (FD-SOI) is gaining a consolidated position on a number of new markets, ranging from Internet of Things (IoT) to automotive, from e-health to big data and machine learning, etc.

This special issue is devoted to the latest developments in power-efficient circuit and system design in the FD-SOI technology, in a broad sense. It will reflect a wide spectrum of research topics from architecture design, to analog, digital, RF, sensors or MEMS modules, microsystems or SoC, modelling and test.

- Energy harvesting and power management circuit for IoT devices.
- Modelling, design, simulation and characterization of Devices, Circuits and Systems for ultra-low voltage and ultra-low power consumption.
- Highly power-efficient circuits for digital and analog computing, RF transmission.
- Co-integration of sensors or MEMS.
- Reconfigurable architectures.
- IoT security features including low-power encryption and authentication.
- Circuits, systems and methods for on-chip energy-efficient machine learning.





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Message from the Editor-in-Chief

Journal of Low Power Electronics and Applications (ISSN 2079-9268) is an open access journal which provides an advanced forum for the studies of electronics for low power applications. A special emphasize is made on ultralow power bio-medical applications. It publishes reviews, regular research papers and short communications.

Our aim is to encourage scientists to publish their experimental and theoretical results in as much detail as possible. There is no restriction on the length of the papers. Full experimental and/or methodical details must be provided.

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Rapid Publication: manuscripts are peer-reviewed and a first decision is provided to authors approximately 22.2 days after submission; acceptance to publication is undertaken in 4.7 days (median values for papers published in this journal in the second half of 2023).

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