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A Novel Direct Current Circuit Breaker with a Gradually Increasing Counter-Current

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Abstract: A reliable and cost-effective mechanical direct current circuit breaker (DCCB) is a promising solution for DC interruption. However, the typical mechanical DCCB has difficulty in interrupting a rated current, because the high oscillating current superimposed on the rated current generates a steep current slope at current zero-crossing (CZC) points, which makes it difficult for the vacuum interrupter to extinguish the arc. The objective of this paper is to present a novel DCCB topology with a gradually increasing counter-current. It utilizes a full-controlled converter, a semi-controlled full bridge, and an LC oscillation branch to generate a gradually increasing counter-current, which is superimposed on any fault current and generates a smooth current slope at CZC points. The proposed DCCB topology is modeled with PSCAD, and the current slope and the initial transient interruption voltage (ITIV) at CZC are analyzed and compared with the typical mechanical DCCB. The results indicate that the current slope at CZC decreases by 57–84% in full-range current interruptions, and the ITIV can be reduced by the same extent. Additionally, the performance of the proposed DCCB is evaluated in a four-terminal HVDC system. A cost and performance comparison is conducted among the main topologies. The obtained results show that the proposed DCCB is a reliable solution for the multi-terminal HVDC system.

Keywords: DC power transmission; HVDC and power electronics; circuit breaker; switching transients

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1. Introduction

With the mature development of offshore wind power technology, sustainable and renewable energy has become the key to solving the energy crisis [1]. The meshed high-voltage direct current (HVDC) grid is the inevitable choice for future long-distance transmission of wind power from offshore to onshore grid [2,3]. Meanwhile, the HVDC circuit breaker is the key equipment to clear the fault and isolate the failed converter station, which plays a crucial role in the reliable operation of the meshed HVDC grid [4].

The absence of current zeros and fast-rising fault current in the DC system make it more difficult for DC circuit breakers (DCCB) to interrupt the fault [5]. Many researchers have proposed individual DC circuit breaker concepts and topologies to interrupt the fault current within several milliseconds [6–10]. These HVDC circuit breakers applied in multi-terminal DC systems can be sorted into two categories according to their interrupting mechanism, namely, the hybrid DC circuit breakers and the mechanical DC circuit breakers [4]. On one hand, the hybrid DC circuit breaker utilizes a large number of fully controlled power electronics to interrupt the fault current directly, resulting in high on-state loss and high cost [11–14]. On the other hand, the mechanical DC circuit breakers utilize a parallel circuit branch to inject an oscillation current and generate current zero-crossing (CZC) points in the vacuum interrupter, thus allowing the vacuum arc to be extinguished [15,16]. The oscillation mechanism of parallel circuit branches in mechanical DC breakers can be classified into two types: active oscillation and passive oscillation. In

an active oscillation DC breaking schema, a high-frequency oscillation current is generated through the discharge of a pre-charged capacitor along an LC path [17,18]. In a passive oscillation DC breaking schema, the oscillation is stimulated by a gas arc or vacuum arc subjected to an external transverse magnetic field with a passive LC path [19,20]. The mechanical DC circuit breakers have the advantages of low on-state losses and low cost, which makes them advantageous to promote the application. The mechanical DC circuit breakers in the Zhangbei DC project interrupt the $\pm$500 kV/25 kA fault current within 3 ms, which is by far the highest DC interruption rating in the world [14].

The reliable extinguishing of vacuum arcs at CZC points becomes a key issue in developing mechanical HVDC CBs [21]. In AC vacuum interrupters development, the extinguishing of vacuum arcs has been well studied [22–24]. However, in DCCB, a high-frequency oscillating current generated by the commutation branch is superimposed on the fault current, making the current slope at CZC very steep. The current slope at CZC is positively related to the remaining plasma density in the vacuum interrupter. Meanwhile, the residual voltage on the pre-charged capacitor in the commutation branch is instantaneously applied to the vacuum interrupter at the CZC point [25]. At the instant of DC interruption, the plasma density in the vacuum interrupter is the highest, and the initial transient interruption voltage (ITIV) applied to the vacuum interrupter is the largest [26], which is the most severe electrical stress on the dynamic insulation of the vacuum switch in the whole DC interruption process. As a result, the current slope at CZC plays a decisive role in ensuring the reliable interruption ability of DC CBs [27]. Jia and Shi investigated the post-arc phenomenon in [28], which indicates that the post-arc and residual plasma increase linearly with $\mathrm{d}u/\mathrm{d}t \times \mathrm{d}i/\mathrm{d}t$. Moreover, only the arcing current within 4.5 µs memory time before CZC influences the post-arc current. Typical mechanical DCCBs utilize a pre-charged LC commutation branch to generate an oscillating current with equal or damped amplitude. The oscillating current is superimposed on fault currents of different amplitudes, which results in higher values of the current slope and ITIV at CZC for smaller fault currents [29]. Therefore, typical mechanical DCCBs are less reliable in interrupting small currents in the order of several tens to hundreds of amperes. In recent years, power electronic devices have been extensively applied in mechanical DC circuit breakers to enhance their performance. Scibreak AB developed a mechanical DC circuit breaker incorporating a voltage source converter in series with an active LC circuit, enabling interruption of up to 10 kA against a transient interruption voltage of 40 kV [30]. Zhuang proposed a topology that combines an LC circuit with parallel IGCTs to enhance the dielectric strength recovery process of the vacuum by delaying the transient recovery voltage after current zero in the vacuum interrupter [31]. Zhang proposed a topology in which a repetitively switched auxiliary electronic switch in the main branch helps an oscillation in the passive LC path [32]. North China Electric Power University enhanced the topology in [32], employing the soft-switching technique [33]. These enhanced topologies with power electronic devices improve the cost and reliability of mechanical DCCBs. However, the oscillation current is forwardly superimposed on the fault current in some half periods, which results in high current arcing between contacts and a steep current crossing in the next oscillation period.

A novel DCCB topology is proposed to overcome the problem of interruption reliability caused by a high current slope and high ITIV at CZC. This topology consists of a full-controlled converter, a semi-controlled full bridge, and an LC oscillation branch. The full-controlled converter is used to change the conduction direction of the oscillating current at CZC so that the discharge direction of the energy storage capacitor is always consistent with the oscillating current, which generates a counter-current with gradually increasing amplitude. The gradually increasing counter-current superimposed on any fault current produces a smoother current slope at CZC and lower ITIV. The vacuum interrupter is driven by an ultra-fast operating mechanism, with fast opening and closing speeds. And the on-state loss is comparable to typical mechanical DCCBs.

The remainder of this paper is organized as follows: Section 2 presents the novel DCCB topology and its working principle and timing sequence. The detailed modeling

of the proposed DCCB and simulation results are demonstrated in Section 3, and the interruption characteristics are compared to the existing mechanical DCCB topology. In Section 4, a higher voltage level DCCB is demonstrated and analyzed in a four-terminal HVDC grid, and the results are analyzed. In Section 5, a cost and performance comparison is made between the proposed topology and the other representative topologies. And the limitations of this research are discussed. Finally, conclusions based on the obtained results of this study are presented in Section 6.

2. Topology and Working Principle

2.1. Topology of Proposed DC Circuit Breaker

The novel topology of the proposed DCCB is shown in Figure 1. The breaker consists of three branches, namely, the main branch, the commutation branch, and the energy absorption branch.

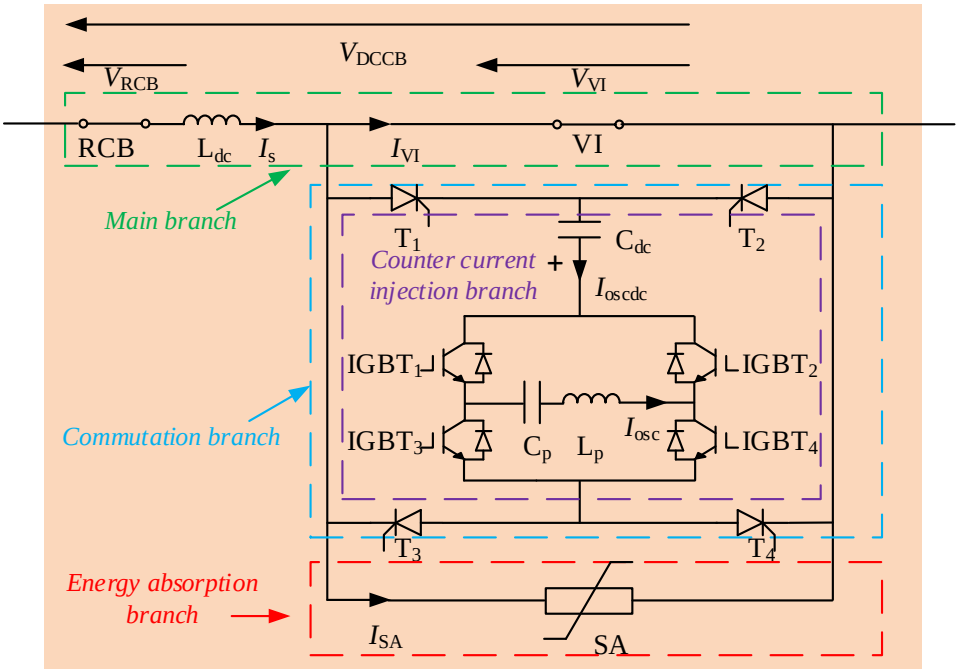

Figure 1. Schematic of the novel DC circuit breaker.

The main current branch consists of a vacuum interrupter (VI), a residual current breaker (RCB), and a current-limiting reactor (L_{dc}). The vacuum interrupter and residual current breaker are both mechanical switches with low ohmic losses in the closed position. So, the rated current flows through the main path with low on-state loss. The current-limiting reactor is used to effectively limit the rate of rise of fault current.

The commutation branch includes a 4-thyristor bridge (T_1~T_4) and a counter-current injection branch. The counter-current injection current branch consists of a pre-charged capacitor (C_{dc}), a 4-IGBT bridge ($IGBT_1$~$IGBT_4$), and an LC oscillation circuit (C_p, L_p). The LC oscillation circuit installed in the 4-IGBT bridge is not pre-charged. The current in the LC oscillation circuit (I_{osc}) is an oscillating current with gradually increasing amplitude. Due to the rectification of the 4-IGBT bridge, the counter-current injection branch generates a unidirectional gradually increasing counter-current (I_{oscdc}) to make an artificial current zero in the main current branch. The 4-thyristor bridge enables the bidirectional interruption by conducting the gradually increasing counter-current with different paths. The energy absorption branch is composed of a surge arrester to protect the DCCB from overvoltage and absorb the residual electromagnetic energy stored in the system.

2.2. Working Principle and Time Sequence

The working sequence of the novel proposed topology is illustrated in Figure 2. The process of current interruption can be divided into six stages. And the typical waveform and status of switches during the current interruption process are shown in Figure 3. I_s, I_{VI}, and I_{SA} represent the current flowing through the total DCCB, vacuum interrupter, and surge arrester, respectively. V_{VI}, V_{RCB}, and V_{DCCB} are the voltage across the vacuum interrupter, the residual current breaker, and the DCCB, respectively. The MB and RCB signals indicate the status of the switches, with a low signal indicating a closed switch and a high signal indicating an open switch. The $T_{1/4}$ represents the trigger signal of thyristors T_1 and T_4. The $IGBT_{1/4}$ represents the control signal for $IGBT_1$ and $IGBT_4$. The $IGBT_{2/3}$ represents the control signal for $IGBT_2$ and $IGBT_3$. The reference directions of the above physical quantities are all shown in Figure 1.

As shown in Figure 2a, the rated current flows through the main branch. At time t_1, a fault occurs, leading to a rapidly rising fault current. At time t_2, the trip signal activates the DCCB to interrupt the fault current. The contacts start to separate with an arc igniting between them.

At time t_3, the gap between contacts reaches a sufficient distance. The commutation branch is enabled to transfer the fault current. The 4-thyristor bridge is triggered according to the direction of the fault current. For example, thyristors T_1 and T_4 conduct when the fault current flows the DCCB from left to right in Figure 2b. During time t_3 and t_4, the 4-IGBT bridge operates in two states. The four IGBTS are switched on and off repeatedly at the oscillation frequency of the circuit to rectify the oscillating current (I_{osc}) to the unidirectional counter-current (I_{oscdc}), as shown in Figure 2b,c. In the first state, the $IGBT_1$ and $IGBT_4$ are triggered, forming an oscillation circuit of C_{dc}—$IGBT_1$—C_p—L_p—$IGBT_4$—T_4—VI—T_1. The C_{dc} discharges through the forming oscillation circuit until the oscillation current I_{osc} crosses zero. Then, the commutation branch turns to the second state, as shown in Figure 2c. In the second state, the $IGBT_2$ and $IGBT_3$ are triggered, forming another oscillation circuit of C_{dc}—$IGBT_2$—L_p—C_p—$IGBT_3$—T_4—VI—T_1. The C_{dc} continues to discharge through the newly formed oscillation circuit until the oscillation current I_{osc} crosses zero again. Subsequently, the commutation branch reverts to the first state. The two pairs of IGBTs are alternatively turned on and turned off when the oscillation current I_{osc} crosses zero. With the rectification by the 4-IGBT bridge, the oscillation current I_{osc} is converted into a unidirectional counter-current I_{oscdc} and injected into the vacuum interrupter. The rectified oscillating current (I_{oscdc}) superimposes the current in the vacuum interrupter (I_{VI}) to create an artificial current zero.

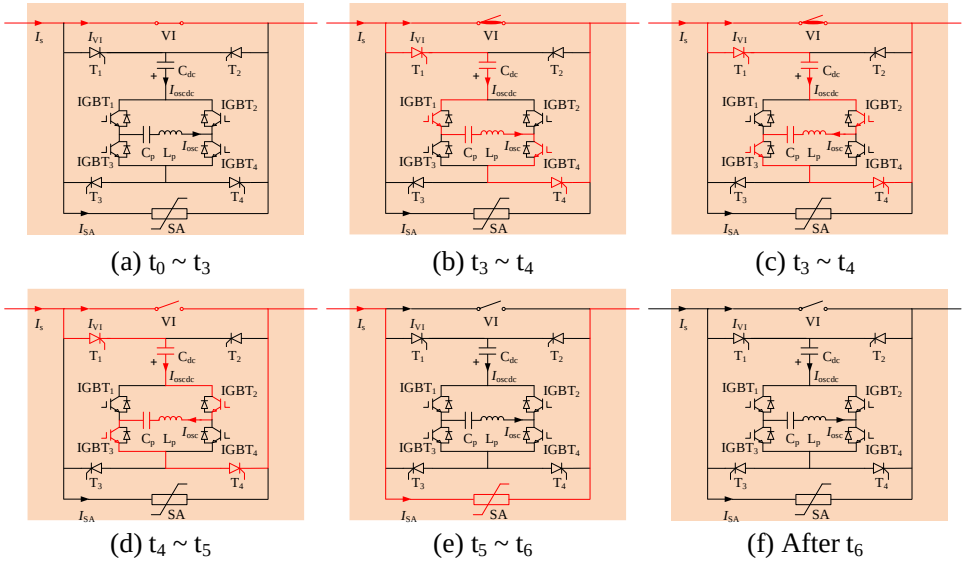

Figure 2. The working sequence of interruption.

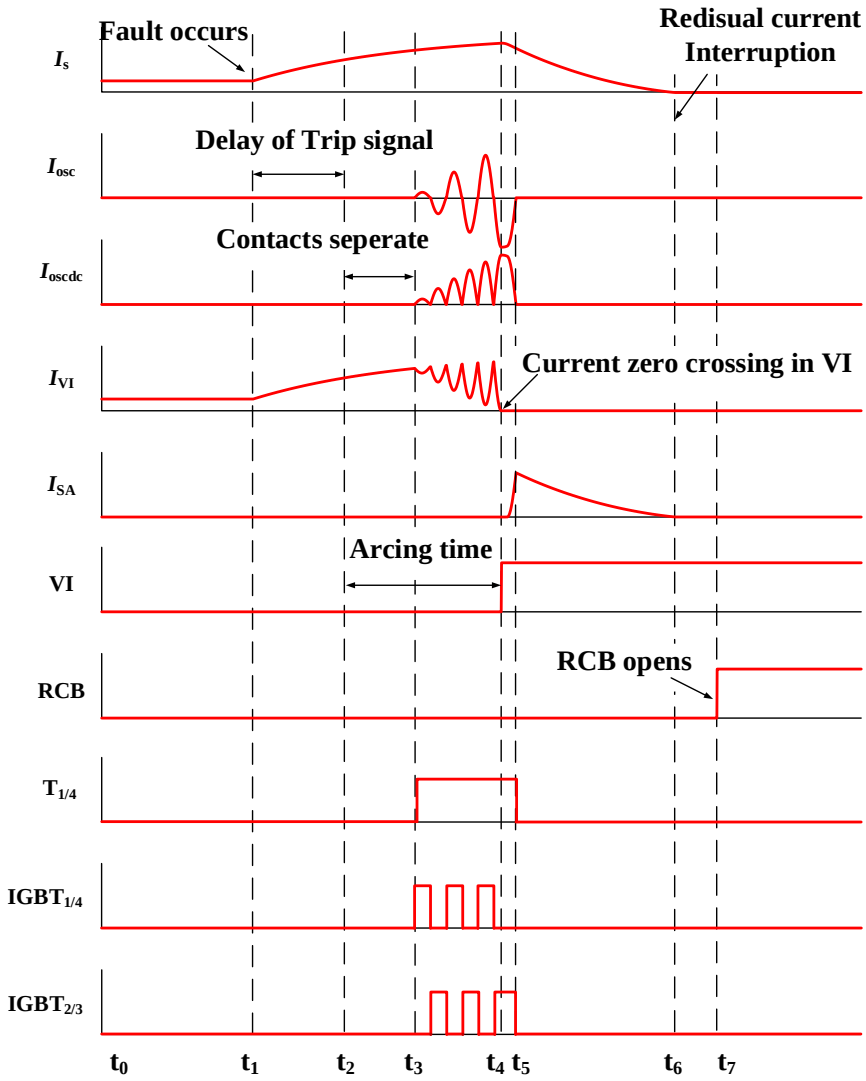

Figure 3. The waveform and status during the interruption.

At time t_4, the current in the vacuum interrupter (I_{VI}) drops to zero. The arc between contacts is extinguished. The vacuum interrupter withstands transient recovery voltage. Figure 2d shows the case that the zero-crossing occurs in the second state of the 4-IGBT bridge. The $IGBT_2$ and $IGBT_3$ keep conducting during t_4 and t_5. The fault current charges capacitors in the commutation branch. The voltage across the surge arrester rises rapidly and reaches the threshold voltage at time t_5. The fault current then transfers to the energy absorption branch. The thyristors T_1 and T_4 and $IGBT_2$ and $IGBT_3$ are turned off at t_5. During time t_5 and t_6, the residual electromagnetic energy stored in the system dissipates in the form of heat by the surge arrester.

At time t_6, the fault current decreases to zero. After a short period of delay, the residual circuit breaker (RCB) opens to disconnect the residual current at time t_7. The fault current is cleared successfully. The process of interruption ends.

2.3. Analysis of the Commutation Process

The process of high-frequency oscillation in the counter-current injection current branch is essential. The current excitation principle can be explained as follows. As shown in Figure 2b, the pre-charged capacitor (C_{dc}) and the 4-IGBTs form a voltage source converter within the vacuum interrupter. Thus, the commutation branch omitted the 4-thyristor bridge can be simplified as a voltage source converter in series with an LC oscillation circuit.

The oscillation in such an oscillation circuit connected with a voltage source converter provides an oscillating current I_{osc} with increasing amplitude.

The oscillation process is illustrated in Figure 4. As shown in Figure 4a, the pre-charged capacitor C_{dc} is in series with the capacitor C_p in the LC oscillation circuit. These two capacitors form an equivalent pre-charged capacitor C_{osc} with voltage $U_{dc.}$ The mathematical expression of C_{osc} is reported in Equation (1).

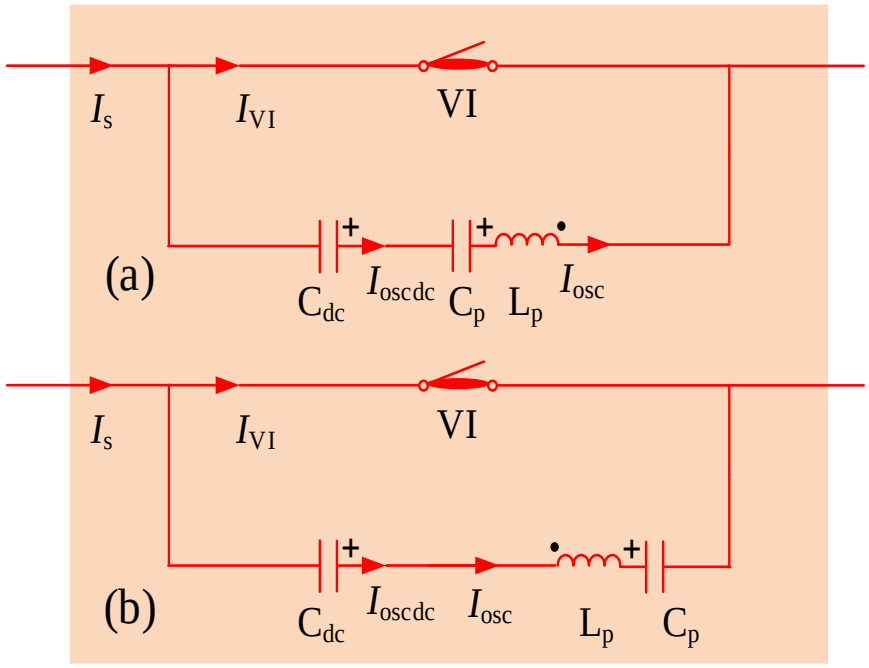

Figure 4. Illustration of oscillation process in commutation branch; (**a**) oscillation circuit in first half-cycle of oscillation; (**b**) oscillation circuit in second half-cycle of oscillation.

$$C_{osc} = C_{dc}C_p/(C_{dc} + C_p) \tag{1}$$

The LC oscillation circuit is described with a second-order differential equation and the initial state of the circuit in Equation (2). The commutation process results in a zero-input response of the LC oscillation circuit.

$$\begin{aligned} &L_pC_{dc}\tfrac{d^2u_{dc}}{dt^2} + u_{dc} + u_{C_p} + E_{arc} = 0 \\ &u_{dc}(0) = U_{dc};\ \tfrac{du_{dc}}{dt}(0) = 0;\ u_{C_p}(0) = 0 \end{aligned} \tag{2}$$

E_{arc} in Equation (2) is the voltage of the vacuum arc, which is usually about 20 V and can be neglected to simplify the analysis. The differential equation using C_{osc} can be simplified and it is reported in Equation (3):

$$\begin{aligned} &L_pC_{osc}\tfrac{d^2u_{C_{osc}}}{dt^2} + u_{C_{osc}} = 0 \\ &u_{C_{osc}}(0) = U_{dc};\ \tfrac{du_{C_{osc}}}{dt}(0) = 0 \end{aligned} \tag{3}$$

Thus, the current amplitude I_1 and frequency f_{LC} are obtained by the formula reported in Equation (4).

$$\begin{aligned} &I_1 = U_{dc}\sqrt{C_{osc}/L_p} \\ &f_{LC} = 1/(2\pi\sqrt{L_pC_{osc}}) \end{aligned} \tag{4}$$

The voltage across C_p can be calculated by its constitutive relation and initial state according to Equation (5):

$$\begin{aligned} C_p \frac{du_{C_p}}{dt} &= i \\ u_{C_p}(0) &= 0 \end{aligned} \tag{5}$$

The voltage across C_{dc} can be obtained by Equation (6):

$$u_{dc} = u_{C_{osc}} - u_{C_p} \tag{6}$$

After a half-cycle discharging, the voltage of capacitor C_{osc} is reversed and has its voltage $-U_{dc}$. Since the capacitance of C_{dc} is much larger than that of C_p, the voltage of C_{dc} remains U_{dc}. So, the voltage of C_p reaches $-2U_{dc}$.

As shown in Figure 4b, the connection of C_p and L_p is inversed at the second half-cycle. Now, the voltage of C_{osc} turns to $3U_{dc}$, resulting in the oscillating current with a new amplitude of 3 I_1. After the second half-cycle, the connection of the oscillation circuit turns to the first state as shown in Figure 4a. The new period of oscillation begins.

During the commutation process, the oscillating current adds 2 I_1 every half-cycle, and the current peak in the Nth half-cycle is $(2N-1)I_1$.

The voltage of C_{osc} and oscillating current in the time domain can be expressed with Equation (7) as follows:

$$\begin{aligned} V_{C_{osc}}(t) &= (2N-1)U_{dc}\cos(2\pi f_{LC}t) \\ I_{osc}(t) &= (2N-1)I_1\sin(2\pi f_{LC}t) \end{aligned} \tag{7}$$

With the rectification of the 4-IGBT bridge, the injected counter-current I_{oscdc} is presented with Equation (8) as follows:

$$I_{oscdc}(t) = (-1)^{N-1}(2N-1)I_1\sin(2\pi f_{LC}t) \tag{8}$$

The current slope in the vacuum interrupter at the zero-crossing is important for the interruption, which influences greatly the probability of reignition. Only when the current slope is lower than a critical value, which is related to the material of contacts of the vacuum interrupter, can the interruption of the current at zero-crossing be successfully carried out.

The instant of zero-crossing t_4 satisfies the following Equation (9):

$$I_{oscdc}(t_4) = (-1)^{N-1}(2N-1)I_1\sin(2\pi f_{LC}t_4) = I_s \tag{9}$$

The number of half-cycles N is required to obtain t_4. And it is limited by two inequalities reported in Equation (10):

$$\begin{aligned} (2N-1)I_1 &\geq I_s \\ (2N-3)I_1 &< I_s \end{aligned} \tag{10}$$

N can be expressed as $\lceil (I_s + I_1)/2I_1 \rceil$, meaning the ceiling value of $(I_s + I_1)/2I_1$.

The instant of zero-crossing t_4 is expressed with Equation (11) as follows:

$$2\pi f_{LC}t_4 = \arcsin\left(\frac{-I_s}{(2N-1)V_{DC}}\sqrt{\frac{L_P}{C_{OSC}}}\right) \tag{11}$$

So, the slope at zero-crossing of I_{VI} can be obtained by Equation (12):

$$\begin{aligned} S &= \frac{di_{VI}}{dt}\Big|_{t=t_4} = -I'_{oscdc}(t_4) \\ &= (-1)^N 2\pi f_{LC}(2N-1)I_1\cos(2\pi f_{LC}t_4) \end{aligned} \tag{12}$$

At time t_4, the vacuum interrupter withstands an ITIV. ITIV is applied by the commutation branch in parallel with the interrupter. As the circuit stops oscillation, the voltage across

the inductor L_p is zero. ITIV is applied by C_{osc} and can be expressed with Equation (13) as follows:

$$\mathrm{ITIV} = (-1)^N (2N-1) U_{dc} \cos(2\pi f_{LC} t_4) \quad (13)$$

3. Simulation of the DCCB

3.1. Introduction of the Simulation Model

The topology of the proposed DC circuit breaker is modeled in PSCAD. As an example, the simulation model is given in Figure 5. It is assumed that the voltage source is on the left side of the DC circuit breaker, while the short circuit fault is on the right side. And the parameters of the simulation model are given in Table 1. The rated voltage and current of the DC system are 10 kV and 2 kA, respectively.

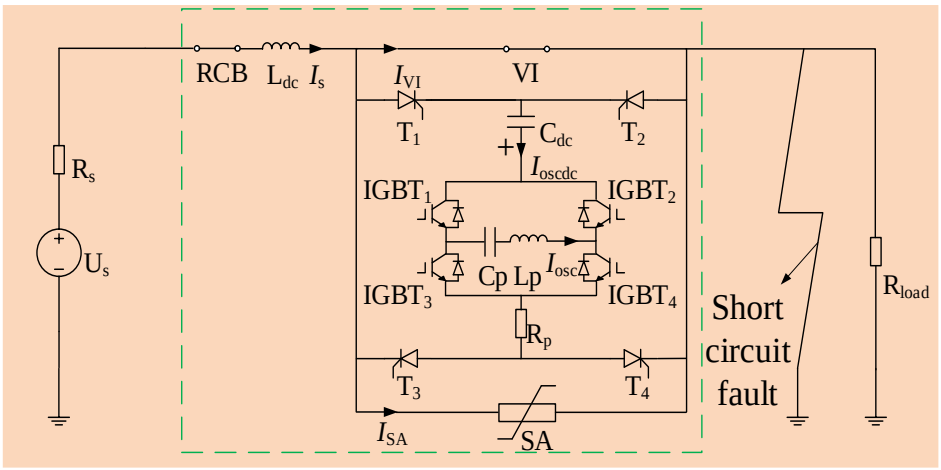

Figure 5. The simulation model of DC interruption.

Table 1. Main parameters of the simulation model.

Parameter	Description	Value
U_s	Source voltage	10 kV
R_s	Source resistance	0.1 mΩ
R_{load}	Load resistance	5 Ω
R_{fault}	Fault resistance	1.25 Ω
L_{dc}	Inductance of current-limiting reactor	0.5 mH
C_{dc}	Capacitance of pre-charged capacitor	5 mF
U_{dc}	Charging voltage of the pre-charged capacitor	1200 V
C_p	Capacitance of the oscillation capacitor	13 μF
L_p	Inductance of oscillation inductor	20 μH
R_p	Resistance of parasitic resistor	0.01 Ω
U_{SA}	Protection voltage of surge arrester	15 kV

With these parameters given in Table 1, the commutation branch injects a gradually increasing counter-current I_{oscdc}, which has its first current peak I_1 as 0.96 kA and frequency f_{LC} as 9.87 kHz.

The current slope at zero-crossing and the recovery of dielectric strength are considered in the simulation. The stroke of a fast vacuum CB is introduced in the simulation to evaluate the process of dielectric recovery strength. Three conditions are necessary to successfully interrupt the current:

1. An artificial CZC point which allows the arc to extinguish;
2. The current slope di/dt at the CZC point is lower than a critical value, which is set as 1000 A/μs. The arc reignites with a higher current slope at the CZC point;
3. The dielectric recovery strength of the vacuum interrupter can withstand the transient recovery voltage.

3.2. Simulation Results of Rated and Fault Current Interruptions

The simulation results of a 2 kA-rated current interruption are given in Figure 6. The trip signal is sent to the DCCB at t = 0 ms. The ultra-fast mechanism drives the contacts of the vacuum interrupter to separate as soon as the DCCB receives the trigger signal. At t = 0.53 ms, the commutation branch is enabled as the gap of contacts is sufficient. The gradually increasing counter-current I_{oscdc} reaches 2 kA in its second half-cycle. The time for oscillation in the commutation branch is 66 μs. The gradually increasing counter-current superimposes the system current and creates an artificial CZC. The current in vacuum interrupter I_{VI} is interrupted at the current zero-crossing, and system current I_S is transferred to the commutation branch. The current slope at zero-crossing is −94 A/μs. The vacuum interrupter withstands an ITIV of −2.01 kV and a TRV with a peak of 13.43 kV. The system current charges the oscillation capacitor C_p to the threshold voltage of the surge arrester. The charging time lasts 0.12 ms. The surge arrester conducts at t = 0.71 ms and absorbs electromagnetic energy. The time for energy absorption lasts 106 μs. The interruption time from receiving the trip signal to the interrupting current is 0.82 ms.

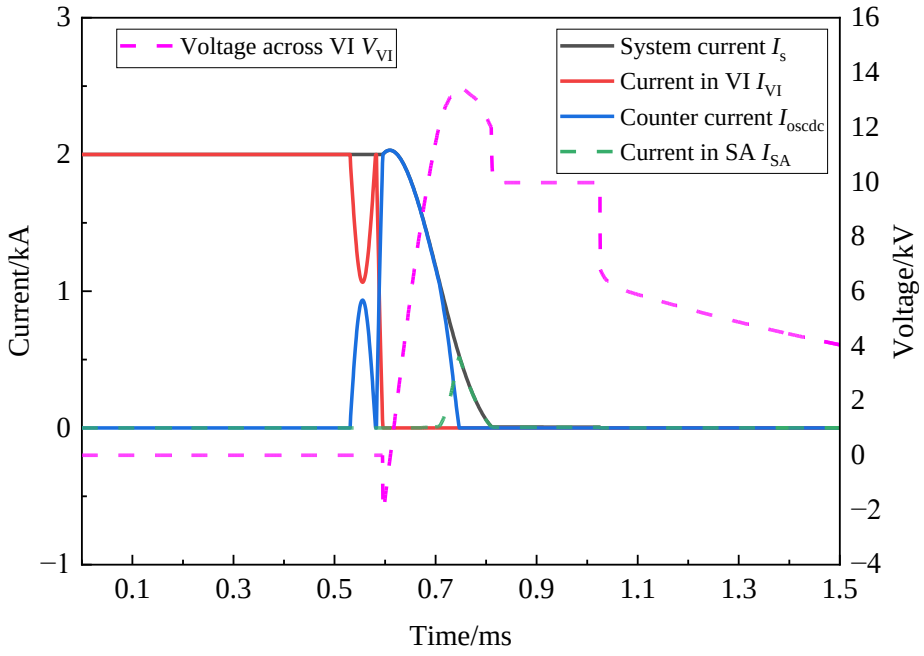

Figure 6. Simulation results of rated current interruption.

The simulation results of a 10 kA fault current interruption are given in Figure 7. A short fault occurs at t = 0.2 ms. The system current I_s rises rapidly to 7.7 kA at t = 1.2 ms when the DCCB receives the trip signal. The CB works with the typical sequences as indicated before. It takes 8 half-cycles (384 μs) for the counter-current to reach 10 kA. The current slope at CZC is −182 A/μs. The ITIV and TRV peaks are −3.47 kV and 15.05 kV, respectively. The time for energy absorption lasts 0.48 ms. The total interruption time is 1.42 ms.

According to the above simulation results, this novel DCCB can interrupt 2 kA-rated current and 10 kA fault current in a 10 kV system with limited current slope and ITIV at zero-crossing. For the rated current interruption, the total interruption time is 0.82 ms, and the current slope and ITIV at zero-crossing are −94 A/μs and −2.01 kV, respectively. For

the fault current interruption, the total interruption time is 1.42 ms, and the current slope and ITIV at zero-crossing are −182 A/μs and −3.47 kV, respectively.

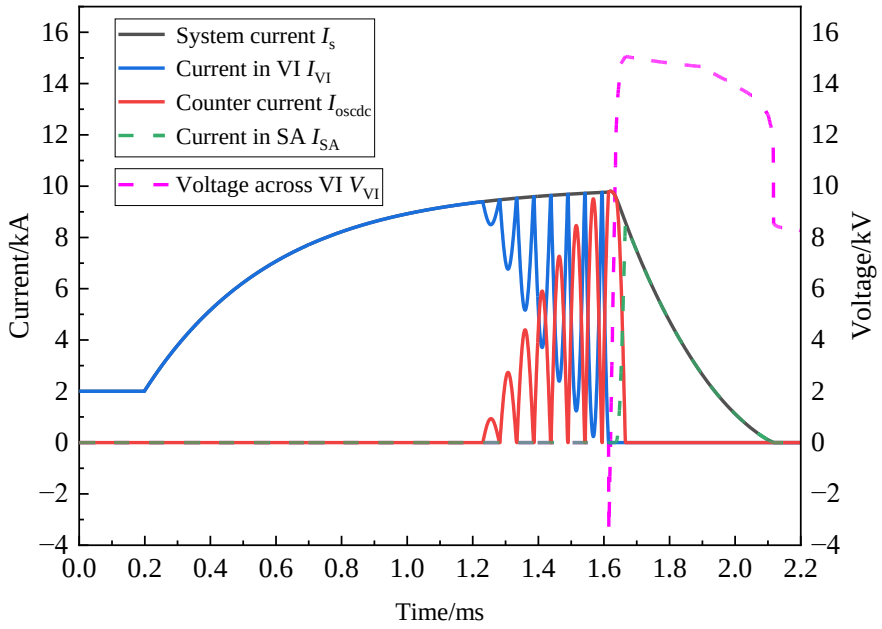

Figure 7. Simulation results of fault current interruption.

3.3. Comparison of Characteristics of DC Circuit Breakers

The current slope at CZC is one of the important factors for successful interruption. To study the impact of current value on the current slope, multiple simulations are conducted with different system currents. The results are given in Figure 8. Each dot represents an interruption simulation.

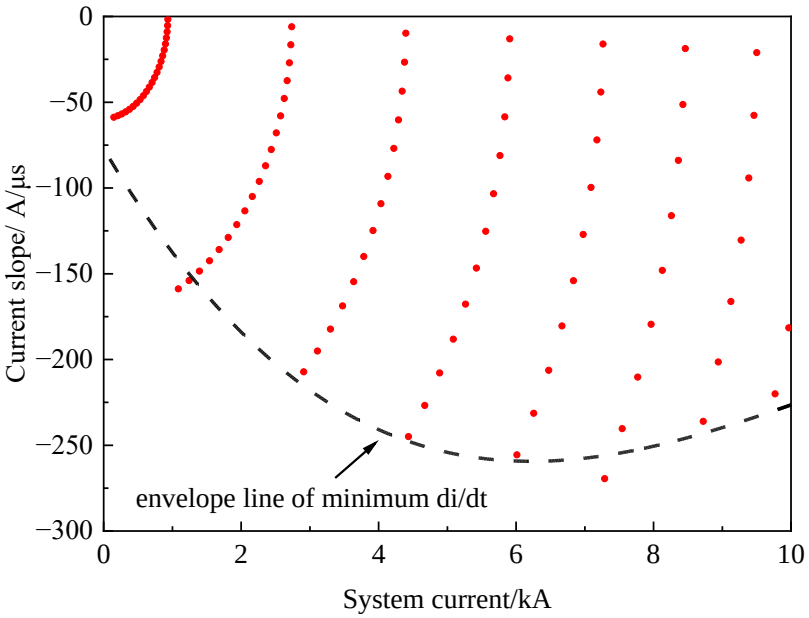

Figure 8. Current slope with regard to different system currents.

The red dots illustrate the current slopes at zero-crossing under varying fault current conditions, demonstrating periodicity. These dotscan be divided into 8 groups. The *N*th group presents the results of interruption in *N*th half-cycles of the injected counter-current. The slope decreases to zero as the system current increases in each current range. The

minimum current slope of each current range decreases initially, followed by an increase. The minimum slope of all current ranges is −269 A/μs when the system current is 7 kA.

The ITIV across the vacuum interrupter is applied by the change in the voltage of oscillation inductor L_p at CZC. And the change in the voltage of the oscillation inductor can be expressed by Equation (14):

$$\Delta U_{L_p} = -L_p \frac{di_{osc}}{dt} = L_p \frac{di_{VI}}{dt} \tag{14}$$

Since the derivation of oscillating current is much larger than that of system current, the second equation holds, which links the current slope and ITIV at zero-crossing. Thus, the ITIV is a linear function of the current slope.

The influence of the current value on the ITIV is given in Figure 9, which presents similar trends as that in Figure 8. The bule dots illustrate the ITIV at zero-crossing under varying fault current conditions, demonstrating periodicity.The minimum ITIV of all current ranges is −5.3 kV when the system current is 7 kA.

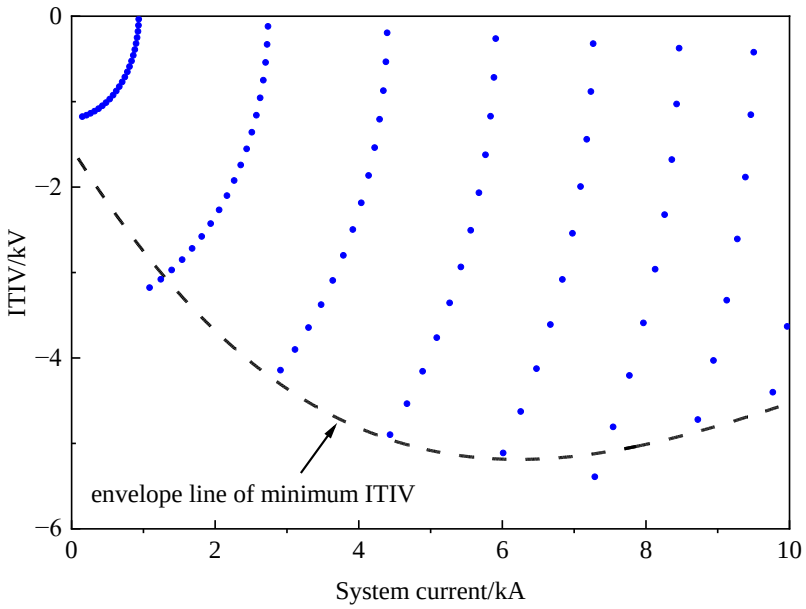

Figure 9. ITIV with regard to different system currents.

A typical mechanical DCCB based on LC oscillation is modeled to make a comparison with the proposed DCCB. Their main parameters are given in Table 2.

Table 2. Main parameters of the DC circuit breakers with the novel and typical topologies.

Parameter	Description	Novel Topology	Typical Topology
L_{dc}	Inductance of current-limiting reactor	0.5 mH	0.5 mH
C_{dc}	Capacitance of pre-charged capacitor	5 mF	-
U_{dc}	Charging voltage of pre-charged capacitor	1200 V	-
C_p	Capacitance of oscillation capacitor	13 μF	20 μF
U_p	Charging voltage of oscillation capacitor	-	10 kV
L_p	Inductance of oscillation inductor	20 μH	13 μH
R_p	Resistance of parasitic resistor in commutation branch	0.01 Ω	0.01 Ω
U_{SA}	Protection voltage of surge arrester	15 kV	15 kV
f_{LC}	Frequency of oscillation	9.87 kHz	9.87 kHz

The oscillation capacitor in the typical topology is charged by the system. Thus, the charging voltage of the oscillation capacitor is the system voltage. The parameters in detail

given in Table 2 allow both two topologies to clear a maximal fault current of 12 kA in a 10 kV system.

The comparisons of the current slope and ITIV between the novel topology and the typical topology are shown in Figures 10 and 11, respectively. The typical mechanical DCCB has a good performance at fault current interruption with a small current slope and ITIV. However, the current slope and ITIV decrease rapidly with a smaller current, which causes severe electrical stress on the vacuum interrupter. As an example, for 1 kA small current interruptions, it has a large current slope of −750 A/μs and a high ITIV of −9.7 kV. In such a case with a large slope and high ITIV, a probable arc reignition may happen in the vacuum interrupter, resulting in a failed interruption.

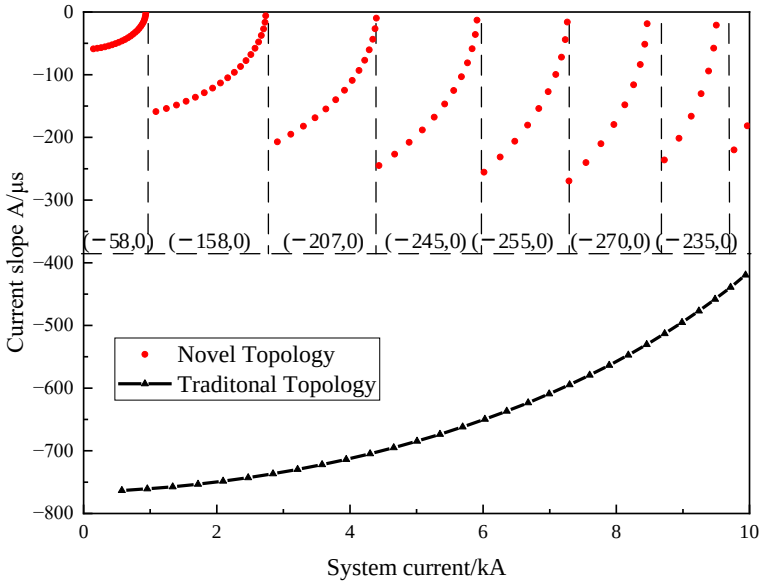

Figure 10. Comparison of di/dt between the two topologies.

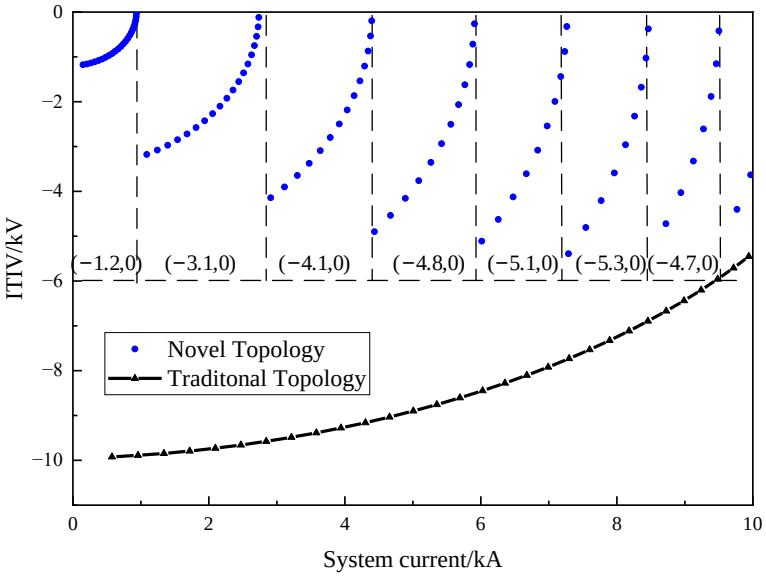

Figure 11. Comparison of ITIV between the two topologies.

Compared to the typical topology, the proposed topology can decrease the current slope at zero-crossing by 79.3% for 1 kA current interruption and 84.9% for rated current interruptions. In the case of fault current interruptions, the proposed topology can also

decrease the current slope by 57%. And the ITIV for the full current range is lower than that of the typical one, which is helpful for the recovery of dielectric strength.

In a DC system, the range of current can be very large. With this proposed topology, the DCCB has the capacity to limit the slope at zero-crossings under −269 A/μs and ITIV under −5.3 kV for currents from 0–10 kA in a 10 kV system. Compared to the typical mechanical DCCB, this novel topology is more reliable for full-range current interruption.

Above all, the proposed topology has several advantages, such as conducting current with low on-state loss in normal situations, interrupting full-range current with low-current slope and low ITIV at zero-crossing. The last two characteristics help the dielectric strength recovery process, resulting in more reliable operation than the typical topology of mechanical DCCBs. The proposed topology overcomes the drawbacks of the typical topology of mechanical DCCSs. It is promising for application in MTDC systems with a large range of current.

4. Simulation in MTDC Network

Nowadays, most VSC-HVDC projects in operation are in the form of point-to-point connections. The multi-terminal network presents some technical challenges to be addressed. One of the main challenges is the lack of reliable HVDC CBs. The MTDC technology requires CBs with high current interruption capacity and shorter interruption time. To verify the performance of this novel topology, a series of simulations of interruptions in the MTDC network is carried out in this section.

A meshed bipolar 4-terminal MTDC network is established in PSCAD. The structure of the MTDC network is presented in Figure 12. Two offshore wind farms are connected to the onshore AC grid by terminal 3 and terminal 4. The system parameters of the MTDC network are shown in Table 3. Two pairs of CBs installed at the DC at the ends of cable-linked terminal 1 and terminal 4 are triggered to clear the fault current. The main parameters of the CBs are shown in Table 4.

The rated current of this 4-terminal MTDC network is 0.4 kA. The current direction at the positive pole is from terminal 4 to terminal 1. And the current direction at the negative pole is inverse.

A pole-to-pole short circuit fault occurs at the middle point of the DC cable. The fault occurs at 50 ms. Due to the discharging of capacitors in the sub-module of MMC terminals, the fault current rises rapidly. After about ten milliseconds, the DCCBs are triggered and interrupt the fault current. The fault current at the four poles has very different values and changing trends, which presents a challenge to the proposed topology.

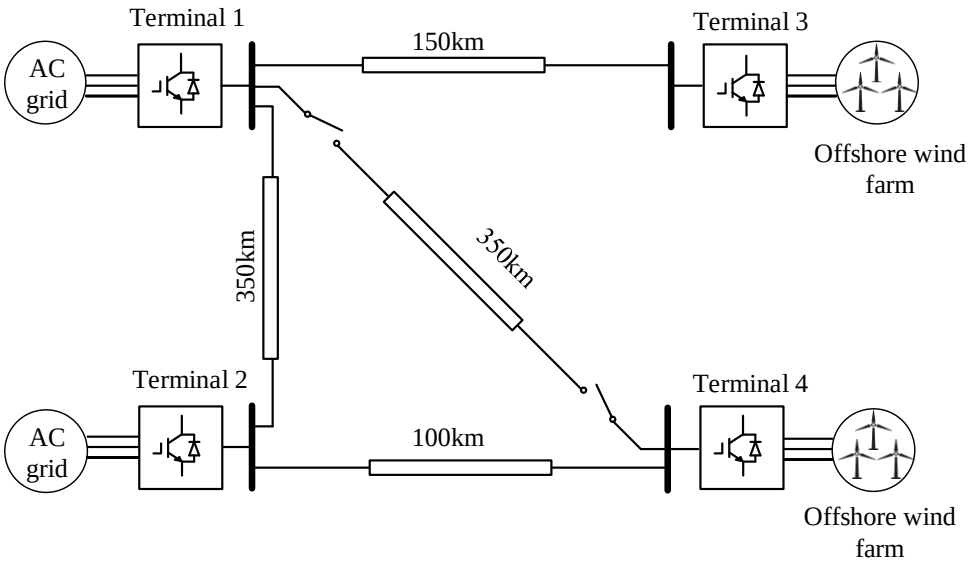

Figure 12. A 4-terminal MTDC network connected to offshore wind farm.

Table 3. MTDC network parameters.

Parameter	Value			
Terminal	1	2	3	4
Control mode	PVdc	PVdc	PQ	PQ
Rated converter power	1200 MW	1200 MW	1000 MW	1000 MW
DC voltage	±320 kV			
AC voltage	400 kV	155 kV	400 kV	155 kV
AC frequency	50 Hz			
Sub-module capacitor	8.8 mF			
Converter arm reactor	42 mH			
Number of sub-module	175			
Converter arm resistor	80 mΩ			
Fault resistance	0.1 Ω			

Table 4. Main parameters of the MTDC simulation model.

Parameter	Value
L_{dc}	140 mH
C_{dc}	667 μF
U_{dc}	12 kV
C_p	2 μF
L_p	127 μH
R_p	0.1 Ω
U_{SA}	770 kV

As shown in Figure 13, the fault current at the positive pole of terminal 1 decreases to −0.26 kA when it is interrupted. Since the fault current is small, it is interrupted at the first half-cycle of I_{oscdc}. The current of the surge arrester is in the order of just several amperes. The time for energy absorption is negligible. The current slope at zero-crossing is 120.6 A/μs, while the ITIV is 10.7 kV. Limited by the simulation step size, the current slope at zero-crossing and ITIV do not fully conform to the formula derived before. In such a situation of small current interruption, this proposed topology has a smaller current slope at zero-crossing and ITIV than the typical topology, which verifies the conclusion of the previous section.

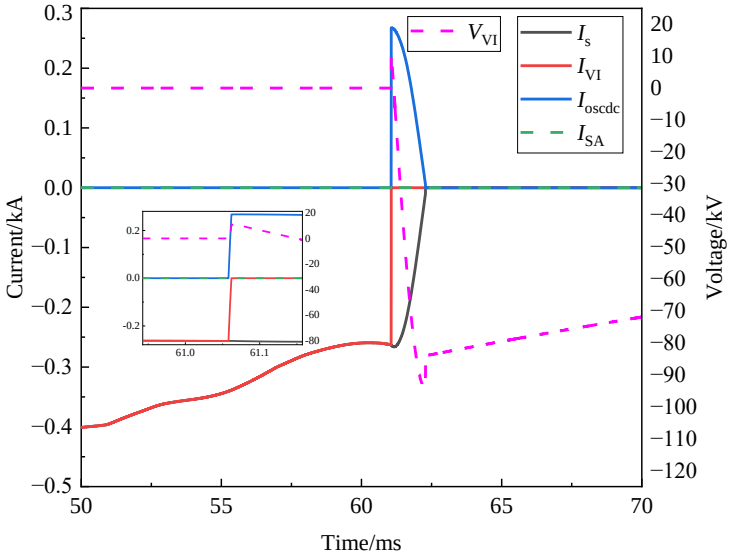

Figure 13. Simulation results of CB at the positive pole of terminal 1.

The results at the negative pole of terminal 1 are given in Figure 14, which is very different from the previous situation. The fault current at the negative pole of terminal 1 changes its direction and drops to −7 kA. The value of the fault current remains within the interrupting range of the CB. It takes 4 half-cycles to interrupt the fault current. And the energy absorption lasts 3 ms. The slope at zero-crossing is 255.3 A/μs, while the ITIV is 47.3 kV.

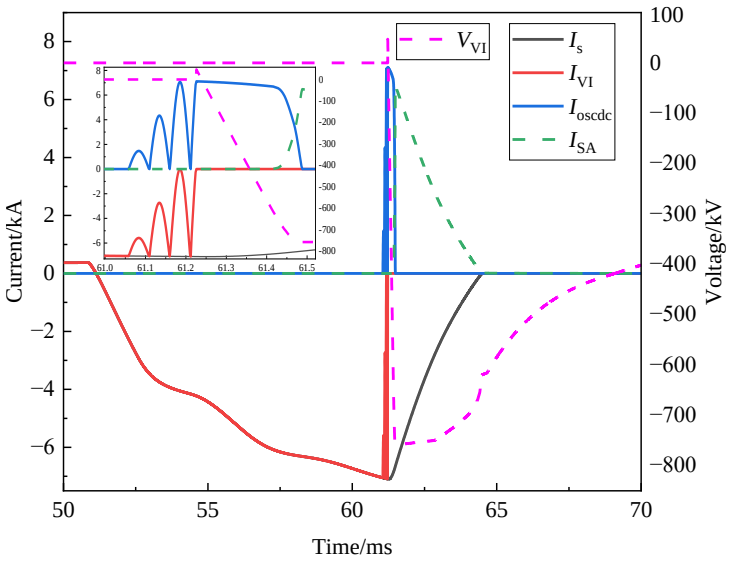

Figure 14. Simulation results of CB at the negative pole of terminal 1.

As shown in Figure 15, the fault current at the positive pole of terminal 4 rises from 0.4 kA to 1 kA. It is interrupted at the first half-cycle of I_{oscdc}. The slope at zero-crossing is −8.9 A/μs, while the ITIV is −7.5 kV. The current of a surge arrester is in the order of just several amperes.

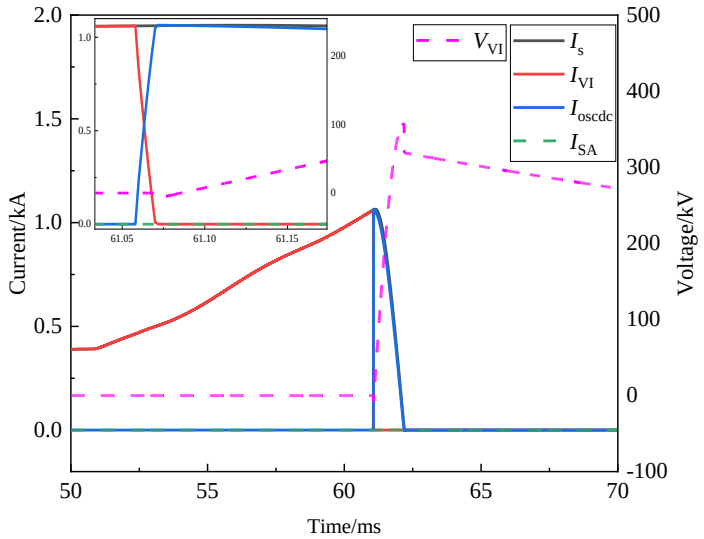

Figure 15. Simulation results of CB at the positive pole of terminal 4.

The simulation results of CB at the negative pole of terminal 4 are given in Figure 16. The fault current at the negative pole of terminal 4 drops from 0.4 kA to −7 kA. It takes 3 half-cycles to interrupt the fault current. The slope at zero-crossing is 10.3 A/μs, while the ITIV is 9.2 kV. The slope at zero-crossing is small because the fault current is interrupted when the counter-current reaches its third peak value. The energy absorption lasts about 3 ms.

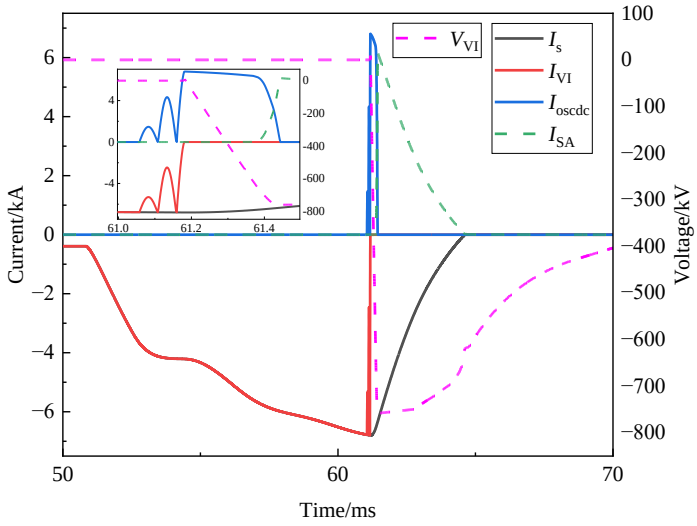

Figure 16. Simulation results of CB at the negative pole of terminal 4.

In such a pole-to-pole short circuit fault, the 4 CBs show their capacity to interrupt bidirectional currents with different values. The novel CB has a good performance in clearing the whole range of bidirectional currents successfully.

5. Discussion

5.1. Cost and Performance Comparison

In order to provide a clearer overview of the topology proposed in this article, a cost and performance comparison is conducted among typical mechanical DC circuit breakers in [18], typical hybrid DC circuit breakers in [11], voltage-assisted resonant current (VARC) DC circuit breaker in [30], and the proposed topology with a rated voltage 320 kV and current 16 kA. The comparative analysis is shown in Table 5, where 1 p.u. represents CNY 10,000. Since the cost of the mechanical switch in the main branch and the surge arrester in the energy absorption branch are determined by the interruption capacity, the cost comparison primarily focuses on the commutation branch, which includes the oscillation circuit, power electronic device, and necessary auxiliary components.

The cost of the capacitor is proportional to its maximum energy capacity, with a linear coefficient of 1.5 RMB/J. The cost of the inductor can be neglected in comparison to that of the capacitor. The same power electronic devices are selected to ensure a fair comparison during the cost comparison. The IEGT ST3000GXH31A and diode 3000GXHH32 are chosen, both of which have a rating of 4.5 kV/3 kA. The cost of power electronic devices is determined by marketing investigation. The combination of an IEGT and a diode cost 4 p.u.

As shown in Table 5, the cost of the proposed topology is only 36% of typical MCB. The cost of the oscillation capacitor with the same voltage level increases linearly with its capacitance. The proposed topology significantly reduces the cost of oscillation capacitors by utilizing a much smaller capacitor. The cost of the proposed topology is only 10% of that of a typical HCB. While the typical HCB requires hundreds of IEGTs in series to actively interrupt the fault current, the proposed topology employs only four IEGTs. The reduced cost for IEGTs more than compensates for the increased cost of the oscillation circuit. Furthermore, the typical HCB necessitates a load-commutation switch, cooling facility, and RCD snubber, which significantly increases the cost. In comparison to a VARC MCB, the proposed topology can decrease the cost by 13%. The proposed topology optimizes the structure and parameters of the oscillation circuit, making use of every half wave of oscillation to inject a counter-current. It employs a pre-charged capacitor with lower voltage and an oscillation capacitor with larger capacitance, resulting in a total cost of capacitors lower than that of a VARC MCB.

Table 5. Comparative analysis of the main DCCB topologies.

Parameter	Typical MCB [18]	Typical HCB [11]	VARC MCB [30]	Proposed Topology
Interruption capacity	320 kV/16 kA	320 kV/16 kA	320 kV/16 kA	320 kV/16 kA
Oscillation capacitor	10 μF(480 kV)	0	660 nF (480 kV)/ 1 mF (24 kV)	2 μF (480 kV)/ 667μF(12 kV)
Oscillation inductor	500 μH	0	380 μH	127 μH
Power electronic device	-	4.5 kV/3 kA IEGT Diode	4.5 kV/3 kA IEGT Diode	4.5 kV/3 kA IEGT Diode Thyristor
Total cost of commutation branch	173 p.u.	640 p.u.	71 p.u.	62 p.u.
Zero-crossing method	Oscillation current injection	Force interruption by PE	Oscillation current injection	Counter-current injection
Power loss	Very low	high	Very low	Very low
Auxiliaries	Injection switch	Load-commutation switch, cooling facilities, RCD snubber	Pre-charged device	Pre-charged device
Structural complexity	Simple	Complex	Simple	Simple
Control complexity	Simple	Complex	Medium	Medium
Reliability	Low	High	Medium	High

As for performance, all three MCBs are capable of creating current zero by injecting high-frequency current into a vacuum interrupter. However, the proposed topology sets itself apart from the other two MCBs by modulating the oscillation current. It injects a counter-current that consistently opposes the fault current in the vacuum interrupter. The difference results in a lower density of residual plasma density and a smooth current slope at current zero. Thus, the interruption with the proposed topology is more reliable than the other two topologies. Compared to the typical HCB, the proposed topology also has the advantage of low on-state loss. In addition, the proposed topology features fewer power electronic devices, which translates to a simpler structure and control. The power electronic devices in the proposed topology switch softly at current zero, which significantly reduces the requirements for the power electronic device's hard-switching capability.

The results of the comparative analysis suggest that the proposed topology is more cost-effective and features a simple structure and control. The proposed topology stands out by injecting a counter-current consistently opposing the fault current, enhancing interruption reliability.

5.2. Limitation of the Research

In this subsection, the limitation of this research is discussed.

In the analysis of the commutation process, simplifications are made by omitting the parasitic resistor. The parasitic resistor dissipates the electrical energy stored in C_{dc} as thermal energy during the oscillation process. In the section of simulation, the parasitic resistor is considered and demonstrates its impact on the counter-current in Figure 7. It slows down the acceleration of the counter-current and limits the maximum current generated by the oscillation circuit. However, the specific influences of the parasitic resistor on the oscillation process have not been thoroughly investigated in this article. This phenomenon could hinder the broader adoption of this proposed topology in practical applications.

In the section on simulation, three critical prerequisites are proposed for a successful interruption, which include the current zero. The current slope at current zero and the dielectric recovery strength. The dielectric recovery strength of the vacuum interrupter at current zero is assessed based on its cold withstand voltage, which depends on the contact

distance. The actual dielectric strength during interruption is observed to be inferior to the cold withstand voltage with the presence of plasma and metal droplets between the contacts. Thus, these three conditions are necessary but insufficient conditions for a successful interruption.

To validate the proposed topology, a prototype of DCCB based on this proposed topology is under construction. The aforementioned limitations will be addressed and refined. The control strategy of the DCCB and the reliability of the proposed topology will be subject to validation in subsequent experimental research.

6. Conclusions and Prospects

This article presented a novel topology of mechanical DCCB, which utilized a full-controlled converter and a semi-controlled full bridge to generate a counter-current with gradually increasing amplitude. The current slope and ITIV at zero-crossing are computed and analyzed. Compared with the typical mechanical DCCB, the proposed topology overcomes the problem of all-range current interruption reliability caused by a high current slope and high ITIV at CZC. The comparative analysis of cost and performance with other representative DCCBs indicates the benefits of the proposed topology. The following conclusions can be reached from the above results:

The gradually increasing counter-current superimposed on the all-range fault current produces a smooth slope at CZC and lower ITIV. This promotes the current interruption reliability of the vacuum interrupter during DC interruption.

According to the calculation and comparison with typical DCCB topology, the current slope at zero-crossing decreases by 57–84% during full-range fault current interruption, and the ITIV can be reduced to the same extent.

The performance of the proposed DCCB topology is demonstrated in a $\pm$320 kV four-terminal bipolar HVDC grid. Simulation results show that a DCCB with a gradually increasing counter-current can interrupt the fault current at the positive pole and negative pole of both ends of a transmission line.

The proposed topology is more cost-effective and features a simple structure and control. It can reduce the costs of commutation branches by 64%, employing a few power electronic devices and a suitable oscillation circuit. Further research should consider the impact of parasitic parameters more carefully, for example, the parasitic resistor and inductor that influence the commutation. A prototype of DCCB based on this proposed topology is under construction. The control strategy of the DCCB and the reliability of the proposed topology will be subject to validation in subsequent experimental research. These efforts aim to validate and improve the proposed topology, laying a solid foundation for its widespread adoption in practical applications.

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