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Optimal Design of a Submodule Capacitor in a Modular Multilevel Converter for Medium Voltage Motor Drives

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Abstract: This paper proposes an algorithm for determining the optimal capacitance by utilizing a mathematical model of a submodule (SM) capacitor in a modular multilevel converter (MMC) specifically for medium voltage motor drives (MVDs). By approximating the voltage fluctuation of the SM capacitor during low-frequency operation, it is feasible to ascertain the minimum capacitance required for the SM capacitor, ensuring that its voltage fluctuations remain within an acceptable limit that is predefined as a specified value. Moreover, the study considered the injection of both a high-frequency common-mode voltage (CMV) and a circulating current to alleviate the SM voltage fluctuation during the acceleration of motor drives. The effectiveness of the proposed method is validated through verification using time-domain simulation results obtained using the MATLAB/SIMULINK software and real-time simulation results acquired using the OPAL-RT simulator platform.

Keywords: modular multilevel converter (MMC); optimal sizing of submodule (SM) capacitor; SM capacitor voltage ripple limit; high frequency injection (HFI); variable speed motor drives (VMD)

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1. Introduction

Modular multilevel converters (MMCs) have become an attractive multilevel converter topology for medium-to-high-voltage and high-power applications owing to their advantages regarding modular design, low harmonic distortion of the output voltage, and low switching frequency [1–5]. Consequently, MMCs have been extensively used in various industrial applications, including high-voltage direct current (HVDC) transmission systems [6–10], static synchronous compensators (STATCOM) [11–14], and medium voltage motor drives (MVDs) [15–24]. In addition to the salient features, submodule (SM) capacitors exhibit substantial voltage fluctuations at low frequencies, necessitating the selection of a sufficiently large capacitance to minimize this variability. However, this causes the converter system to be oversized and expensive, thereby restricting the applicability of the MMC system. In theory, the voltage ripple in an SM capacitor is directly proportional to the amplitude of the output current and inversely proportional to the operating frequency. This results in a significant voltage ripple in the SM when the motor drives operate at low speeds, particularly during startup [25]. Owing to these considerations, numerous studies have been conducted to improve the dynamic performance of converter systems when motor drives operate at low speeds [17,18,25–30].

Injecting high-frequency sinusoidal waveforms of the common-mode voltage (CMV) and a circulating current into each arm results in a significant reduction in the voltage fluctuation of the SM capacitor [18,25,26]. Through this control strategy, the transfer of high-frequency components between the upper and lower arms enables more frequent charging and discharging of the SM capacitor, effectively suppressing voltage fluctuations without affecting the three-phase output currents (Figure 1). However, the injection of

high-frequency components gives rise to a CMV on the motor side, leading to the potential harming of the motor winding and the deterioration of the motor bearings [17]. Furthermore, the incorporation of sinusoidal waveforms induces elevated current stress in each arm, leading to increased power loss. To alleviate the current stress in each arm, a high-frequency square-wave CMV and circulating current are injected into each arm as an alternative to sinusoidal high-frequency components [27]. Nevertheless, the use of a square-waveform CMV may lead to significant dv/dt issues at the motor terminal, posing a threat to the lifespan of motor bearings and rendering them unsuitable for practical applications. Similarly, the proposed method involves the introduction of a flying-capacitor MMC (FC-MMC) to alleviate arm current stress and SM capacitor voltage fluctuations without introducing a CMV to the motor winding [28–30].

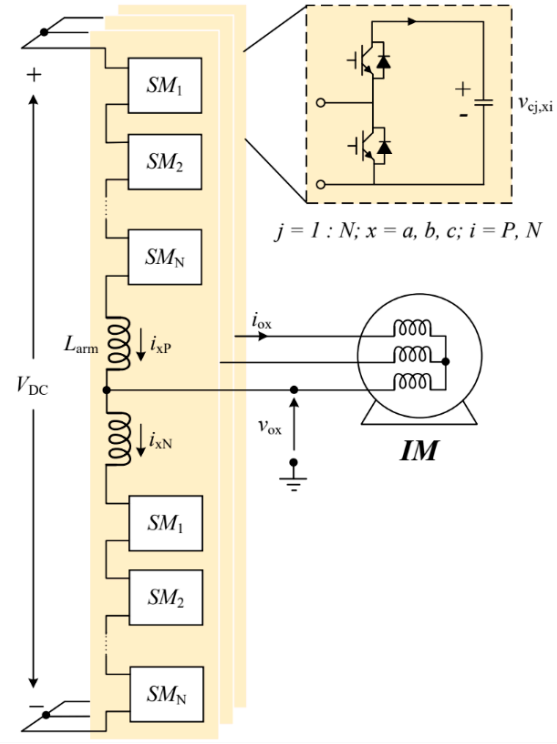

Figure 1. Circuit configuration of a three-phase MMC.

Although employing a substantial capacitance can minimize SM voltage fluctuations, it results in the MMC system being oversized and expensive. Consequently, determining the appropriate size of the SM capacitor is crucial, as it establishes the minimum capacitance required to attain the optimal performance in the MMC-based motor drive system. The examination and evaluation of the SM capacitance in high-voltage direct current (HVDC) transmission systems using the MMC topology are presented in [31–33]. Merlin et al. introduced a mathematical model to predict the minimum required size of SM capacitors to maintain the voltage ripple within permissible limits [34]. In [35–37], SM capacitance was determined by assessing the arm energy fluctuation. However, these approaches only size the SM capacitance by considering the fundamental frequency components of an MMC system.

This paper proposes a mathematical model for sizing SM capacitors by estimating the SM voltage to ensure that the SM voltage fluctuates within an allowable limit during low-frequency operation for motor drive applications. The main technical contributions of this study are as follows.

- The approach of utilizing a high-frequency CMV and circulating current injection to minimize SM capacitor voltage fluctuations during low-speed or standstill operations of the motor drive is mathematically explained in detail.

- An algorithm is formulated to estimate the SM capacitor voltage ripple, which is employed to optimize the SM capacitance in accordance with the system specifications for the allowable SM capacitor voltage ripple limit (Δv_{lim}).

The remainder of the paper is structured as follows: Section 2 outlines the MMC circuit and its operation and provides a suppression of the SM voltage ripple during low-frequency operation. In Section 3, we introduce the proposed optimal algorithm for designing SM capacitors based on estimating the SM voltage fluctuations under variable frequency operations. Sections 4 and 5 demonstrate the efficacy of the proposed method through time-domain simulations using MATLAB/SIMULINK R2021a software and real-time simulations using the Opal-RT platform. Finally, Section 6 summarizes the key contributions and conclusions of this study.

2. Circuit and Operation of Modular Multilevel Converter

2.1. Circuit Operation

A schematic representation of a three-phase MMC connected to an induction motor (IM) is shown in Figure 1. The MMC comprises three phases, with each phase composed of two arms. The arm linked to the positive bar is termed the upper arm, whereas the arm connected to the negative bar is referred to as the lower arm. Each arm consists of N_{sm}-identical SMs connected in series with a buffer inductor (L_{arm}) designed to control the circulating currents within the converter arising from voltage disparities between the arms. The SM circuit can take the form of a half-bridge (HB), full-bridge (FB), or flying-capacitor power circuit. In this investigation, the HB circuit was employed for its simplicity, featuring two power semiconductor devices, denoted as IGBT T_1 and T_2, along with an isolated capacitor (C_{dc}) and freewheeling diodes.

The configuration and function of the HB-SM are shown in Figure 2. The SM capacitor (C_{dc}) is regulated to be charged, discharged, or bypassed based on the direction of the arm current and switching state of the IGBT devices. During the ON state of S_1, the SM capacitor voltage (v_{sm}) increases in the positive direction of the arm current ($i_{arm} > 0$), indicating the charged mode, and decreases in the negative direction of the arm current ($i_{arm} < 0$), signifying the discharged mode, as illustrated in Figure 2a,b, respectively. In the OFF state of S_1, the SM capacitor voltage remains constant, representing the bypassed mode, irrespective of the arm current direction, as illustrated in Figure 2c,d.

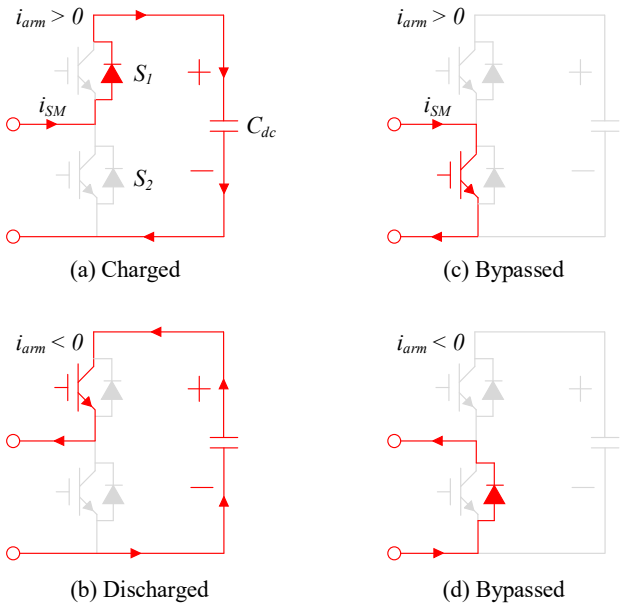

Figure 2. The switching state of an HB-SM: (**a**) charged, (**b**) discharged, (**c**,**d**) bypassed.

2.2. Voltage Ripple Reduction under Low-Frequency Operation

Assuming that the output voltage (v_x) and current (i_x) exhibit symmetrical sinusoidal waveforms, they can be represented as per Equation (1):

$$\begin{cases} v_x = V_x \cos(\omega t + \delta_x) \\ i_x = I_x \cos(\omega t + \delta_x - \phi_x) \end{cases} \quad (1)$$

where v_x and i_x correspond to the output voltage and output current of phase x, respectively (x = a, b, and c represent phases a, b, and c); V_x and I_x denote the amplitudes of the output voltage and current; while δ_x represents the initial phase angle of phase x (with a = 0, b = $-2\pi/3$, and c = $2\pi/3$); and ϕ_x signifies the phase shift between voltage and current.

In accordance with Kirchhoff's voltage law (KVL), the voltages across the upper and lower arms (v_{xP} and v_{xN}) can be formulated as expressed in Equation (2). By substituting the three-phase output voltage from Equation (1) into the upper and lower arm voltage expressions in Equation (2), the arm voltages can be represented as expressed in Equation (3).

$$\begin{cases} v_{xP} = \frac{1}{2} V_{DC} - v_x \\ v_{xN} = \frac{1}{2} V_{DC} + v_x \end{cases} \quad (2)$$

$$\begin{cases} v_{xP} = \frac{1}{2} V_{DC} - V_x \cos(\omega t + \delta_x) \\ v_{xN} = \frac{1}{2} V_{DC} + V_x \cos(\omega t + \delta_x) \end{cases} \quad (3)$$

where v_{xP} and v_{xN} represent the upper and lower arm voltages of phase x, and V_{DC} denotes the DC-link voltage.

The upper arm current and lower arm current (i_{xP} and i_{xN}) of phase x can be expressed as shown in (4).

$$\begin{cases} i_{xP} = \frac{1}{2} i_x + i_{circ,x} \\ i_{xN} = -\frac{1}{2} i_x + i_{circ,x} \end{cases} \quad (4)$$

where i_{xP} and i_{xN} are the upper and lower arm currents of phase x, and $i_{circ,x}$ is the circulating current of phase x.

As previously noted, the SM voltage ripple experiences significant fluctuations during the startup operation of motor drives, owing to its inverse proportionality to the frequency of operation. To mitigate this voltage fluctuation in the SM, a high-frequency CMV denoted as v_h, along with the circulating current (i_h), is introduced into each arm. This injection enhances the exchange of high-frequency components between the arms of the converter. The introduced high-frequency voltage and current are expressed as indicated in Equations (5) and (6).

$$v_h = V_h \cos(\omega_h t) = \frac{M_{\max} V_{dc}}{2} \cos(\omega_h t) \quad (5)$$

$$i_h = I_h \cos(\omega_h t) \quad (6)$$

where v_h and i_h represent the high-frequency voltage and current injected into each arm, respectively; V_h and I_h denote the amplitudes of the injected high-frequency voltage and current, respectively; ω_h represents the frequency of v_h; and i_h, M_{max} is a coefficient representing the modulation margin (M_{max} = 0.85–0.95).

The upper and lower arm voltages (v_{xP} and v_{xN}), which account for the introduced high-frequency voltage (v_h), can be obtained as expressed in Equation (7).

$$\begin{cases} v_{xP} = \frac{1}{2} V_{DC} - v_x - v_h \\ v_{xN} = \frac{1}{2} V_{DC} + v_x + v_h \end{cases} \quad (7)$$

Moreover, the upper and lower arm currents (i_{xP} and i_{xN}), factoring in the injected high-frequency circulating current (i_h), are represented in Equation (8). It is important to

highlight that the frequency (f_h) must be chosen to be less than one-tenth of the switching frequency of the converter ($f_h \leq f_{sw}/10$) to ensure effective controllability.

$$\begin{cases} i_{xP} = \frac{1}{2}i_x + i_{cirx,dc} + i_h \\ i_{xN} = -\frac{1}{2}i_x + i_{cirx,dc} + i_h \end{cases} \tag{8}$$

The instantaneous powers of the upper and lower arms (P_{xP}, P_{xN}) can be determined, as outlined in Equation (9), and derived from Equation (10) by multiplying the arm voltage and current from Equations (7) and (8), respectively.

$$\begin{cases} P_{xP} = \left(\frac{1}{2}V_{DC} - v_x - v_h\right)\left(\frac{1}{2}i_x + i_{cirx,dc} + i_h\right) \\ P_{xN} = \left(\frac{1}{2}V_{DC} + v_x + v_h\right)\left(-\frac{1}{2}i_x + i_{cirx,dc} + i_h\right) \end{cases} \tag{9}$$

where P_{xP} and P_{xN} represent the instantaneous power of the upper and lower arm in phase x, respectively.

$$\begin{cases} P_{xP} & = \frac{1}{4}V_{DC}i_x + \frac{1}{2}V_{DC}i_{cirx,dc} + \frac{1}{2}V_{DC}i_h - \frac{1}{2}v_x i_x \\ & \quad -v_x i_{cirx,dc} - v_x i_h - \frac{1}{2}v_h i_x - v_h i_{cirx,dc} - v_h i_h \\ P_{xN} & = -\frac{1}{4}V_{DC}i_x + \frac{1}{2}V_{DC}i_{cirx,dc} + \frac{1}{2}V_{DC}i_h - \frac{1}{2}v_x i_x \\ & \quad +v_x i_{cirx,dc} + v_x i_h - \frac{1}{2}v_h i_x + v_h i_{cirx,dc} + v_h i_h \end{cases} \tag{10}$$

The powers in the upper and lower arms consist of fundamental, second, and high-frequency components injected into each arm to mitigate the SM voltage ripple, as expressed in Equation (10). The high-frequency components have a minimal impact on the voltage ripple, which is primarily influenced by the fundamental and second harmonics [38]. Consequently, the high-frequency components were disregarded, and only the fundamental and second-order harmonic components were considered, as indicated in Equation (11).

$$\begin{cases} P_{xP} = \frac{1}{2}V_{DC}i_{cirx,dc} - \frac{1}{2}v_x i_x + \frac{1}{4}V_{DC}i_x - v_x i_{cirx,dc} - \frac{1}{2}V_h I_h \\ P_{xN} = \frac{1}{2}V_{DC}i_{cirx,dc} - \frac{1}{2}v_x i_x - \frac{1}{4}V_{DC}i_x + v_x i_{cirx,dc} + \frac{1}{2}V_h I_h \end{cases} \tag{11}$$

At a steady state, the first and second terms in Equation (11) are equal because of the power balance between the DC and AC sides. The remaining terms consist of both fundamental and high-frequency components, representing the power exchange within the converter induced by the AC and DC components of the circulating currents, respectively, leading to fluctuations in the SM capacitor voltage. Based on these terms, the DC circulating current $i_{circx,dc}$ can be calculated as expressed in Equation (12).

$$i_{cirx,dc} = \frac{v_x i_x}{V_{DC}} \tag{12}$$

As expressed in Equation (11), the powers in the upper and lower arms are similar, with certain terms having opposite signs, and there is no difference between the upper and lower arms in the SM voltage fluctuation control. For simplicity, only the upper arm power was examined to mitigate the SM voltage fluctuation.

$$P_{xP,rpl} = \frac{1}{4}V_{DC}i_x - v_x i_{cirx,dc} - \frac{1}{2}V_h I_h \tag{13}$$

where $P_{xP,rpl}$ represents the power ripple of phase x in the upper arm.

To mitigate the SM voltage fluctuation, the ripple in the upper arm power is regulated to zero ($P_{xP,rpl} = 0$). By substituting the circulating current from Equation (12) into the arm power ripple in Equation (13), the magnitude of the high-frequency components can be

determined, as expressed in Equation (14). The magnitude of the high-frequency current injected into each arm can be calculated as expressed in Equation (15).

$$\frac{1}{2}V_h I_h = \frac{1}{4}V_{DC} i_x - \frac{v_x^2 i_x}{V_{DC}} \tag{14}$$

$$I_h = \frac{1}{V_h}\left(\frac{1}{2}V_{DC} - \frac{2v_x^2}{V_{DC}}\right) i_x \tag{15}$$

By substituting the magnitude of the injected high-frequency current from Equation (15) into Equation (6), the injected high-frequency current can be represented as indicated in Equation (16).

$$i_h = \frac{1}{V_h}\left(\frac{1}{2}V_{DC} - \frac{2v_x^2}{V_{DC}}\right) i_x \cos(\omega_h t) \tag{16}$$

Consequently, the voltage fluctuation in the SM capacitor is alleviated during low-frequency operations through the injection of a high-frequency current into each arm of the MMC system.

3. Design SM Capacitor in Low-Speed Range of Medium Voltage Motor Drives

In this section, an optimal design algorithm for the SM capacitor is presented, which relies on the estimation of the SM voltage ripple during the low-frequency operation of motor drives. The proposed method ensures that the voltages of the SM capacitors fluctuate within a predefined limit by considering the voltage ripple requirements of the system.

3.1. Estimation of Submodule Voltage Fluctuation

The power ripple in the upper arm can be obtained by substituting Equation (12) into Equation (13), as expressed in Equation (17). Similarly, the power ripple in the lower arm can be represented by Equation (18). Subtracting the power ripple of the lower arm from that of the upper arm yields the power ripple for the corresponding phase, as expressed in Equation (19).

$$P_{xP,rpl} = V_{DC}\left(\frac{1}{4} - \frac{v_x^2}{V_{DC}^2}\right) i_x - \frac{1}{2}V_h I_h \tag{17}$$

$$P_{xN,rpl} = -V_{DC}\left(\frac{1}{4} - \frac{v_x^2}{V_{DC}^2}\right) i_x + \frac{1}{2}V_h I_h \tag{18}$$

$$P_{x,rpl} = \frac{1}{2}V_{DC} i_x - V_h I_h \tag{19}$$

where $P_{xN,rpl}$ represents the power ripples of phase x in the lower arm.

Integrating the power ripple of the phase ($P_{x,rpl}$) from Equation (19), the energy ripple of phase x ($E_{x,rpl}$) considering the injected high-frequency components can be obtained, as indicated in Equation (20).

$$E_{x,p-p} = \int \left(\frac{1}{2}V_{DC} i_x - V_h I_h\right) dt \tag{20}$$

where $E_{x,p-p}$ represents the energy ripple of phase x.

Assuming that the energy distributed among each SM is equal, the relationship between the energy ripple of phase x and the SM capacitor voltage ripple can be established, as expressed in (21).

$$\begin{aligned} E_{x,p-p} &= \tfrac{N_{sm}C_{dc}}{2}\left(v_{c,\max}^2 - v_{c,\min}^2\right) \\ &= N_{sm}C_{dc}v_c\Delta v_{p-p} \end{aligned} \tag{21}$$

where $E_{x,p-p}$ is the energy ripple of phase x in the upper arm, and Δv_{p-p} is the peak–peak voltage ripple of the SM capacitor.

By substituting the energy ripple from Equation (21) into Equation (20), the SM voltage ripple can be derived, as expressed in Equation (22). The process of estimating the SM voltage fluctuation based on the energy fluctuation is illustrated in Figure 3.

$$\Delta v_{p-p} = \frac{1}{C_{dc}} \int \left(\frac{1}{2} i_x - \frac{V_h I_h}{V_{DC}} \right) dt \tag{22}$$

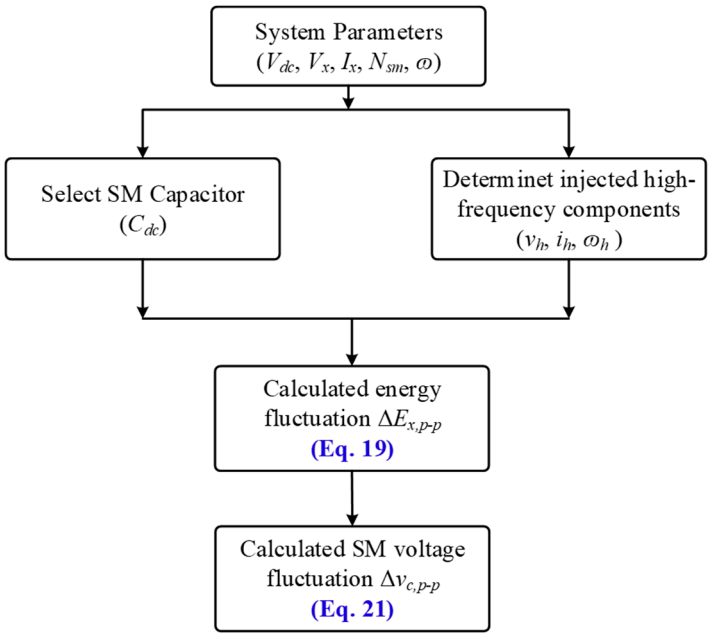

Figure 3. Procedure of estimating SM voltage fluctuation ($\Delta v_{c,p-p}$).

3.2. Optimal Sizing Algorithm of the SM Capacitor

Figure 4 illustrates the optimal design algorithm for SM capacitance, employing a mathematical model to estimate the SM voltage fluctuation during low-frequency operations. In addition, the voltage ripple limit ($\Delta v_{c,lim}$) of the SM capacitor is predefined as a system requirement, which ensures that the SM capacitor voltage fluctuates within an allowable limit.

Initially, the SM capacitance is selected to guarantee that the voltage fluctuation of the SM capacitor remains within the specified limit as per the system requirement ($\Delta v_{p-p} \leq \Delta v_{lim}$). It is important to emphasize that the value of Δv_{lim} may vary based on the specific requirements of the different systems. Consequently, the minimum capacitance must adhere to the given constraint, as expressed by Equation (23).

$$C_{dc} \geq \frac{1}{\Delta v_{\text{lim}}} \int \left(\frac{1}{2} i_x - \frac{V_h I_h}{V_{DC}} \right) dt \tag{23}$$

Based on the system parameters and the high-frequency components injected into each arm during low-frequency operations, the energy ripple and SM voltage fluctuation can be estimated using the outlined procedure of the proposed algorithm, as illustrated in Figure 3. By assessing the SM voltage ripple against the defined voltage ripple limit, the optimal capacitance of the SM capacitor can be identified using the proposed algorithm procedure outlined in Figure 4. Figure 5 depicts the changes in the SM capacitor voltage fluctuation (Δv_{p-p}) under the influence of the injected high-frequency components, considering the variations in capacitance and operational frequency. Furthermore, the system permits SM capacitor voltages to fluctuate within an acceptable range of Δv_{lim} = 10%. For an operational frequency of f_n = 10 Hz, the SM voltage ripple can reach 2.8% with a higher SM capacitance of C_{dc} = 3500 µF. However, the system can be optimized by selecting an SM capacitance of C_{dc} = 1000 µF while still meeting the system requirement of Δv_{lim}.

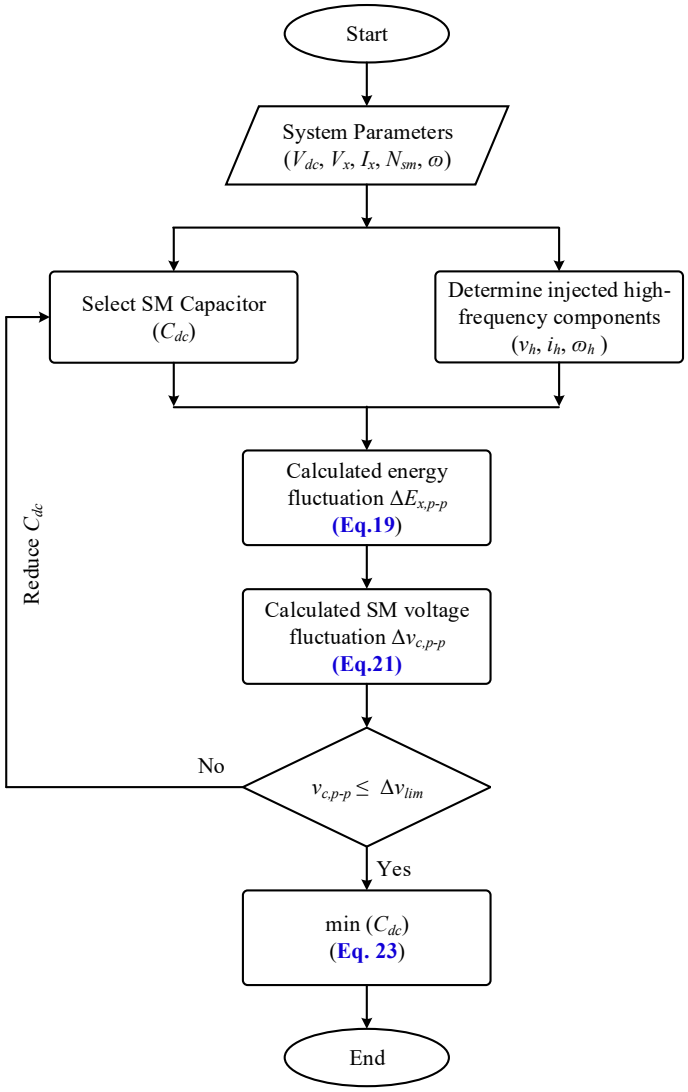

Figure 4. Sizing SM capacitor algorithm.

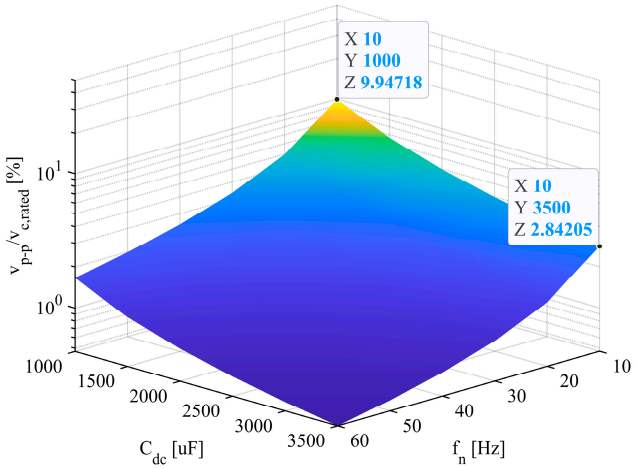

Figure 5. Variation in SM capacitor voltage ripple (Δv_{p-p}) as influenced by varying capacitance (C_{dc}) and operational frequency (f_n).

If the SM voltage ripple exceeds the voltage limit ($\Delta v_{c,p-p} > \Delta v_{lim}$), the SM capacitance must be increased to mitigate the voltage ripple value. If the SM voltage ripple is lower than the voltage limit ($\Delta v_{c,p-p} < \Delta v_{lim}$), the SM capacitance must be reduced to optimize the capacitance value. This process is iterated until the voltage ripple approaches the voltage ripple limit ($\Delta v_{c,p-p} \approx \Delta v_{lim}$), leading to the determination of the optimal SM capacitance. In this investigation, a voltage ripple limit of Δv_{lim} = 10% was selected, corresponding to a rated SM voltage of $v_{c,rated}$ = 1600 V, which is established as an acceptable limit for the SM capacitor voltage. Consequently, the SM capacitance was selected as C_{dc} = 1000 µF to ensure that the SM voltage fluctuation was $\Delta v_{lim} \leq 10\%$.

3.3. SM Voltage Balancing Control

Figure 6 depicts the SM capacitor voltage balancing control employing the high-frequency injection method. This method encompasses phase average voltage control, individual SM voltage control, and SM voltage reference generation [27]. The average phase voltage ($\overline{V}_{cx}$), expressed in Equation (24), is regulated to track the reference value of the average voltage (V_c^*) using a proportional–integral (PI) controller, as illustrated in Figure 6a. The output from the phase voltage controller ($i^*_{cirx,dc}$) serves as the reference for the circulating current controller. Additionally, the circulating current ($i_{cir,x}$) was controlled to adhere to the circulating current reference while incorporating a high-frequency component (i_h).

$$\overline{V}_{cx} = \frac{1}{2N_{sm}} \sum_{j=1}^{N_{sm}} \left(V_{cj,xu} + V_{cj,xl} \right) \tag{24}$$

where $\overline{V}_{cx}$ is the capacitor voltage average of phase x; $V_{cj,xu}$ and $V_{cj,xl}$ are the jth SM voltages of the upper and lower arms, respectively; and N_{sm} is the number of SM per arm.

The control of the individual SM voltages is presented in Figure 6b, where each SM voltage is regulated to track the voltage reference (V_c^*). Furthermore, the direction of the arm currents (i_{xP} and i_{xN}) determines the polarity of the controller output, which can be employed for SM voltage reference generation. A block diagram illustrating the SM voltage reference generation in the upper and lower arms with a high-frequency common-mode voltage (CMV) injected into each arm is shown in Figure 6c and expressed mathematically in Equations (25) and (26), respectively.

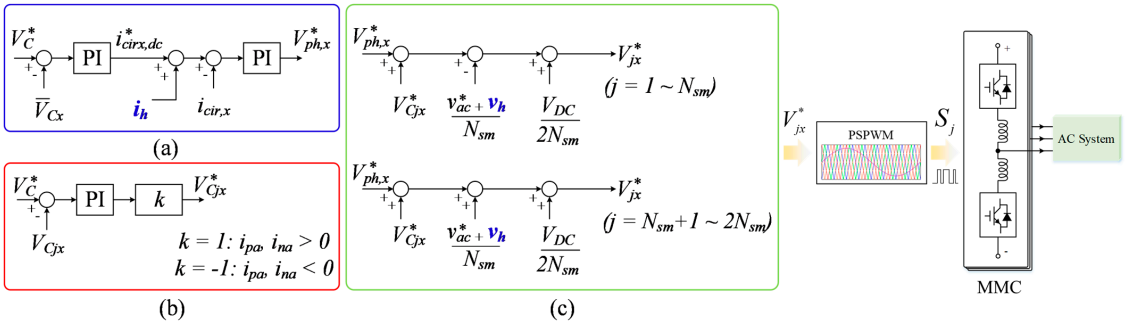

Figure 6. SM voltage balancing control based on the high-frequency injection method: (**a**) phase voltage balancing and circulating current control, (**b**) individual SM voltage control, (**c**) SM voltage reference generation.

$$V_{jx}^* = V_{ph,x}^* + V_{Cjx}^* - \frac{v_{ac}^* + v_h^*}{N_{sm}} + \frac{V_{DC}}{2N_{sm}} \quad (j = 1:4) \tag{25}$$

$$V_{jx}^* = V_{ph,x}^* + V_{Cjx}^* + \frac{v_{ac}^* + v_h^*}{N_{sm}} + \frac{V_{DC}}{2N_{sm}} \quad (j = 5:8) \tag{26}$$

3.4. Overall System Control

Figure 7 illustrates a comprehensive control block diagram of the MMC-based motor drive system, encompassing both motor control and converter control. Motor drive control employs the field-oriented control (FOC) method, which consists of an outer loop controller and an inner loop controller. In the outer loop controller, the actual motor speed (ω) and rotor flux (ψ) are regulated to track the reference values of ω* and ψ*, thus providing the direct–quadrature (d-q) axis current references (i_d^* and i_q^*) and stator current angle (θ_r). In the inner controller, the measured stator current (i_d and i_q) is regulated to follow the reference values i_d^* and i_q^*. The output of the FOC control provides voltage commands (m_a, m_b, and m_c), which are utilized to generate modulation signals for SM voltage reference generation. Further details regarding the FOC method for controlling motor drives using the d-q reference frame can be found in [39].

Regarding MMC control, the control strategy for SM voltage balancing encompasses the average SM voltage balancing control, individual SM voltage balancing control, and circulating current control, contributing to the generation of the SM voltage reference. A detailed discussion of the components of the SM capacitor voltage balancing control is provided in Section 3.3. Additionally, the high-frequency common-mode voltage (CMV) injection method was employed to mitigate the SM voltage fluctuation during the standstill/low-speed period of the motor drives. The phase-shifted pulse-width modulation (PSPWM) scheme is utilized to generate the switching state of the power switching devices, as depicted in Figure 7.

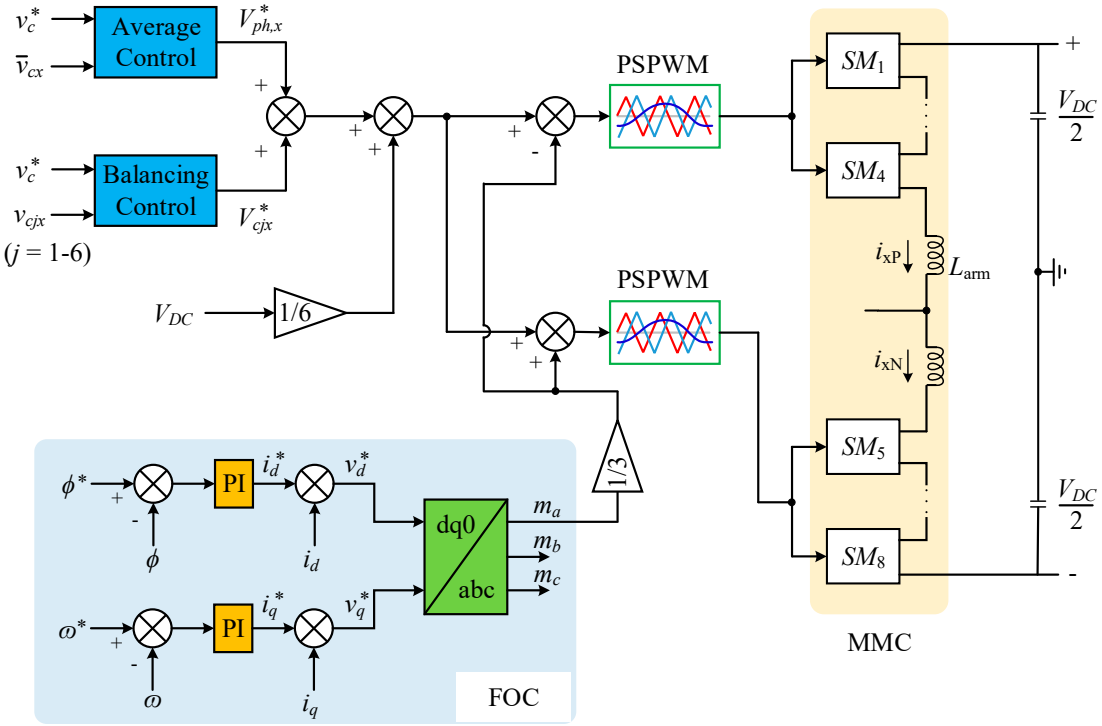

Figure 7. Overall control block diagram of the MMC system.

4. Simulation Results

In this section, we verify the efficiency of the proposed approach in reducing the size of the SM capacitor using time-domain simulation with MATLAB/SIMULINK software and real-time simulation using the OPAL/RT platform. The motor converter system consisted of an induction motor (IM) and a three-phase MMC with 3 SMs per arm, totaling 18 SMs. The system parameters are listed in detail, as shown in Table 1.

Table 1. System Parameters.

Parameters	Symbol	Values
DC-link voltage	V_{DC}	4800 V
Number of SMs per arm	N_{SM}	3
Arm inductance	L_{arm}	1.5 mH
SM capacitance	C_{dc}	1000 uF
Switching frequency	f_{sw}	2000 Hz
Nominal frequency	f_n	60 Hz
Rated voltage	V_{rated}	3300 V
Rated current	I_{rated}	215 A
Rated speed	ω_{rated}	1800 rpm
Rated torque	T_{rated}	5306 N.m
Voltage ripple limit	Δv_{lim}	10%

The variation in the SM voltage ripple, according to the variation in the operating frequency and considering high-frequency components injected into each arm to eliminate the SM capacitor voltage fluctuation, is illustrated in Figure 8. Theoretically, the SM voltage fluctuation is inversely proportional to the operation frequency, resulting in significant voltage fluctuation at a very low frequency operation (f_n = 1 Hz) without injecting high-frequency CMV (Δv_{p-p} = 16,074 V), reducing significantly ($\Delta v_{c,p-p}$ = 159.155 V) with the support of injected high-frequency components, as shown in Figure 8. Therefore, the SM capacitor voltage ripple must be mitigated during the standstill/low-speed operation of the motor drive to ensure a high performance of the system.

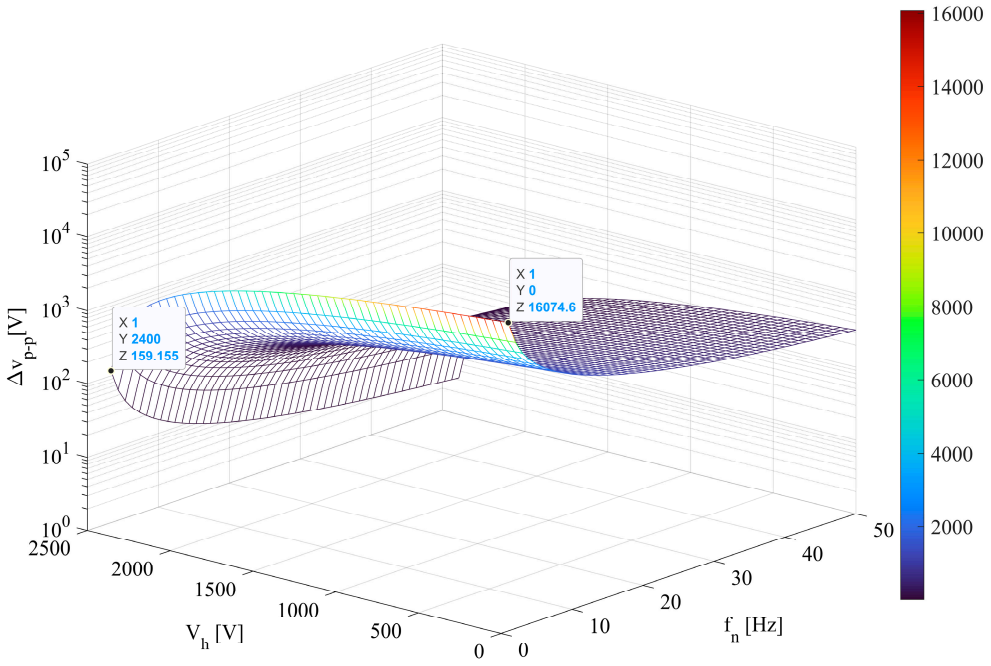

Figure 8. Variation in SM capacitor voltage ripple ($\Delta v_{c,p-p}$) based on injected high-frequency components and operating frequency (f_n).

The effectiveness of the proposed algorithm for estimating SM voltage fluctuations is validated by comparing the estimated SM capacitor voltage fluctuation, as defined in Equation (22), and the real values of the SM voltages in the upper arm (v_{cu}) and lower arm (v_{cl}). This comparison is depicted as shown in Figure 9a,b. It is evident that the estimated SM voltage, indicated by the red line, closely tracked the real values of the individual SM voltages in terms of both shape and magnitude. The simulation involved high-frequency components injected at a very low motor speed, with four SMs integrated

into each converter arm and a DC-link voltage of 8000 V. The proposed algorithm exhibited excellent efficiency in estimating SM voltage fluctuations, with an error of less than 1%, as illustrated in Table 2 and Figure 10.

Figure 11 presents a recommendation for optimizing the SM capacitance at various operating frequencies using the proposed algorithm, based on the predefined system requirement for the SM voltage ripple limit (Δv_{lim}). Assuming that the system allows for a maximum voltage ripple of Δv_{lim} = 10%, the SM capacitance can be designed as C_{dc} = 1000 µF, as illustrated in Figure 11. The performance of the MMC-based motor drive system, considering the optimal SM capacitance of C_{dc} = 1000 µF and a high-frequency CMV injection, is shown in Figure 12. With the selected SM capacitance of C_{dc} = 1000 µF, the SM capacitor voltages were maintained in balance at the rated voltage of 1600 V, ensuring that the voltage fluctuations remained within the acceptable range defined by the system requirement of Δvlim.

Table 2. Performance comparison of SM voltage ripple estimation method.

Frequency [f_n]	Voltage Ripple Estimation	Real SM Voltage Ripple
5 Hz	9.8%	9.5%
10 Hz	8.6%	8.1%
15 Hz	6%	6.6%
20 Hz	5.4%	5.8%
25 Hz	3.6%	4.2%
30 Hz	2.2%	2.9%

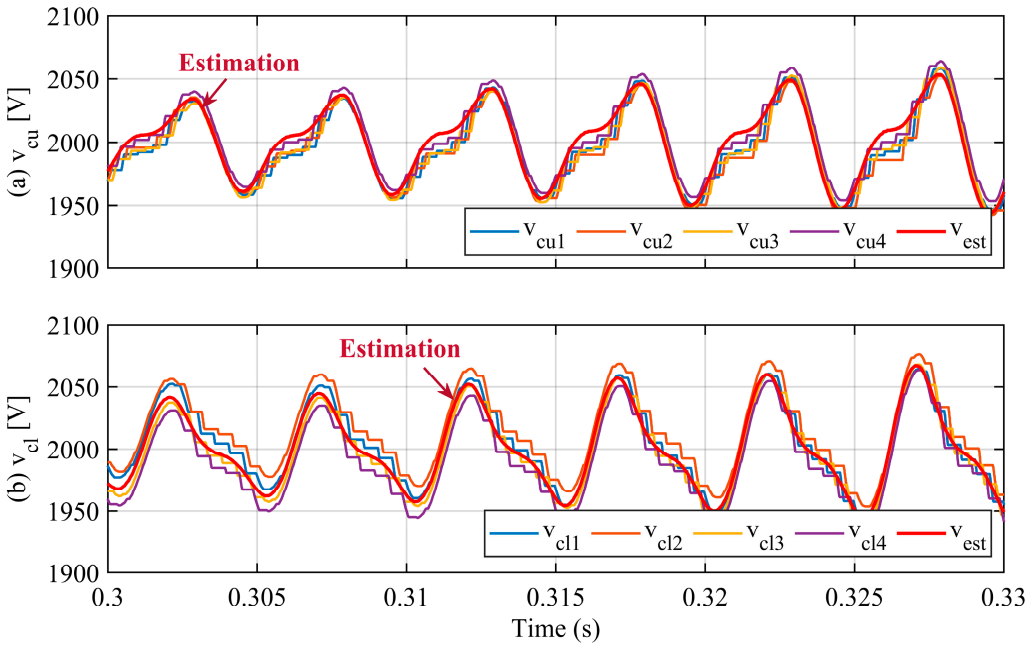

Figure 9. The performance of SM voltage estimation algorithm: (**a**) upper arm SM capacitor voltage, (**b**) lower arm SM capacitor voltage.

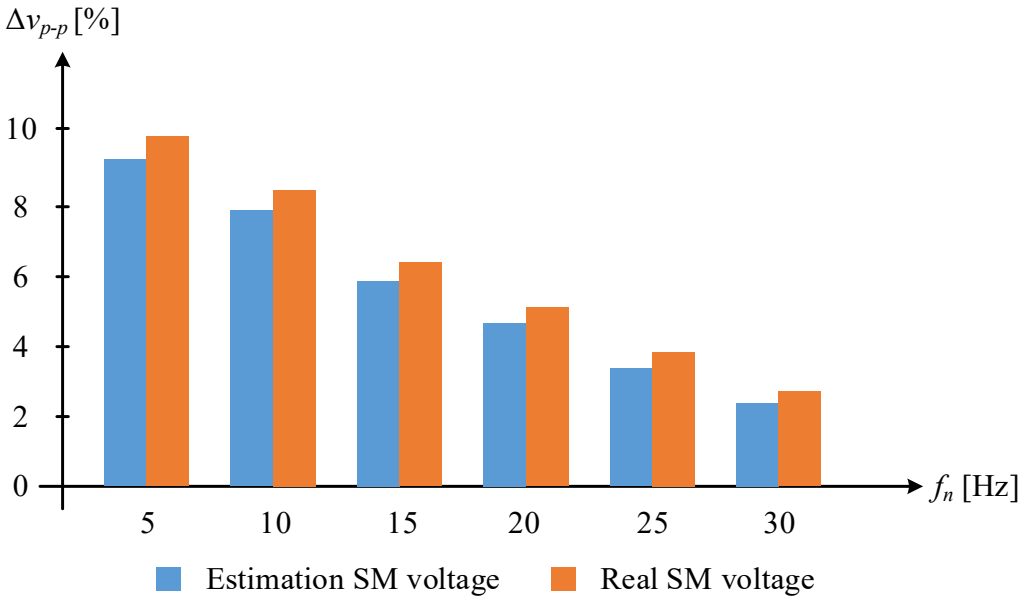

Figure 10. Performance comparison of SM voltage ripple estimation method.

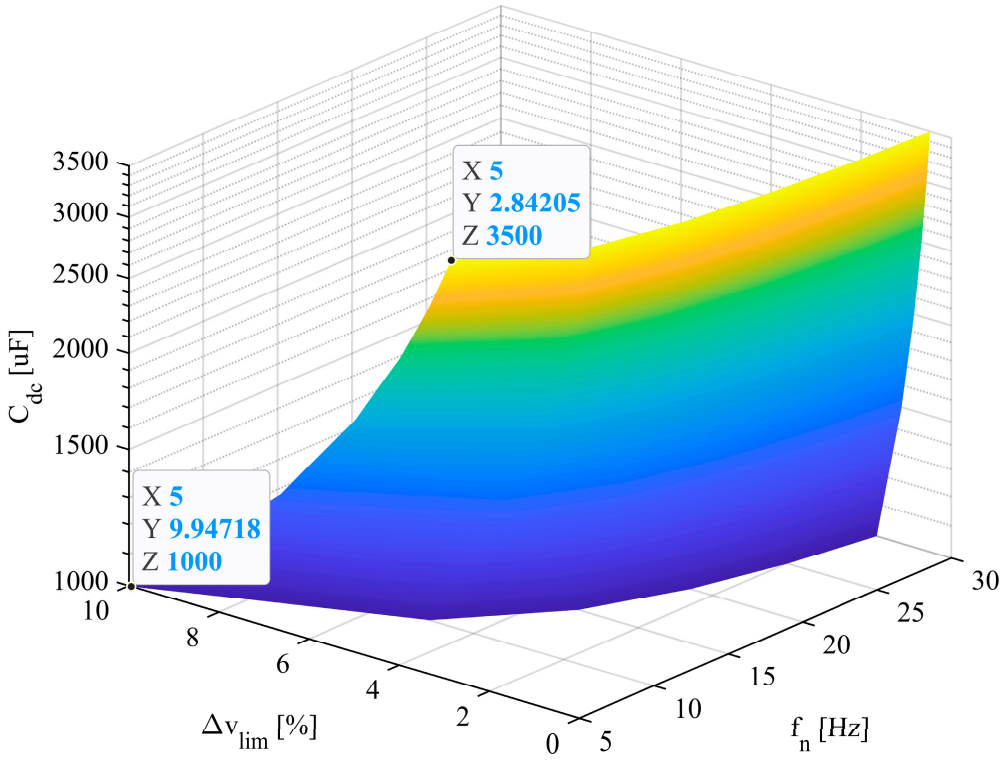

Figure 11. Design of SM capacitance at different operating frequencies based on the predetermined voltage ripple limit (Δv_{lim}).

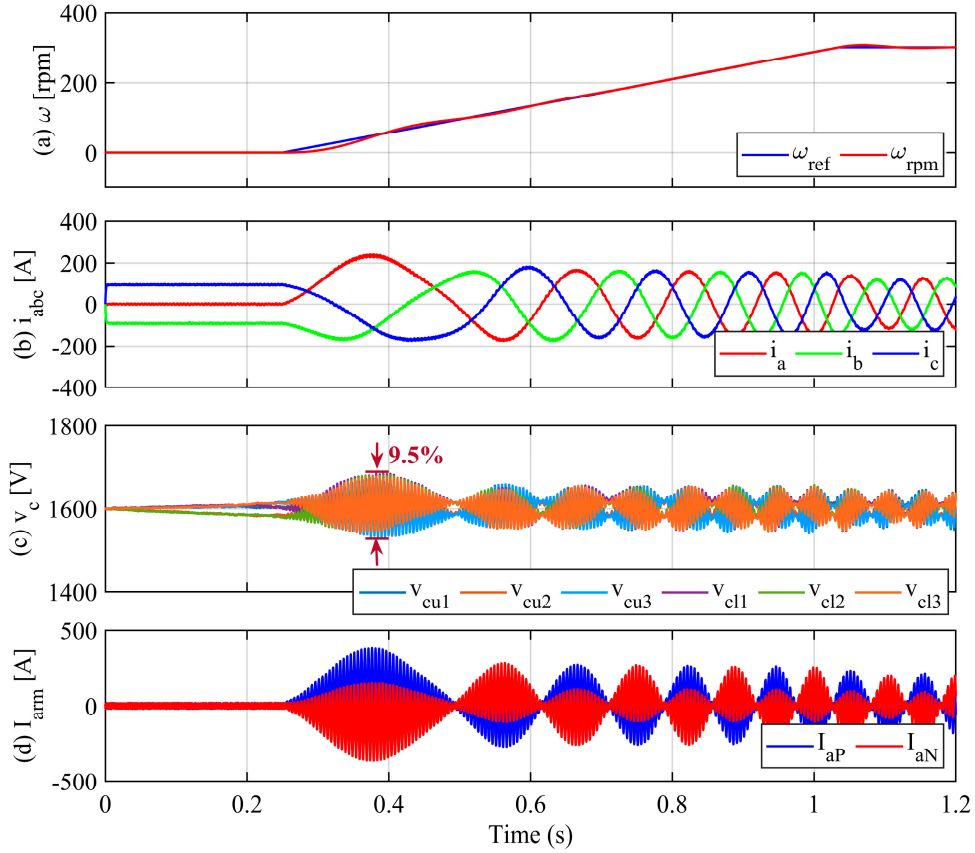

Figure 12. Performance of the MMC with proposed SM capacitance selection: (**a**) motor speed, (**b**) three-phase current, (**c**) SM capacitor voltage, (**d**) arm currents.

5. Real-Time Simulation

In this section, we evaluate the effectiveness of the proposed algorithm through real-time simulations using an OPAL-RT 5707 real-time simulator. These simulations ensured that computations occurred in real-time and were consistent with the results obtained from the hardware setup. The system configuration of the real-time simulator is illustrated in Figure 13, consisting of an OPAL-RT5707 real-time simulator, an RT-Lab target PC, an interface PC, and an oscilloscope. Initially, the proposed algorithm was conducted on the MATLAB/SIMULINK platform, seamlessly integrated into RT-LAB. Subsequently, real-time simulations were conducted using multiple cores. It is important to note that the OPAL-RT/FPGA analog output is limited to a range of ±16 V, requiring the application of a scaling factor for the effective visualization of the analog output waveforms.

Figure 14 illustrates the effectiveness of the proposed algorithm in estimating the voltage of the SM capacitor. The estimation, denoted by (22), was compared with the actual SM capacitor voltage. Owing to equipment constraints, only one SM voltage in both the upper and lower arms was compared with its estimated value. As shown in Figure 14a,b, the red lines representing the estimated SM capacitor voltage closely track the blue lines representing the real SM capacitor voltage. This observation validates the robust performance of the proposed algorithm for accurately estimating SM capacitor voltages.

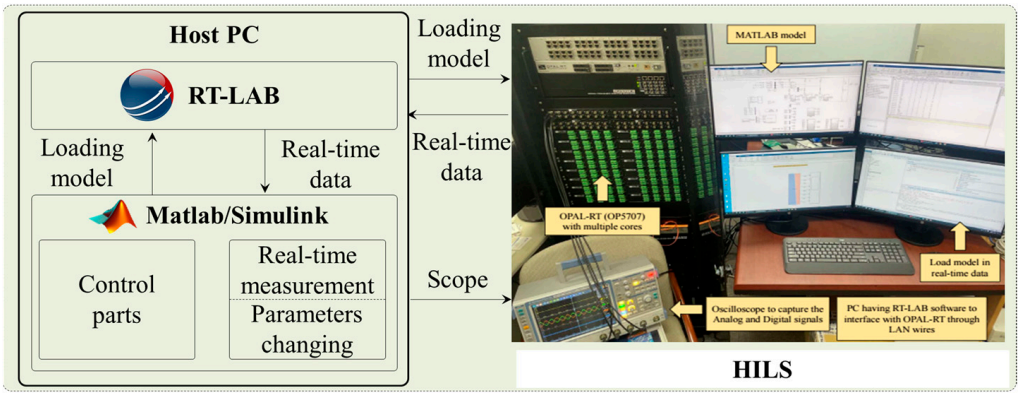

Figure 13. Establishment of a real-time simulation in laboratory using OPAL-RT simulator.

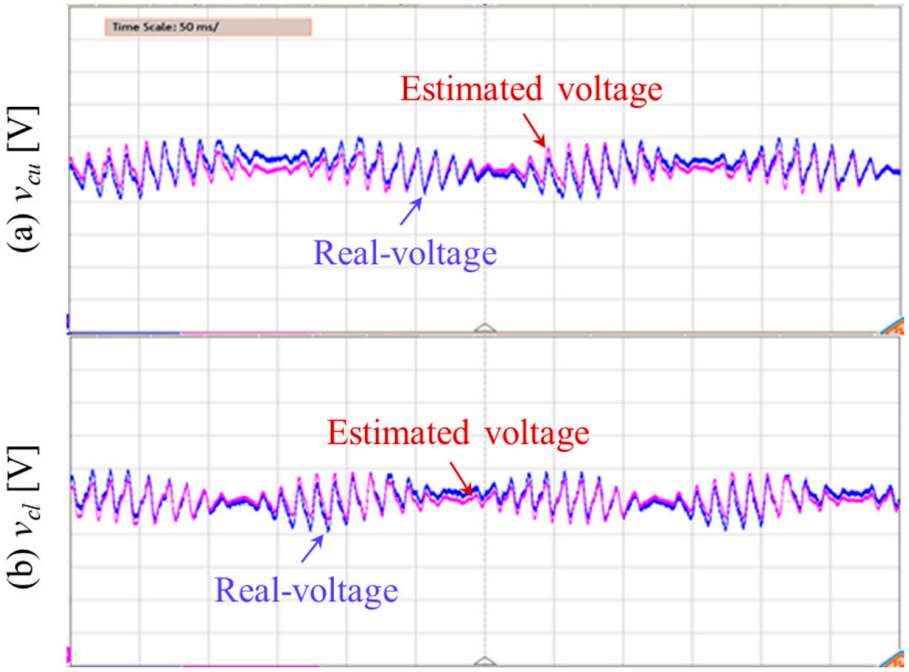

Figure 14. The performance of the proposed voltage estimation algorithm: (**a**) SM capacitor voltage in the upper arm, (**b**) SM capacitor voltage in the lower arm.

With the estimated SM capacitor voltage shown in Figure 14, the optimal SM capacitance of C_{dc} = 1000 µF was selected to ensure that the SM capacitor voltage fluctuated within the predefined range of the system specification. The performance of the proposed algorithm in fine-tuning the capacitance of the SM was evaluated at exceptionally low motor speeds of ω = 150 rpm using a real-time simulator, as shown in Figure 15. As indicated in Figure 15b, the voltages across the SM capacitors were maintained at equilibrium at the rated voltage of $v_{c,rated}$ = 1600 V, and the fluctuations in the SM capacitor voltages remained within 10%. This demonstrates compliance with the system requirements specifying Δv_{lim} = 10%.

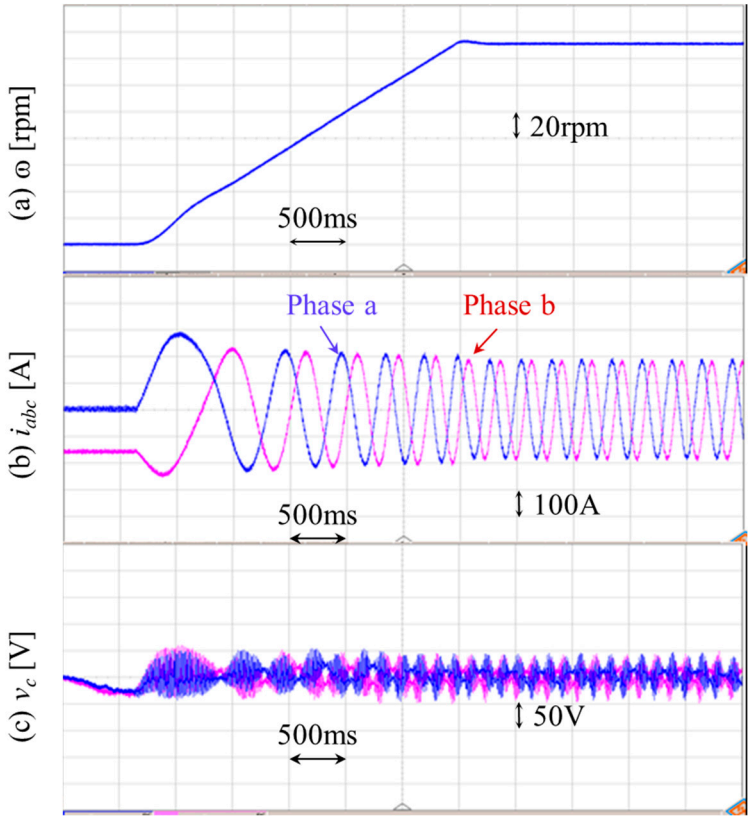

Figure 15. Real-time performance of the proposed algorithm: (**a**) motor speed, (**b**) output current, (**c**) SM capacitor voltage.

6. Conclusions

This paper proposes an optimal design algorithm to determine the optimal capacitance of SM capacitors in an MMC, using a proposed SM voltage ripple estimation algorithm to ensure that the SM voltages fluctuate within an acceptable range during low-frequency operations. Additionally, the concept of high-frequency CMV and circulating current injected into each arm has been conducted to minimize SM capacitor voltage fluctuations during low-speed or standstill operations of motor drives. Consequently, the proposed algorithm demonstrates exceptional precision, predicting the SM capacitor voltage ripple with a variance of less than 1%. The effectiveness of the proposed method was verified using time-domain simulation results with MATLAB/SIMULINK software and real-time simulation results with the OPAL-RT simulator platform. The simulation results demonstrate that the capacitance value obtained through the proposed optimal design algorithm guarantees that the SM capacitor voltage fluctuates within an acceptable range of Δv_{lim} = 10%.

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Conflicts of Interest: The authors declare no conflicts of interest.

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