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A Systematic Method for Scaling Coefficients of the Continuous-Time Low-Pass ΣΔ Modulator Using a Simulink-Based Toolbox

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Abstract: The sigma-delta modulator (SDM) is one of the well-established data converter architectures. It is well-known for achieving a high signal-to-noise ratio (SNR). In the SDM, the integrators in the loop filter could suffer from overloading if the signal swing exceeds its maximum level, which leads to performance and SNR degradation. Thus, scaling the system coefficients is needed, such that there is no overloading for the integrators. In this work, we present a systematic general method that could be used for scaling the signal swings in the continuous-time low-pass sigma-delta modulator (SDM). The proposed method can be applied to any continuous-time low-pass SDM architecture, and it includes the scaling of all the possible combinations of the system coefficients. Moreover, an open-source Simulink-based toolbox that includes the systematic method is presented. This toolbox could help the designer to execute the scaling process and the simulations in an efficient way. In addition to that, a design example is discussed to illustrate the proposed method, wherein the presented toolbox is used for simulations, and the simulation results are shown.

Keywords: sigma-delta modulator; coefficients scaling; analog-to-digital conversion; system level optimization; modelling; MATLAB; Simulink; toolbox

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1. Introduction

The sigma-delta modulator (SDM) is the most commonly used data converter in high-precision applications. It can perform high-resolution data conversion using the oversampling and noise-shaping techniques. There is a recent trend nowadays to use the sigma-delta modulator in high-speed applications. For such applications, the continuous-time sigma-delta modulator is widely used. The continuous-time sigma-delta modulator is preferred over the discrete-time sigma-delta modulator due to its higher speed and its lower power consumption [1,2].

In continuous-time sigma-delta modulators, the integrators could suffer from overloading if the output signal swing exceeds the full-scale limit. This overloading causes degradation in the performance of the modulator that can be noticed when implementing the circuits, wherein the signal is clipped if its swing is larger than the full-scale limit. Therefore, one important step in the system-level design of the SDM is to perform scaling for the system coefficients, such that the integrators' output swings are within the full-scale limit, so that there is no overloading [3,4].

Figure 1 shows a general third-order continuous-time low-pass sigma-delta modulator. It includes all the possible system coefficients. It includes feedforward coefficients ("k" coefficients), input feedforward coefficients ("b" coefficients), resonators ("g" coefficients), and feedback DAC coefficients ("a" coefficients). There are two types of coefficients that are included: the resistive types (ending with "R") and the capacitive types (ending with "C"). For the feedback DACs, each one can be either a resistive DAC or a current DAC. The third-order SDM includes three integrators. Each integrator supports three input paths:

including resistive input paths (R), capacitive input paths (C), and DAC input paths (D). It also includes an adder block and a quantizer block. The quantizer can be a single-bit or a multi-bit quantizer. This general third-order SDM is used for illustration in this work; however, the same concepts can be applied to any other order.

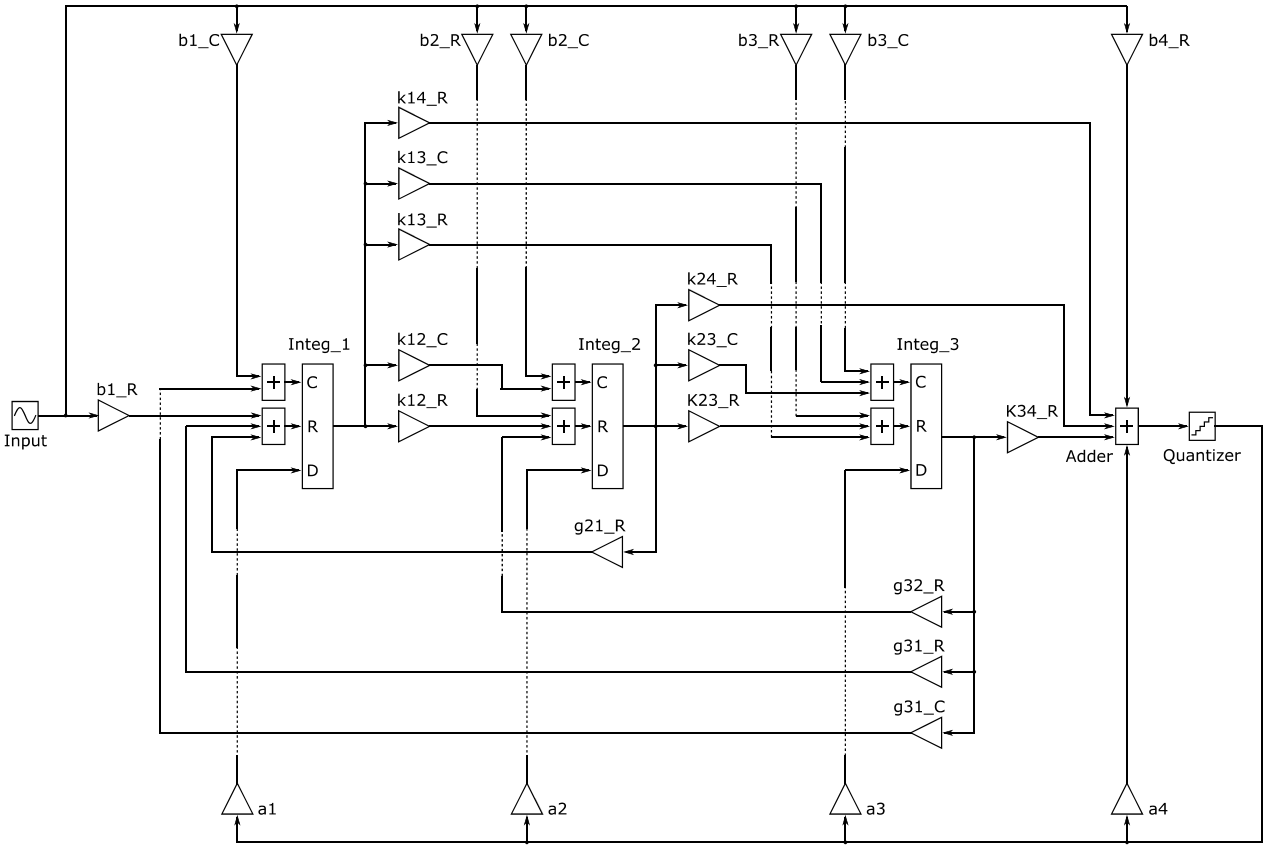

Figure 1. Simplified general diagram of a third-order continuous-time low-pass SDM.

Several methods for SDM coefficient scaling have been published before. A systematic method for scaling integrators' output swings in sigma-delta modulators has been proposed in [5]. Another systematic method for scaling integrators' output swings in resonator-based continuous-time sigma-delta modulators has been proposed in [6]. Moreover, another method for scaling the feedback coefficients of continuous-time sigma-delta modulators has been proposed in [7]. These methods can be used to scale integrators' output swings by scaling the system coefficients, while preserving both the signal transfer function (STF) and the noise transfer function (NTF). However, these methods still have some limitations.

First, every one of these methods discusses only one specific filter type of the sigma-delta modulator, either SDM with feedback filter architecture or SDM with feedforward filter architecture. However, various published designs tend to have a hybrid architecture, including both feedforward and feedback coefficients at the same time, which helps to reduce the STF peaking while ensuring that the integrators' output swing is not large [8–13]. Such hybrid architecture was not included in the previous three methods. Second, they do not include the scaling technique for the input feedforward coefficients ("b" coefficients), which have been used in some recent designs [14–16]. Third, they do not include the scaling technique for the capacitive-type coefficients, which have been used in several published sigma delta modulators [17–21]. Fourth, they only include the simplest integrator model (1/S), but they do not include other models for the integrator, such as the opamp-based RC integrator with a series resistor and capacitor in the feedback network, which has been used in multiple SDM designs [22–27], or the one with a parallel resistor and capacitor

in the feedback network, which has been used in some SDM designs [28,29]. Fifth, they do not include the method of adjusting the signal swing at the input of the quantizer, which is needed to avoid the overloading of the quantizer. Sixth, none of these methods discussed the trade-off between the integrator output swing and the linearity specification of the integrator.

With respect to the tools for the automation of this scaling process, one well-known option is the MATLAB-based Schreier Delta-Sigma toolbox [30]. It can perform the scaling of the coefficients automatically to adjust the signal swings, and it generates the scaled coefficients. However, it has the same limitations mentioned before in previous scaling methods, with the exception that it includes the option to scale the input feedforward coefficients ("b" coefficients).

In this work, a systematic general method for the scaling of the signal swings in the continuous-time low-pass sigma-delta modulator is proposed. This method overcomes the limitations mentioned before. First, the proposed method is a generic method that could be applied to any SDM architecture, including the scaling of all the possible system coefficients (feedforward coefficients, feedback coefficients, and resonators). Second, it includes the scaling technique of the input feedforward coefficients ("b" coefficients). Third, it provides the scaling method for capacitive-type coefficients in addition to resistive-type coefficients. Fourth, it includes various integrator models that are not included in the previous reported methods, such as the opamp-based RC integrator with a series resistor and capacitor in the feedback network, or the one with a parallel resistor and capacitor in the feedback network. Fifth, it includes the option of adjusting the signal swing at the input of the quantizer. Sixth, it includes the non-linearity effect of the integrator to deduce the trade-off between the integrator output swing and the integrator non-linearity.

Moreover, an open-source MATLAB and Simulink-based toolbox has been included in this work (link in the references section) [31]. This toolbox can be easily used to simulate continuous-time sigma-delta modulators and to scale signal swings, with the proposed systematic method included inside the toolbox. The user can enter the system coefficients, simulate the system, and deduce the needed scaling of the swings. Then, he can select the scaling factor needed for each block, and the new coefficients will be calculated automatically. Hence, this toolbox greatly aids in automating the process of scaling SDM system coefficients.

The paper is organized as follows: In Section 2, the integrator block is discussed in detail, presenting the different models included for the integrator and discussing integrator non-linearity modelling after that. In Section 3, the proposed systematic method for scaling the integrators' output swings, and the proposed method for adjusting the signal swing at the input of the quantizer are both presented. In Section 4, a design example is discussed for illustration, and the toolbox simulation results are shown. Section 5 concludes the paper.

2. Modelling of the Integrator

Before discussing the proposed systematic scaling method, it is crucial to first discuss the model of the integrator that can be used in the continuous-time low-pass SDM. The proposed toolbox, accompanied by the proposed systematic method, includes various models for the opamp-based RC integrator. The integrator model can generally support resistive input path, capacitive input path, and DAC input path. The DAC could be a current DAC or a resistive DAC. Regarding the integrator feedback network, the included designs have three types of the feedback networks: a capacitor, a capacitor with a series resistor, and a capacitor with a parallel resistor.

Figure 2 shows a simplified schematic of the family of opamp-based RC integrator designs included in the study. A summary of the included designs of the opamp-based RC integrator is presented in Table 1. The definitions of the main circuit parameters related to Figure 2 are shown in Table 2. The output expressions of the included designs of the opamp-based RC integrator are shown in Table 3. The negative sign due to the inverting gain of the single-ended opamp-based RC integrator is neglected for simplicity. It is worth

mentioning that the opamp is assumed to be ideal for simplicity because non-idealities, such as its finite gain and bandwidth do not have any significant effect on the system coefficients scaling process. Table 4 includes the definitions of the input coefficients used in the equations mentioned in Table 3. Table 5 includes the definitions of some parameters used in the equations mentioned in Table 3.

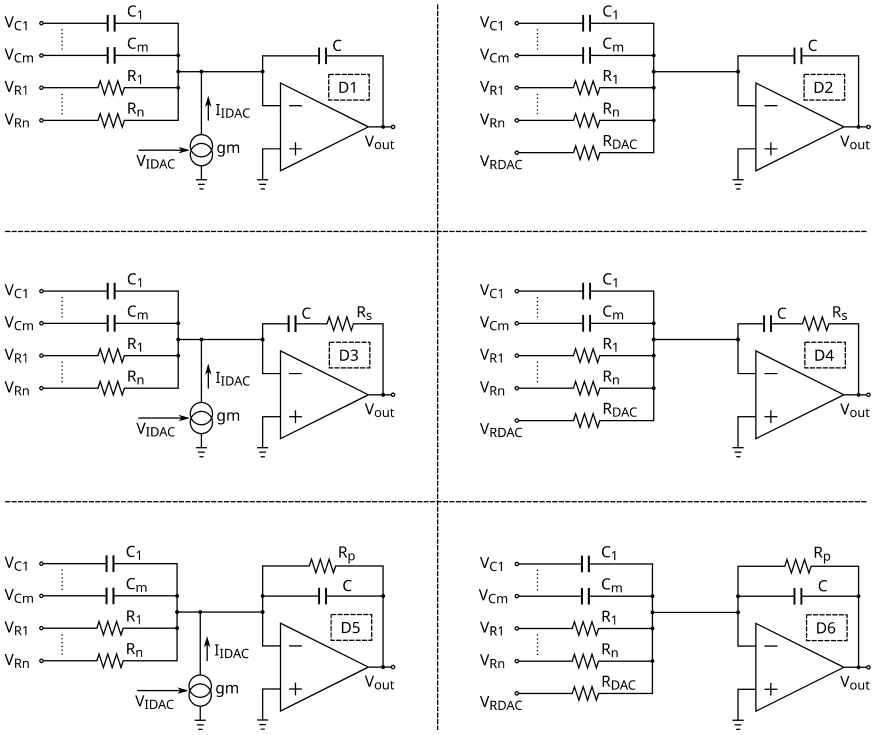

Figure 2. Schematic of the included designs of the opamp-based RC integrator.

Table 1. Included designs of the opamp-based RC integrator.

Design #	Input Path Type	DAC Type	Feedback Network
D1	Resistive and Capacitive	Current DAC	C
D2	Resistive and Capacitive	Resistive DAC	C
D3	Resistive and Capacitive	Current DAC	C + series R
D4	Resistive and Capacitive	Resistive DAC	C + series R
D5	Resistive and Capacitive	Current DAC	C + parallel R
D6	Resistive and Capacitive	Resistive DAC	C + parallel R

Table 2. Main circuit parameters of the opamp-based RC integrator.

Parameter	Definition
C	Integrator capacitor in the feedback network.
R_P	Parallel resistor with the capacitor in the feedback network.
R_S	Series resistor with the capacitor in the feedback network.
R_i	Resistor of the resistive input path. There are (n) resistive input paths $(R_1, \ldots, R_n)$.
C_i	Capacitor of the capacitive input path. There are (m) capacitive input paths $(C_1, \ldots, C_m)$.
V_{Ri}	Input signal of the resistive input path of the integrator. There are (n) resistive path input signals $(V_{R1}, \ldots, V_{Rn})$.

Table 2. *Cont.*

Parameter	Definition	
V_{Ci}	Input signal of the capacitive input path of the integrator. There are (m) capacitive path input signals ($V_{C1}, \ldots, V_{Cm}$).	
gm	Transconductance of the current DAC. $I_{IDAC} = gm \cdot V_{IDAC}$	(1)
V_{IDAC}	Input signal of the current DAC input path.	
R_{DAC}	Resistor of the resistive DAC input path.	
V_{RDAC}	Input signal of the resistive DAC input path.	

Table 3. Output expressions of the included designs of the opamp-based RC integrator.

Design #	Output Expression	
D1	$Vout = \frac{S\cdot(\sum_{i=1}^{m} K_{Ci}V_{Ci})+(\sum_{i=1}^{n} F_sK_{Ri}V_{Ri})+(F_sK_{IDAC}V_{IDAC})}{S}$	(2)
D2	$Vout = \frac{S\cdot(\sum_{i=1}^{m} K_{Ci}V_{Ci})+(\sum_{i=1}^{n} F_sK_{Ri}V_{Ri})+(F_sK_{RDAC}V_{RDAC})}{S}$	(3)
D3	$Vout = \frac{\left(\sum_{i=1}^{m}\left(\left(S^2\cdot\frac{XP}{F_s}\right)+S\right)\cdot K_{Ci}\ V_{Ci}\right)+(\sum_{i=1}^{n}((S\cdot XP)+F_s)\cdot K_{Ri}V_{Ri})+(((S\cdot XP)+F_s)\cdot K_{IDAC}\ V_{IDAC})}{S}$	(4)
D4	$Vout = \frac{\left(\sum_{i=1}^{m}\left(\left(S^2\cdot\frac{XP}{F_s}\right)+S\right)\cdot K_{Ci}\ V_{Ci}\right)+(\sum_{i=1}^{n}((S\cdot XP)+F_s)\cdot K_{Ri}V_{Ri})+(((S\cdot XP)+F_s)\cdot K_{RDAC}\ V_{RDAC})}{S}$	(5)
D5	$Vout = \frac{S\cdot(\sum_{i=1}^{m} K_{Ci}\ V_{Ci})+(\sum_{i=1}^{n} F_sK_{Ri}V_{Ri})+(F_sK_{IDAC}V_{IDAC})}{S+\frac{1}{TP}}$	(6)
D6	$Vout = \frac{S\cdot(\sum_{i=1}^{m} K_{Ci}\ V_{Ci})+(\sum_{i=1}^{n} F_sK_{Ri}V_{Ri})+(F_sK_{RDAC}V_{RDAC})}{S+\frac{1}{TP}}$	(7)

Table 4. Definitions of the input coefficients.

Coefficient	Definition	
K_{Ri}	Coefficient of the resistive input path. $K_{Ri} = \frac{1}{F_s\cdot R_i\cdot C}$	(8)
K_{Ci}	Coefficient of the capacitive input path. $K_{Ci} = \frac{C_i}{C}$	(9)
K_{IDAC}	Coefficient of the current DAC input path. $K_{IDAC} = \frac{gm}{F_s\cdot C}$	(10)
K_{RDAC}	Coefficient of the resistive DAC input path. $K_{RDAC} = \frac{1}{F_s\cdot R_{DAC}\cdot C}$	(11)

Table 5. Definitions of some parameters used in Table 3.

Parameter	Definition	
F_s	Sampling frequency.	
TP	$TP = R_P \cdot C$	(12)
XP	$XP = \left(\frac{1}{K_{Ri}}\cdot\frac{R_S}{R_i}\right) = R_S\cdot F_s\cdot C$	(13)

Figure 3 shows the simplified general diagram of the model of the integrator. There are three types of input paths: the resistive input path, capacitive input path, and the DAC input path (which can be either current DAC or resistive DAC). There is a transfer function block for each one of the three paths based on the derived equations from (2) to (7). The model also includes a saturation block which includes the option of swing limitation beyond a certain threshold. Moreover, it has the option to include the non-linearity effect of the opamp. This will be discussed in the next paragraph.

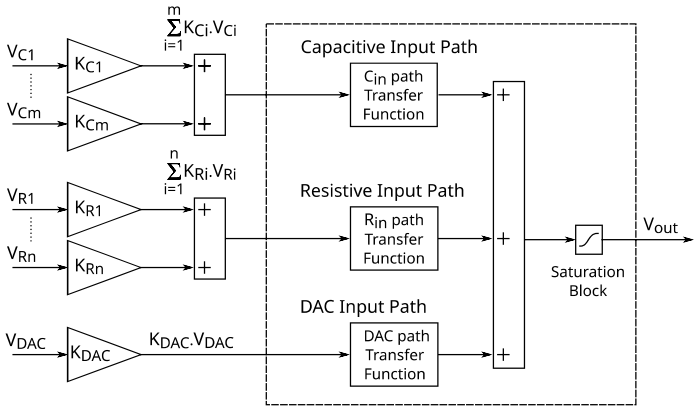

Figure 3. Simplified general block diagram of the model of the opamp-based RC integrator.

One important thing that was not included in the previous methods [5–7] is the non-linearity effect of the opamp gain used in the integrator. In real circuits, as the output swing of the integrator becomes large (even within the allowed full-scale limit), the output impedance of the opamp can be affected due to the change in the available headroom on the CMOS transistors, and hence the gain of the opamp can vary with the output swing level. Such non-linearity in the opamp gain leads to harmonic distortion and degradation in the SNDR (Signal to Noise and Distortion Ratio). Thus, it is important to include such an effect in the integrator model to see the non-linearity effect versus the output swing level.

Equations (14) and (15) describe the transfer function of this block given that the input is within the full-scale limit. Ideally (i.e., with no included non-linearity), the output equals the input. However, by including the non-linearity effect, there will be a smooth gain compression in the transfer function.

The term (α) represents the non-linearity. If its value is zero, this means that the block is perfectly linear (non-linearity is not included). As its value becomes larger than zero, this means more non-linearity. Figure 4 shows the characteristics of this block for different values of (α). In this graph, both the input and the output are normalized over the full-scale limit.

$$Vout = Vin \; ; \; if \; \alpha = 0 \tag{14}$$

$$Vout = \frac{1}{tanh(\alpha)} \cdot tanh(\alpha \cdot Vin) \; ; \; if \; \alpha \neq 0 \tag{15}$$

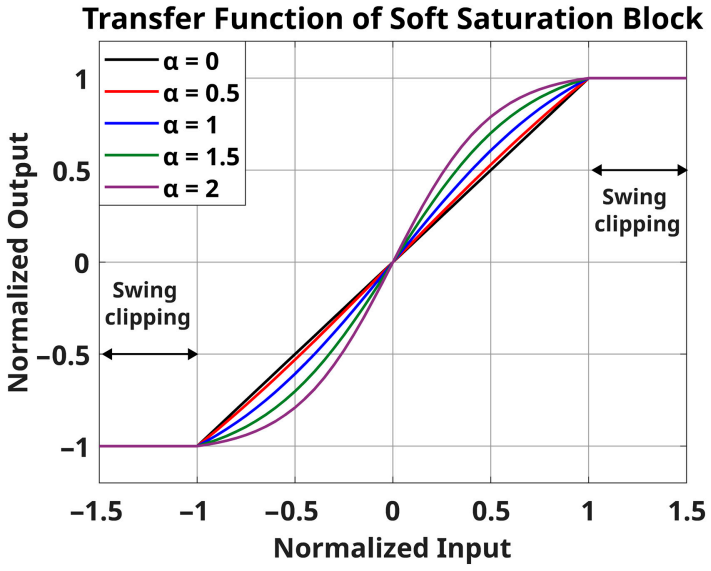

Figure 4. Transfer function of the soft saturation block for different values of (α).

3. Proposed Systematic Method for Scaling the Signal Swings

3.1. Proposed Method for Scaling the Integrators' Output Swings

Now, after discussing the model of the integrator, the general idea of the scaling method of the integrator's output swing is discussed here. Figure 5 shows the general basic concept of this method. If it is desired to scale the integrator output swing by factor (F), all the input paths of the integrator are scaled by the factor (F), and all the paths connected to the output of the integrator are scaled by ($1/F$). There are three input paths of the integrators: the resistive input path, the capacitive input path, and the DAC input path. The paths connected to the output of the integrator are the resistive path and the capacitive path. By using this scaling method, the signal transfer function (STF) and the noise transfer function (NTF) of the SDM are not affected at all.

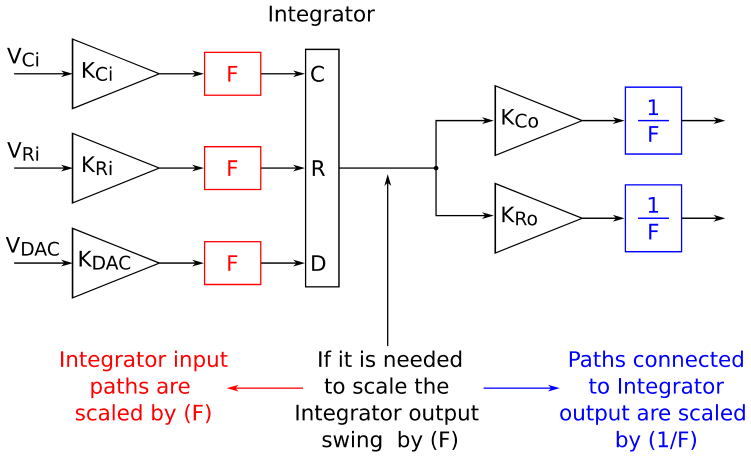

Figure 5. General ideas for scaling integrator output swings.

3.2. Proposed Method for Adjusting the Quantizer Input Signal Swing

In addition to the scaling of the integrator output swing, this paper presents a method to adjust the signal swing at the input of the quantizer. For adjusting the signal swing at the input of the quantizer, all the input paths to the quantizer are scaled by the factor (F_q), and all the paths connected to the output of the quantizer (which are the feedback DACs) are scaled by ($1/F_q$).

This proposed method has no effect on the noise transfer function (NTF). However, it has an effect on the signal transfer function (STF). The whole STF is scaled by the factor (F_q). Therefore, for example, if the signal swing at the input of the quantizer is scaled by (F_q = 0.7), the STF magnitude will be multiplied by 0.7, which means that its magnitude will decrease by 3 dB and the SNR will decrease by 3 dB.

Figure 6 shows the simplified diagram of the original SDM before adjusting the quantizer input signal swing. The quantizer is modelled as a gain block (Kq) (wherein Kq is the gain of the quantizer) and the quantization noise is added after it. The STF and NTF of the system can be deduced using th diagram below, and they are given by (16) and (17).

$$STF = \frac{X(S) \cdot K_q}{1 + D(S) \cdot K_q \cdot Y(S)} \tag{16}$$

$$NTF = \frac{1}{1 + D(S) \cdot K_q \cdot Y(S)} \tag{17}$$

If the input path of the quantizer is scaled by (F_q), and the output path of the quantizer is scaled by ($1/F_q$), the new simplified diagram of the modified SDM is shown in Figure 7.

The new STF and NTF of the system can be deduced using the diagram below, and they are given by (18) and (19).

$$STF\ after\ including\ F_q = \frac{X(S)\cdot K_q \cdot F_q}{1+\frac{1}{F_q}\cdot D(S)\cdot K_q \cdot F_q \cdot Y(S)} = \frac{X(S)\cdot K_q \cdot F_q}{1+D(S)\cdot K_q \cdot Y(S)} \quad (18)$$

$$NTF\ after\ including\ F_q = \frac{1}{1+\frac{1}{F_q}\cdot D(S)\cdot K_q \cdot F_q \cdot Y(s)} = \frac{1}{1+D(S)\cdot K_q \cdot Y(S)} \quad (19)$$

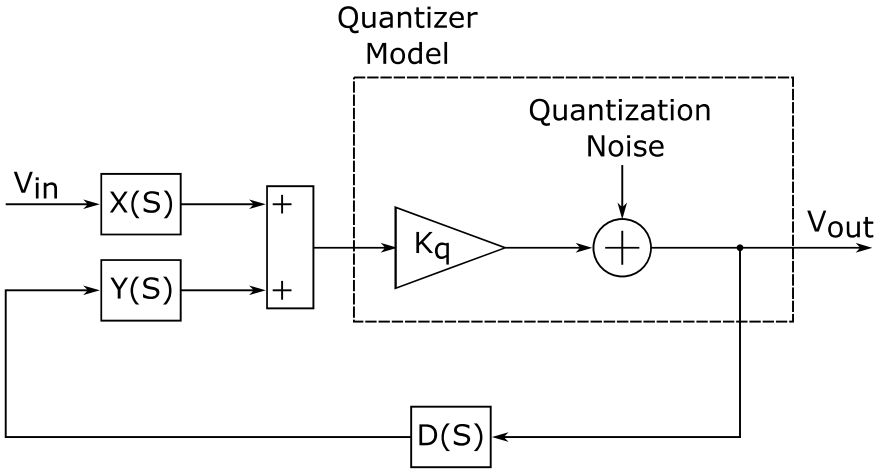

Figure 6. Simplified SDM diagram before adjusting the quantizer input signal swing.

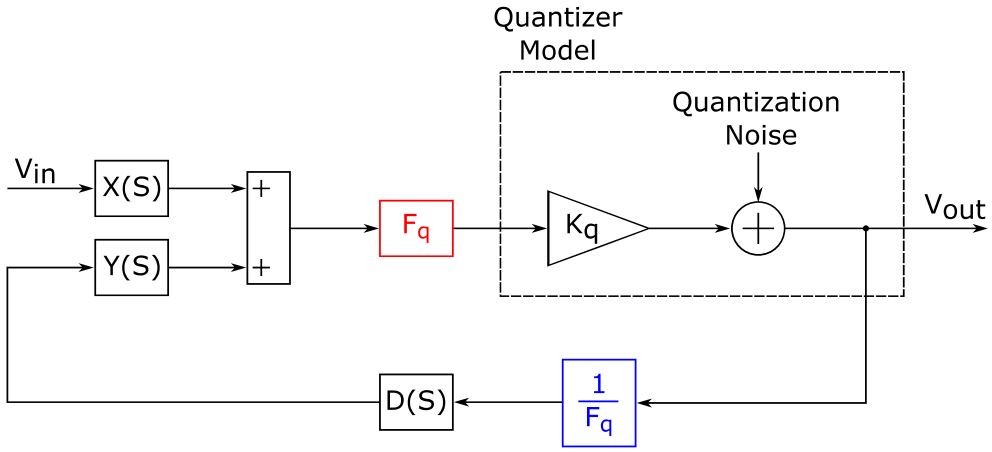

Figure 7. Simplified SDM diagram after adjusting the quantizer input signal swing.

It is clear from the previous equations that the NTF will remain unchanged, while the STF will change. For the STF, the denominator remains the same, while the numerator is multiplied by the factor (F_q).

It is important to mention that adjusting the signal swing at the input of the quantizer (using F_q) is not exactly linear; this is because the quantizer is a non-linear block in reality. Furthermore, it is also worth mentioning that using the scaling factor (F_q) could lead to a very small change in the output swings of the integrators. That can be noticed in the design example discussed later.

3.3. Summary of the Scaling Factors

By applying the proposed methods mentioned above to the general third-order SDM shown in Figure 1, Table 6 presents a summary. This table shows the scaling factor of each

coefficient in the SDM, wherein (F_1) is the scaling factor of the first integrator output swing, (F_2) is the scaling factor of the second integrator output swing, (F_3) is the scaling factor of the third integrator output swing, and (F_q) is the factor used for adjusting the quantizer input signal swing. The third-order SDM is used for illustration; however, the same concept can be applied to any other order.

Table 6. Scaling factor for each coefficient in a third-order SDM.

Coeff.	Scaling Factor	Coeff.	Scaling Factor	Coeff.	Scaling Factor
k12_R	$\frac{F_2}{F_1}$	b1_R	F_1	k13_R	$\frac{F_3}{F_1}$
k23_R	$\frac{F_3}{F_2}$	b2_R	F_2	k14_R	$\frac{F_q}{F_1}$
k34_R	$\frac{F_q}{F_3}$	b3_R	F_3	k24_R	$\frac{F_q}{F_2}$
a1	$\frac{F_1}{F_q}$	b4_R	F_q	k12_C	$\frac{F_2}{F_1}$
a2	$\frac{F_2}{F_q}$	b1_C	F_1	k13_C	$\frac{F_3}{F_1}$
a3	$\frac{F_3}{F_q}$	b2_C	F_2	k23_C	$\frac{F_3}{F_2}$
a4	$\frac{F_q}{F_q} = 1$	b3_C	F_3	g32_R	$\frac{F_2}{F_3}$
				g21_R	$\frac{F_1}{F_2}$
				g31_R	$\frac{F_1}{F_3}$
				g31_C	$\frac{F_1}{F_3}$

4. Design Example and Simulation Results

4.1. Design Example

For further illustration, a design example is discussed here. The proposed method is applied to a fourth-order SDM. The presented Simulink-based toolbox was used to perform the simulations and the scaling required. Figure 8 shows the simplified diagram of the design example. Figure 9 shows the detailed equivalent circuit diagram. It is a fourth-order continuous-time low-pass sigma-delta modulator with both feedforward coefficients and feedback current DACs. There are four integrators. Each of the first and the second integrators is an opamp-based RC integrator having a capacitor in the feedback network, and its output equation can be defined as mentioned in (2). The third integrator is an opamp-based RC integrator with a resistor parallel to the capacitor in the feedback network, and its output can be defined as mentioned before in (6). The fourth integrator is an opamp-based RC integrator having a series resistor with the capacitor in the feedback network, and its output can be defined as mentioned before in (4). Two types of coefficients are used: the resistive-type and the capacitive-type. There are two resistive-type resonators as well. A multi-bit quantizer is used (4 bits) in this modulator. A delay (0.5 Ts) is included after the quantizer to model the delay of the D-latch that follows the quantizer. The used oversampling ratio (OSR) is 16. Table 7 shows the values of the coefficients of the design example before performing the scaling.

Table 7. Values of the coefficients for the design example before scaling.

Coeff.	Value	Coeff.	Value	Coeff.	Value
k12_R	0.802	a1	−0.356	k13_R	0.129
k23_R	0.333	a2	−1.158	k25_R	0.155
k34_R	0.81	a3	−1.403	k12_C	0.2
k45_R	0.444	a4	−2.04	k13_C	0.129
b1_R	0.7	a5	−0.58	k23_C	0.0737
b3_R	0.45	g21_R	−0.0377	TP_3	50/Fs
		g43_R	−0.0062	XP_4	0.1

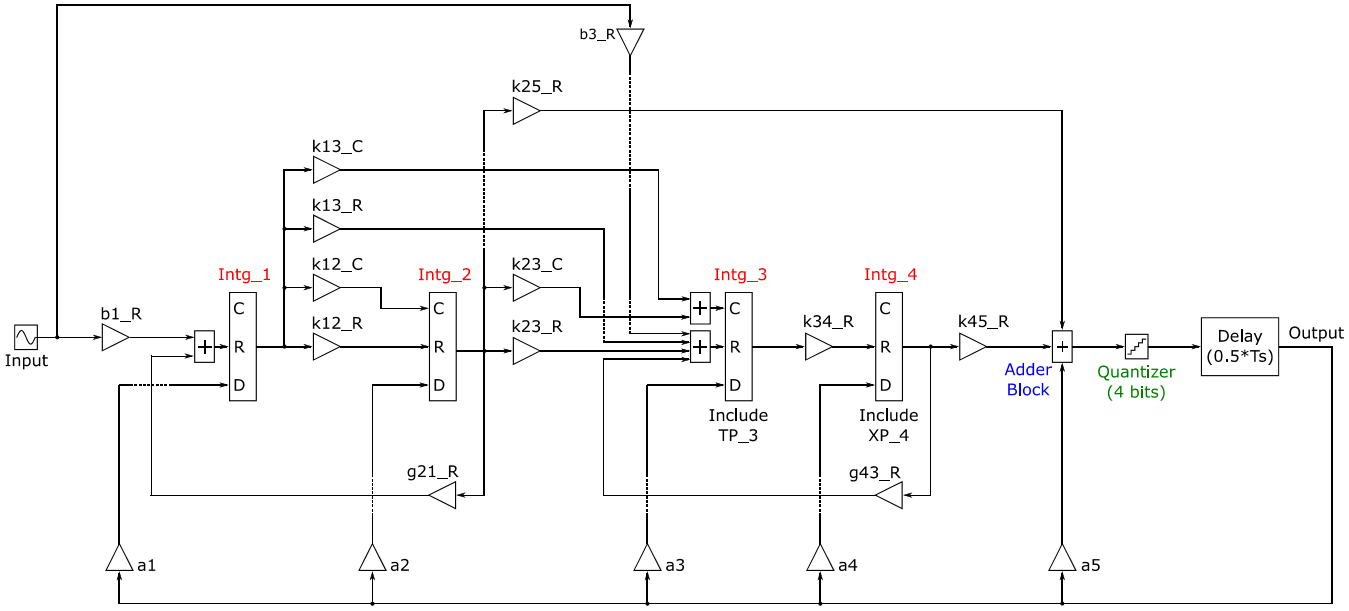

Figure 8. Simplified diagram of the design example.

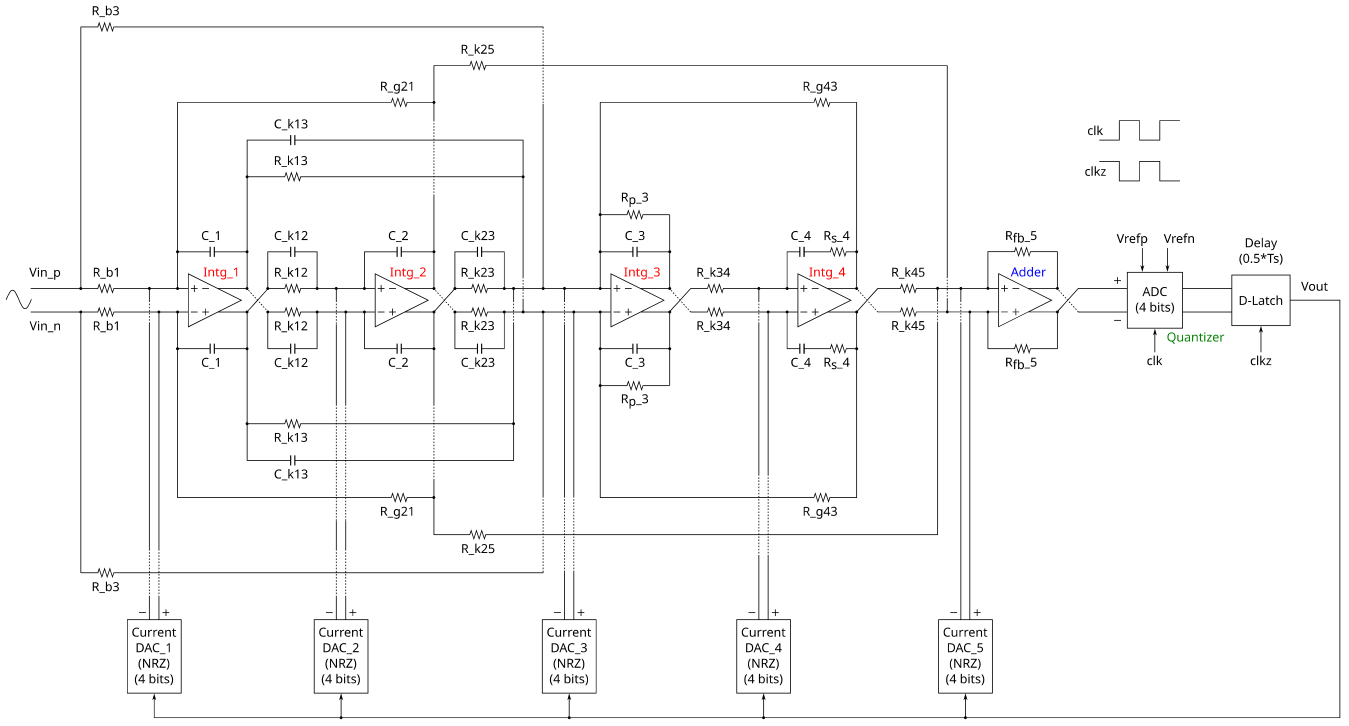

Figure 9. Detailed equivalent circuit diagram for the design example.

4.2. Simulation Conditions and Observing the Swings

To simulate the SDM, an input signal whose amplitude equals 70% of the full scale is used for testing. Table 8 shows the normalized signals swings (i.e., normalized over the full-scale limit) in the SDM before performing any scaling. It is clear that the output swings of the integrators need to be scaled. It can also be noticed that the signal swing at the input of the quantizer needs to be adjusted.

Table 8. Normalized signal swings in the SDM before scaling.

Signal	Normalized Swing	Signal	Normalized Swing
Integrator 1 output	1.6	Integrator 4 output	3
Integrator 2 output	3.4	Quantizer input	1.25
Integrator 3 output	2.95		

4.3. Applying the Proposed Scaling Method

Applying the proposed systematic method to this fourth-order design example, the scaling factor of each coefficient in the SDM can be deduced as shown in Table 9, wherein (F_1), (F_2), (F_3), (F_4) are the scaling factors of the first integrator output swing, the second integrator output swing, the third integrator output swing, and the fourth integrator output swing, respectively. The term (F_q) is the factor used for adjusting the quantizer input signal swing.

Table 9. Scaling factor for each SDM coefficient in the design example.

Coeff.	Scaling Factor	Coeff.	Scaling Factor	Coeff.	Scaling Factor
k12_R	$\frac{F_2}{F_1}$	a1	$\frac{F_1}{F_q}$	k13_R	$\frac{F_3}{F_1}$
k23_R	$\frac{F_3}{F_2}$	a2	$\frac{F_2}{F_q}$	k25_R	$\frac{F_q}{F_2}$
k34_R	$\frac{F_4}{F_3}$	a3	$\frac{F_3}{F_q}$	k12_C	$\frac{F_2}{F_1}$
k45_R	$\frac{F_q}{F_4}$	a4	$\frac{F_4}{F_q}$	k13_C	$\frac{F_3}{F_1}$
b1_R	F_1	a5	$\frac{F_q}{F_q} = 1$	k23_C	$\frac{F_3}{F_2}$
b3_R	F_3	g21_R	$\frac{F_1}{F_2}$	g43_R	$\frac{F_3}{F_4}$

4.4. Simulations and Verification of Swing Scaling

The verification of the swing scaling is divided into three parts. In the first part of the verification, the scaling of the output swings of the integrators is verified alone without adjusting the signal swing at the input of the quantizer. In the second part of the verification, adjusting the signal swing at the input of the quantizer is verified alone, without scaling the output swings of the integrators. In the third part of the verification, the two concepts are verified together. These concepts are scaling the output swings of the integrators and adjusting the signal swing at the input of the quantizer.

Table 10 shows the normalized signal swings before scaling for the original SDM, the scaling factors used for each block, and the normalized swings after the scaling in each part of the verification.

Table 10. Summary of the verification of swing scaling.

	Original SDM	First Part of Verification		Second Part of Verification		Third Part of Verification	
Signal	Normalized Swing before Scaling	Scaling Factor	Normalized Swing after Scaling	Scaling Factor	Normalized Swing after Scaling	Scaling Factor	Normalized Swing after Scaling
Integrator 1 output	1.6	$F_1 = 0.5$	0.8	$F_1 = 1$	1.62	$F_1 = 0.5$	0.81
Integrator 2 output	3.4	$F_2 = 0.25$	0.85	$F_2 = 1$	3.42	$F_2 = 0.25$	0.855
Integrator 3 output	2.95	$F_3 = 0.25$	0.74	$F_3 = 1$	2.98	$F_3 = 0.25$	0.745
Integrator 4 output	3	$F_4 = 0.25$	0.75	$F_4 = 1$	3.11	$F_4 = 0.25$	0.78
Quantizer input	1.25	$F_q = 1$	1.25	$F_q = 0.7$	0.93	$F_q = 0.7$	0.93

Figure 10 shows the spectrum of the output of the modulator before and after the scaling in the first part of the verification. It is clear that the spectrum is identical in the two cases. Comparing the SNDR before and after the scaling in this part, it remains around 89.5 dB. This means that the STF and NTF remain unchanged.

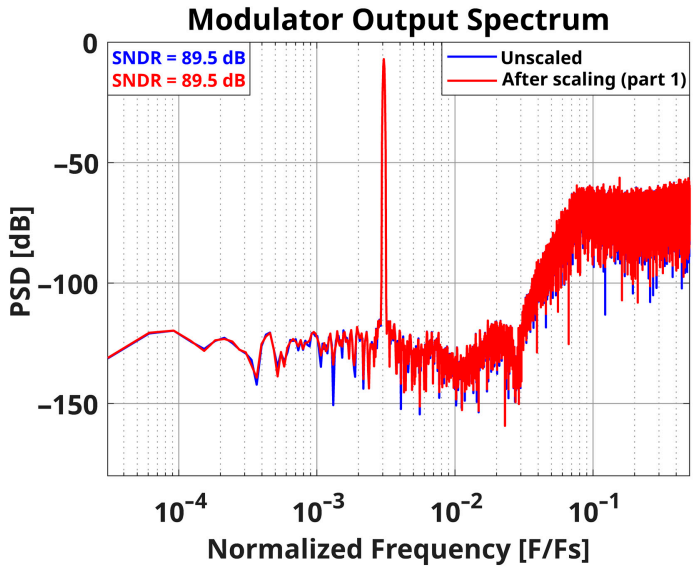

Figure 10. Modulator output spectrum in the first part of verification.

Figure 11 shows the spectrum of the output of the modulator before and after the scaling in the second part of the verification. Figure 12 shows the spectrum of the output of the modulator before and after doing the scaling in the third part of the verification. From these two parts, it is clear that the spectrum after scaling is identical to the unscaled version except that the magnitude of the signal itself is decreased. Since the signal swing at the input of the quantizer is scaled by 0.7 (−3 dB) (using $F_q = 0.7$), the STF magnitude is scaled by the same value. As a result, the signal magnitude will decrease by 3 dB, which means that the SNDR will degrade by 3 dB. Comparing the SNDR before and after performing the scaling, the SNDR equals 86.5 dB after scaling in the second and in the third part of the verification, whereas it was 89.5 dB before scaling. This agrees with the deduced Equations (18) and (19).

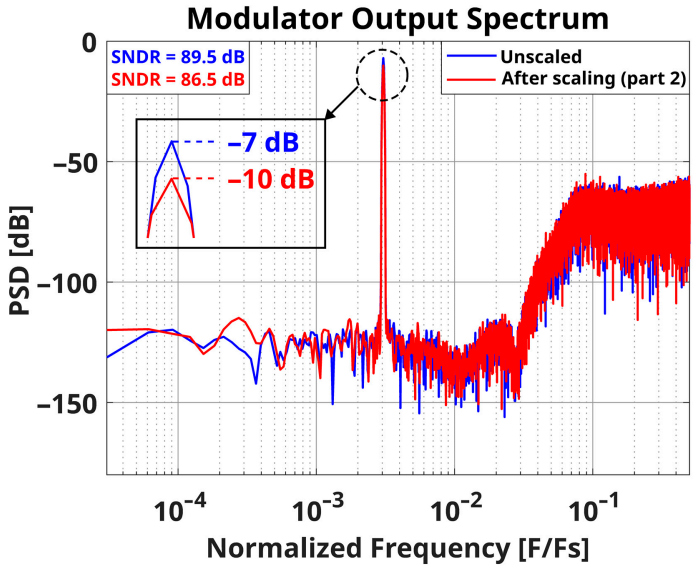

Figure 11. Modulator output spectrum in the second part of verification.

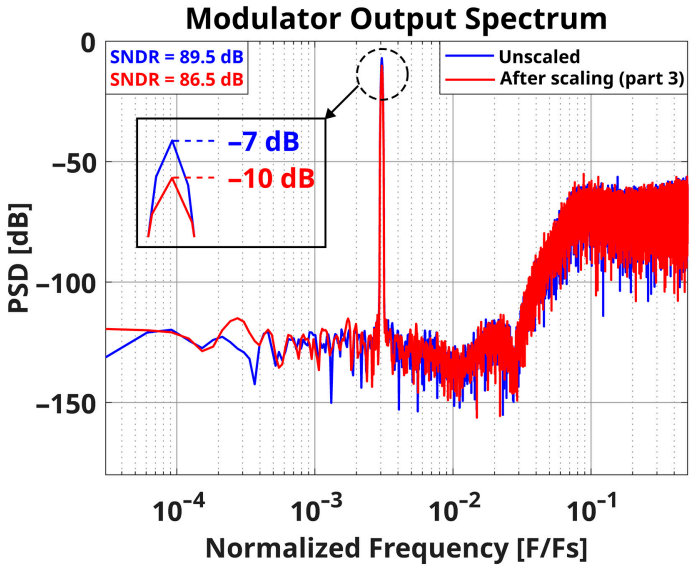

Figure 12. Modulator output spectrum in the third part of verification.

4.5. Simulations and Verification of Integrator Non-linearity

In SDM, the first integrator is the most critical block for linearity, whereas the other following integrators are less critical. This is because any error due to the non-linearity of the second, third, and fourth integrators is divided by the gain of the previous stages when referring to the input, making it negligible compared to the error resulting from the first integrator.

In this part of the verification, the non-linearity effect of the first integrator is shown. Different values (0.3, 0.4, 0.5, 0.6) of the non-linearity coefficient (α) of the first integrator are simulated twice. The first simulation is performed using (F_1 = 0.25), and the second simulation is performed using (F_1 = 0.5). The values of (F_2), (F_3), (F_4), and (F_q) are kept at 0.25, 0.25, 0.25, and 0.7, respectively, during the two tests.

Figure 13 shows the SNDR of the SDM versus the non-linearity coefficient (α) of the first integrator. The tradeoff between the non-linearity of the first integrator and its output swing is shown. It can be concluded that as the output swing of the integrator becomes smaller (F_1 becomes smaller), the SNDR is better for the same value of the non-linearity coefficient (α).

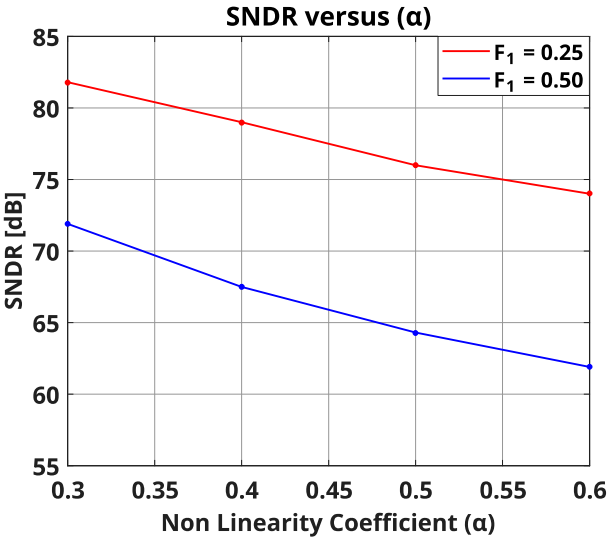

Figure 13. SNDR versus the non-linearity coefficient (α) of the first integrator.

5. Conclusions

This paper presents a systematic method for scaling the signal swings in the low-pass continuous-time sigma-delta modulator. This method overcomes the limitations mentioned in the previous reported methods. Moreover, a MATLAB and Simulink-based toolbox has been included in this work. The toolbox can be easily used to simulate the continuous-time sigma-delta modulators and to scale the signal swings. The analysis of the proposed method was discussed in detail. Furthermore, a design example was discussed for illustration, and the toolbox simulation results were presented.

In summary, Table 11 shows a comparison between this work and the previously published research.

Table 11. Comparison between this work and the previously published research.

Point of Comparison	[5]	[6]	[7]	[30]	This Work
SDM architecture	Either feedforward or feedback	Either feedforward or feedback	Feedback	Either feedforward or feedback	Generic architecture (all possible combinations of coefficients are included)
R feedforward coeff.	Yes	Yes	No	Yes	Yes
C feedforward coeff.	No	No	No	No	Yes
R input feedforward coeff.	No	No	No	Yes	Yes
C input feedforward coeff.	No	No	No	No	Yes
R resonator	Yes	Yes	No	Yes	Yes
C resonator	No	No	No	No	Yes
Integrator model	(1/S)	(1/S)	(1/S)	(1/S)	Multiple models
Includes adder block	Yes	Yes	No	Yes	Yes
Includes scaling of the quantizer input	No	No	No	No	Yes
Includes toolbox for the process automation	No	No	No	Yes	Yes

Author Contributions: Conceptualization, B.M.Z.; Methodology, B.M.Z.; Validation, B.M.Z.; Formal analysis, B.M.Z.; Investigation, B.M.Z.; Resources, B.M.Z.; Writing—original draft, B.M.Z. and M.A.H.; Writing—review and editing, B.M.Z. and M.A.H.; Visualization, M.A.H.; Supervision, H.A.O. and H.A.E. All authors have read and agreed to the published version of the manuscript.

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