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Effects of Annealing Temperature on Bias Temperature Stress Stabilities of Bottom-Gate Coplanar In-Ga-Zn-O Thin-Film Transistors

Yuyun Chen [1], Yi Shen [1,*], Yuanming Chen [1], Guodong Xu [1], Yudong Liu [1] and Rui Huang [2,*]

[1] Guangdong Provincial Key Laboratory of Automotive Display and Touch Technologies, Shantou Goworld Display Technology Co., Ltd.,12 Longjiang Rd., Shantou 515065, China; yyunchen@goworld-lcd.com (Y.C.); ymchen@goworld-lcd.com (Y.C.); guodxu@goworld-lcd.com (G.X.); ydliu@goworld-lcd.com (Y.L.)
[2] School of Materials Science and Engineering, Hanshan Normal University, Chaozhou 521041, China
* Correspondence: yishen@goworld-lcd.com (Y.S.); rhuang@hstc.edu.cn (R.H.)

Abstract: Defect annihilation of the IGZO/SiO_2 layer is of great importance to enhancing the bias stress stabilities of bottom-gate coplanar thin-film transistors (TFTs). The effects of annealing temperatures (T_a) on the structure of the IGZO/SiO_2 layer and the stabilities of coplanar IGZO TFTs were investigated in this work. An atomic depth profile showed that the IGZO/SiO_2 layer included an IGZO layer, an IGZO/SiO_2 interfacial mixing layer, and a SiO_2 layer. Higher T_a had only one effect on the IGZO layer and SiO_2 layer (i.e., strengthening chemical bonds), while it had complex effects on the interfacial mixing layer—including weakening M-O bonds (M: metallic elements in IGZO), strengthening damaged Si-O bonds, and increasing O-related defects (e.g., H_2O). At higher T_a, IGZO TFTs exhibited enhanced positive bias temperature stress (PBTS) stabilities but decreased negative bias temperature stress (NBTS) stabilities. The enhanced PBTS stabilities were correlated with decreased electron traps due to the stronger Si-O bonds near the interfacial layer. The decreased NBTS stabilities were related to increased electron de-trapping from donor-like defects (e.g., weak M-O bonds and H_2O) in the interfacial layer. Our results suggest that although higher T_a annihilated the structural damage at the interface from ion bombardment, it introduced undesirable defects. Therefore, to comprehensively improve electrical stabilities, controlling defect generation (e.g., by using a mild sputtering condition of source/drain electrodes and oxides) was more important than enhancing defect annihilation (e.g., through increasing T_a).

Keywords: annealing temperature; In-Ga-Zn-O; thin-film transistors; depth profile; X-ray photoelectron spectroscopy; bias temperature stress stabilities; interfacial mixing layer

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1. Introduction

Indium-gallium-zinc oxide (IGZO) thin-film transistors (TFTs) are quite popular in the display field, due to their high mobility and transparency, large-area uniformity, and low-temperature processability [1–3]. Positive bias temperature stress (PBTS) and negative bias temperature stress (NBTS) stabilities determine the on-state and off-state stabilities of IGZO TFTs, respectively, both of which are key issues for applications [4,5]. In order to enhance the electrical stabilities and maintain the uniformity of amorphous IGZO TFTs, the active layers require annealing at a temperature that is higher than the deposition temperature (room temperature in most cases) but lower than the crystallization temperature (i.e., ~600 °C) [6–8]. Although the effects of annealing temperatures (T_a) on the IGZO films or the transfer characteristics of the as-fabricated IGZO TFTs have been studied [6,9–16], limited attention has been paid to their PBTS and NBTS stabilities, which are more important technical indicators. The structural origin (generally at the atomic scale) for the effects of T_a on bias stress stabilities has not been fully investigated.

Configurations of IGZO TFTs primarily involve a top-gate staggered structure, a bottom-gate staggered structure, a top-gate coplanar structure, and a bottom-gate coplanar structure [3]. Among these configurations, bottom-gate structures are commonly used for prototype displays since the gate metals at the bottom enable to blocking of the backlights. Compared with the staggered structure, the coplanar structure has some advantages such as simpler fabrication methods, lower contact resistances with source and drain electrodes, and smaller stray capacitances. Nevertheless, extra defects may be introduced at the interface between the active layer and the insulator of coplanar TFT during deposition and patterning of source/drain layers, which would affect the successive deposition of the active layer and result in poor electrical stabilities. Controlling the post-treatment temperature is important for coplanar TFTs to achieve a high-quality interface and active layer structure and enhance electrical stabilities.

In this work, the bottom-gate coplanar TFTs with IGZO films annealed at different T_a were prepared and their bias temperature stress stabilities were compared. The atomic structures of IGZO/dielectric layers were examined to understand the structural origin since the electrical instabilities were closely related to de-trapping or trapping of charged particles near or at the IGZO/dielectric interface [5,17–20]. Considering that multiple elements are irregularly involved within IGZO/dielectric layers, depth profiling was performed by X-ray photoelectron spectroscopy (XPS) for a detailed structural analysis.

2. Method

The bottom-gate coplanar IGZO TFTs were prepared using the following steps: 100 nm Mo, 200 nm SiO_2, and 100 nm Mo were deposited on the glass substrates successively, which were the gate electrode, insulation dielectric, and source/drain electrode of the oxide TFTs. After magnetron sputtering deposition, each of the above layers was patterned using wet-etching methods. Then the active films were deposited by mid-frequency (MF) magnetron sputtering of the IGZO targets (In_2O_3: Ga_2O_3: ZnO = 1:1:2 mol%). The IGZO films were annealed in air at different temperatures (T_a = 300 °C and 400 °C) for one hour and wet etched for the desired channel size (10 μm in length and 50 μm in width). Here, T_a below 250 °C was not considered, because it was found that the IGZO layer was not sufficiently oxidized at 250 °C and it was difficult to turn the TFTs off. T_a over 400 °C was not considered either since Mo was slightly oxidized at 400 °C and their conductivity may be more or less reduced. At last, 1 μm polymethyl methacrylate (PMMA) passivation layers were coated and patterned to expose the gate, source, and drain electrodes.

A P100 Source Meter was used to measure the transfer characteristics of our IGZO TFTs. During the drain current (I_{DS}) measurement, the gate voltage (V_{GS}) varied from −10 V to +20 V and the drain-source voltage (V_{DS}) was maintained at 10.1 V. Based on the I_{DS}-V_{GS} transfer curves, we extracted some electrical parameters, including saturation mobility μ, subthreshold swing SS, the ratio of on-state to off-state current I_{on}/I_{off}, and the threshold voltage V_{th}. The SS was calculated from the reciprocal of the maximum slope in the log (I_{DS})-V_{GS} transfer curves. The μ and V_{th} were calculated by linear extrapolation of the $I_{DS}^{1/2}$-V_{GS} transfer curves [21,22].

The electrical stabilities of IGZO TFTs were evaluated using positive bias temperature stress (PBTS) and negative bias temperature stress (NBTS) tests. During PBTS tests, V_{GS}, V_{DS}, and environmental temperature (T) were maintained at +20 V, 0.1 V, and 60 °C, respectively. During NBTS tests, V_{GS}, V_{DS}, and T were set at −20 V, 0.1 V, and 60 °C, respectively.

The depth profile of IGZO/SiO_2 layers was collated using scanning X-ray photoelectron spectroscopy (XPS) (PHI 5000 V Versa Probe III, Chigasaki, Japan) with a monochromatic Al Kα X-ray source (1486.6 eV, 50 W, 15 kV). To control/minimize the charge building, a conductive mask was used to provide a conducting pathway and charge neutralization facilities of XPS instruments were applied. When the XPS spectra were collected, the base vacuum of the testing chamber was kept at 6.9×10^{-8} Pa. The broad survey spectra were collected for the original surface, which included C1s signals. Then, the depth profiles

were further collected after every 0.5 min Ar^+ sputtering. The energy and area of the Ar^+ beam were set at 2 keV and 3 mm × 3 mm, respectively. The profiles of element contents (including carbon, oxygen, gallium, zinc, and indium) were obtained from these spectra. The C1s region showed that the carbon contamination was sufficiently removed after the first 0.5 min of sputtering. C1s at 284.8 eV for carbon on the surface were chosen for calibration. The core-level spectra were fitted using the Gaussian/Lorentzian function with Shirley-type background subtraction. The IGZO layers were also characterized using scanning electron spectroscopy (Gemini 450, Zeiss, Cambridge, UK).

3. Results

3.1. XPS Characterization

In-depth photoelectron spectra in the range of 150~170 eV for IGZO/SiO_2 samples annealed at different temperatures (T_a) are given in Figure 1. With increasing depth from the IGZO surface, variations in the photoelectron spectra can be divided into three stages. First, only one component centered at ~161.0 eV was observed in the spectra, the position of which agreed with that of the Ga3s component for the Ga_2O_3 reference samples [23]. This component can be attributed to the Ga-O bonds within the IGZO layer. The position as well as line shapes of the spectra at the first stage were almost unchanged (see the green spectra in Figure 1), indicating a uniform IGZO layer. Second, the Ga3s component shifted towards a lower binding energy (BE) side and an additional component at ~153.0 eV appeared. BE of the latter component was close to that of the Si2s component of SiO_2 [24]. Such double-peak spectra suggest an IGZO-SiO_2 interfacial mixing layer, the thickness of which was ~15 ± 2 nm. The interfacial mixing layer can be seen as the result of the implantation of atoms from the oxide target into the SiO_2 surface. Third, there was only one Si2s component in the following spectra, which can be attributed to the signal from a SiO_2 layer. The above variations indicate that the film structure of IGZO/SiO_2 includes three parts: an IGZO layer, an IGZO/SiO_2 interfacial mixing layer, and a SiO_2 layer. The effects of T_a on the atomic structures of these three parts were further investigated.

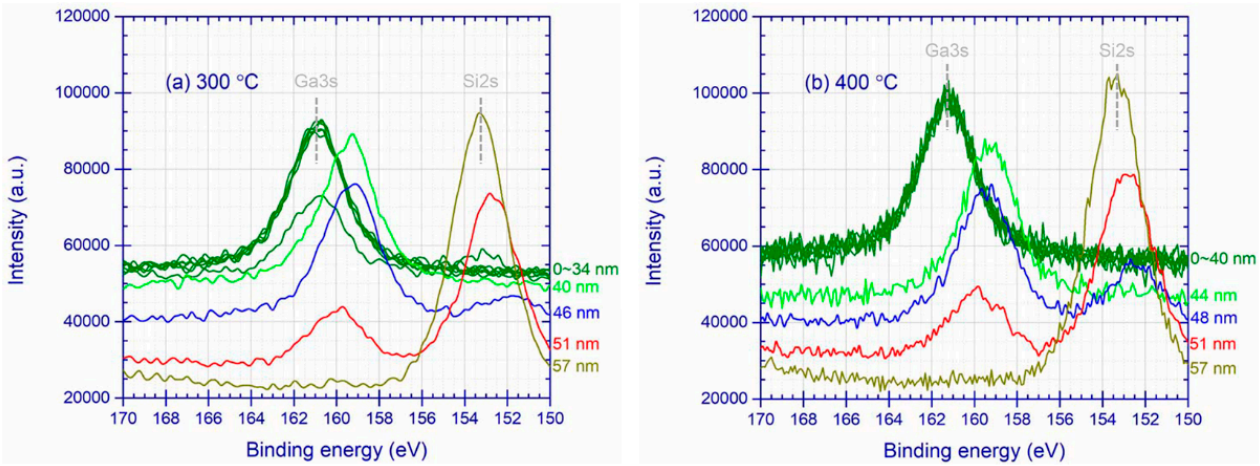

Figure 1. In-depth photoelectron spectra in the range of 150~170 eV for IGZO/SiO_2 samples annealed at 300 °C (**a**) and 400 °C (**b**).

3.1.1. IGZO Layer

Figure 2 displays core-level spectra collected at a depth of ~5 nm from the surface to exemplify the uniform structure of the IGZO layer. In Figure 2a–c, there were symmetric components centered at ~161.0 ± 0.1 eV, ~1022.15 ± 0.15 eV, and ~445.05 ± 0.15 eV, which were in agreement with those of the Ga3s, Zn2p, and In3d components of Ga_2O_3, ZnO, and In_2O_3 reference samples, respectively [23,25,26]. These components arose from Ga-O, Zn-O, and In-O bonds in the IGZO layer. The fitting spectra, which were generated from a one-component model, agreed well with the experimental spectra in Figure 2a–c. The

fitting results (see in Table 1) showed that at higher T_a, the full width of half maximum (FWHM) was nearly unvaried, but the position of these components shifted towards the higher BE side (i.e., +0.3 eV). These phenomena suggest an enhancement in the binding energy of Ga-O, Zn-O, and In-O bonds within the IGZO layer.

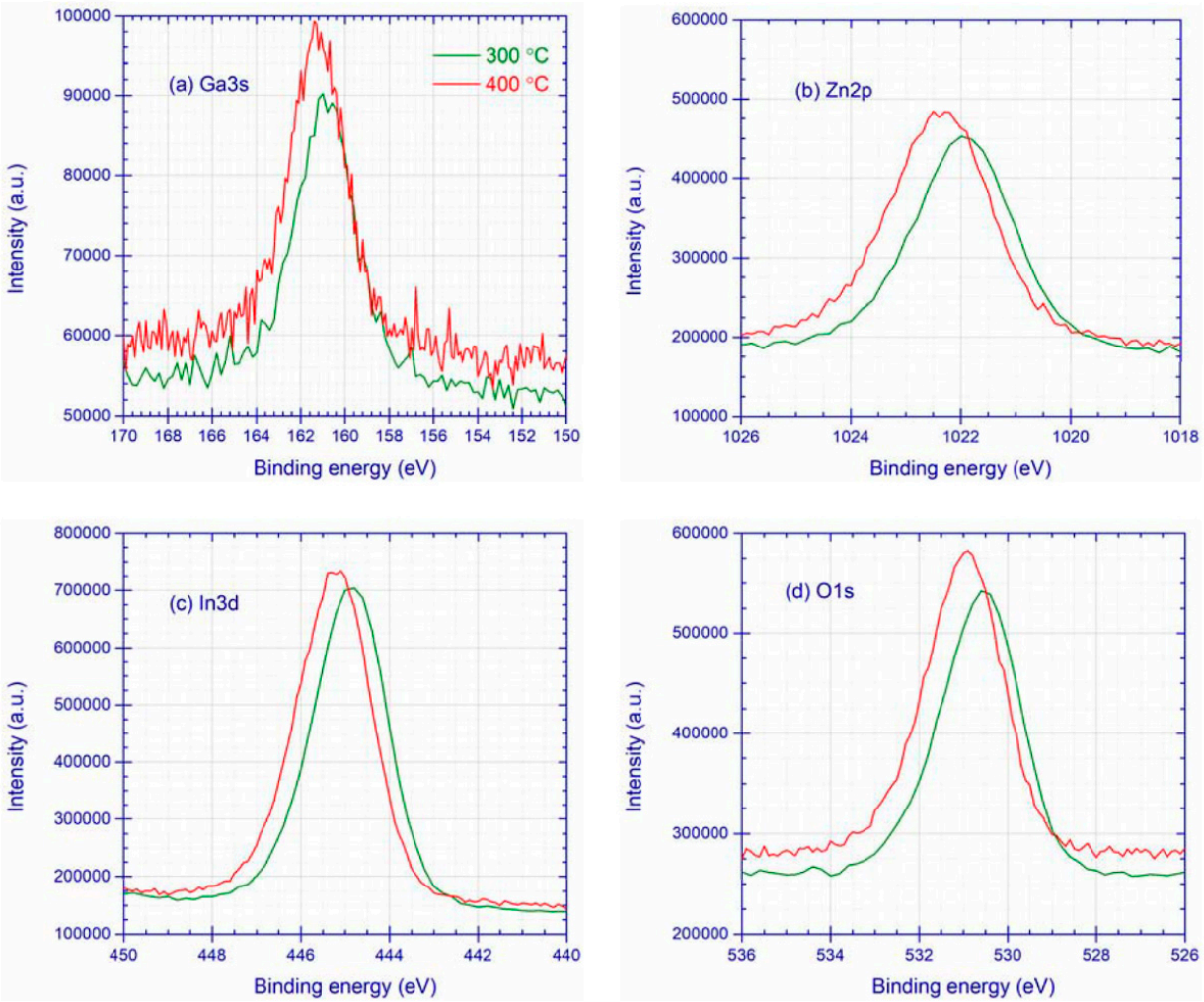

Figure 2. (**a**) Ga3s, (**b**) Zn2p, (**c**) In3d, and (**d**) O1s spectra of the IGZO layer annealed at 300 °C and 400 °C. The spectra were collected at a depth of 5 nm from IGZO surface.

Table 1. Parameters extracted by fitting the core-level spectra in Figure 2.

T_a (°C)	Ga3s		Zn2p		In3d		O1s
	Position (eV)	FWHM (eV)	Position (eV)	FWHM (eV)	Position (eV)	FWHM (eV)	A_{OII} (%)
300	160.9	3.3	1022.0	2.2	444.9	2.0	21
400	161.2	3.3	1022.3	2.2	445.2	2.0	21

In Figure 2d, asymmetric O1s spectra consist of one major component (O_I) at ~530.9 ± 0.4 eV and a sub-component (O_{II}) on the high-BE side. Generally, O_I and O_{II} components were considered to be the result of M-O (M represents the metallic elements in IGZO) bonds and oxygen vacancies, respectively [27–29]. However, Idriss believes that a signal arising from an oxygen vacancy is impossible, based on the following reasons [30]. First, it is unreasonable in principle that photoelectron spectroscopy enables one to measure the kinetic energy of a missing electron. Second, the surface oxygen vacancies would

be oxidized instantaneously in an ambient environment due to the strong adsorption energy of H_2O, and thus ex situ measurements of oxygen vacancies were impossible. The sub-component in O1s spectra for metallic oxides is thus attributed to some structural imperfections containing oxygen atoms, such as hydroxyls, water molecules, and organic contaminants [30,31]. In our case, the correlation between the sub-component and organic contaminants was excluded since there were no C1s signals for the spectra collected from the IGZO layer. Fitting spectra generated from a double-component model agreed well with the experimental O1s spectra, and the area ratio of the O_{II} component (A_{OII}%) was calculated. It was found that A_{OII}% for the IGZO layer was not sensitive to T_a, suggesting that comparable O-related imperfections were introduced into the IGZO layer at both T_a.

3.1.2. IGZO-SiO_2 Interfacial Mixing Layer

The atomic structures of the IGZO-SiO_2 interfacial mixing layer were further studied. In Figure 3a–c, the Ga3s, Zn2p, and In3d components at 159.90 ± 0.01 eV, 1021.35 ± 0.05 eV, and 444.1 ± 0.1 eV, respectively, were observed in the core-level spectra of the interfacial mixing layer annealed at both T_a. Compared with those for the IGZO layer, the BE of these components for the interfacial mixing layer (Table 2) was relatively lower. Additionally, full width of half maximum (FWHM) values of the Zn2p and In3d components for the interfacial layer (Table 2) were larger than those for the IGZO layer. These differences indicate that the M-O chemical bonds in the interfacial mixing layer were weaker and more disordered than those in the IGZO layer. At higher T_a, the Ga3s and Zn2p components were almost unvaried, but the In3d component shifted evidently towards the low-BE side (−0.1 eV). These results suggest that Ga-O and Zn-O bonds became somewhat weaker while the In-O bonds turned out to be apparently weakened at higher T_a. This phenomenon can be interpreted in terms of their bond energy, which led to distinct thermal stabilities. The In-O bonds exhibit a relatively lower bond energy and thus are more thermally unstable compared with Ga-O and Zn-O bonds [32,33]. Unlike those in the mixing layer, the In-O bonds within the IGZO layer were enhanced at higher T_a (Figure 2a–c). This distinction can be understood in terms of the dual role of T_a in the atomic structures. The annealing of amorphous semi-conductive oxides (i.e., heat treatment at temperatures below the crystallization temperature) is generally considered a defect in the annihilation process. Under these circumstances, more point defects will be annealed out at elevated temperatures due to their enhanced atomic mobility [34,35] or the combination with ambient gas [6,36]. As a result, the electrical stabilities of the oxides were improved. Nevertheless, some experimental evidence shows that semi-conductive oxides become electrically unstable with increasing ambient temperatures [37–39]. These abnormal phenomena revealed that a defect generation process is also involved in the annealing process, which would compete with the annihilation process and lead to an increase in atomic defects. In our case, the In-O bonds in the interfacial mixing layer were weaker than those in the IGZO layer, and thus they would be more easily broken by thermal vibration at higher T_a. Thus, at higher T_a, defect generation arising from breaking chemical bonds may overwhelm defect annihilation due to enhanced atomic mobility, leading to weakened In-O bonds in the interfacial mixing layer.

Table 2. Parameters extracted by fitting the core-level spectra in Figure 3.

T_a (°C)	Ga3s		Zn2p		In3d		Si2s		O1s
	Position (eV)	FWHM (eV)	Position (eV)	FWHM (eV)	Position (eV)	FWHM (eV)	Position (eV)	FWHM (eV)	A_{OII}%(%)
300	159.91	2.8	1021.38	2.5	444.13	2.4	152.5	3.1	20
400	159.89	3.0	1021.35	2.5	444.02	2.5	152.8	3.1	24

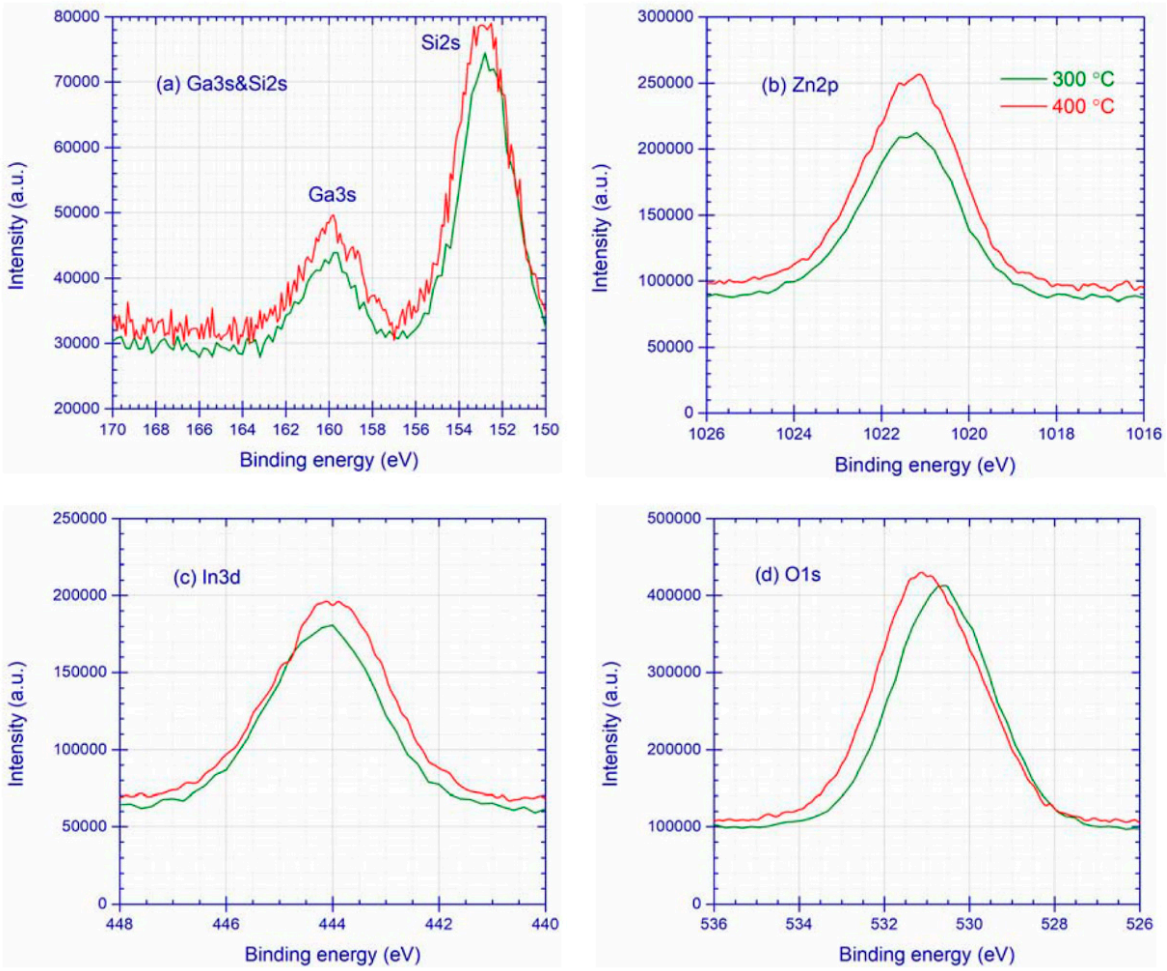

Figure 3. (**a**) Ga3s and Si2s, (**b**) Zn2p, (**c**) In3d, and (**d**) O1s spectra taken from IGZO-SiO_2 interfacial mixing layer annealed at 300 °C and 400 °C.

There was one more component centered at 152.65 ± 0.15 eV in the spectra in the range of 150~170 eV (Figure 3a), which pointed to the Si2s component [24]. The binding energy of this component for the interfacial mixing layer (Table 2) was smaller than that for the SiO_2 layer (as shown in Figure 4a and Table 3), indicating that at the initial growth of IGZO, ion bombardment led to structural damages (for instance, dangling bonds and weak bonds). Although BE of Si2s component for the interfacial layer increased at higher T_a, it was still smaller than that for the SiO_2 layer. These phenomena suggest that although the structural damages at interface resulting from ion bombardment were reduced at higher T_a, they were unable to be totally annihilated.

Table 3. Parameters extracted by fitting the core-level spectra in Figure 4.

T_a (°C)	Si2s		O1s	
	Position (eV)	FWHM (eV)	Position (eV)	FWHM (eV)
300	153.2	3.2	531.5	2.3
400	153.3	3.1	531.6	2.4

In Figure 3d, the O1s spectra at both T_a were asymmetric with a sub-component on the high-BE side. As mentioned above, the sub-component on the high-BE side arises from O-related defects (for example, hydroxyls, water molecules, and organic contaminants). At higher T_a, the intensity of the sub-component increased. The curve-fitting analysis

also showed that the area ratio of the sub-component (A_{OII}%) increased at higher T_a. Both direct observation and indirect analysis showed that higher T_a resulted in more O-related defects in the interfacial mixing layer. Similarly, it has been reported that with an increasing annealing temperature of IGZO, more water molecules were distributed at deeper depths [16,40].

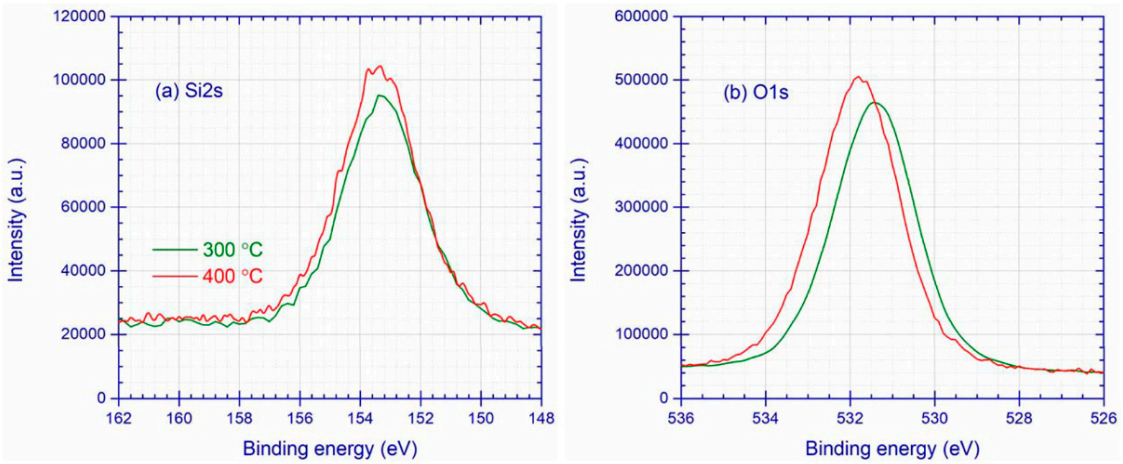

Figure 4. (**a**) Si2s and (**b**) O1s spectra of SiO_2 layer annealed at 300 °C and 400 °C.

3.1.3. SiO_2 Layer

The atomic structures of the SiO_2 layer annealed at different T_a were further studied. Figure 4 presents the Si2s and O1s spectra collected from the SiO_2 layer. At higher T_a, either the Si2p or O1s component shifted towards the high-BE side, indicating stronger Si-O bonds.

It should be noted that the BE values of the Si2s component for our SiO_2 films were lower than those for the SiO_2 bulk (154.7 ± 0.1 eV) [24]. This result was attributed to the atomic disordering within films arising from a far-from-equilibrium sputtering condition.

The above experimental results show the effects of T_a on IGZO/SiO_2 structures and the electrical stabilities of IGZO TFTs. The structural results can be summarized as follows: (1) higher T_a resulted in stronger chemical bonds within the IGZO layer and SiO_2 layers; (2) higher T_a had complex effects on the atomic structure of the IGZO/SiO_2 interfacial mixing layer: stronger Si-O bonds, weaker M-O bonds, and more O-related defects.

3.2. SEM Characterization

Figure 5 displays the surface morphology of IGZO layers annealed at different T_a. IGZO layers annealed at both T_a were columnar structures and their columnar widths were comparable (35 ± 5 nm). This result suggests that annealing temperatures over 300~400 °C had no effect on the surface morphology of IGZO layers.

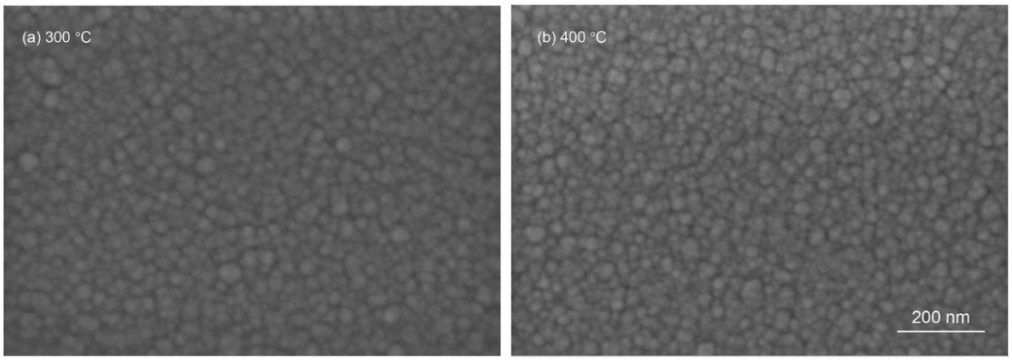

Figure 5. Surface morphology of IGZO annealed at (**a**) 300 °C and (**b**) 400 °C.

3.3. Bias Stress Stabilities

3.3.1. Transfer Characteristics

The transfer characteristics of as-fabricated TFTs with IGZO annealed at different T_a were compared (see the green curves in Figure 6). First, at higher T_a, the transfer curves shifted negatively, indicating a negative shift in the threshold voltage (V_{th}). Actually, many researchers have observed more negative V_{th} for as-fabricated TFTs with IGZO annealed at higher temperatures [6,9,11,12,14,41]. Such a negatively shifted V_{th} at higher T_a was related to the decreased resistance of our IGZO films (R). The R-value of the IGZO annealed at 400 °C (4.1×10^5 Ω) was at least two orders of magnitude less than that of the IGZO annealed at 300 °C (>4×10^7 Ω). The decreased resistance was attributed to the increased carrier concentration because the saturation mobilities of our TFTs with IGZO annealed at different T_a were similar (as listed in Table 4). Second, the slope in the linear region of the transfer curves in the higher-T_a case increased, which suggests a lower subthreshold swing (SS). As suggested for amorphous silicon thin-film transistors, the interfacial trap density (N_{SS}^{Max}) can be estimated from SS by the following equation:

$$N_{SS}^{Max} = \left(\frac{SSlog(e)}{kT/q} - 1 \right) \frac{C_{ox}}{q} \quad (1)$$

where k is the Boltzmann constant, q is the electron charge, T is the temperature, and C_{ox} is the insulator capacitance per unit area [42,43]. Given the fact that the C_{ox} of our SiO_2 dielectric was 2.4×10^{-8} F/cm^2, the N_{ss}^{Max} of our TFTs decreased from 1~2×10^{12}/cm^2 to ~8×10^{11}/cm^2 when T_a increased from 300 °C to 400 °C.

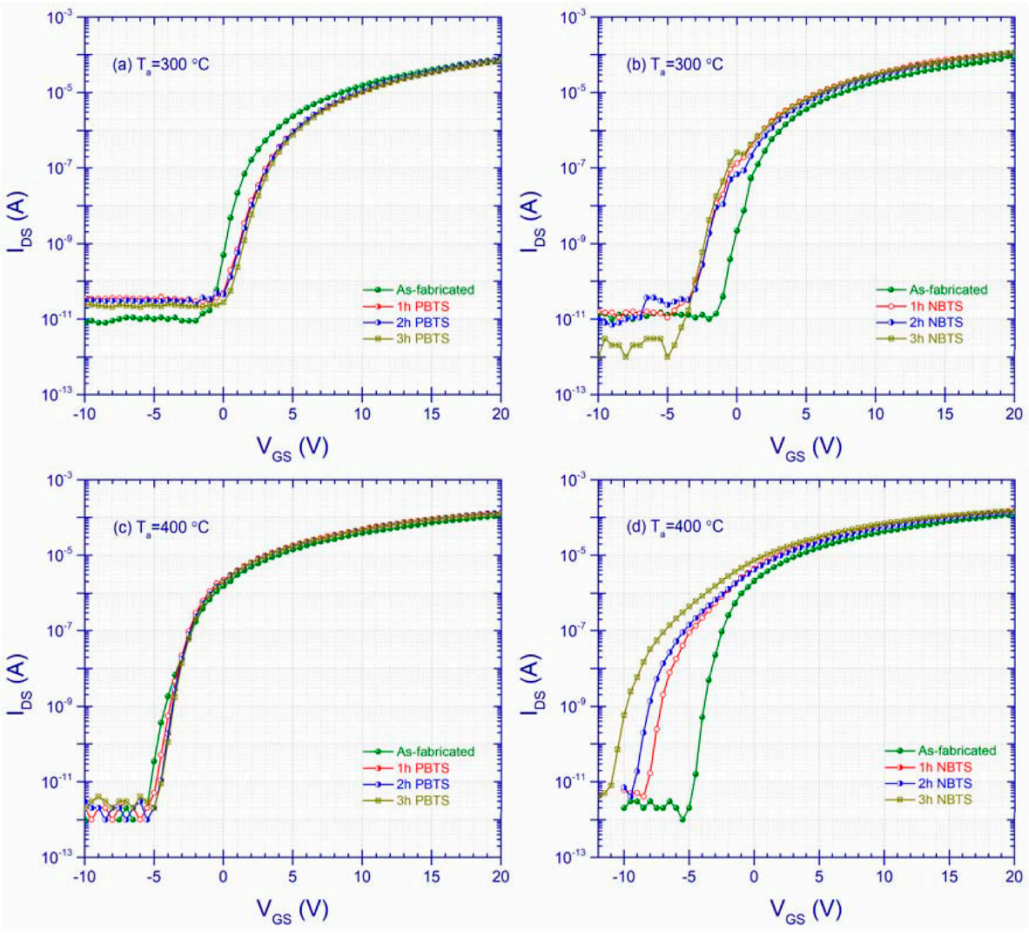

Figure 6. Transfer characteristic curves of the TFTs with IGZO annealed at 300 °C and 400 °C during 3h positive bias temperature stress (PBTS) and negative bias temperature stress (NBTS) (**a**–**d**).

Table 4. The electrical parameters (including mobility μ, subthreshold swing SS, I_{on} and I_{off} ratio I_{on}/I_{off}, threshold voltage V_{th}, and V_{th} shift ΔV_{th}) extracted from the transfer curves in Figure 5.

T_a (°C)	State	μ (cm^2/Vs)	SS (V/dec)	I_{on}/I_{off}	V_{th} (V)	ΔV_{th} (V)
300	As-fabricated	95	0.77	7.6×10^6	1.7	+1.5
	3h PBTS	103	0.72	2.5×10^6	3.2	
400	As-fabricated	93	0.44	3.7×10^7	−3.2	0.0
	3h PBTS	105	0.44	4.2×10^7	−3.2	
300	As-fabricated	103	0.57	8.4×10^6	1.3	−1.9
	3h NBTS	124	0.63	5.6×10^7	−0.6	
400	As-fabricated	95	0.40	6.0×10^7	−2.5	−4.5
	3h NBTS	102	0.54	3.0×10^7	−7.0	

3.3.2. Positive Bias Temperature Stress (PBTS) Stabilities

PBTS stabilities of TFTs with IGZO annealed at 300 °C to 400 °C were further studied. The TFT with IGZO annealed at 300 °C exhibited a positive V_{th} shift (+1.3 V) without any change in SS after 1h PBTS, and then turned out to be stable after 2 h or 3 h of PBTS (Figure 6a). The amplitude of such a ΔV_{th} was smaller than those of the reported oxide TFTs under the same PBTS conditions (Table 5). The positively shifted V_{th} under PBTS is primarily attributed to the electron trapping near or at the semiconductor/insulator (S/I) interface, without generating a new state [17–19]. However, neither position nor shape was varied after PBTS for the TFT with IGZO annealed at 400 °C (Figure 6c), indicating improved PBTS stabilities. Given the fact that the carrier concentration increased at higher T (as discussed in Section 3.3.1), the increased PBTS stabilities correlated with the reduced interface trap (as evident by the smaller SS), which lessened the effects of electron trapping near or at the IGZO/SiO_2 interface.

As revealed by XPS analysis, the improved structural features near/at the IGZO/SiO_2 interface involved stronger Si-O bonds in the interfacial mixing layer. Cho et al. observed that oxide TFT, with stronger Si-O bonds on the insulation surface, exhibited smaller ΔV_{th} under PBTS [44]. In this sense, the reduced interfacial traps, resulting in the enhanced PBTS stabilities at higher T_a, may be due to the strengthened Si-O bonds near/at the interface.

3.3.3. Negative Bias Temperature Stress (NBTS) Stabilities

The effects of T_a on NBTS stabilities were somewhat different from those on PBTS stabilities. The TFT with IGZO annealed at 300 °C showed a negative V_{th} shift (−2.0 V) after 1 h NBTS and became stable after 2 h or 3 h of NBTS (Figure 6b). The amplitude of this negative ΔV_{th} was in the range of the reported values for oxide TFTs under the same NBTS conditions. However, the TFT with IGZO annealed at 400 °C presented a continuous negative V_{th} shift during NBTS, resulting in a larger V_{th} shift (−4.5 V) after 3 h of NBTS (Figure 6d). In other words, higher T_a slightly increased the NBTS instabilities. Similarly, Chen et al. reported that higher a post-annealing temperature resulted in increased negative bias stress instabilities [10]. Three mechanisms for instabilities under negative bias stress have been proposed: hole trapping at the S/I interface [5], defect generation in active layers [18,19], and electron de-trapping at the S/I interface [17,20]. The first mechanism was not considered because the number of holes in n-type semiconductors was negligible. The second mechanism was unable to explain our experimental results since (i) the defect state in the IGZO would result in degradation in SS and μ, rather than the almost unvaried SS and slightly increased μ (Table 4), and (ii) the XPS results revealed that no extra structural defects were introduced into the IGZO layer at higher T_a (see in Section 3.1.1). Therefore, our increased NBTS instabilities at higher T_a were mainly attributed to the enhanced electron de-trapping near or at the S/I interface. Under negative bias stress, the interfacial donor-like defects released electrons towards the IGZO layer and turned out to be positively charged. The released electrons would be trapped within the IGZO layer and thus are not recovered instantly. In the following bias sweeping, the positively charged donor-

like defects and trapped electrons formed a residual field, leading to enhanced electron accumulation in the front channel, which, in turn, resulted in a negative ΔV_{th}.

Our XPS analysis showed that the increased interfacial defects at higher T_a include weakened M-O bonds and increased O-related defects (e.g., water molecules and hydroxyls). Much experimental evidence has shown that the weakened M-O bonds and water molecules were donor-like in nature, which enables the release of electrons and results in a larger V_{th} shift under negative bias stress [29,45,46]. Therefore, the increased NBTS instabilities can be attributed to the weakened M-O bonds and increased water molecules in the IGZO/SiO_2 interfacial mixing layer.

Table 5. Reference data for the bias temperature stabilities of oxide TFTs. BG and TG represent bottom-gate and top-gate configurations.

Configuration	Active Layer	V_{GS} (V)	Temp (°C)	Time (s)	ΔV_{th} (V)	Reference
Coplanar_BG	IGZO	+20	60	3000	2.5	[47]
Staggered_BG	IGZO	+20	60	3600	0.5	[48]
Staggered_BG	IGZTO	+20	60	7200	1.8	[49]
Staggered_BG	IZO	+20	60	7200	3.0	[50]
Staggered_BG	IZO:Pr	+20	60	7200	2.0	[50]
Coplanar_BG	IGZO	+20	60	10,800	1.3	This work
Staggered_BG	SZTO	−20	60	3600	−2	[51]
Staggered_BG	SZTO	−20	60	3600	−2.73	[52]
Staggered_BG	IGZO	−20	60	3600	−0.5	[48]
Staggered_BG	IGZTO	−20	60	7200	0.5	[49]
Staggered_BG	IZO	−20	60	7200	−0.8	[50]
Staggered_BG	IZO:Pr	−20	60	7200	−0.71	[50]
Staggered_BG	IZO	−20	60	10,800	−3.5	[53]
Staggered_BG	HIZO	−20	60	10,800	−3~−1	[54]
Coplanar_BG	IGZO	−20	60	10,800	−2	This work

4. Discussions

The above experimental results showed that the structural quality of the IGZO/SiO_2 interfacial mixing layer was the key structural factor for the electrical stabilities of bottom-gate coplanar IGZO TFTs. In this part, we discuss how the processing conditions affect this key factor in order to propose the main points for preparing electrically stable semiconductive devices.

For bottom-gate coplanar TFTs, structural imperfections forming from the insulation surface are inevitable during the preparation of source/drain electrodes and the active layer [43,55,56]. To enhance the performance of devices, post-heat treatment (for example, by adjusting T_a) is necessary to reduce these structural defects. Therefore, the structural quality of the oxide/insulator interfacial mixing layer depends on the competition between defect generation from ion bombardment and defect annihilation through heat treatment.

Our study, as well as other reported results [10,13,14,57], showed that unlimited enhancement in post-heat treatment by increasing T_a would result in negative effects on oxide TFTs (such as degraded transfer characteristics and electrical stabilities). Seen in this light, higher T_a would play a negative role in defect generation, rather than the generally considered positive role in defect annihilation, when T_a was increased up to a certain degree. In this work, XPS analysis (as schematically drawn in Figure 7) revealed that at higher T_a, although the damaged Si-O bonds were partially annihilated, the weak M-O bonds were easily broken due to thermal vibration. Moreover, more undesired molecules (e.g., water molecules) from the ambient atmosphere were introduced into the interfacial mixing layer at higher T_a because of the enhanced diffusion length. As a result, the electrical stabilities of IGZO TFTs were not comprehensively improved, i.e., enhanced PBTS stabilities but degraded NBTS stabilities. Thus, unlimitedly enhancing annealing temperatures may not be an effective way to improve the structural quality of the interfacial layer. In this regard, controlling defect generation is more important to achieving a high-quality interfacial layer.

To control defect generation during the sputtering of oxides, a mild sputtering condition of source/drain electrodes and oxides or a bombardment-resistant insulation surface (through densifying the film structure) may be required.

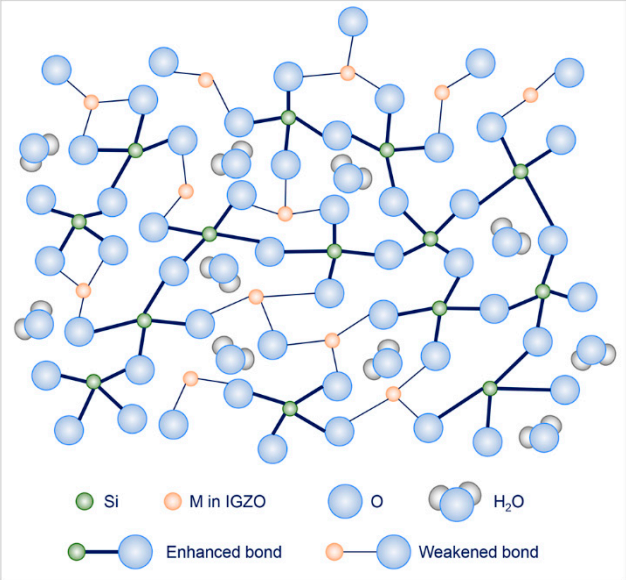

Figure 7. Schematic drawing of dual effects of higher T_a on structure of IGZO-SiO_2 mixing layer: enhanced Si-O bonds, weaker M-O bonds, and more H_2O molecules.

5. Conclusions

In conclusion, the effects of annealing temperatures (T_a) on the IGZO/SiO_2 film structure and electrical stabilities of bottom-gate coplanar IGZO TFTs were investigated to build a process–structure–property holistic link. The XPS results presented a three-layer structure of IGZO/SiO_2: a uniform IGZO layer, an IGZO/SiO_2 interfacial mixing layer, and a SiO_2 layer. Higher T_a had complex effects on the structure of the interfacial mixing layer, though it only resulted in stronger chemical bonds within the IGZO and SiO_2 layers. Particularly, although the damaged Si-O bonds within the interfacial mixing layer were improved at high T_a, the weak M-O bonds (M points to the metallic atoms in IGZO) were thermally disturbed. Additionally, the undesired O-related molecules (e.g., water molecules) were introduced into the interfacial mixing layer. The IGZO TFTs with IGZO annealed at higher T_a exhibited enhanced positive bias temperature stress (PBTS) stabilities but degraded negative bias temperature (NBTS) stabilities. The enhanced PBTS stabilities were attributed to the reduced electron traps due to the stronger Si-O bonds near the IGZO/SiO_2 interfacial mixing layer. The decreased NBTS stabilities were ascribed to the increased electron de-trapping arising from the donor-like defects within the interfacial mixing layer (such as weaker M-O bonds and increased O-related defects). Our results indicate that to achieve enhanced comprehensive performance of IGZO TFTs, controlling defect generation (e.g., by using a mild growth condition of source/drain electrodes and oxides or densifying the SiO_2 layer) may be more significant than enhancing defect annihilation (e.g., by increasing T_a).

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