

Article

# Design and Assessment of Hybrid MTJ/CMOS Circuits for In-Memory-Computation

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**Abstract:** Hybrid magnetic tunnel junction/complementary metal oxide semiconductor (MTJ/CMOS) circuits based on in-memory-computation (IMC) architecture is considered as the next-generation candidate for the digital integrated circuits. However, the energy consumption during the MTJ write process is a matter of concern in these hybrid circuits. In this regard, we have developed a novel write circuit for the contemporary three-terminal perpendicular-MTJs that works on the voltage-gated spin orbit torque (VG+SOT) switching mechanism to store the information in hybrid circuits for IMC architecture. Investigation of the novel write circuit reveals a remarkable reduction in the total energy consumption (and energy delay product) of 92.59% (95.81) and 92.28% (42.03%) than the conventional spin transfer torque (STT) and spin-Hall effect assisted STT (SHE+STT) write circuits, respectively. Further, we have developed all the hybrid logic gates followed by nonvolatile full adders (NV-FAs) using VG+SOT, STT, and SHE+STT MTJs. Simulation results show that with the VG+SOT NOR-OR, NAND-AND, XNOR-XOR, and NV-FA circuits, the reduction in the total power dissipation is 5.35% (4.27%), 5.62% (3.2%), 3.51% (2.02%), and 4.46% (2.93%) compared to STT (SHE+STT) MTJs respectively.

**Keywords:** magnetic tunnel junction; spin-hall effect; spin transfer torque; non-volatile; voltage-gated spin orbit torque; in-memory-computation



**Citation:** Barla, P.; Shivarama, H.; Deepa, G.; Ujjwal, U. Design and Assessment of Hybrid MTJ/CMOS Circuits for In-Memory-Computation. *J. Low Power Electron. Appl.* **2024**, *14*, 3. <https://doi.org/10.3390/jlpea14010003>

Academic Editors: Weigang Wang and Guozhong Xing

Received: 1 November 2023

Revised: 17 December 2023

Accepted: 29 December 2023

Published: 6 January 2024



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## 1. Introduction

In recent years, deep learning and artificial intelligence applications such as image classification, object detection, speech recognition, natural language processing, etc., have been remarkably successful due to their efficient software algorithms [1–3]. However, the hardware supporting these applications still works based on the conventional von-Neumann architecture, where the memory and computational units are separated, and bus/interconnects facilitate communication between the two. As a result, power wastage due to the frequent movement of signals between memory and computational units is remarkably high [4,5]. To add, the delay in these signals is also considerably high for large systems. Meanwhile, at the device level, miniaturization of CMOS poses challenges such as increased power dissipation because of the secondary effects [6]. Though there is constant advancement at the device level, it is clear that one can not solely depend on a single CMOS technology to fulfill all the present-day requirements [7]. In the present scenario, a high demand for a high-speed and power-efficient hardware design exists. To address this, in-memory-computation (IMC) is well-positioned to date [5,8–10]. The idea in IMC is to merge the memory and computation to avoid frequent data movement by providing low-power, high-speed computation. Some literature suggests SRAM as a memory for IMC [11–14]. However, the shortcomings, such as inherent leakage current, the necessity of large numbered transistors to store a single bit, the occupancy of large silicon area, etc., outweigh its other benefits [1]. This triggered a huge interest in the utilization of spintronic devices for IMC [15,16]. The spintronic devices are non-volatile memory (NVM) devices,

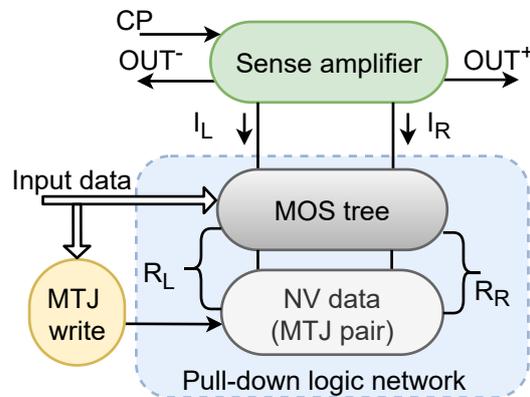
where along with charge, spin of electrons also carries information. Among all spintronic devices, MRAM is the most promising due to its advantages such as higher endurance, fast read/write speeds, long data retention time, scalability, 3D fabrication, and ease of integration with the existing CMOS technology [1,17–19]. To store information bit, MRAM relies on the relative spin orientation of electrons that tunnel across the barrier layer (BL) sandwiched between two ferromagnetic materials, of which one is the free layer (FL) and the other is the pinned layer (PL). Thus forming a magnetic tunnel junction (MTJ). The MTJ is in a low resistance ( $R_P$ ) parallel (P) state when both PL and FL are in the same direction; on the contrary, MTJ is in a high resistance ( $R_{AP}$ ) anti-parallel (AP) state when PL and FL points in the opposite direction. The material used for the PL and FL is CoFe-based, and for BL is MgO. This is due to the achievement of high tunneling magnetoresistance (TMR) with CoFeB/MgO/CoFeB MTJs [20]. Altering the state of MTJ between ( $R_{AP}$ ) and ( $R_P$ ) is called MTJ switching/writing. There are several p-MTJ switching mechanisms such as spin transfer torque (STT) [21,22], spin-Hall effect assisted spin transfer torque (SHE+STT) [23,24], voltage assisted MTJ switching [25–27] etc. Among all, the recently presented voltage-gated spin orbit torque (VG+SOT) switching mechanism [28–30] has attracted the attention of many researchers due to its numerous advantages and is suitable for many applications [31,32]. In VG+SOT, MTJ switching is achieved with the combination of voltage and SHE effect. Encouraged by the developments in the VG+SOT MTJs, we have developed a novel write circuit for the VG+SOT for the IMC architecture. This write circuit is compared with the conventional STT and SHE+STT write circuits in terms of write energy, worst-case write delay, and energy-delay product (EDP). Then we developed all the hybrid logic gates, such as NOR-OR, NAND-AND, and XNOR-XOR followed by three non-volatile full adder (NV-FA) circuits using different MTJs such as STT, SHE+STT, and VG+SOT based on IMC architecture. The performance of all these circuits has been studied in terms of power dissipation, worst-case read delay, and power delay product (PDP). The rest of the paper is organized as follows: The background of IMC architecture, conventional STT and SHE+STT write circuit and their brief working is presented in the Section 2. In Section 3, we have explained the switching mechanism of VG+SOT MTJ and presented the novel VG+SOT write circuit, followed by its working. Then, in the Section 4 we have developed all the hybrid logic gates, i.e., NOR-OR, NAND-AND, XNOR-XOR. In Section 5, we have explained the design and working of NV-FA. The Section 6 presents performance evaluation of all the write circuits, hybrid logic gates and NV-FAs developed based on different MTJs for the IMC architecture. Finally, the paper is concluded in Section 7.

## 2. Background

### 2.1. In-Memory-Computation Architecture

The general structure for the IMC architecture is presented in Figure 1. It consists of (a) sense amplifier (SA), (b) pull-down logic network (PDN) block, and (c) MTJ write block. The SA is nothing but a current-controlled amplifier that senses the logic operations performed by the PDN to produce output ( $OUT^+$ ) and its complement ( $OUT^-$ ). The PDN is a hybrid circuit having CMOS tree integrated with MTJ pair. It performs the logic operation on the input data, result of which is produced by the SA. The integration of MTJ with CMOS is possible due to their resistance compatibility, viz, the  $R_P$  is higher than  $R_{ON}$ . On the contrary,  $R_{AP}$  is less than  $R_{OFF}$ . Where  $R_{ON}$  and  $R_{OFF}$  are CMOS ON and OFF resistances, respectively. The combined resistances of CMOS and MTJ in the left arm ( $R_L$ ) and right arm ( $R_R$ ) decide the corresponding rate of flow of current in the left arm ( $I_L$ ) and right arm ( $I_R$ ). Here we use a pair of MTJ to store a single bit of information. We assume MTJ pair with AP-P state always stores bit 0. Conversely, if the MTJ pair is in P-AP state, we assume information bit 1 is stored. It is noteworthy that the MTJ pair is always complementary to each other. The IMC operates in (a) pre-charge and (b) evaluation phase where the clock pulse (CP) is at 0 and 1, respectively. In the pre-charge phase, inputs are applied to the PDN and both,  $OUT^+$  and  $OUT^-$  are raised to logic 1. During the evaluation phase, logical operations are performed on these inputs at the PDN to produce corresponding  $OUT^+$  and

$OUT^-$ . The  $OUT^+$  and  $OUT^-$  values depend upon the  $R_L$  and  $R_R$ , which in-turn depend on  $I_L$  and  $I_R$ . That is,  $R_L$  and  $R_R$  have inverse relations with  $I_L$  and  $I_R$  currents to produce  $OUT^+$  and  $OUT^-$ . For instance,  $R_L > R_R$  results in  $I_L < I_R$  and produce  $OUT^+ = 0$  and  $OUT^- = 1$ . Otherwise when  $R_L < R_R$  results in  $I_L > I_R$  and produce  $OUT^+ = 1$  and  $OUT^- = 0$ .

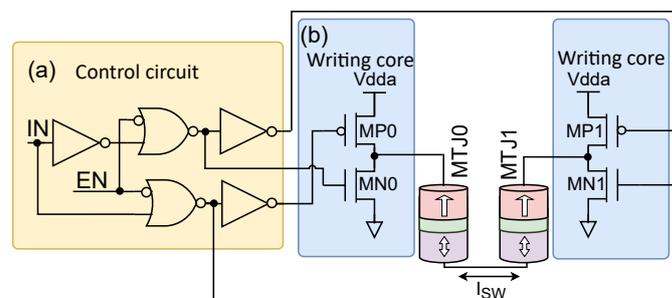


**Figure 1.** General IMC Block diagram consisting of sense amplifier, MOS logic tree along with MTJ pair and MTJ write. The input data presented to the CMOS logic tree are volatile in nature whereas the information stored in the MTJ pair is non-volatile.

Based on magnetic anisotropy, there are two types of MTJs. i.e., in-plane magnetic anisotropy MTJ (i-MTJ) and perpendicular-plane magnetic anisotropy MTJ (p-MTJ). Depending upon the type of MTJ (i-MTJ/p-MTJ), several switching techniques have been developed. The p-MTJ is superior due to smaller size, larger thermal stability, smaller switching current, ease of scaling compared to the i-MTJ [33]. Hence, we have focused on the p-MTJ devices in our work.

### 2.2. Spin Transfer Torque Write Circuit

The conventional STT p-MTJ switching circuit is presented in Figure 2 [6]. MTJ pair MTJ0-MTJ1 are used to store single-bit information. Bi-directional current ( $I_{SW}$ ) is used for changing the status of MTJs between AP and P. When  $EN = 0$ , the  $I_{SW}$  flow is disabled. On the contrary,  $I_{SW}$  flows in the writing core only when  $EN = 1$ . Assume bit 1 needs to be written into the MTJ pair, which was earlier stored with bit 0, i.e., its configuration must be changed from AP-P to P-AP. Switching is initiated upon asserting  $EN = 1$  and  $IN = 1$ . Now the transistors MN1, and MP0 are OFF, whereas MN0 and MP1 are ON. This forces the  $I_{SW}$  via the path  $V_{dda}$ -MP1-MTJ1-MTJ0-MN0-GND. Hence, the switching of the MTJ pair, i.e., P-AP, is achieved. Similarly, switching the MTJ pair from P-AP to AP-P to store bit 0 can be achieved by making  $EN = 1$  and  $IN = 0$ .

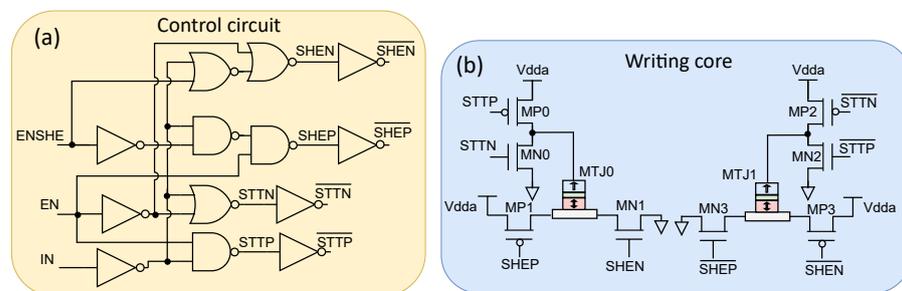


**Figure 2.** Conventional STT p-MTJ write circuit, consisting of (a) control circuit and (b) writing core. Bi-directional  $I_{SW}$  flows through the MTJ pair to switch its state between P and AP.

Simple structure, ease of working, and potential to achieve higher density circuits make the STT-MTJs one of the most suitable commercial products [21,34]. However, the STT-MTJ suffers from several disadvantages. Frequent flow of  $I_{SW}$  to switch the status of MTJ can break down the BL over a period of time. Apart from that, as the read and write paths are the same in the STT-MTJ, there is a chance of erroneous writing into the MTJ while the reading current passes through it, causing a read disturbance error. Most significantly, the STT-MTJ suffers the incubation delay, which is stochastic in nature. As a result, the switching delay of STT-MTJ is large, making it less favorable for high-speed applications.

### 2.3. Spin-Hall Effect Assisted Spin Transfer Torque Write Circuit

Some of the disadvantages of the STT writing mechanism are overcome with the three terminal SHE+STT p-MTJ [23,24]. For example, a separate read and write path of SHE+STT MTJ overcomes the read disturbance error. Meanwhile, the SHE effect considerably reduces the STT current, thereby eliminating the chances of BL breakdown. Furthermore, the incubation delay observed during the writing of STT-MTJ disappears in the SHE+STT p-MTJ, making it suitable for high-speed applications. Figure 3 shows the conventional SHE+STT p-MTJ switching circuit [35]. Compared with the STT p-MTJ switching circuit, an ENSHE input signal with EN and IN signals is present here. ENSHE controls the flow of SHE current. If we assume writing the MTJ pair with the information bit 1, then signals IN, EN, and ENSHE are asserted to logic 1. So the transistors MP0 and MN2 are OFF, whereas the rest are ON. This simultaneously initiates the flow of SHE current ( $I_{SHE}$ ) and STT current  $I_{STT}$ . Path for  $I_{SHE}$  is Vdda-MP1-MTJ0-MN1-GND and Vdda-MP3-MTJ1-MN3-GND. Whereas the  $I_{STT}$  path is, Vdda-MP1-MTJ0-MN0-GND and Vdda-MP2-MTJ1-MN3-GND. As a result, the MTJ pair enters into the meta-stable state. After a small period, the ENSHE signal is made as logic 0. Hence, the transistors MN1 and MP3 are turned OFF to cease the  $I_{SHE}$  flow. Whereas the  $I_{STT}$  continues to flow and completes the switching of p-MTJ into P-AP, and information bit 1 is written. In a similar way, writing the information 0 into the MTJ pair can be done by making  $IN = 0$ .



**Figure 3.** Schematic of SHE+STT p-MTJ write circuit consisting of (a) control circuit and (b) writing core.

Though SHE+STT p-MTJ is comparatively better than STT-MTJ, it suffers from the joule heating effect and ohmic losses due to the flow of current. Meanwhile, to handle these currents, one needs transistors with large size causing area overhead [36].

### 3. Voltage Gated Spin Orbit Torque: Mechanism and Novel Write Circuit

One significant method to overcome the ohmic loss and joule heating effect is incorporating the voltage to switch the p-MTJ status. Recent literature reveals that applying a voltage across p-MTJ can alter its magnetic anisotropy [37–40]. This effect is called voltage-controlled magnetic anisotropy (VCMA). The VCMA effect can switch the MTJ status. However, achieving deterministic MTJ switching with the VCMA effect requires either a precise voltage pulse or external assistance from a magnetic field or a small STT/SHE current. Since generating a precise voltage pulse or producing an external magnetic field in practical conditions is challenging [41,42], some circuits were developed with two terminal p-MTJs with VCMA+STT switching regime [42–44]. However, applying STT current poses the disadvantages of dielectric breakdown and read disturbance errors. Given this,

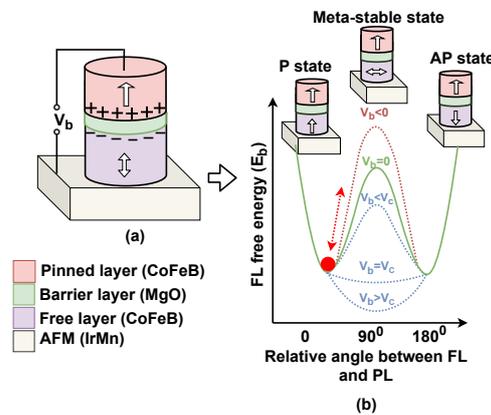
a combination of VCMA in conjunction with SHE is employed to switch the MTJ status deterministically. Hence, a new type of p-MTJ switching regime called VG+SOT has been developed that combines the advantages of VCMA and SHE [45–48]. The VG+SOT p-MTJ is formed by mounting the combination PL/BL/FL on top of antiferromagnetic material (AFM) such as IrMn3 [49,50] as shown in the Figure 4a. The AFM material in VG+SOT p-MTJ generates SOT and provides an in-plane exchange bias ( $\vec{H}_{EX}$ ). However, the  $\vec{H}_{EX}$  developed here is weak. Hence, the SOT alone can not switch the MTJ deterministically. Nevertheless, with assistance from the VCMA effect, the SOT generated can accurately switch the FL’s magnetic orientation in VG+SOT p-MTJ [30,51]. VCMA effect is generated by applying a small voltage ( $V_b$ ), greater than or equal to the critical voltage ( $V_c$ ) across the p-MTJ that lowers the energy barrier ( $E_b$ ) (Figure 4b). This initiates a free precession of FL’s magnetic orientation. At the same time, a SHE current is forced through AFM to fix the FL’s magnetic orientation in a specific direction, i.e., either to P and AP. It is noteworthy that applying a negative  $V_b$  increases  $E_b$ . The relationship between  $E_b$  is modeled as a function of  $V_b$  and given in the Equation (1) as,

$$E_b(V_b) \approx \left[ K_i(V_b) - 2\pi M_s^2 (N_z - N_{x,y}) t_f \right] \cdot A. \tag{1}$$

where  $K_i(V_b)$  is the voltage-dependent interfacial PMA (perpendicular magnetic anisotropy),  $M_s$  is the saturation magnetization,  $t_f$  is the thickness of the FL,  $V_b$  is the bias voltage,  $A$  is the sectional area of the MTJ,  $N_z$  and  $N_{x,y}$  are the demagnetization factors of the MTJ in the perpendicular and in-plane directions. The  $V_c$ , which is minimum voltage required to completely eliminate  $E_b$  is defined by the Equation (2,)

$$V_c = \Delta(0) k_B T t_{ox} / \zeta A. \tag{2}$$

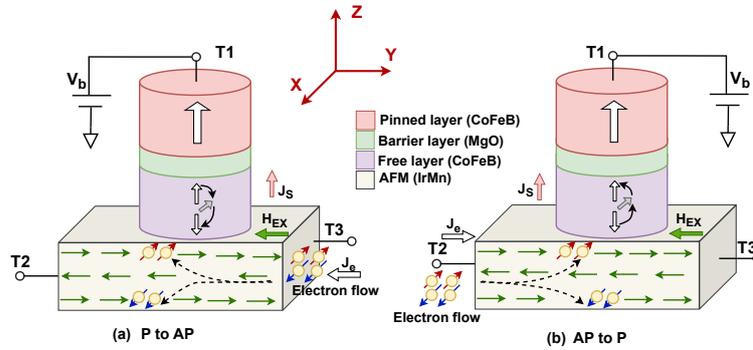
where  $\Delta(0)$  is thermal stability under zero voltage,  $k_B$  is the Boltzmann constant,  $T$  is temperature,  $t_{ox}$  is the thickness of the oxide layer, and  $\zeta$  is the VCMA coefficient.



**Figure 4.** VCMA effect in VG+SOT. (a) Application of positive  $V_b$  causes the accumulation charges across the barrier layer resulting in (b) lowering of  $E_b$ , thereby the FL’s magnetic orientation is in meta–stable state. This can assist in switching of MTJ status.

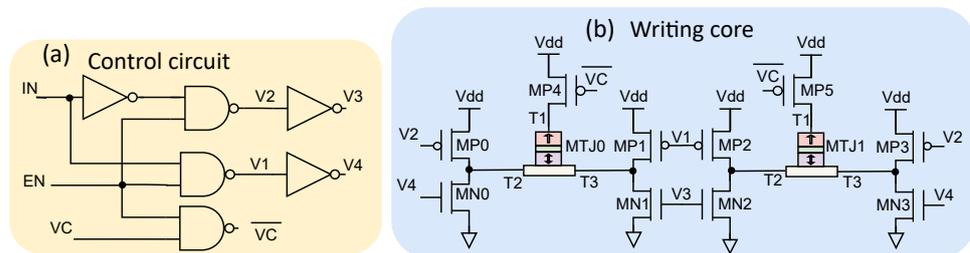
Figure 5 presents the VG+SOT p-MTJ switching mechanism. Consider switching VG+SOT p-MTJ from P to AP state. Here, the unpolarized in-plane electrons ( $\vec{j}_e$ ) are forced through the AFM in the  $-Y$  direction. Due to a strong spin orbit coupling (SOC), SHE is observed in the AFM, which results in the deflection of opposite spin electrons (which are in  $\pm X$  direction) in transverse,  $\pm Z$  direction creating a spin current  $\vec{j}_s$  in  $Z$ -direction. Hence, there is an accumulation of electrons (oriented in  $-X$  direction) at the interface of AFM/FL. This exerts SOT to tilt the FL’s magnetic orientation from the  $Z$ -direction toward the  $XY$ -plane. The presence of in-plane  $\vec{H}_{EX}$  causes the FL’s magnetic orientation to precessionally rotate around the field and move toward the direction of  $\vec{H}_{EX}$  (here it

is Y-direction) by damping action. Meanwhile, the application of VCMA would lower the  $E_b$  to switch the FL's magnetic orientation towards the  $-Z$ -direction. Hence, the MTJ switches from AP to P state. Similarly, the switching of the MTJ from P to AP is achieved by reversing the direction of  $\vec{J}_e$  (Figure 5b).



**Figure 5.** Schematic of switching action in VG+SOT.  $V_b$  is applied to lower the  $E_B$ . Meanwhile (a)  $\vec{J}_e$  is forced through through AFM in  $-Y$  direction. Accumulation of spin polarized electrons (in  $-x$  direction) exerts SOT and alter its magnetic orientation from  $Z$  direction towards  $XY$ -plane. Under the influence of  $\vec{H}_{EX}$  the magnetic orientation in the  $XY$ -plane precess and switches to  $-Z$ -direction, thereby completing switching of MTJ from P to AP. To switch the MTJ from (b) AP to P, direction of the  $\vec{J}_e$  is reversed.

The proposed VG+SOT p-MTJ write circuit is presented in Figure 6. The write circuit is disabled when  $EN = 0$ , as all the transistors in the writing core are disabled. Upon the application of  $EN = 1$ , depending upon the  $IN$  signal, the MTJ pair is written with either bit 0 or 1. Assume, previously, bit 0 is stored in the MTJ pair, i.e., it is in AP-P state, and we want to write bit 1, i.e., the MTJ pair needs to be switched to P-AP. This can be initiated by asserting  $EN = 1$ ,  $IN = 1$ , and  $VC = 1$ . Hence the intermediate voltages  $V1, V2, V3$  and  $V4$  are at 0101 which turns ON transistors  $MP1, MN0, MP2, MN3, MP4$  and  $MP5$ , whereas  $MP0, MN1, MP3$  and  $MN2$  are OFF. As a result, a VCMA voltage ( $VC$ ) is applied to the MTJ pair; simultaneously, a SOT current ( $I_{SOT}$ ) flowing through the AFM applies a SOT on the FL's magnetic orientation. The direction of  $I_{SOT}$  is  $V_{dd}$ - $MP1$ - $MTJ0$ ( $T3$ - $T2$ )- $MN0$ - $GND$  and  $V_{dd}$ - $MP2$ - $MTJ1$ ( $T2$ - $T3$ )- $MN3$ - $GND$ . After 200 ps, the  $VC$  is disabled whereas the  $I_{SOT}$  flows, completing the MTJ pair switching from AP-P to P-AP state. Hence, the writing of bit 1 into the MTJ pair is achieved. Similarly, writing bit 0 into the MTJ pair is achieved by making  $IN = 0$ .

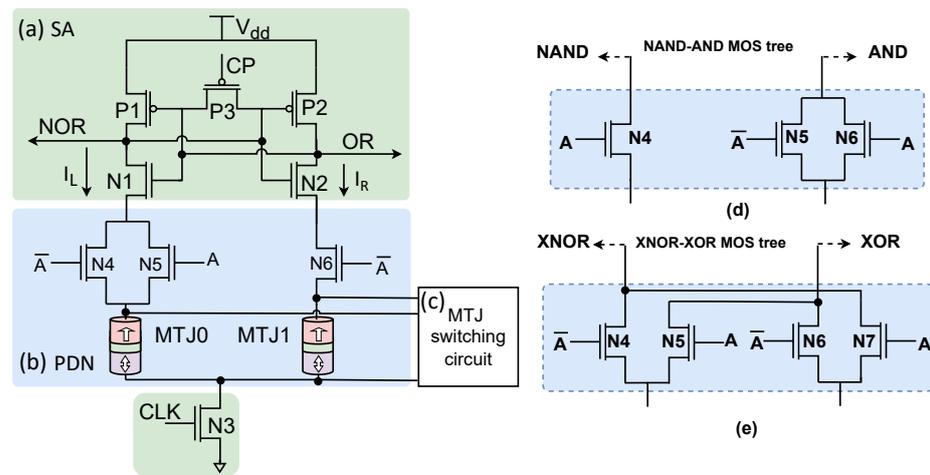


**Figure 6.** VG+SOT write circuit showing (a) control and (b) writing core.

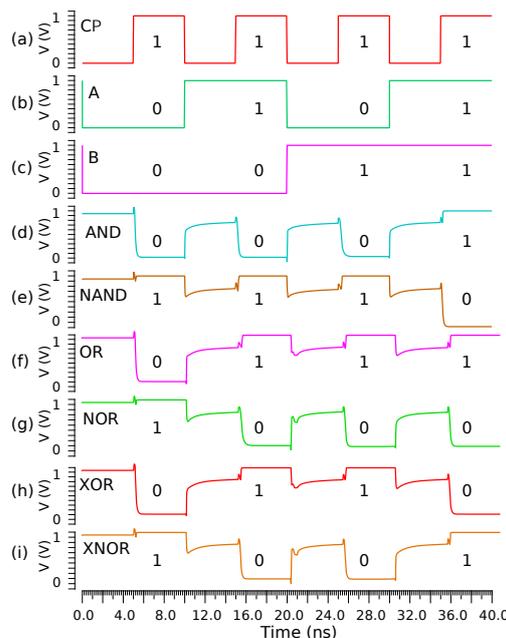
#### 4. Logic Gates Based on IMC

We have developed various logic gates based on the IMC architecture, and are presented in Figure 7. We have chosen the contemporary SA [52], which produces a quicker output response and dissipates lower power than its conventional counterpart [53]. For the purpose of explanation, we chose the operation of the NOR-OR logic gate, and the inputs applied are  $A = 0$  and  $B = 1$ . During the pre-charge phase,  $CP = 0$ , SA transistor  $N3$  is OFF, and  $P3$  is ON. This facilitates sharing the NOR and OR output to reach logic 1 ( $V_{dd}-V_{th}$ ).

Meanwhile, inputs A and B are applied to the PDN. Here, the writing of the information (input B) occurs, i.e., MTJ0-MTJ1 are at P-AP state. The circuit enters into the evaluation phase by making CP = 1. Now the SA transistors, N3, is ON whereas P3 is OFF. In the PDN, N5 is OFF; meanwhile, both N4 and N6 are ON. This creates two current paths  $I_L$  and  $I_R$ , i.e.,  $I_L$  is from NOR-N1-N4-MTJ0-N3-GND.  $I_R$  is from OR-N2-N6-MTJ1-N3-GND. As the MTJ0-MTJ1 pair is in P-AP status, the branch resistance  $R_L < R_R$ , resulting in a quicker discharge of  $I_L$  compared to  $I_R$ . So, the NOR node is discharged to the GND, making it logic 0. On the contrary, the OR node is pulled up to logic 1. Similarly, the working of the circuit for other inputs is realized. In Figure 7a, by replacing the MOS tree with Figure 7d,e, one can realize NAND-AND and XNOR-XOR logic gates respectively. Figure 8 shows the timing diagram of the logic gates for a clock frequency of 100 MHz.



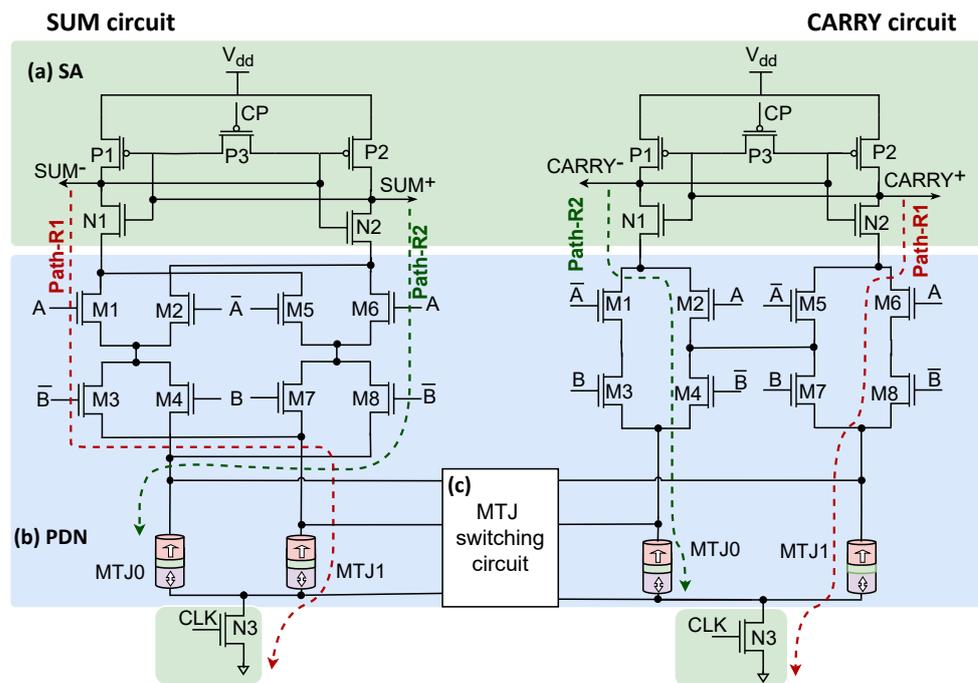
**Figure 7.** Circuit for NOR–OR gate based on IMC showing (a) SA, (b) PDN for NOR-OR logic gates and (c) MTJ switching block. Use MOS tree from (d,e) to obtain NAND–AND and XNOR–XOR respectively. Here two terminal p–MTJs are shown for STT logic gates. Replace them by three terminal MTJs to get SHE+STT/VG+SOT logic gates.



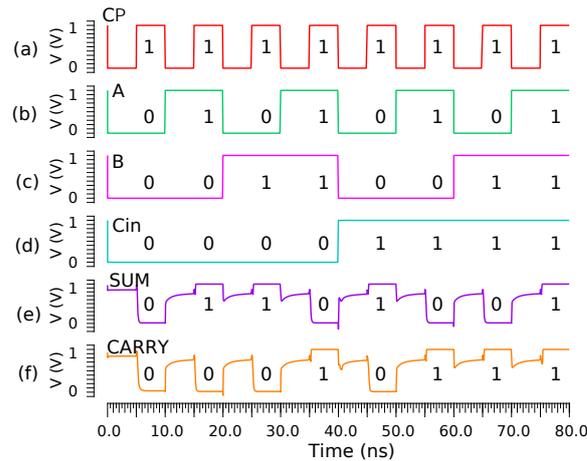
**Figure 8.** Simulated waveform for various hybrid logic gates showing inputs (a) CP, (b) A, (c) B and corresponding outputs (d) AND, (e) NAND, (f) OR, (g) NOR, (h) XOR, (i) XNOR.

### 5. IMC Based Full Adder

Having developed all the logic gates, we developed NV-FA based on IMC architecture with different types of MTJs shown in Figure 9. The working of this FA is in line with the IMC based logic gates, where there are two operating phases: pre-charge and evaluation. In the pre-charge ( $CP = 0$ ), all the outputs, sum ( $SUM^+$ ) and its complement ( $SUM^-$ ), and carry ( $CARRY^+$ ), and its complement ( $CARRY^-$ ) are at logic 1 ( $V_{dd}-V_{th}$ ). Meanwhile, input A, B, and  $C_{in}$  are applied to the PDN. During the evaluation ( $CP = 1$ ), these inputs are processed to produce outputs ( $SUM^+/SUM^-$  and  $CARRY^+/CARRY^-$ ). Imagine the inputs applied in the pre-charge phase are  $A = 1, B = 0,$  and  $C_{in} = 0$ . During the evaluation phase, both in SUM and CARRY circuits, there are two routes, Path-R1 and Path-R2, from their respective nodes to the GND. This is because, in the PDN of the SUM circuit, transistors M1, M3, M6, and M8 are ON, whereas the other transistors are OFF. The Path-R1 is via  $SUM^- - N1 - M1 - M3 - MTJ1 - N3 - GND$ . Path-R2 is via  $SUM^+ - N2 - M6 - M8 - MTJ0 - N3 - GND$ . As  $C_{in} = 0$ , the MTJ pair is in AP-P state. So, the total resistance in Path-R1 < Path-R2. Hence, the  $SUM^-$  node is pulled down to GND, and the  $SUM^+$  node is pulled up to  $V_{dd}$ . Therefore,  $SUM^+ = 1$  and  $SUM^- = 0$ . Similarly, in the carry circuit, the total resistance in Path-R1 < Path-R2. Path-R1 is via  $CARRY^- - N1 - M2 - M4 - MTJ0 - N3 - GND$ , and Path-R2 is via  $CARRY^+ - N2 - M6 - M8 - MTJ1 - N3 - GND$ . So the  $CARRY^+ = 0$  and  $CARRY^- = 1$ . Likewise, the working of NV-FA for other input combinations can be realized. Figure 10 shows the timing diagram of the IMC based NV-FA for a clock frequency of 100 MHz.



**Figure 9.** NV-FA based on IMC consisting of (a) SA (b) PDN for SUM and CARRY circuit with (c) MTJ switching block. Here two terminal STT p–MTJ are shown for STT NV–FA. By replacing them with three terminal SHE+STT/VG+SOT p–MTJs we can obtain SHE+STT/VG+SOT NVFA circuit.



**Figure 10.** Various inputs; (a) CP, (b) A, (c) B (d)  $C_{in}$  and corresponding outputs; (e) SUM, (f) CARRY waveform for NV–FA based on IMC.

### 6. Simulation Results and Discussion

To assess the performance of the write, hybrid logic gates, and NV-FA circuits, we performed the simulation using the Cadence Virtuoso tool with 45nm CMOS generic process design kit. The model for the VG+SOT p-MTJ is adopted from Ref. [30], and the parameters used during the simulation work are shown in Table 1.

**Table 1.** VG+SOT p-MTJ parameters set during the simulation. Rest of the parameters are retained as mentioned in ref. [30].

Parameter	Description	Value
TMR(0)	TMR ratio with zero bias	200%
Shape	MTJ Surface shape	circle
a	MTJ Surface length	32 nm
b	MTJ Surface width	32 nm
r	MTJ Surface radius	16 nm
w	AFM width	50 nm
d	AFM thickness	3 nm
l	AFM length	60 nm
$t_{sl}$	Free layer thickness	1.1 nm
$t_{ox}$	MgO barrier thickness	1.4 nm
RA	Resistance-area product	650 $\Omega \cdot \mu\text{m}^2$

#### 6.1. Write Circuits

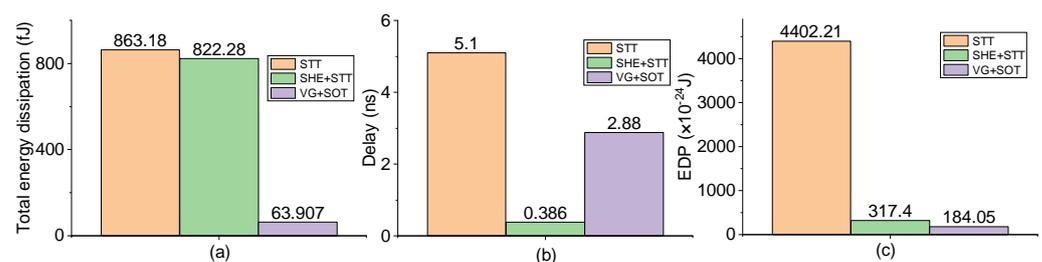
Table 2 shows the performance comparison of the various write circuits. We can observe that the control circuit’s energy dissipation is comparatively lower than the writing core. This is because the control circuitry consists of only logic gates, whereas the writing core contains MTJ pair. The energy required to switch the MTJ pair is always higher than the rest of the circuitry. Among all the write circuitry, the least total energy consumption is observed with the VG+SOT p-MTJ circuit, followed by SHE+STT and STT. In writing core, VG+SOT write circuit consumes 92.0% and 92.68% less energy than SHE+STT and STT, respectively. The control circuit of the VG+SOT write circuit consumes 70.93% and 34.6% lower energy than SHE+STT and STT, respectively. The total energy dissipation of VG+SOT write circuit is 92.28%, and 92.59% lower than SHE+STT and STT, respectively. In VG+SOT switching, thanks to the VCMA effect, the p-MTJ’s energy barrier gets lowered, facilitating its switching with an application of  $I_{SOT}$  current through the AFM. However, the worst-case write delay of VG+SOT is 86.59% more than SHE+STT write circuitry. Meanwhile, the delay of the VG+SOT write circuit is less than STT by 43.52%. The higher delay in the VG+SOT

switching mechanism is because, when  $I_{SOT}$  current is applied, the SOT is responsible for tilting FL's magnetic orientation from its original position towards the XY-plane. Now, the p-MTJ is in a meta-stable state. Switching is assisted by the presence of  $\vec{H}_{EX}$ , where the FL's magnetic orientation initially precesses and settles down. The time taken to precess and then settling of FL's magnetic orientation causes the delay. Meanwhile, with SHE+STT switching, once the magnetic orientation is in the XY plane, its precession is almost zero, and STT torque forces switching of p-MTJ quickly. Hence, the delay is the least. However, with STT switching, due to the stochastic nature of STT p-MTJ, there is an initial delay in misaligning the FL's magnetic orientation from its initial position. This results in higher delay. The EDP, product of total energy dissipation and worst case write delay of VG+SOT write circuit, is lesser than the rest. The EDP of the VG+SOT write circuit is 42.03% and 95.81% lower than SHE+STT and STT write circuits, respectively. Regarding the number of transistors, the STT write circuitry uses only 22 MOS, whereas the SHE+STT write circuitry uses almost double, i.e., 46 MOS transistors. However, the VG+SOT write circuitry uses only 6 additional MOS (i.e., 28) compared to STT. Figure 11 shows a bar chart plot of the total energy consumption, worst-case write delay, and the EDP among the various write circuits. In Figure 12, we have presented the simulated waveform for all the write circuits together. To begin with, bit 1 is stored in the MTJ pair. At T1, writing of the bit 0 is initiated, followed by writing of the bit 1 at T2. We have also shown redundant write conditions at time T3. Writing the information bit 0/1 is completed after a brief delay as shown in the Table 2.

**Table 2.** Performance comparison between STT, SHE+STT, and VG+SOT writing.

MTJ Switching Technique	STT	SHE+STT	VG+SOT
Writing core Energy/bit (fJ)	861.9	819.4	63.07
Control circuit Energy/bit (fJ)	1.28	2.88	0.837
Total Energy/bit (fJ) <sup>a</sup>	863.18	822.28	63.907
Worst case delay (ns)	5.1	0.386	2.88
Energy delay product ( $\times 10^{-24}$ ) <sup>b</sup>	4402.21	317.4	184.05
No. of MOS	22	46	28

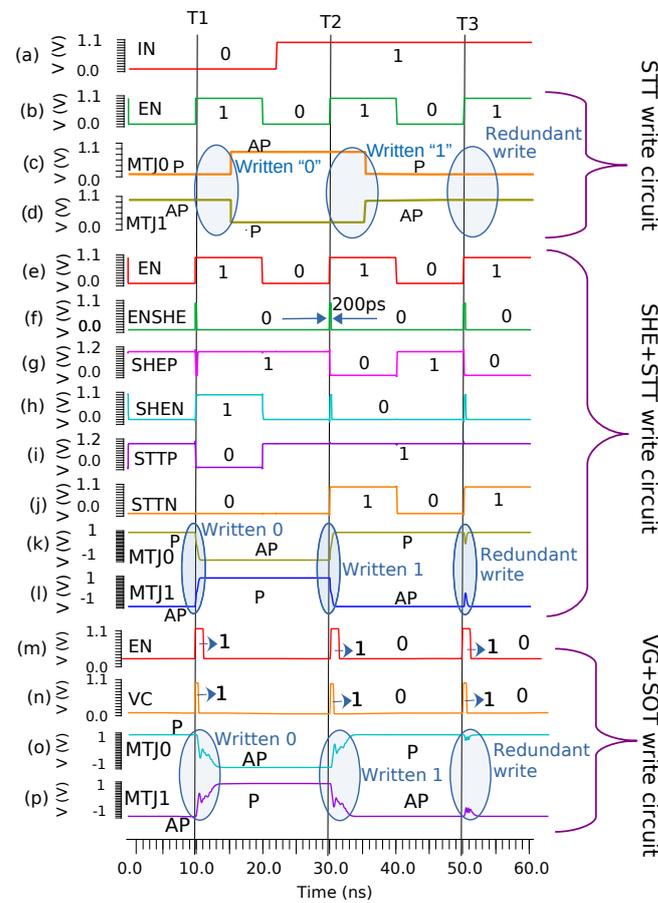
<sup>a</sup> = Writing core energy/bit + Control circuit Energy/bit. <sup>b</sup> = Total energy/bit \* Worst case delay.



**Figure 11.** Comparison of (a) total energy dissipation, (b) delay, and (c) EDP among different write circuits.

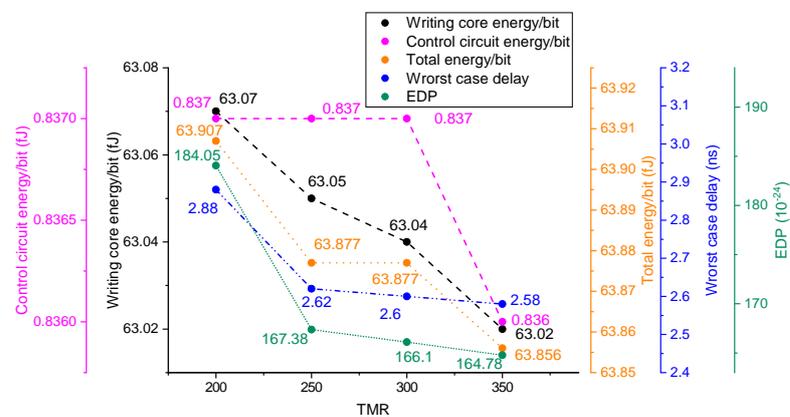
Overall, the VG+SOT write circuit is superior to its other counterpart except for the write delay. VG+SOT p-MTJ write circuit has an increased write delay compared to the SHE+STT. Recent research has actively identified ferrimagnetic alloy materials, such as cobalt-gadolinium (CoGd), as efficient replacements for the AFM [54], primarily due to their ability to reduce delay significantly. Ferrimagnetic materials can reduce the switching delay to subnanoseconds. However, more effort is required to integrate ferrimagnets with conventional MTJ to develop practical applications [55]. Meanwhile, efforts have been made to develop an efficient all-antiferromagnetic tunnel junction (AATJ) [56]. The AATJ structure is made of Mn3Pt/MgO/Mn3Pt/MnPt combination. With AATJ, although a switching

speed in the range of picoseconds can be achieved, the maximum TMR achieved with it is approximately 100% at room temperature. Hence, its practical application is limited.



**Figure 12.** Simulated waveform for (b–d) STT, (e–l) SHE+STT and (m–p) VG+SOT write circuits. The input data (a) IN is common whereas the other enable signals and switching of the MTJ pairs for the different write circuits are shown separately.

We have investigated the effect of TMR variation on the VG+SOT write circuit parameters, as shown in Figure 13. Here, we have increased the TMR from 200 to 350 in steps of 50. Notice that as the TMR value increases, the total energy/bit, worst case delay, and EDP decreases slightly. Hence, we can say achieving a higher TMR is vital for the design of efficient hybrid circuits.



**Figure 13.** VG+SOT write circuit’s performance variation with the respect to variation in TMR.

It is crucial to study the reliability of the VG+SOT write circuit for the process and mismatch variations that could happen during its fabrication. Hence, we have performed the Monte-Carlo simulations on VG+SOT write circuit by incorporating 3% variations in TMR,  $t_{sl}$ , and  $t_{ox}$  along with CMOS variations, and the results energy/bit are tabulated in Table 3. Here, we can notice that the total energy/bit value is always less than  $\approx 68$  fJ.

**Table 3.** Energy consumption of VG+SOT write circuit during Monte-Carlo simulation of 200 runs.

Design Type	Min	Max	Mean	Std Divination
Writing core energy/bit (fJ)	56.52	67.08	62.33	2.782
Control circuit energy/bit (fJ)	0.749	0.883	0.833	0.031
Total energy/bit (fJ)	57.269	67.963	63.163	2.813

### 6.2. Performance of Logic Gates

Table 4 shows the performance comparison of logic gates with different p-MTJ circuits. The static power dissipation of all the logic gates is considered to be zero. This is because as a nonvolatile MTJ pair is utilized to store input B, we can turn off the supply in the standby mode without losing the stored bit. During active mode, the bit stored is readily available for computation without the write/restoration process. However, there is a steady-state power dissipation observed with gates, as shown in Table 4. In the NOR-OR gates, the dynamic power dissipation of the VG+SOT is least followed by STT and SHE+STT based gates. VG+SOT consumes 65.22% and 67.02% lower dynamic power than STT and SHE+STT NOR-OR gates respectively. The total power dissipation of VG+SOT is least followed by SHE+STT and STT. VG+SOT gate dissipates 4.27%, and 5.35% lower total power than SHE+STT and STT gates, respectively. The worst-case read delay of SHE+STT based NOR-OR gates least followed by STT, and VG+SOT. SHE+STT based NOR-OR gate's worst case read delay is 12.95%, and 90.16% lower than STT, and VG+SOT, respectively. The PDP is calculated by multiplying total power with worst case read delay. The PDP SHE+STT based NOR-OR gate is least followed by STT and VG+SOT. The PDP of the SHE+STT gate is 13.98% and 89.73% lower than the STT and VG+SOT gates, respectively.

**Table 4.** Comparison between various logic gates operating at 100 MHz.

Gate	NOR-OR			NAND-AND			XNOR-XOR			
	p-MTJ	STT	SHE+STT	VG+SOT	STT	SHE+STT	VG+SOT	STT	SHE+STT	VG+SOT
Static power (nW)	0 <sup>a</sup>	0 <sup>a</sup>								
Dynamic power (nW)	55.83 <sup>b</sup>	53.51 <sup>b</sup>	68.16 <sup>b</sup>	55.48 <sup>b</sup>	53.99 <sup>b</sup>	62.96 <sup>b</sup>	57.92 <sup>b</sup>	58.89 <sup>b</sup>	68.14 <sup>b</sup>	19.34
Total power (nW)	81.42 <sup>c</sup>	80.5 <sup>c</sup>	77.06 <sup>c</sup>	84.43 <sup>c</sup>	82.32 <sup>c</sup>	79.68 <sup>c</sup>	90.67 <sup>c</sup>	89.29 <sup>c</sup>	87.48 <sup>c</sup>	86.52
Delay (ps)	112.43	97.86	995.02	85.93	85.04	769.14	125.12	76.47	989.14	76.47
PDP (aJ)	9.15	7.87	76.67	7.25	7	61.28	11.34	6.82	86.52	6.82

Note: Write circuit has been excluded in the tabulated values. Static, dynamic and total power dissipation are the average values. <sup>a</sup> In standby mode power is switched off, resulting in zero static power. <sup>b</sup> Static power dissipation in steady state condition. <sup>c</sup> Total power dissipation = static power + dynamic power in active mode.

In the NAND-AND gates, the dynamic power dissipation of the VG+SOT is least followed by SHE+STT and STT based gates. VG+SOT consumes 40.98% and 42.24% lower dynamic power than SHE+STT and STT gates respectively. The total power dissipation of VG+SOT is least followed by SHE+STT and STT. VG+SOT gate dissipates 3.2% and 5.62% lower total power than SHE+STT and STT gates, respectively. The worst-case read delay of SHE+STT based NAND-AND gates least followed by STT and VG+SOT. SHE+STT based gate's worst-case read delay is 1.03% and 88.94% lower than STT and VG+SOT,

respectively. The PDP SHE+STT based NAND-AND gates is least followed by STT and VG+SOT. The PDP of SHE+STT gate is 3.44%, and 88.57% lower than STT and VG+SOT gates, respectively.

In the XNOR-XOR gates, the dynamic power dissipation of the VG+SOT is least followed by SHE+STT and STT based gates. VG+SOT consumes 36.38% and 40.96% lower dynamic power than SHE+STT and STT gates respectively. The total power dissipation of VG+SOT is least followed by SHE+STT and STT. VG+SOT gate dissipates 2.02% and 3.51% lower total power than SHE+STT and STT gates, respectively. The worst-case read delay of SHE+STT based XNOR-XOR gates least followed by STT and VG+SOT. SHE+STT based gate's worst-case read delay is 38.88% and 92.26% lower than STT and VG+SOT respectively. The PDP SHE+STT based XNOR-XOR gates is least followed by STT and VG+SOT. The PDP of SHE+STT is 39.85%, 92.11% lower than STT and VG+SOT based gates respectively.

We can observe that total power dissipation in all the logic gates is the least with VG+SOT logic gates, followed by SHE+STT and STT. However, the read delay of SHE+STT based logic gates is lower. This is because the IrMn3, AFM material in VG+SOT p-MTJ has higher resistivity, i.e., 278  $\mu\Omega\text{cm}$  [30], whereas the Ta, HM material in SHE+STT p-MTJ has a lower resistivity of 190  $\mu\Omega\text{cm}$  [57]. A higher resistivity of IrMn3 poses a higher resistance in the discharge current path with VG+SOT based logic gates, resulting in higher read delay. However, we know that based on the inputs, during the evaluation phase, one of the outputs (either  $\text{OUT}^+$  or  $\text{OUT}^-$ ) is discharged to GND, whereas the other one is raised to Vdd. Here, the value of  $\text{OUT}^+$  and  $\text{OUT}^-$  is constant, whereas the discharge path resistance of VG+SOT is more due to the higher resistivity of AFM. Hence, we observe a lower power dissipation with VG+SOT circuits. Nevertheless, a higher delay causes a larger PDP with VG+SOT based logic gates. Figure 14 shows the bar chart plot of the dynamic, total power dissipation, worst-case read delay, and PDP for various logic gates circuits.

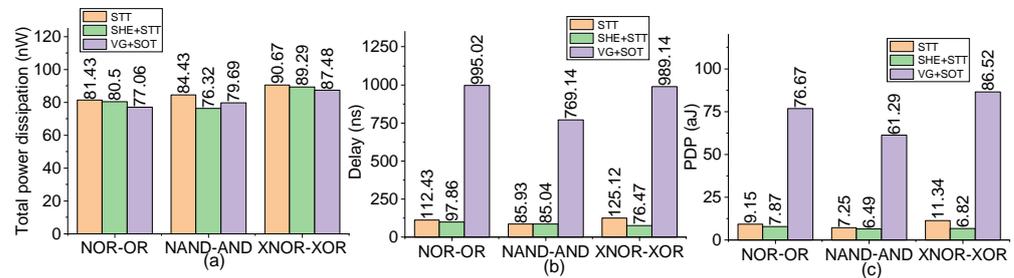


Figure 14. Comparison of (a) total power dissipation, (b) delay, and (c) PDP among all logic gates.

### 6.3. Performance of NV-FA Circuits

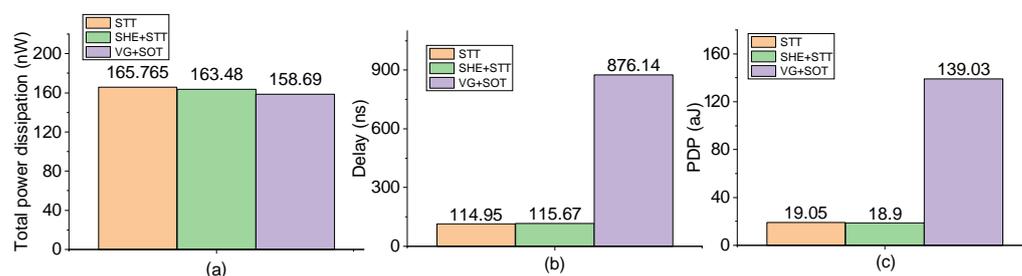
Table 5 show the performance comparison of NV-FA circuits with various p-MTJs.

Table 5. Performance comparison between various NV-FA with STT, SHE+STT, and VG+SOT p-MTJs operating at a frequency of 100 MHz.

NVFA	STT	SHE+STT	VG+SOT
Static power (nW)	0 <sup>a</sup> (119.4 <sup>b</sup> )	0 <sup>a</sup> (119.75 <sup>b</sup> )	0 <sup>a</sup> (145.7 <sup>b</sup> )
Dynamic power (nW)	46.36	43.73	12.99
Total power (nW)	165.76 <sup>c</sup>	163.48 <sup>c</sup>	158.69 <sup>c</sup>
Delay (ps)	114.95	115.67	876.14
PDP (aJ)	19.05	18.9	139.03

Note: Write circuit has been excluded in the tabulated values. Static, dynamic and total power dissipation are the average values. <sup>a</sup> In standby mode power is switched off, resulting in zero static power. <sup>b</sup> Static power dissipation in steady state condition. <sup>c</sup> Total power dissipation= static power + dynamic power in active mode.

The dynamic power dissipation of the VG+SOT based NV-FA is least followed by SHE+STT and STT based NV-FA. VG+SOT based NV-FA consumes 70.29% and 71.98% lower dynamic power than SHE+STT and STT NV-FAs, respectively. The total power dissipation of VG+SOT based NV-FA is least followed by SHE+STT and STT. VG+SOT NV-FA dissipates 2.93% and 4.26% lower power than SHE+STT and STT NV-FA, respectively. The worst case read delay of STT based NV-FA is least followed by SHE+STT, and VG+SOT based NV-FAs. STT based NV-FA's worst case read delay is 0.62% and 86.87% lower than SHE+STT and VG+SOT based NV-FA, respectively. The PDP SHE+STT NV-FA is least followed by STT and VG+SOT. The PDP of SHE+STT NV-FA is 0.78% and 86.4% lower than STT and VG+SOT based NV-FAs respectively. The reason for the increased read delay and PDP is the same as that of VG+SOT logic gates discussed in the previous section. Figure 15 shows the bar chart plot of the dynamic, total power dissipation, worst-case read delay, and PDP for various NV-FA circuits.



**Figure 15.** Comparison of (a) total power dissipation, (b) delay, and (c) PDP between various NV-FA circuits.

### 7. Conclusions

In this paper, we have developed a novel write circuit for VG+SOT p-MTJs based on IMC architecture. Simulation results show that the novel write circuit consumes significantly less energy and EDP than conventional STT and SHE+STT write circuits. However, the worst-case write delay of the novel write circuit is more than the others. Then we developed all the logic gates, such as NOR-OR, NAND-AND, and XNOR-XOR, followed by three different types NV-FA with VG+SOT, STT, and SHE+STT p-MTJs based on IMC architecture. Results obtained from the simulation reveal that VG+SOT-based logic gates and NV-FA dissipate lower power than their other counterparts. Based on the results of this paper, we foresee a higher usage of VG+SOT-based hybrid circuits in low-power applications in the future.

**Author Contributions:** P.B.: Conceptualization, Investigation, Methodology, Validation, Writing—original draft, Writing—review & editing. H.S.: Writing—review & editing. G.D.: Writing—review. U.U.: Writing—review. All authors have read and agreed to the published version of the manuscript.

**Funding:** Manipal Academy of Higher Education, Manipal has provided the APC for this research article.

**Data Availability Statement:** Data available upon reasonable request.

**Conflicts of Interest:** The authors declare no conflict of interest.

### Abbreviations

The following abbreviations are used in this manuscript:

P	Parallel
AP	Antiparallel
PL	Pinned layer
FL	Fixed layer
BL	Barrier layer
IMC	In-memory-computation

MTJ	Magnetic tunnel junction
p-MTJ	Perpendicular magnetic tunnel junction
STT	Spin transfer torque
MRAM	Magnetoresistance random access memory
SRAM	Static random access memory
SHE+STT	Spin-Hall effected assisted Spin transfer torque
VCMA	Voltage controlled magnetic anisotropy
VG+SOT	Voltage-gated spin orbit torque
SOI	Spin-orbit interaction
SOC	Spin orbit coupling
HM	Heavy metal
AFM	Antiferromagnetic material
LLG	Landau–Lifshitz–Gilbert

## References

- Haensch, W.; Raghunathan, A.; Roy, K.; Chakrabarti, B.; Phatak, C.M.; Wang, C.; Guha, S. Compute in-Memory with Non-Volatile Elements for Neural Networks: A Review from a Co-Design Perspective. *Adv. Mater.* **2023**, *35*, 2204944. [CrossRef] [PubMed]
- Seo, J.s.; Saikia, J.; Meng, J.; He, W.; Suh, H.S.; Anupretham; Liao, Y.; Hasssan, A.; Yeo, I. Digital Versus Analog Artificial Intelligence Accelerators: Advances, trends, and emerging designs. *IEEE Solid-State Circuits Mag.* **2022**, *14*, 65–79. [CrossRef]
- LeCun, Y.; Bengio, Y.; Hinton, G. Deep learning. *Nature* **2015**, *521*, 436–444. [CrossRef] [PubMed]
- Burr, G.W.; Lim, S.; Murmann, B.; Venkatesan, R.; Verhelst, M. Fair and Comprehensive Benchmarking of Machine Learning Processing Chips. *IEEE Des. Test* **2021**, *39*, 18–27. [CrossRef]
- Ielmini, D.; Wong, H.S.P. In-memory computing with resistive switching devices. *Nat. Electron.* **2018**, *1*, 333–343. [CrossRef]
- Zhao, W.; Prenat, G. (Eds.) *Spintronics-Based Computing*; Springer International Publishing: Cham, Switzerland, 2015.
- Collaert, N. Advancements in IC Technologies: A look toward the future. *IEEE Solid-State Circuits Mag.* **2023**, *15*, 80–86. [CrossRef]
- Yu, S.; Jiang, H.; Huang, S.; Peng, X.; Lu, A. Compute-in-Memory Chips for Deep Learning: Recent Trends and Prospects. *IEEE Circuits Syst. Mag.* **2021**, *21*, 31–56. [CrossRef]
- Sebastian, A.; Le Gallo, M.; Khaddam-Aljameh, R.; Eleftheriou, E. Memory devices and applications for in-memory computing. *Nat. Nanotechnol.* **2020**, *15*, 529–544. [CrossRef]
- Verma, N.; Jia, H.; Valavi, H.; Tang, Y.; Ozatay, M.; Chen, L.Y.; Zhang, B.; Deaville, P. In-Memory Computing: Advances and Prospects. *IEEE Solid-State Circuits Mag.* **2019**, *11*, 43–55. [CrossRef]
- Dong, Q.; Sinangil, M.E.; Erbagci, B.; Sun, D.; Khwa, W.S.; Liao, H.J.; Wang, Y.; Chang, J. 15.3 A 351TOPS/W and 372.4GOPS Compute-in-Memory SRAM Macro in 7 nm FinFET CMOS for Machine-Learning Applications. In Proceedings of the 2020 IEEE International Solid-State Circuits Conference—(ISSCC), San Francisco, CA, USA, 16–20 February 2020; pp. 16–20. [CrossRef]
- Jiang, Z.; Yin, S.; Seo, J.S.; Seok, M. C3SRAM: An In-Memory-Computing SRAM Macro Based on Robust Capacitive Coupling Computing Mechanism. *IEEE J. Solid-State Circuits* **2020**, *55*, 1888–1897. [CrossRef]
- Zhang, J.; Wang, Z.; Verma, N. In-Memory Computation of a Machine-Learning Classifier in a Standard 6T SRAM Array. *IEEE J. Solid-State Circuits* **2017**, *52*, 915–924. [CrossRef]
- Gonugondla, S.K.; Kang, M.; Shanbhag, N. A 42pJ/decision 3.12TOPS/W robust in-memory machine learning classifier with on-chip training. In Proceedings of the 2018 IEEE International Solid - State Circuits Conference—(ISSCC), San Francisco, CA, USA, 11–15 February 2018; pp. 11–15. [CrossRef]
- Rajput, P.J.; Bhandari, S.U.; Wadhwa, G. A Review on—Spintronics an Emerging Technology. *Silicon* **2022**, *14*, 9195–9210. [CrossRef]
- Qin, J.; Sun, B.; Zhou, G.; Guo, T.; Chen, Y.; Ke, C.; Mao, S.; Chen, X.; Shao, J.; Zhao, Y. From Spintronic Memristors to Quantum Computing. *ACS Mater. Lett.* **2023**, *5*, 2197–2215. [CrossRef]
- Kang, W.; Deng, E.; Wang, Z.; Zhao, W. Spintronic Logic-in-Memory Paradigms and Implementations. *Appl. Emerg. Mem. Technol.* **2020**, *63*, 215–229.
- Yu, S.; Chen, P.Y. Emerging Memory Technologies: Recent Trends and Prospects. *IEEE Solid-State Circuits Mag.* **2016**, *8*, 43–56. [CrossRef]
- Finocchio, G.; Di Ventra, M.; Camsari, K.Y.; Everschor-Sitte, K.; Khalili Amiri, P.; Zeng, Z. The promise of spintronics for unconventional computing. *J. Magn. Magn. Mater.* **2021**, *521*, 167506. [CrossRef]
- Ikeda, S.; Hayakawa, J.; Ashizawa, Y.; Lee, Y.M.; Miura, K.; Hasegawa, H.; Tsunoda, M.; Matsukura, F.; Ohno, H. Tunnel magnetoresistance of 604% at 300K by suppression of Ta diffusion in CoFeB/MgO/CoFeB pseudo-spin-valves annealed at high temperature. *Appl. Phys. Lett.* **2008**, *93*, 082508–1–082508–3. [CrossRef]
- Spin-Transfer Torque DDR Products|Everspin. 2023. Available online: <https://www.everspin.com/spin-transfer-torque-ddr-products> (accessed on 17 July 2023).
- Golonzka, O.; Alzate, J.G.; Arslan, U.; Bohr, M.; Bai, P.; Brockman, J.; Buford, B.; Connor, C.; Das, N.; Doyle, B.; et al. MRAM as Embedded Non-Volatile Memory Solution for 22FFL FinFET Technology. In Proceedings of the 2018 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 1–5 December 2018; pp. 1–5. [CrossRef]

23. van den Brink, A.; Cosemans, S.; Cornelissen, S.; Manfrini, M.; Vaysset, A.; Van Roy, W.; Min, T.; Swagten, H.J.M.; Koopmans, B. Spin-Hall-assisted magnetic random access memory. *Appl. Phys. Lett.* **2014**, *104*, 012403. [[CrossRef](#)]
24. Lin, X.; Zhu, L. Magnetization switching in van der Waals systems by spin-orbit torque. *Mater. Today Electron.* **2023**, *4*, 100037. [[CrossRef](#)]
25. Deng, J.; Liang, G.; Gupta, G. Ultrafast and low-energy switching in voltage-controlled elliptical pMTJ. *Sci. Rep.* **2017**, *7*, 1–10. [[CrossRef](#)]
26. Sarwat, S.G. Materials science and engineering of phase change random access memory. *Mater. Sci. Technol.* **2017**, *33*, 1890–1906. [[CrossRef](#)]
27. Long, M.; Zeng, L.; Gao, T.; Zhang, D.; Qin, X.; Zhang, Y.; Zhao, W. Self-Adaptive Write Circuit for Magnetic Tunneling Junction Memory With Voltage-Controlled Magnetic Anisotropy Effect. *IEEE Trans. Nanotechnol.* **2018**, *17*, 492–499. [[CrossRef](#)]
28. Yoshida, C.; Tanaka, T.; Ataka, T.; Hoshina, M.; Furuya, A. Field-free reliable magnetization switching in a three-terminal perpendicular magnetic tunnel junction via spin-orbit torque, spin-transfer torque, and voltage-controlled magnetic anisotropy. *J. Phys. D Appl. Phys.* **2022**, *55*, 365003. [[CrossRef](#)]
29. Wu, H.; Zhang, J.; Cui, B.; Razavi, S.A.; Che, X.; Pan, Q.; Wu, D.; Yu, G.; Han, X.; Wang, K.L. Field-free approaches for deterministic spin-orbit torque switching of the perpendicular magnet. *Mater. Futures* **2022**, *1*, 022201. [[CrossRef](#)]
30. Zhang, K.; Zhang, D.; Wang, C.; Zeng, L.; Wang, Y.; Zhao, W. Compact Modeling and Analysis of Voltage-Gated Spin-Orbit Torque Magnetic Tunnel Junction. *IEEE Access* **2020**, *8*, 50792–50800. [[CrossRef](#)]
31. Wu, Y.C.; Garello, K.; Kim, W.; Gupta, M.; Perumkunnil, M.; Kateel, V.; Couet, S.; Carpenter, R.; Rao, S.; Van Beek, S.; et al. Voltage-Gate-Assisted Spin-Orbit-Torque Magnetic Random-Access Memory for High-Density and Low-Power Embedded Applications. *Phys. Rev. Appl.* **2021**, *15*, 064015. [[CrossRef](#)]
32. Wang, C.; Zhang, D.; Zhang, K.; Zeng, L.; Wang, Y.; Hou, Z.; Zhang, Y.; Zhao, W. Magnetic Nonvolatile SRAM Based on Voltage-Gated Spin-Orbit-Torque Magnetic Tunnel Junctions. *IEEE Trans. Electron Devices* **2020**, *67*, 1965–1971. [[CrossRef](#)]
33. Diény, B.; Chshiev, M. Perpendicular magnetic anisotropy at transition metal/oxide interfaces and applications. *Rev. Mod. Phys.* **2017**, *89*, 025008. [[CrossRef](#)]
34. Shao, Q.; Li, P.; Liu, L.; Yang, H.; Fukami, S.; Razavi, A.; Wu, H.; Wang, K.; Freimuth, F.; Mokrousov, Y.; et al. Roadmap of spin-orbit torques. *IEEE Trans. Magn.* **2021**, *57*, 800439. [[CrossRef](#)]
35. Wang, Z.; Zhao, W.; Deng, E.; Zhang, Y.; Klein, J.O. Magnetic non-volatile flip-flop with spin-Hall assistance. *Phys. Status Solidi RRL* **2015**, *9*, 375–378. [[CrossRef](#)]
36. Lee, H.; Lee, A.; Wang, S.; Ebrahimi, F.; Gupta, P.; Amiri, P.K.; Wang, K.L. Analysis and Compact Modeling of Magnetic Tunnel Junctions Utilizing Voltage-Controlled Magnetic Anisotropy. *IEEE Trans. Magn.* **2018**, *54*, 4400209. [[CrossRef](#)]
37. Grezes, C.; Ebrahimi, F.; Alzate, J.G.; Cai, X.; Katine, J.A.; Langer, J.; Ocker, B.; Khalili Amiri, P.; Wang, K.L. Ultra-low switching energy and scaling in electric-field-controlled nanoscale magnetic tunnel junctions with high resistance-area product. *Appl. Phys. Lett.* **2016**, *108*, 012403. [[CrossRef](#)]
38. Miura, K.; Yabuuchi, S.; Yamada, M.; Ichimura, M.; Rana, B.; Ogawa, S.; Takahashi, H.; Fukuma, Y.; Otani, Y. Voltage-induced magnetization dynamics in CoFeB/MgO/CoFeB magnetic tunnel junctions. *Sci. Rep.* **2017**, *7*, 42511. [[CrossRef](#)] [[PubMed](#)]
39. Song, J.; Ahmed, I.; Zhao, Z.; Zhang, D.; Sapatnekar, S.S.; Wang, J.P.; Kim, C.H. Evaluation of Operating Margin and Switching Probability of Voltage-Controlled Magnetic Anisotropy Magnetic Tunnel Junctions. *IEEE J. Explor. Solid-State Comput. Devices Circuits* **2018**, *4*, 76–84. [[CrossRef](#)]
40. Song, C.; Cui, B.; Li, F.; Zhou, X.; Pan, F. Recent progress in voltage control of magnetism: Materials, mechanisms, and performance. *Prog. Mater. Sci.* **2017**, *87*, 33–82. [[CrossRef](#)]
41. Kang, W.; Ran, Y.; Zhang, Y.; Lv, W.; Zhao, W. Modeling and Exploration of the Voltage-Controlled Magnetic Anisotropy Effect for the Next-Generation Low-Power and High-Speed MRAM Applications. *IEEE Trans. Nanotechnol.* **2017**, *16*, 387–395. [[CrossRef](#)]
42. Kang, W.; Ran, Y.; Lv, W.; Zhang, Y.; Zhao, W. High-Speed, Low-Power, Magnetic Non-Volatile Flip-Flop With Voltage-Controlled, Magnetic Anisotropy Assistance. *IEEE Magn. Lett.* **2016**, *7*, 1–5. [[CrossRef](#)]
43. Zarei, A.; Safaei, F. Power and area-efficient design of VCMA-MRAM based full-adder using approximate computing for IoT applications. *Microelectron. J.* **2018**, *82*, 62–70. [[CrossRef](#)]
44. Zarei, A.; Safaei, F. LIMITA: Logic-in-Memory Primitives for Imprecise Tolerant Applications. *IEEE Trans. Circ. Syst. I* **2021**, *68*, 4686–4699. [[CrossRef](#)]
45. Lau, Y.C.; Betto, D.; Rode, K.; Coey, J.M.D.; Stamenov, P. Spin-orbit torque switching without an external field using interlayer exchange coupling. *Nat. Nanotechnol.* **2016**, *11*, 758–762. [[CrossRef](#)]
46. Fukami, S.; Zhang, C.; DuttaGupta, S.; Kurenkov, A.; Ohno, H. Magnetization switching by spin-orbit torque in an antiferromagnet-ferromagnet bilayer system. *Nat. Mater.* **2016**, *15*, 535–541. [[CrossRef](#)] [[PubMed](#)]
47. Qian, L.; Chen, W.; Wang, K.; Wu, X.; Xiao, G. Spin Hall effect and current induced magnetic switching in antiferromagnetic IrMn. *AIP Adv.* **2018**, *8*, 115323. [[CrossRef](#)]
48. Manchon, A.; Železný, J.; Miron, I.M.; Jungwirth, T.; Sinova, J.; Thiaville, A.; Garello, K.; Gambardella, P. Current-induced spin-orbit torques in ferromagnetic and antiferromagnetic systems. *Rev. Mod. Phys.* **2019**, *91*, 035004. [[CrossRef](#)]
49. Hirohata, A.; Yamada, K.; Nakatani, Y.; Prejbeanu, I.L.; Diény, B.; Pirro, P.; Hillebrands, B. Review on spintronics: Principles and device applications. *J. Magn. Magn. Mater.* **2020**, *509*, 166711. [[CrossRef](#)]

50. Jenkins, S.; Chantrell, R.W.; Evans, R.F.L. Exchange bias in multigranular noncollinear IrMn<sub>3</sub>/CoFe thin films. *Phys. Rev. B* **2021**, *103*, 014424. [[CrossRef](#)]
51. Alla, S.; Kumar Joshi, V.; Bhat, S. Field-free switching of VG-SOT-pMTJ device through the interplay of SOT, exchange bias, and VCMA effects. *J. Appl. Phys.* **2023**, *134*, 013901. [[CrossRef](#)]
52. Thapliyal, H.; Sharifi, F.; Kumar, S.D. Energy-Efficient Design of Hybrid MTJ/CMOS and MTJ/Nanoelectronics Circuits. *IEEE Trans. Magn.* **2018**, *54*, 1–8. [[CrossRef](#)]
53. Zhao, W.; Chappert, C.; Javerliac, V.; Noziere, J.P. High Speed, High Stability and Low Power Sensing Amplifier for MTJ/CMOS Hybrid Logic Circuits. *IEEE Trans. Magn.* **2009**, *45*, 3784–3787. [[CrossRef](#)]
54. Cai, K.; Zhu, Z.; Lee, J.M.; Mishra, R.; Ren, L.; Pollard, S.D.; He, P.; Liang, G.; Teo, K.L.; Yang, H. Ultrafast and energy-efficient spin-orbit torque switching in compensated ferrimagnets. *Nat. Electron.* **2020**, *3*, 37–42. [[CrossRef](#)]
55. Jeong, J.; Ferrante, Y.; Faleev, S.V.; Samant, M.G.; Felser, C.; Parkin, S.S.P. Termination layer compensated tunnelling magnetoresistance in ferrimagnetic Heusler compounds with high perpendicular magnetic anisotropy. *Nat. Commun.* **2016**, *7*, 10276. [[CrossRef](#)]
56. Qin, P.; Yan, H.; Wang, X.; Chen, H.; Meng, Z.; Dong, J.; Zhu, M.; Cai, J.; Feng, Z.; Zhou, X.; et al. Room-temperature magnetoresistance in an all-antiferromagnetic tunnel junction. *Nature* **2023**, *613*, 485–489. [[CrossRef](#)] [[PubMed](#)]
57. Wang, Z.; Zhao, W.; Deng, E.; Klein, J.O.; Chappert, C. Perpendicular-anisotropy magnetic tunnel junction switched by spin-Hall-assisted spin-transfer torque. *J. Phys. D Appl. Phys.* **2015**, *48*, 065001. [[CrossRef](#)]

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