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# Development and 24 Hour Behavior Analysis of a Peak-Shaving Equipment with Battery Storage

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Received: 22 February 2019 ; Accepted: 24 May 2019; Published: 29 May 2019


**Abstract:** This paper presents the development of a peak-shaving equipment, composed by a multilevel converter in a cascaded H-bridge topology and battery banks on the DC links. Between specific time periods, when the demand is higher, the equipment injects active power from the batteries into the grid to provide support to the system. During the other times of the day, when the demand is lower, the converter charges its battery banks with the exceeding (and low producing cost) energy from the grid. The charge and discharge control algorithms are implemented in a digital signal processor (DSP). The precise time of the day information is obtained from a real-time-clock from a global positioning system module (GPS), which communicates with the DSP through the serial interface. This paper presents the control algorithms and experimental results obtained in a 24 h continuous operation of the equipment.

**Keywords:** batteries; energy storage; multilevel converters; peak-shaving

## 1. Introduction

The conventional electrical grid is usually designed with a capacity over its nominal to support peaks in demand. This results in the grid operating on its limits during some periods and well below its maximum capacity, and therefore, with low efficiency, on other periods [1]. In order to increase its efficiency, energy storage systems have been installed. Thus, during low demand periods, the energy is stored to be used later (when the grid is close to its limits). Also, the increase of intermittent renewable energy sources on the grid is another aspect that motivates the use of energy storage systems [2], as they are able to equalize fluctuations and compensate the mismatch of power generation and consumption [3].

A review of energy storage systems is presented in [4]. These systems may store energy under different forms: electrochemical energy (stored in batteries [5] or as hydrogen/fuel cells [6]), magnetic field energy stored in superconducting magnetic energy storage (SMES) [7]), electric field energy (stored in supercapacitors/ultracapacitors [8]), kinetic energy (stored in flywheels [9]), potential energy (stored in pumped hydroelectric storage (PES) [10]), or as compressed air (stored in compressed air energy storage (CAES)) [11]). Each of these systems has its own advantages and disadvantages,

depending on the requirements of the application. According with [12], these requirements can be classified into two main categories: applications requiring high power density (bursts of high power for short periods of time—in these cases, SMES, supercapacitors/ultracapacitors, and flywheels are more appropriate)) and applications requiring high energy density (constant power for larger operation times—in these cases, CAES, PHS, and batteries are more appropriate—although for CAES and PHS the required infrastructure might be an inconvenient).

Concerning a peak-shaving application, it is desired that the storage system be able to inject power in the grid for at least some hours (relatively high energy density) with fast response and relatively easy control. This implies in the battery storage as one of the preferable solutions, as they present very fast response time, high efficiency, low self-discharge, and can be used in a modular structure [3], besides being the most cost-efficient technology for this application [4].

The principle of electricity generation and storage in a battery is presented in [5]. A battery is formed by two electrodes (a cathode and an anode) immersed in an electrolyte. During discharge (electricity generation), the electrons travel from the anode to the cathode through an external circuit (the load). During charge (electricity storage), an external voltage source force the electrons on the reverse path, from the cathode to the anode. Among the popular battery technologies, lead-acid is considered a mature and low-cost technology [13]. On the other hand, it has less energy and power density than other technologies, such as lithium-ion [13]. Due to its high energy-to-weight ratio, lithium-ion is the preferred technology for portable applications and electric vehicles [14]. However, lithium-ion prices are elevated due to limited lithium resources and also due to the required safety protections [14]. Considering a stationary peak-shaving application, the weight of the equipment is not a major concern, but its cost is. Also, the simpler control and robustness of lead-acid batteries is the decisive factor in its favor, concerning the equipment described in the text that follows.

In a recent paper [15], the authors have presented a grid support equipment using a multilevel converter and storage on lead-acid batteries. In that work, the energy injection on the grid was performed based on the real-time monitoring of the installation site voltage. However, an overloaded grid may not present a drop on its voltage readings (e.g., when the transformers are equipped with tap changers). Hence, this present paper is an extension on the former, proposing the injection of energy on predetermined times (that are known to present peaks of demand). Although the DSP TMS320F28335 [16] that controls the equipment has precise timers, after some months from the initial adjustment of time, some error is expected. This error tends to increase as months pass by—culminating to a point where the equipment might inject power outside the peak times and, worse, charge the batteries when the grid is already overloaded. Considering that this equipment might be installed at the end of a long radial line, maybe in rural areas, it is imperative that the adjustment of clock time occurs automatically, without operator intervention. Aiming energy injection to the grid on a precise time interval and batteries charging also on precise times, a real-time-clock (RTC) from a GPS module [17] has been used. This module communicates with the DSP from one of its serial UART interfaces.

Some preliminary results of the equipment using the GPS module have been submitted to a Brazilian conference [18], however, due to the limited length of that paper, only a few details about the implementation were presented. Moreover, both [18] and [15] were written in Portuguese, and thus are restricted to only a fraction of readers. This present paper is an extension of both, presenting details on the serial communication between the GPS module and the DSP, the algorithm to decode the received time information and the algorithm to control charge and discharge of the batteries (including a protection against over-discharge), hence all the details needed for a proper replication of the presented results. This extension also presents a 24-hour analysis of the equipment operation, including all stages of battery operation. This present paper is also intended to serve as a reference design for more complex applications in the field of energy storage, presenting in detail all necessary implementation blocks. Section 2 presents a detailed description of the developed equipment, including all algorithms and control loops. Section 3 presents a procedure of serial communication between the GPS module

and the TMS320F28335 DSP, including an algorithm to decode the received time information and determine the amount of power to be injected on the grid. Section 4 presents the experimental setup. Section 5 presents the experimental results, obtained during a 24 h continuous operation of the setup.

## 2. Developed Equipment for Peak-Shaving

Figure 1 presents an overview of the control of the developed equipment. Its electrical circuit is presented in Figure 2. This equipment is composed by a multilevel converter in a cascaded H-bridge topology. Each bridge has a bank of lead-acid batteries on its DC link. The algorithms for battery charge and discharge are presented in Section 2.1. These algorithms generate a reference value for the AC on the converter side of the transformer ($i_S'$). As this current must be in phase with the installation site voltage ($v_S$), a phase-locked-loop (PLL) must be used. The algorithm of the PLL is presented in Section 2.2. A current control loop is also required to guarantee that the measured $i_S'$ follows exactly its reference. A proportional plus resonant (PR) controller to perfectly track the current reference is presented in Section 2.3. The output of the PR controller represents the reference voltage at the output of each of the H-bridges ($v_1$, $v_2$ and $v_3$). A procedure for the implementation of multilevel pulse width modulation (PWM) based on phase-shifted triangular carriers is presented in Section 2.4.

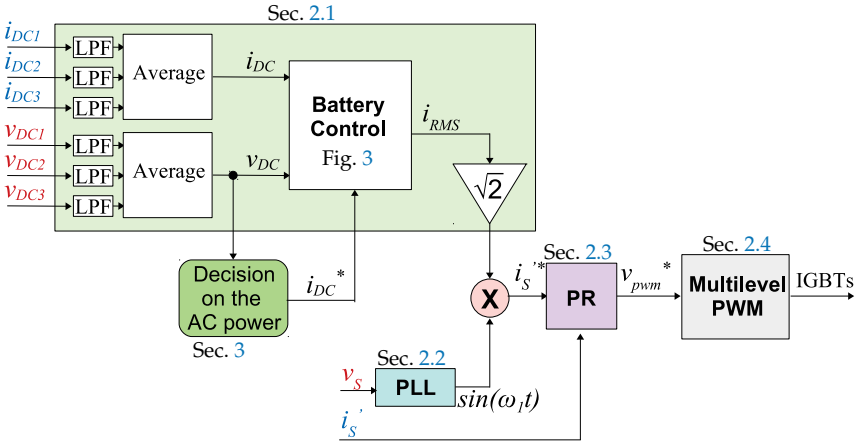


**Figure 1.** Overview of the control of the developed equipment.

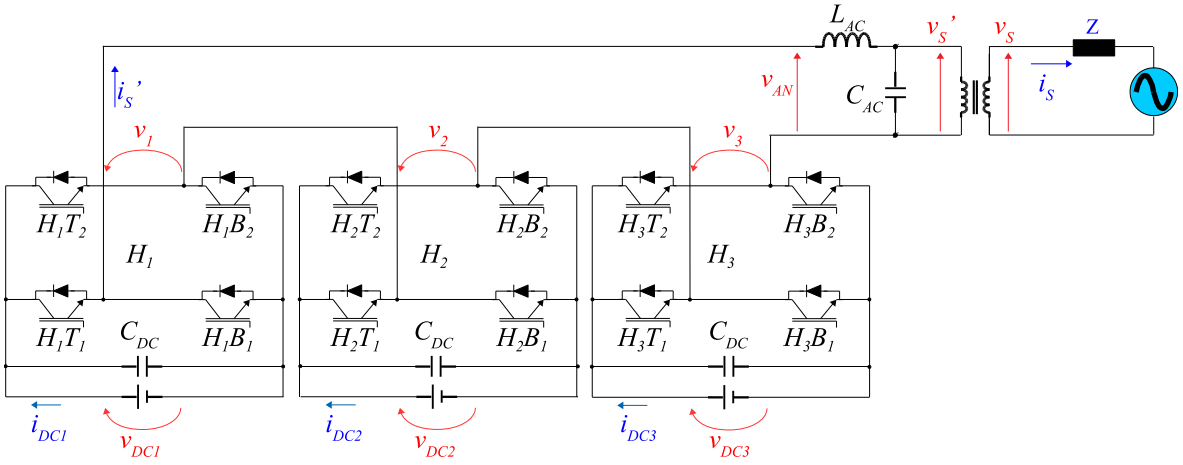


**Figure 2.** Electrical circuit of the developed equipment.

### 2.1. Batteries Charge and Discharge Control

As described in [15], the charging process for the lead-acid type of battery has three distinct stages:

- *Stage I*: The battery voltage $v_{DCx}$ (where $x$ indicates the bridge number) increases gradually, while a constant current $i_{DCx}$ is imposed by the controller;

- *Stage II*: The battery voltage is kept constant by the controller, while its current drops to near zero;
- *Stage III*: The battery voltage is kept constant by the controller, while a minimum current is drawn only to maintain the charge. At this stage, the battery is already fully charged and is said to be "floating".

Both DC voltages $v_{DCx}$ and DC $i_{DCx}$ are controlled indirectly by acting on the AC $i_S{}'$. Following the sign convention adopted in Figure 2, if the converter is controlled to draw an AC $i_S{}'$ 180° out of phase in relation to the supply voltage $v_S$ (in order to obtain the phase reference from $v_S$, a PLL (discussed in Section 2.2) has been used), the resulting DC will be negative—thus charging the batteries and increasing the DC voltages. Conversely, if the converter is controlled to draw an AC $i_S{}'$ in phase with the supply voltage $v_S$, the resulting DC will be positive—thus discharging the batteries and reducing the DC voltages. The amplitude of the AC can be controlled by small increments/decrements of a step-size $\Delta i_{RMS}$. Based on this principle, Figure 3 presents a simple algorithm that implements all three stages of charge and also the discharge.

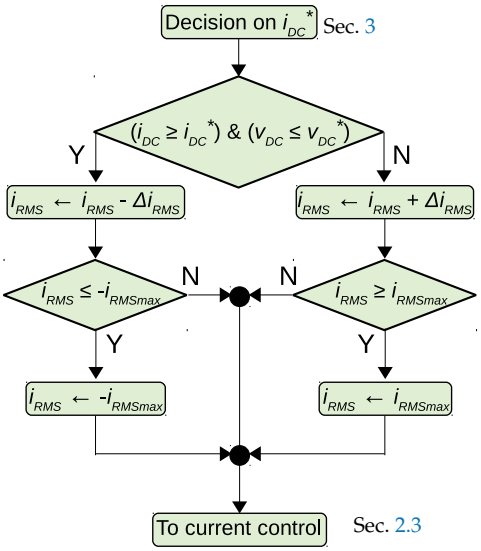


**Figure 3.** Algorithm for battery control.

Both the DC voltages $v_{DCx}$ and DC $i_{DCx}$ on each bridge have ripples imposed on their average values. To extract their average values, each of these signals pass through digital low pass filters LPF blocks on Figure 1). Then, a simple arithmetic average is performed between the low-pass-filtered voltages to obtain the average DC voltage $v_{DC}$ and between the low-pass-filtered currents to obtain the average DC $i_{DC}$.

While in *stage I*, the average DC voltage $v_{DC}$ is lower than its reference value $v_{DC}{}^*$. If the average DC $i_{DC}$ is greater or equals its reference value $i_{DC}{}^*$ (i.e., $i_{DC}$ is less negative than $i_{DC}{}^*$), then the converter must decrease (or increase negatively) the amplitude of its AC by small increments $\Delta i_{RMS}$ in order to obtain a more negative average DC $i_{DC}$. Otherwise, if $i_{DC}$ is more negative than $i_{DC}{}^*$, the converter must increase (or decrease negatively) the amplitude of its AC by small increments $\Delta i_{RMS}$ in order to obtain a smaller negative average DC $i_{DC}$. In both cases, saturations can be imposed if $i_{RMS}$ is smaller than its minimum allowed value $-i_{RMSmax}$ or greater than its maximum allowed value $i_{RMSmax}$.

The same logic applies to *stage II* and *stage III*. While in these stages, the average DC $i_{DC}$ is greater than its reference value $i_{DC}{}^*$ (i.e., $i_{DC}$ is less negative than $i_{DC}{}^*$). If the average DC voltage $v_{DC}$ is smaller or equals its reference value $v_{DC}{}^*$, then the converter must decrease (or increase negatively) the amplitude of its AC by small increments $\Delta i_{RMS}$ in order to increase the average DC voltage $v_{DC}$. Otherwise, if $v_{DC}$ is greater than $v_{DC}{}^*$, then the converter must increase (or decrease negatively) the

amplitude of its AC by small increments $\Delta i_{RMS}$ in order to decrease the average DC voltage $v_{DC}$. In both cases, the $i_{RMS}$ value is kept between $-i_{RMSmax}$ and $i_{RMSmax}$ by saturation.

While in discharge mode, the reference value for DC $i_{DC}{}^*$ is positive and is controlled in the same manner through increments/decrements on the AC RMS reference value $i_{RMS}$. Usually, during discharge, the average DC voltage $v_{DC}$ is lower than its reference value $v_{DC}{}^*$. If the average DC $i_{DC}$ is greater or equals its reference value $i_{DC}{}^*$, then the converter must decrease the amplitude of its AC by small increments $\Delta i_{RMS}$ in order to obtain a smaller average DC $i_{DC}$. Otherwise, if $i_{DC}$ is smaller than $i_{DC}{}^*$ or if $v_{DC}$ is greater than $v_{DC}{}^*$, the converter must increase the amplitude of its AC by small increments $\Delta i_{RMS}$ in order to obtain a higher average DC $i_{DC}$. Also, in all cases, the $i_{RMS}$ value is kept between $-i_{RMSmax}$ and $i_{RMSmax}$ by saturation.

Given a proper AC RMS reference value $i_{RMS}$, obtained through the flowchart of Figure 3, its peak value is obtained by a simple multiplication by $\sqrt{2}$. It is clear that, in order to guarantee the correct active power flow, the phase angle of the AC must match the phase angle of the installation site voltage $v_S$, either as 0° in the battery discharge or as 180° in the battery charge modes. This is achieved by the multiplication of the obtained AC peak reference with the output of a PLL block (discussed in Section 2.2). The resulting signal is the reference value for the AC current controller (discussed in Section 2.3).

### 2.2. Phase Locked Loop

In order to achieve proper synchronization between the AC and the installation site voltage, a PLL must be used. A digital implementation of a PLL is presented in [19]. This implementation has the advantage that it can be used on single-phase systems, does not require a PI controller and has a fast dynamic response. Its block diagram is presented in Figure 4.

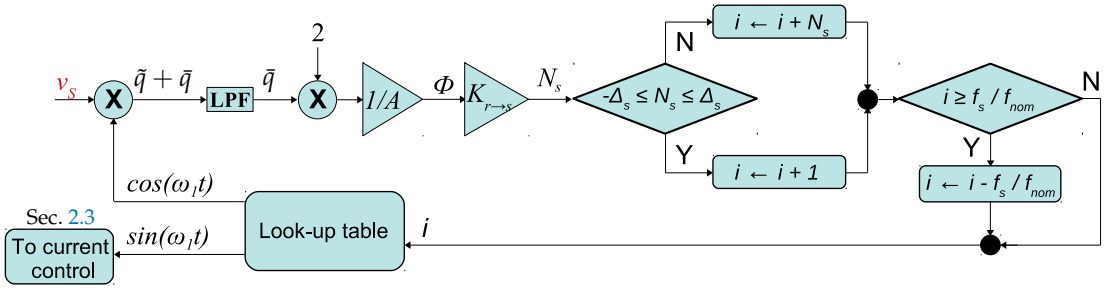


**Figure 4.** PLL to synchronize the AC with the installation site voltage.

The installation site voltage $v_S$ is multiplied by the feedback quadrature output (which has an initial phase $\Phi$ in relation to $v_S$). This results in a signal composed by an oscillating component ($\tilde{q}$) and a constant component ($\bar{q}$). A low-pass filter is used to extract only the constant component. In [19] a mathematical analysis shows that this constant component relates to the phase difference between the PLL output and the input voltage $\Phi$ as (1).

$$2 \cdot \bar{q} = A \cdot \sin(\Phi) \Rightarrow \frac{2 \cdot \bar{q}}{A} = \sin(\Phi) \approx \Phi \,, \tag{1}$$

where $A$ is the nominal amplitude of the installation site voltage.

The phase error $\Phi$ is converted from radians to number of samples $N_s$ (where the conversion ratio is given by (2)), in order to shift a pointer $i$ in a look-up table of sine/cosine functions proportionally to the error.

$$K_{r\to s} = \frac{f_s}{f_{nom} \cdot 2 \cdot \pi} \,, \tag{2}$$

where $f_s$ is the sampling frequency and $f_{nom}$ is the nominal frequency of the installation site voltage.

When the estimated angle $\omega_1 t$ is close enough to the voltage angle, the phase error $\Phi$ will be near zero and the number of samples in the look-up table differing from the correct one will be small.

The maximum error allowed is $\Delta_s$, lagging or leading. For $f_s = 10$ kHz, $\Delta_s$ has been set as 1 sample. For higher sampling frequencies, this tolerance can be increased. If the number of samples of error is between the tolerance band (from $-\Delta_s$ to $\Delta_s$), then PLL is said to be *locked* with $v_S$ and the index $i$ on the look-up table can be increased by one, pointing to the next correct sample. However, if the error is outside the tolerance band, the index $i$ is increased by $N_s$ samples, forcing the convergence.

An excursion from 0 to $f_s/f_{nom}$ (which is the number of samples in one complete cycle of the nominal frequency) is allowed for the pointer $i$. Whenever an increment in $i$ results in a value outside this range, a subtraction of $f_s/f_{nom}$ makes it return to the corresponding position inside the buffer.

Finally, the resulting value $i$ points to the correct value of two outputs in the pre-allocated look-up table. One of the outputs is the quadrature signal $\cos(\omega_1 t)$, that is feedback to the next cycle of estimation. The other output, $\sin(\omega_1 t)$ is a perfectly sinusoidal signal, varying from $-1$ to 1 in amplitude and in phase with the installation site voltage $v_S$. This signal is multiplied by the amplitude of the AC current (determined in Section 2.1). The result is the sampled time-domain reference value to the current control (discussed in Section 2.3).

### *2.3. AC Control Loop*

The multiplication of the amplitude reference of the AC (from Section 2.1) with the unity vector synchronized with the installation site voltage (from Section 2.2) results in the reference AC ${i_S}'^*$ on the converter side of the transformer of Figure 2. A current control loop is required to guarantee that the measured ${i_S}'$ follows correctly this reference. Another important point to consider is that the gate drivers of the H-bridges, in order to avoid simultaneous conduction of the IGBTs in the same leg, introduce a dead-time on the PWM pulses. This dead-time, if not compensated, may introduce distortions on the measured current. Thus, the goal of the current controller is to perfectly track the component at the fundamental frequency responsible for battery charge/discharge and also compensate for the harmonic distortions caused by the dead-time.

For three-phase systems, usually, the control is performed on a d-q reference frame, thus the control variables are constant in relation to time, hence PI controllers have been used without major issues. However, for single-phase systems, the d-q reference frame is not achievable without adaptations. Thus the control variables have sinusoidal components, that cannot be tracked properly by PI controllers without a steady state error.

In order to properly track sinusoidal references, a PR (Proportional plus Resonant) controller can be used. This controller, presented in Figure 5 in its continuous form, is composed by a proportional gain $k_P$ and resonant transfer functions tuned on each sinusoidal component desired to be compensated. It is desired that the fundamental component of the measured current ${i_S}'$ follows exactly its reference value ${i_S}'^*$. However, it is also desired that the harmonic components caused by the PWM dead-time be minimized. Thus, the reference input of the controller contains only the fundamental component from ${i_S}'^*$, while the harmonic components reference are set to zero. The difference between the desired ${i_S}'^*$ and the measured ${i_S}'$ is the error signal $e$, which is amplified by the gain $k_P$ (in order to act on the transient response) and by the resonant transfer functions at the desired frequencies (in order to act on the steady-state response). Each of the resonant transfer functions is defined by a gain $k_{Rh}$ and a resonance frequency $\omega_h = h \cdot 2 \cdot \pi \cdot f_{nom}$, where $h$ is the harmonic order.

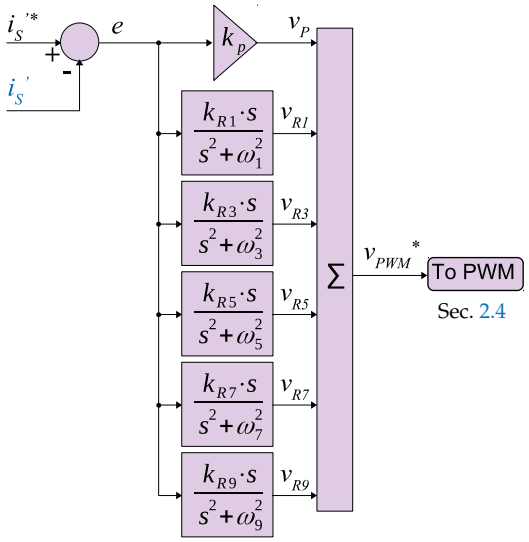


**Figure 5.** Proportional plus resonant current controller on continuous domain.

In a DSP, the continuous domain controller of Figure 5 is implemented as the difference Equation (3), according to the discretization procedure presented in [20].

$$v_{PWM}{}^*(t) = k_P \cdot e(t) + \sum_h b_h \cdot k_{Rh} \cdot [e(t) - e(t-2)] - \sum_h [a_{1h} \cdot v_{Rh}(t-1) + a_{2h} \cdot v_{Rh}(t-2)] \ , \quad (3)$$

where $a_{1h}$, $a_{2h}$ and $b_h$ are parameters defined by (4), dependent on the sampling time $T_s = 1/f_s$ and the resonant frequency $\omega_h$ for each $h = 1, 3, 5, 7, 9$.

$$\begin{cases} a_{0h} = 4/T_s^2 + \omega_h^2 \ ; \\ a_{1h} = \left[-8/T_s^2 + 2 \cdot \omega_h^2\right] / a_{0h} \ ; \\ a_{2h} = 1 \ ; \\ b_i = [2/T_s] \, / a_{0h} \ . \end{cases} \quad (4)$$

The output $v_{PWM}{}^*$ is the reference voltage of the multilevel PWM modulator (discussed in Section 2.4).

### *2.4. Multilevel Pulse Width Modulation*

The reference voltage generated by the current controller (from Section 2.1) must be reproduced by the multilevel converter of Figure 2. In order to do so, the IGBTs from each H-bridge must chop each of the DC voltages, in a controlled fashion, to achieve output voltages whose average values are proportional to the input reference. Hence, the control pulses of the IGBTs must have their width modulated proportionally to the reference voltage, in a process known as pulse width modulation (PWM). Figure 6 presents a graphical procedure for the generation of PWM pulses for a seven-level converter, using phase-shifted triangular carriers. One of the well-known methods of PWM in H-bridges, is the *unipolar* PWM by comparison of the reference signal with two triangular carriers (180° out of phase from each other), as presented in ([21], pp. 215–218). The name *unipolar* came from the fact that the output voltage at each H-bridge switches from only one pole at a time, between $+v_{DC}$ and zero and between $-v_{DC}$ and zero, as shown in the plots $v_1$, $v_2$ and $v_3$ of Figure 6. An extension of this method to multilevel converters is presented in ([22], pp. 127–131), adding a phase-shift on the carriers of each bridge. The sum of the individual output voltages connected in series results in the staircase pattern seen in the plot $v_{AN}$ of Figure 6, due to the phase-shifts on each voltage transition.

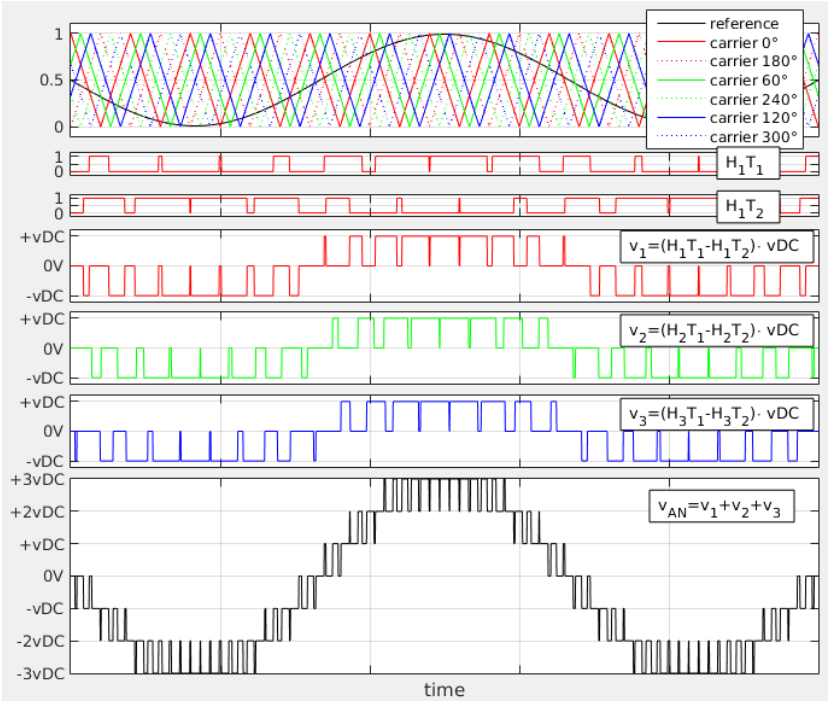


**Figure 6.** Graphical procedure for the PWM generation through comparison with phase-shifted carriers.

The top plot of Figure 6 presents the reference signal to the PWM modulator and the triangular carriers. The two carriers for the bridge $H_1$ are represented in red color. The two carriers for the bridge $H_2$ are represented in green color. The two carriers for the bridge $H_3$ are represented in blue color. For each bridge, the two carriers are 180° out of phase from each other, where the ones plotted in continuous lines control the first leg (IGBTs $H_xT_1$ and $H_xB_1 = \overline{H_xT_1}$) and the ones plotted in dotted lines control the second leg (IGBTs $H_xT_2$ and $H_xB_2 = \overline{H_xT_2}$). From one bridge to the other, there must be a phase difference relating to the number of H-bridges in the converter ($H$), as $180°/H$. Hence, for three bridges, the carriers from one bridge to the other must be 60° out of phase.

The *unipolar* PWM rules apply for each of the bridges. Thus, whenever the reference signal is greater than the corresponding continuous line carrier, the gate signal $H_xT_1$ will receive a logic level 1. Also, whenever the reference signal is less than the corresponding dotted line carrier, the gate signal $H_xT_2$ will receive a logic level 1. From the circuit of Figure 2, the output of each bridge $v_x$ is the equivalent of the subtraction of the gate pulses ($H_xT_1 - H_xT_2$) multiplied by the DC voltage. The converter output voltage $v_{AN}$ is the result of the sum of all series H-bridge individual output voltages. Due to the effect of the phase-shift in the carriers, the transitions in the individual output voltages $v_x$ are also phase-shifted, which results in the staircase pattern on $v_{AN}$. The number of voltage levels at the resulting output $v_{AN}$ is related to the number of H-bridges used in the converter as $2 \cdot H + 1$. Hence, for three bridges, the number of voltage levels at the output of the converter is equal to seven ($+3v_{DC}$, $+2v_{DC}$, $+1v_{DC}$, 0V, $-1v_{DC}$, $-2v_{DC}$ and $-3v_{DC}$).

The TMS320F28335 DSP has six independent PWM modules, implemented in hardware—thus, no processing resources are wasted in the generation of the PWM pulses. Each of the six modules has a programmable counter, equivalent to each of the six carriers of Figure 6. The options of comparison are set by programmable registers. The documentation on these modules is presented in [23]. Concerning multilevel phase-shift PWM, some specific configurations are required, which are presented in [24].

## 3. Decision on the AC Power

In order to establish a proper DC reference for the battery control (described in Section 2.1) the algorithm of Figure 7 is proposed. It is based on the precise information on the time of the day, that is received from an Adafruit GPS module [17] via UART serial communication (Section 3.1). Once

powered up, the GPS module starts to continuously send commands in the *NMEA 0183* [25] standard. The *NMEA 0183* commands are decoded and the time of the day is extracted (Section 3.2).

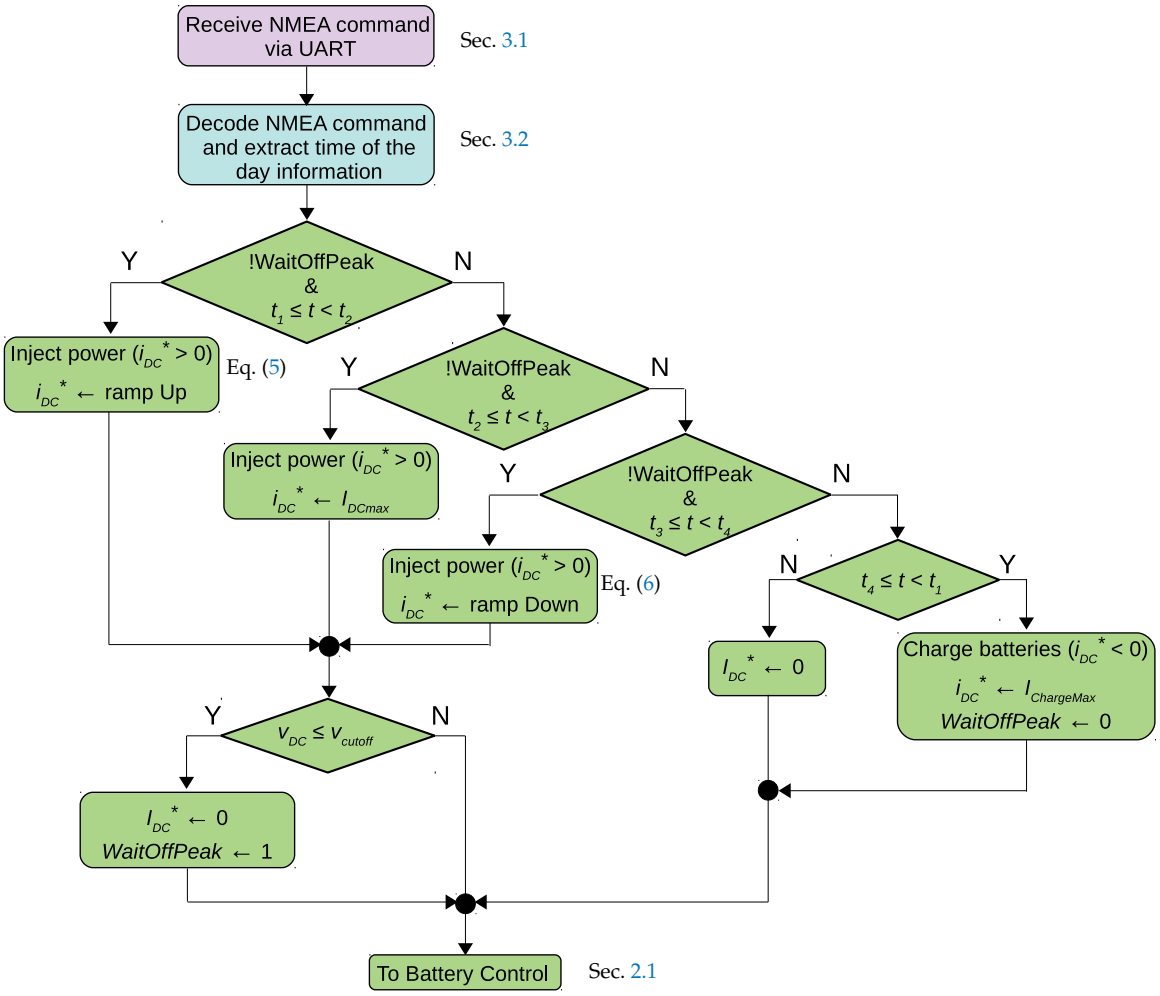


**Figure 7.** Algorithm to establish the reference DC.

The flowchart of Figure 7 establishes four time intervals, where different values for the reference DC ${i_{DC}}^*$ are chosen on each one of them. From $t_1$ until $t_2$, the utility company is entering the peak time, thus the current injection on the grid starts with a reference ${i_{DC}}^* = 0A$ to battery control algorithm (Section 2.1) at $t = t_1$ and increases in ramp, following Equation (5), until reaching the maximum DC reference value ${i_{DC}}^* = I_{DCmax}$ (which corresponds to the maximum rating of the equipment) at $t_2$. From $t_2$ until $t_3$, it is the peak time, thus the equipment remains injecting its maximum current. From $t_3$ until $t_4$, the utility company is leaving the peak time, thus the current injection on the grid starts with its maximum reference at $t = t_3$ and decreases in ramp, following Equation (6), until reaching the zero DC reference value at $t_4$.

$$ {i_{DC}}^* = I_{DCmax} \cdot \frac{t - t_1}{t_2 - t_1} \, . \tag{5} $$

$$ {i_{DC}}^* = I_{DCmax} \cdot \left( 1 - \frac{t - t_3}{t_4 - t_3} \right) \, . \tag{6} $$

From $t_4$ until $t_1$ of the next day, the equipment is charging its batteries. During the whole *stage I* of battery charging, the DC reference value is the constant $I_{ChargeMax}$ (with negative polarity). Then, during *stage II* and *stage III*, the battery control acts on the DC voltage.

Although the control of lead-acid batteries is very flexible and safe, in order to maintain their lifetime, some care is still necessary, as the prevention of overcharge (which is performed in Figure 3, while keeping the measured $v_{DC}$ below the floating voltage $v_{DC}{}^{*}$) and over-discharge (introduced in Figure 7).

To avoid over-discharge the battery, while in discharge mode, the measured voltage $v_{DC}$ must not fall below the battery cut-off voltage $v_{cutoff}$. Under normal circumstances, if the ratings of the equipment are well designed, this is a condition that is not supposed to happen. However, Figure 7 presents a protection against over-discharge. If the condition $v_{DC} \leq v_{cutoff}$ is detected, the DC reference is immediately cut to zero and a flag *WaitOffPeak* is set. This flag remains active until the end of the peak time, in order to avoid charging the batteries when the grid is lacking resources. Then, after the end of the peak time, at $t_4$, the batteries are recharged.

It is important to note that the chosen profile for power injection on the grid, is based on estimations concerning Brazilian residential consumer data, as those presented in [26]. However, the algorithm can be easily adapted to different scenarios.

### *3.1. UART Serial Communication between the Adafruit GPS Module and the TMS320F28335 DSP*

When powered up, the Adafruit GPS module [17] starts sending NMEA codes [25] through its *TX* output pin with a baud rate of *9600bps*, *8 data bits*, *no parity bits* and *1 stop bit* (*8N1*). The NMEA codes are composed of ASCII characters, always starting by the characters *$* or *!* (in case of the Adafruit GPS module, only the *$* starts codes) and always ending with the characters <*CR*> (carriage return, coded in hexadecimal as *0x0D*) followed by <*LF*> (line feed, coded in hexadecimal as *0x0A*). After the *$* character, there are five characters that identify the NMEA command. The complete list of the standard NMEA commands can be seen in [25]; however each vendor can use only a few of them. In case of the Adafruit GPS module, the commands that are sent are *GPGGA*, *GPGSA*, *GPRMC*, and *GPVTG*—each of them carrying some specific information in the characters that follow, until the <*CR*><*LF*> characters. Specifically for the algorithm of Figure 7, only the information of the time of the day is required. This information is easily extracted from the *GPRMC* command, as shown in Section 3.2. The remainder of this current subsection deals with the setup of UART serial communication on the TMS320F28335 DSP. Thus, for readers using another type of DSP/microcontroller, the instructions given may not apply and they may skip to Section 3.2. In this case, the specific documentation on their platform must be consulted in order to achieve a *8N1-9600bps* serial communication with the GPS module.

The TMS320F28335 has three SCI (Serial Communication Interface) modules that implement the UART protocol with some extra features not necessary in this project. Each of these three interfaces, called *A*, *B*, and *C*, has its own *TX* pin (from which the DSP sends data) and *RX* pin (from which the DSP receives data) multiplexed with general purposed I/O pins (GPIO). Thus, the *TX* pin from the GPS module must be connected to one of the *RX* pins on the DSP. Specifically for this project, the *SCI-C* is being used, whose *RX* pin is multiplexed with *GPIO62*.

The procedure to configure *SCI-C* is summarized in Figure 8. The first step is to configure the multiplexers in order to use *GPIO62* pin as the reception to *SCI-C*. This is performed writing the binary value $01_2$ on *bits 29-28* of the register *GPBMUX2* ([27], p. 76). When using the *ControlSuite* libraries, this is easily performed with the first C instruction presented in Figure 8, where the decimal value $1_{10}$ (equivalent to the binary $01_2$) is written to an organized *struct*. It is important to note that, when using the *ControlSuite* libraries, it is not necessary to access the registers by their memory address nor to know the specific bits, as the library uses mnemonic aliases that are more intuitive to the user.

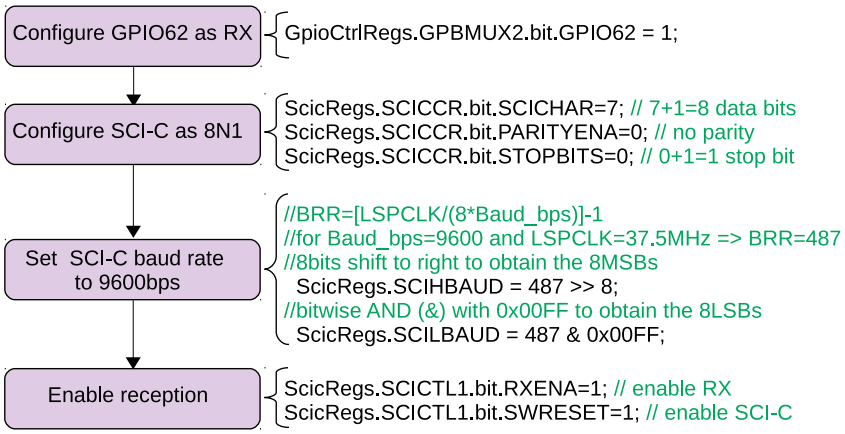


**Figure 8.** Initialization procedure for SCI-C (using the *ControlSuite* libraries).

The second step in the procedure of Figure 8 is to configure the serial data frame of *SCI-C* as *8N1*. This is performed acting on bits *7* (to configure the number of stop bits), *6-5* (to configure parity bits) and *2-0* (to configure the number of data bits) of register *SCICCR* ([28], pp. 26–27). When using the *ControlSuite* libraries, the bit field *SCICHAR* addresses directly the bits *2-0*. The decimal value written to this field is the desired number of data bits minus one—hence, for 8 data bits, $SCICHAR = 7$. The bit field *PARITYENA* addresses the bit *5*. With a zero written on it, the value of bit *6* (that would set parity to odd or even) is disregarded—hence, for no parity, $PARITYENA = 0$. The bit field *STOPBITS* addresses bit *7*. The decimal value written to this field is the desired number of stop bits minus one—hence, for 1 stop bit, $STOPBITS = 0$.

The third step in the procedure of Figure 8 is to configure the baud-rate of *SCI-C* as *9600bps*. The baud-rate is configured in two 8-bit registers concatenated as a 16-bit word ($BRR$): *SCIHBAUD* (with the 8 most significant bits) and *SCILBAUD* (with the 8 least significant bits) ([28], p. 30). The relationship between the desired baud-rate in bps ($Baud_{bps}$) and the 16 bit word ($BRR$) is defined in (7) and is dependent on the internal clock that controls the SCI module ($LSPCLK$). Considering a $LSPCLK = 37.5$ MHz and a desired $Baud_{bps} = 9600$ bps, then $BRR = 487$. In C language, a simple way to extract the 8 most significant bits out of a 16-bit number is an 8-bit shift to the right, using the operator »8. Also, the the 8 least significant bits can be extracted with a bit-wise *AND* operation (using the operator &) with a bit mask of ones (in hexadecimal, $0x00FF$).

$$BRR = \frac{LSPCLK}{8 \cdot Baud_{bps}} - 1\,. \tag{7}$$

Finally, reception through the SCI-C can be enabled on register *SCICTL1*: *bit 0* to enable the reception line RX and *bit 5* to put the SCI-C out of the reset condition ([28], pp. 28–29). When using the *ControlSuite* libraries, the bit field *RXENA* addresses directly the bit *0* and the bit field *SWRESET* addresses directly the bit *5*. Both must be written with a value *1* to enable the reception.

The procedure of Figure 8 is executed only once, during initialization of the DSP. Then, during normal execution of the complete control algorithm of Figure 1, inside a real-time infinite loop, the DSP is constantly receiving data from the GPS. The area in memory where the received 8-bit data are stored are the *bits 7-0* of the register *SCIRXBUF* (called *RXDT*). These data can be accessed, using the ControlSuite libraries as *ScicRegs.SCIRXBUF.bit.RXDT*. Whenever new data have arrived in *RXDT*, the *bit 6* of the register *SCIRXST* (called *RXRDY*) is set. This bit can be accessed as *ScicRegs.SCIRXST.bit.RXRDY*. Figure 9 presents a flowchart to get the received 8-bit characters from *RXDT* and group them in a string that contains the NMEA command from the GPS.

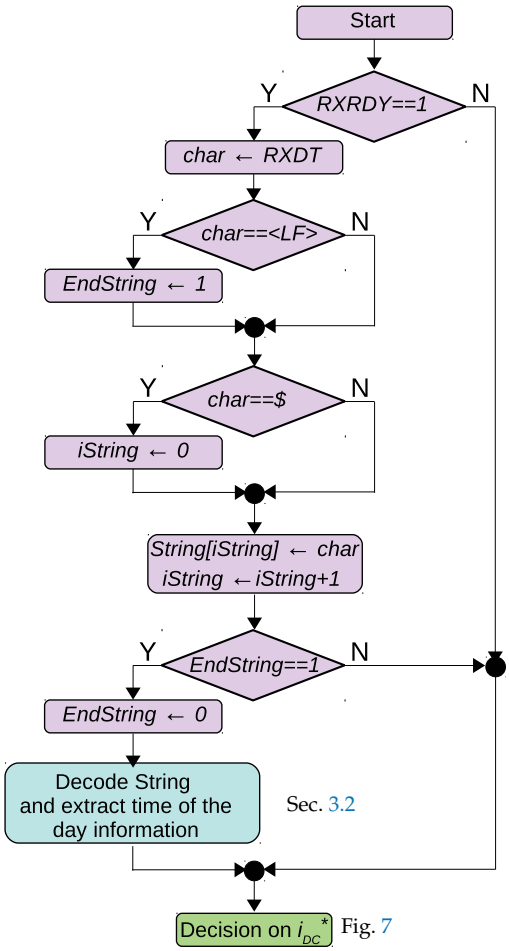


**Figure 9.** Algorithm for reception of NMEA command on the TMS320F28335 DSP.

At each real-time computing cycle (executed at each $T_s = 1/f_s$) the *RXRDY* bit is tested to check if a new character has arrived from the GPS. If the test results in false, then the processor continues to the previously explained algorithms. However, if the test results in true, it means that a new valid 8-bit character has arrived in *RXDT*. This value is stored in a variable *char*. As explained previously, an NMEA command sent through the Adafruit GPS module will always start with the character *$* and end with the character <*LF*> (Line Feed). Hence, these two possibilities must be tested. If the received character is the <*LF*>, then a flag EndString is set to indicate that the NMEA command has been fully received and can be processed (in Section 3.2). If the received character is the *$*, then the index (*iString*) that points to the characters forming the string (*String*) returns to zero to start a new command. In all cases, the received character *char* is grouped in the string *String* and the index *iString* is increased by one.

### 3.2. Decoding of GPS Commands

Once the NMEA command is properly received (Section 3.1) through the serial UART channel, the time of the day information can be extracted from it. From the possible NMEA commands sent by Adafruit GPS module, the time of the day can be extracted from the *$GPRMC* command. This command also carries some additional information, but not necessary for this application. The time of the day information is located in the first 18 characters (from 0 to 17) of the *$GPRMC* command, in the format given in Table 1. The character on the index *17* carries the information about synchronism between the GPS module and the satellites, a condition known in the GPS jargon as *FIX*. If the character *17* is *A*, then the *FIX* is established and time information is valid. Otherwise, the whole string can be ignored, as the time of the day would be invalid.

**Table 1.** Characters of interest in the *$GPRMC* command.

| iString | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | ... |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| String[] | $ | G | P | R | M | C | , | h | h | m | m | s | s | . | s | s | , | A | , | ... |

Figure 10 presents a flowchart to decode the received string and extract the time of the day information. The first six characters (from *0* to *5*) are compared with the string *"$GPRMC"* (in the C language this is performed using the function *strncmp()*). If the test results in false, then a command other than the *GPRMC* has been received and will be ignored. In this case, the processor continues with the algorithm of Figure 7. If the comparison with *"$GPRMC"* results in true, then the character in index *17* of the received string is compared with the character *"A"*. If the test results in false, then this is an indication that the GPS is not synchronized with the satellites and the time of the day would be invalid. In this case, the processor continues with the algorithm of Figure 7. If the comparison with the character *"A"* results in true, then the characters in indexes from *7* to *15* are valid and can be extracted.

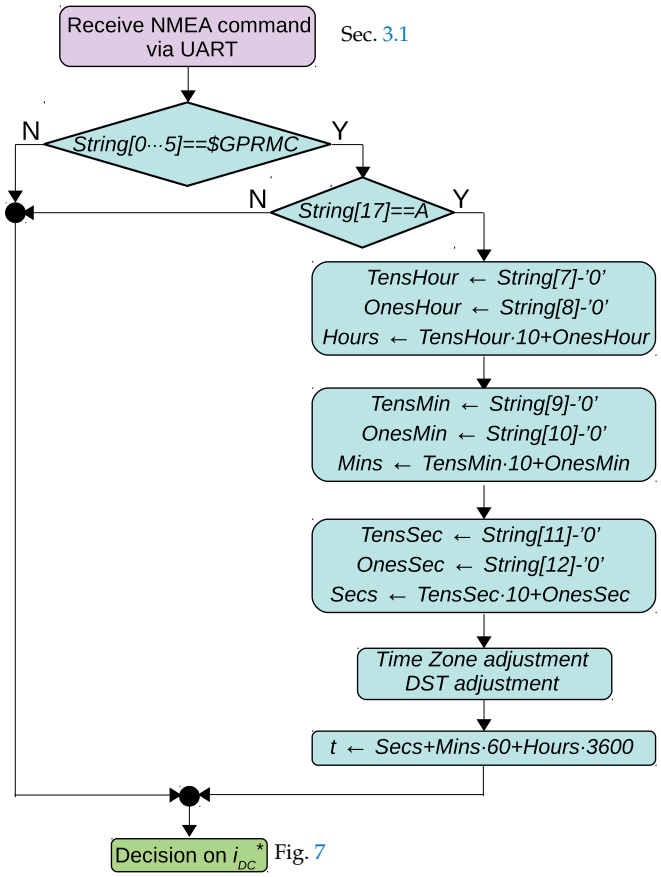


**Figure 10.** Algorithm for decoding of NMEA command and extraction of time of the day.

The characters from *7* to *15* contain the time information in the format *hhmmss.ss*. However, they are a string of ASCII characters representing numbers—and not arithmetic numbers, that could be used in arithmetic operations. The conversion from an ASCII number to an arithmetic number, in the C language, is easily performed with the subtraction of the ASCII code *"0"* from the original ASCII character code.

The character of index *7* represents the tens of hours, while the character of index *8* represents the ones of hours. After the conversion from ASCII to arithmetic number, the number of hours is computed by attribution of a weight of 10 to the tens and a weigh of 1 to the ones. The same procedure is repeated for the minutes and seconds. The characters of indexes *14* and *15*, representing the tenths and hundredths of seconds can be ignored.

The time obtained from the satellites is always in reference to the UTC (Coordinated Universal Time). Thus a time zone adjustment must be performed, adding or subtracting the local offset. Also the received time is not automatically adjusted in case of *Daylight Saving Time* (DST). This adjustment must be performed, adding or subtracting one hour, according to predefined dates.

Finally, the time $t$ is calculated as the *number of seconds after midnight*, since this simplifies the comparisons with the predefined peak time intervals $t_1$, $t_2$, $t_3$, and $t_4$ (in the algorithm of Figure 7), grouping hours, minutes and seconds into a single numerical variable. This value is obtained by the sum of the seconds with the minutes multiplied by 60 and the hours multiplied by 3600.

## 4. Experimental Setup

Figure 11 presents a photo of the test setup, with the identification of its elements in Table 2. The details at the right of the figure present the front side of the H bridges (manufactured by a Brazilian vendor called *Supplier*) and a zoom on the GPS board. In order to input the analog signals indicated in Figure 1 into the DSP, Hall effect sensors (indicated as numbers *3*, *5*, *7*, *9*, *11*, *13*, *15*, and *17*) are used for both DC and AC voltages and currents. Signal conditioning circuits with operational amplifiers (indicated as numbers *4*, *6*, *8*, *10*, *12*, *14*, *16*, and *18*) are used in order to provide gains and offsets that fit the signals into the 0 V∼3 V analog inputs of the DSP. The signals are sampled at $f_s = 10$ kHz and processed through the general algorithm presented in Figure 1. The PWM module of the DSP outputs to the H-bridges with a switching frequency of $f_{PWM} = 5$ kHz. As the digital I/O pins of the DSP work with TTL 3.3 V voltage levels, conversion circuits have been used to translate the digital signals from 3.3 V to the 15 V used in the bridges. The digital inputs of the bridges are isolated with optical fibers. Numbers *24*, *25*, and *26* indicate the optical transmitters. From them, the optical fibers reach the receivers (indicated as numbers *27*, *28*, and *29*) on the opposed side of the test bench (shown in the blue detail). The received digital PWM signals pass through gate drivers (indicated as numbers *30*, *31*, and *32*) in order to condition them to drive the IGBTs in the power blocks (indicated as numbers *33*, *34*, and *35*).

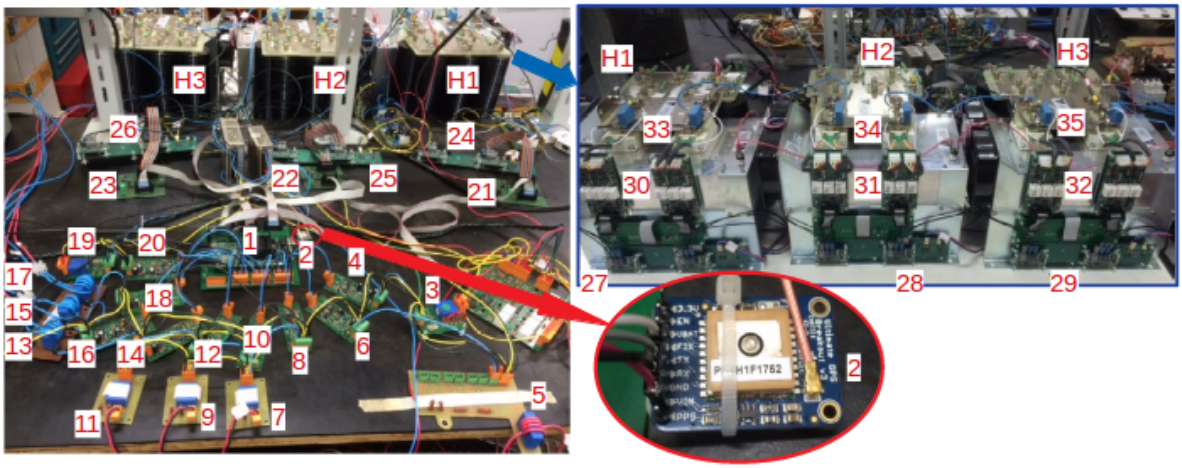


**Figure 11.** Photo of the experimental setup (whose elements are identified in Table 2) with details of the front side of the inverters and of the GPS module.

**Table 2.** Identification of the elements in the test setup of Figure 11.

| | |
|---|---|
| 1 | TMS320F28335 DSP |
| 2 | Adafruit GPS module |
| 3 | Hall effect sensor $v_S$ |
| 4 | Signal conditioning with OpAmps $v_S$ |
| 5 | Hall effect sensor $i_S$ |
| 6 | Signal conditioning with OpAmps $i_S$ |
| 7, 9, 11 | Hall effect sensor $v_{DC1,2,3}$ |
| 8, 10, 12 | Signal conditioning with OpAmps $v_{DC1,2,3}$ |
| 13, 15, 17 | Hall effect sensor $i_{DC1,2,3}$ |
| 14, 16, 18 | Signal conditioning with OpAmps $i_{DC1,2,3}$ |
| 19, 20 | Spare boards—not in use |
| 21, 22, 23 | Conversion 3.3V⇔15V |
| 24, 25, 26 | Fiber Optic Transmitters |
| 27, 28, 29 | Fiber Optic Receivers |
| 30, 31, 32 | Gate drivers |
| 33, 34, 35 | IGBT power blocks |

The parameters of the power circuit are presented in Table 3. The proportional gain of Figure 5 is $k_p = 6$. The resonant gains of Figure 5 are $k_{R1} = 1000$, $k_{R3} = 400$, $k_{R5} = 400$, $k_{R7} = 200$ and $k_{R9} = 200$.

**Table 3.** Parameters of the power circuit.

| | |
|---|---|
| Source | $v_S = 127$ V ($\pm$10%) $-$ 60 Hz |
| Transformer | 127 V/ 440 V $-$ 2.5 kVA |
| Maximum RMS current allowed on $i_S{}'$ | $i_{RMSmax} = 10$ A |
| Filter Inductor | $L_{AC} = 2.77$ mH |
| Filter Capacitor | $C_{AC} = 10$ µF |
| Battery banks (at each H-bridge) | series connection of 3 12V-Lead-Acid-60Ah |
| Battery bank floating voltage reference | $v_{DC}{}^* = 40.5$ V |
| Battery bank cut-off voltage | $v_{cutoff} = 35$ V |
| Maximum DC current injection | $I_{DCmax} = +3.8$ A |
| Maximum DC current on battery charge | $I_{ChargeMax} = -1.6$ A |

## 5. Experimental Results

Figures 12–17 present the experimental results. Two fluke power and energy analyzers have been used in order to log 24 h continuous operation of the setup described in Section 4. The first logger measured the DC $i_{DC1}$ and the DC voltage $v_{DC1}$ on bridge $H_1$ (it is assumed that the behavior s on $H_2$ and $H_3$ are similar). The second logger measured the AC $i_S$ and the AC voltage $v_S$, both on the source side of the transformer. Besides voltage and current, both instruments were also configured to log the instantaneous power at each 10 minutes. The data from both instruments were combined in the curves of Figure 12. Also a Tektronix oscilloscope with four isolated channels has been used in order to show the waveforms of the AC voltage on the source side of transformer ($v_S$), AC on the converter side of transformer ($i_S{}'$), DC voltage at bridge $H_1$ ($v_{DC1}$) and DC current at bridge $H_1$ ($i_{DC1}$) at selected instants of time. The waveforms are shown in Figures 13–17. Figure 12 also shows the instants of time when the waveforms of Figures 13–17 were taken.

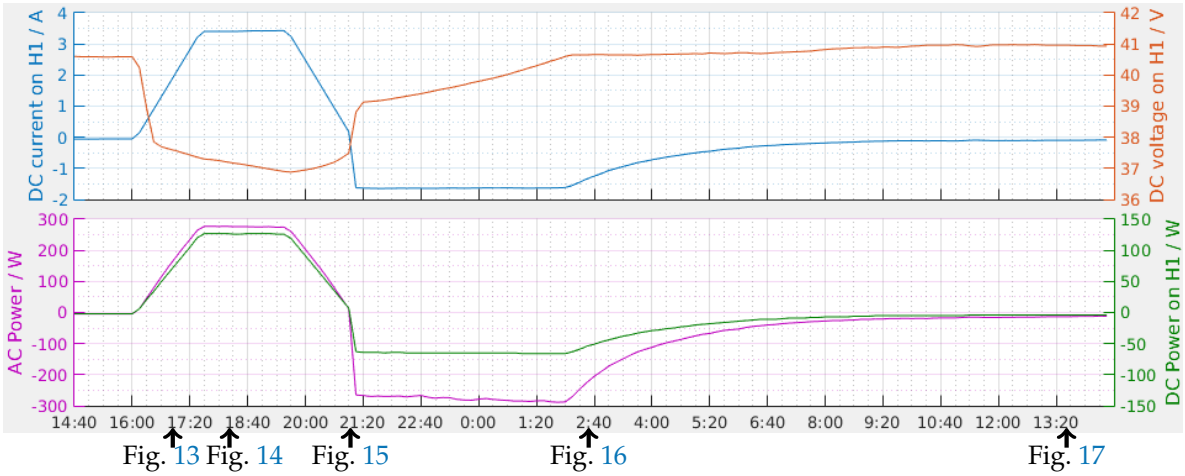


**Figure 12.** 24 h log of key signals, sampled at each 10min.

The two loggers were programmed to start data collection at 14 : 30 and stop it at 14 : 30 of the next day. The batteries were all previously fully charged at the start of the data collection. Hence, from $t = 14:30$ to $t = t_1 = 16:00$ (the start of power injection), the batteries remain on *stage III* of charging, with a minimum AC and DC, as seen in the plots of Figure 12: almost zero AC power, almost zero DC power and almost zero DC. During this interval, the DC voltage is kept around its floating voltage reference $v_{DC}{}^* = 40.5V$.

At $t = t_1 = 16:00$ the converter starts to inject active power into the grid as an ascending ramp, according to (5). At the end of the ascending ramp (at $t_2 = 17:30$) the reference for the DC current reaches its maximum limit ($I_{DCmax} = +3.8$ A). Figure 12 shows, during the interval $t_1 = 16:00 \leq t < t_2 = 17:30$, the ascending ramps on the AC power, DC power and DC. It can be noticed that, at the transition from *stage III* charging to discharging, the battery voltage has an initially abrupt drop and, then, starts a slow discharge (that depends on the current being injected). Figure 13 presents the waveforms at an intermediary power injection, taken at $t = 16:45$. It can be noticed that the AC current is in phase with the AC voltage, hence injecting power according to the sign convention of Figure 2. The DC current has a second harmonic ripple superposed on a positive average value (hence injecting power according to the sign convention of Figure 2). The DC voltage is shown with almost null ripple.

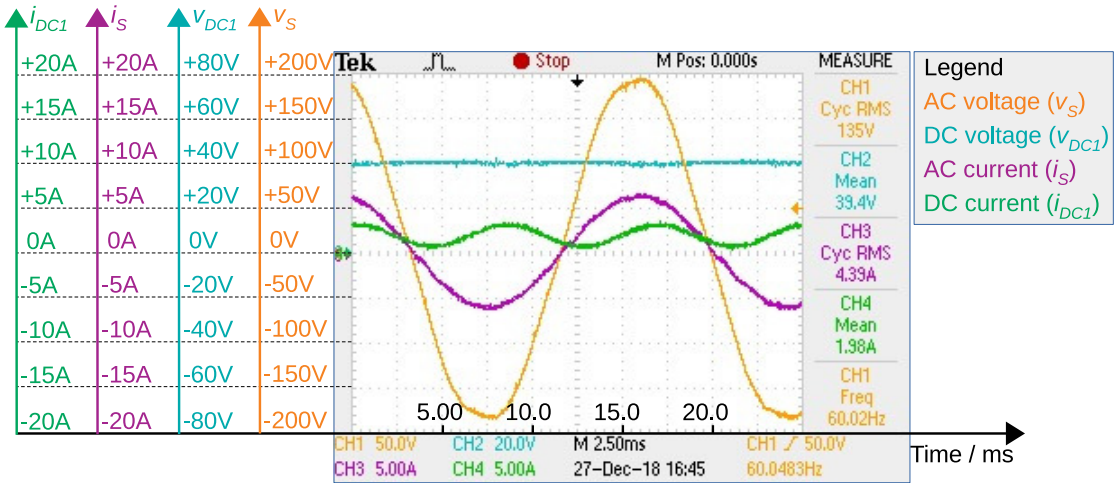


**Figure 13.** Measurements at 16:45 (of day 1)—Converter injecting active power (medium) on the grid.

During the interval $t_2 = 17:30 \leq t < t_3 = 19:30$, the power injection to the grid is constant and maximum. This can be seen clearly on the plots of the AC power, DC power and DC of Figure 12 during

this interval. During this constant discharge period, the battery voltage is slowly dropping its value. Figure 14 presents the waveforms during maximum power injection, taken at $t = 18:19$. Comparing Figure 14 with Figure 13, it can be seen that the AC has increased its amplitude and RMS value, the DC current has increased its average value (to its reference value at this period $i_{DC}{}^{*} = I_{DCmax} = +3.8$ A) and the DC voltage slightly dropped its average value.

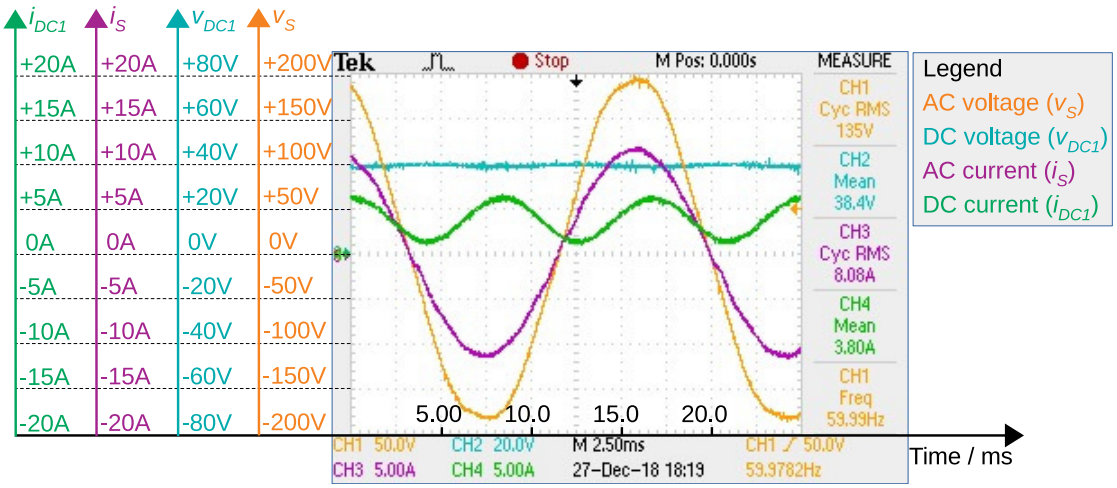


**Figure 14.** Measurements at 18:19 (of day 1)—Converter injecting active power (maximum) on the grid.

At $t = t_3 = 19:30$ the converter starts to reduce active power injection into the grid, as a descending ramp, according to (6). At the end of the descending ramp (at $t_4 = 21:00$) the reference for the DC reaches zero. Figure 12 shows, during the interval $t_3 = 19:30 \leq t < t_4 = 21:00$, the descending ramps on the AC power, DC power and DC. It can be noticed that, as the discharging current decreases past a given value, the DC voltage starts to slowly rise.

At $t = t_4 = 21:00$ the converter starts to charge its batteries, initially as *stage I* charging. The duration of each stage will depend on the specific battery model and on the reference DC and reference DC voltage. From Figure 12 it can be seen that the charge remains in *stage I* (constant DC and linear increase in DC voltage) until around 02:00 (of the next day), when the DC voltage reaches its reference and the DC starts to slowly drop to zero (from its negative reference). Figure 15 presents the waveforms at the beginning of *stage I* charge, taken at $t = 21:01$. It can be noticed that the AC is 180° out of phase with the AC voltage, hence charging the batteries according to the sign convention of Figure 2. The DC has a negative average value (hence charging the batteries according to the sign convention of Figure 2).

It can be noticed in Figure 12 that at around $t = 02:00$ (of day 2) the DC voltage reaches its reference and the DC starts to decrease its negative value. Until the DC reaches a minimum value near zero, the batteries charge in *stage II*. The transition from *stage II* to *stage III* is not clear (as the DC never reaches zero), but, in Figure 12, it can be considered to have happened around 10:00 (of day 2). Figure 16 presents the waveforms at the beginning of *stage II* charge, taken at $t = 02:32$. Comparing Figure 16 with Figure 15, it can be seen that the AC current has decreased its amplitude and RMS value, the DC has decreased its negative average value and the DC voltage has increased its average value.

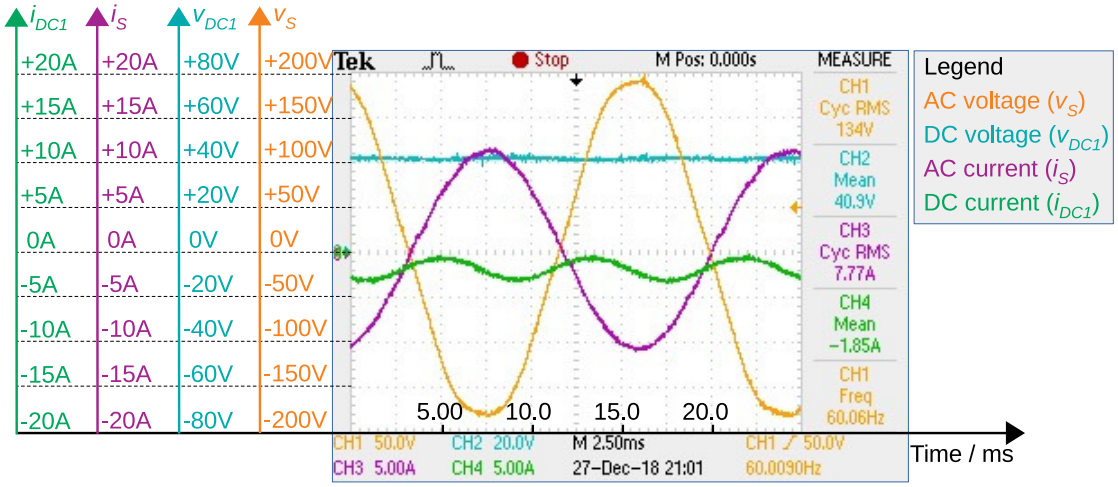


**Figure 15.** Measurements at 21:01 (of day 1)—Converter charging the batteries (stage I).

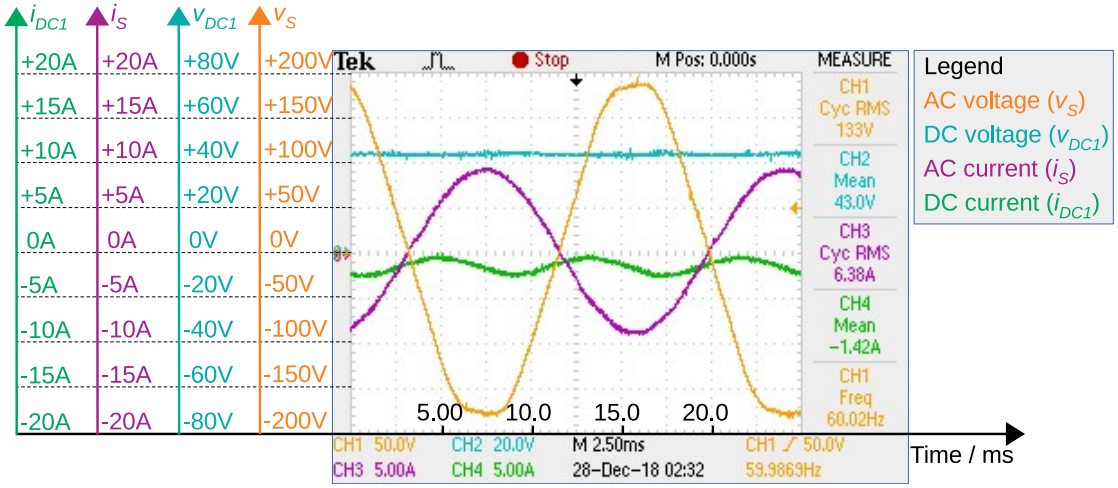


**Figure 16.** Measurements at 02:32 (of day 2)—Converter charging the batteries (stage II).

Past $t = 10:00$ (of day 2) the batteries can be considered fully charged. The converter only needs to supply a minimum DC current to them in order to keep their DC voltage around the floating reference $v_{DC}{}^* = 40.5V$. It can be noticed in Figure 12 that the DC voltage is kept around its floating reference and the DC current, DC power, and AC power are kept near zero. Figure 17 presents the waveforms at *stage III* charge, taken at $t = 13:31$. Comparing Figure 17 with Figure 16, it can be seen that the AC current has well decreased its amplitude and RMS value to almost zero, the DC current has also well decreased its negative average value and the DC voltage has increased its average value.

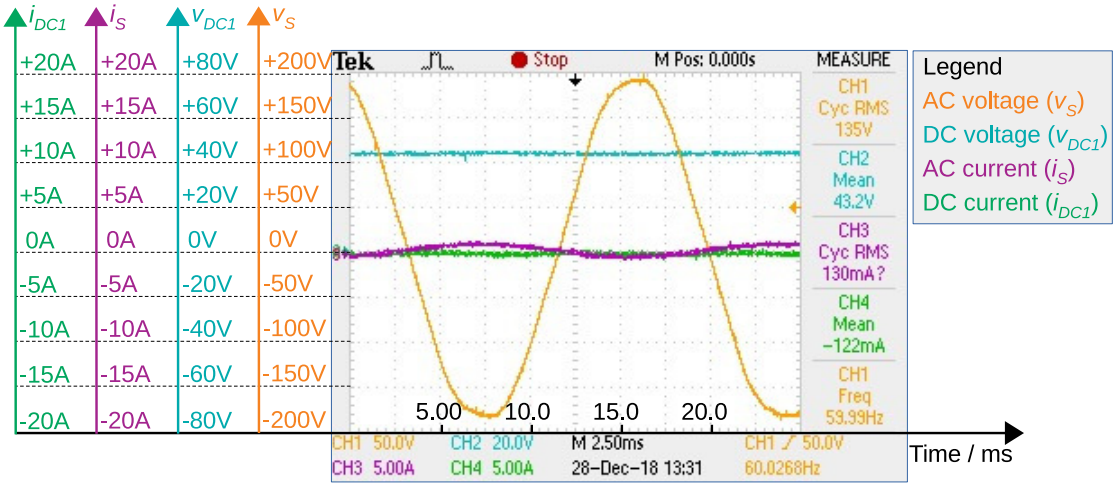


**Figure 17.** Measurements at 13:31 (of day 2)—Converter charging the batteries (stage III).

## 6. Conclusions

This paper presented the development of equipment for peak-shaving with battery type energy storage. It is intended to be used either by utilities on low voltage distribution feeders or by consumers aiming to profit from differential tariffs according to the time of the day. The precise time of the day information is obtained from a GPS module that communicates via UART with the TMS320F28335 DSP that implements the control of the equipment.

The peak time periods have been determined based on Brazilian residential consumer data. However, they can be easily adapted to different scenarios. A trapezoidal profile has been chosen for the power injection into the grid. During the pre-peak intermediate period, the equipment increases the power injection as a ramp from zero to maximum. During the peak period, the equipment injects maximum power into the grid. During the post-peak intermediate peak period, the equipment decreases the power injection as a ramp from maximum to zero. Outside the peak times (when the energy cost is less expensive), the equipment charges its batteries (consuming power from the grid).

Besides the control algorithms required for the proper operation of the equipment (battery control, PLL, AC control and multilevel PWM), it has also been presented a procedure for UART communication between the DSP and the GPS module. The procedure must be very similar to all DSPs in the Texas Instruments C2000 family. Even in case of a processor from another vendor, the algorithm to extract the time of the day information can be used, as long as an 8N1-9600bps UART communication is established.

Experimental results obtained in a single-phase 127 V test bench have been presented. These results were obtained during a continuous 24 h operation of the equipment. Key variables, such as DC power, AC power, battery current, and battery voltage have been logged throughout this period to show their behavior graphically under different stages of operation.

Detailed descriptions of all control algorithms and the experimental setup have been presented, in order to facilitate the replication of the presented results and also to serve as reference material for more complex designs.

As future work, the real-time measurement of the temperature on the batteries is recommended in order to dynamically set the reference floating voltage based on the temperature. This action can prolong the life expectancy of the batteries.

**Author Contributions:** Conceptualization, G.L.-T., E.L.B., D.M., and J.S.F.; methodology, W.C.S., R.B.G., R.R.P., and L.E.B.-d.-S.; software, W.C.S. and R.B.G.; investigation, W.C.S., B.S.T., and P.A.d.O.; resources, G.L.-T., E.L.B., D.M., and J.S.F.; writing, W.C.S.; supervision, R.B.G., G.L., E.L.B., R.R.P., and L.E.B.-d.-S.

**Acknowledgments:** The authors would like to thank the following Brazilian Research Agencies: CNPq, CAPES, FAPEMIG, and ANEEL R&D for the support of this project.

**Conflicts of Interest:** The authors declare no conflict of interest.

## Abbreviations

The following abbreviations are used in this manuscript:

| | |
|---|---|
| ASCII | American Standard Code for Information Interchange |
| CAES | Compressed Air Energy Storage |
| DSP | Digital Signal Processor |
| DST | Daylight Saving Time |
| GPS | Global Positioning System |
| IGBT | Insulated Gate Bipolar Transistor |
| LPF | Low Pass Filter |
| NMEA | National Marine Electronics Association |
| PHS | Pumped Hydroelectric Storage |
| PI | Proportional Integral controller |
| PLL | Phase Locked Loop |
| PR | Proportional plus Resonant controller |
| PWM | Pulse Width Modulation |
| RTC | Real Time Clock |
| SCI | Serial Communication Interface |
| SMES | Superconducting Magnetic Energy Storage |
| UART | Universal Asynchronous Receiver-Transmitter |
| UTC | Coordinated Universal Time |

## List of Symbols

The following symbols are used in this manuscript:

| | | |
|---|---|---|
| $\Delta i_{RMS}$ | Step size of AC current reference | A |
| $\Delta_s$ | Maximum number of samples allowed for PLL phase error | - |
| $\Phi$ | PLL phase error | rad |
| $\omega_h$ | Resonant frequency of PR controller of harmonic order $h$ | rad/s |
| $a_{0h}$, $a_{1h}$, $a_{2h}$ | Autoregressive coefficients of discretized resonant transfer functions of order $h$ | - |
| $A$ | Nominal amplitude of utility voltage | V |
| $b_h$ | Input coefficients of discretized resonant transfer functions of order $h$ | - |
| $C_{AC}$ | AC filter capacitor | F |
| $C_{DC}$ | DC capacitors at each H-bridge | F |
| $e$ | PR controller current error | A |
| $f_{nom}$ | Nominal frequency of utility voltage | Hz |
| $f_s$ | Sampling frequency | Hz |
| $i$ | PLL look-up table pointer | - |
| $I_{ChargeMax}$ | Maximum DC current at battery charge | A |
| $i_{DC1,2,3}$ | DC currents on battery banks 1, 2 and 3 | A |
| $i_{DC}$ | Averaged DC current of the battery banks | A |
| ${i_{DC}}^*$ | DC current reference of the battery banks | A |
| $I_{DCmax}$ | Maximum DC current at battery discharge | A |
| $i_{RMS}$ | RMS value of AC current reference | A |
| $i_{RMSmax}$ | Maximum RMS value of AC current reference | A |
| $i_S$ | AC current at utility side of the transformer | A |
| ${i_S}'$ | AC current at converter side of the transformer | A |
| ${i_S}'^*$ | AC current reference for PR controller | A |
| $k_P$ | Proportional gain of PR controller | V/A |
| $k_{Rh}$ | Resonant gain of PR controller of harmonic order $h$ | V/A |

| | | |
|---|---|---|
| $K_{r\to s}$ | Gain for conversion of PLL phase error to number of samples | 1/rad |
| $L_{AC}$ | AC filter inductor | H |
| $N_s$ | PLL phase error converted to number of samples | - |
| $\tilde{q}$ | Oscillating component of PLL quadrature signal | V |
| $\bar{q}$ | Constant component of PLL quadrature signal | V |
| $t$ | Time of the day | s |
| $t_1$ | Start time of ramp-up current injection | s |
| $t_2$ | Start time of maximum current injection | s |
| $t_3$ | End time of maximum current injection | s |
| $t_4$ | End time of ramp-down current injection | s |
| $T_s$ | Sampling period | s |
| $v_{1,2,3}$ | Individual output voltages of H bridges | V |
| $v_{AN}$ | Composed multilevel output voltage | V |
| $v_{cutoff}$ | Cut-off voltage of battery banks | V |
| $v_{DC1,2,3}$ | DC voltages at battery banks 1, 2 and 3 | V |
| $v_{DC}$ | Averaged DC voltage of the battery banks | V |
| $v_{DC}{}^*$ | DC floating voltage reference of the battery banks | V |
| $v_{PWM}{}^*$ | Output of PR controller | V |
| $v_{Rh}$ | Output of resonant transfer function of harmonic order $h$ | V |
| $v_S$ | AC voltage at utility side of the transformer | V |
| $v_S{}'$ | AC voltage at converter side of the transformer | V |

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