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# A Novel Control Approach to Hybrid Multilevel Inverter for High-Power Applications

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**Abstract:** This paper proposes a hybrid control scheme for a newly devised hybrid multilevel inverter (HMLI) topology. The circuit configuration of HMLI is comprised of a cascaded converter module (CCM), connected in series with an H-bridge converter. Initially, a finite set model predictive control (FS-MPC) is adopted as a control scheme, and theoretical analysis is carried out in MATLAB/Simulink. Later, in the real-time implementation of the HMLI topology, a hybrid control scheme which is a variant of the FS-MPC method has been proposed. The proposed control method is computationally efficient and therefore has been employed to the HMLI topology to mitigate the high-frequency switching limitation of the conventional MPC. Moreover, a comparative analysis is carried to illustrate the advantages of the proposed work that includes low switching losses, higher efficiency, and improved total harmonic distortion (THD) in output current. The inverter topology and stability of the proposed control method have been validated through simulation results in MATLAB/Simulink environment. Experimental results via low-voltage laboratory prototype have been added and compared to realize the study in practice.

**Keywords:** multilevel inverter (MLI); model predictive control (MPC); hybrid multilevel inverter



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## 1. Introduction

Over recent decades, multilevel converters (MLCs) have found popular in high-power applications. The reasons for their widespread acceptance are the capability to share the high-voltage stresses among the devices, low conduction and switching losses, and improved power quality with minimum harmonic distortion [1,2]. An attempt to enhance the power quality to IEEE standards, i.e., 5% current total harmonic distortion (THD), necessitates the generation of higher output voltage levels of the converter. However, the increase in output voltage level requires more components and floating capacitors, which results in increased cost and size of the converter system. Hybrid converter topologies as a combination of the conventional converters have achieved great attention from researchers [3–5] due to their minimum requirement of components count. The hybrid converter is the cascade arrangement of dissimilar converters, which reduces the necessity of component requirements for the same output voltage levels.

Maintaining the power quality of the hybrid multilevel inverters (HMLIs) at acceptable standards (IEEE-519) is a challenge. Many advanced control methods have been

developed in recent decades. The selective harmonic elimination pulse width modulation (SHE-PWM) [6] is a common control method used in the HMLIs. The SHE-PWM offers good switching losses control, but its modulation raises the angle calculation complexity. More advanced control techniques are applied to hybrid converters, namely the sinusoidal PWM (SPWM) [7,8] and the model predictive control (MPC) [9]. The MPC has been a promising control method for nearly three decades in industry and academia due to its numerous advantages for MLCs [10]. This control technique is easily realized with less tuning complexity and can also include nonlinear systems and constraints easily. Moreover, the MPC directly achieves its objectives without angular calculation and reference voltage approximation methods, which reduces its implementation complexity in power electronic systems [11]. Finite set model predictive control (FS-MPC) has been achieved popularity in power electronic systems due to its simple and flexible implementation [9]. The discrete nature of FS-MPC allows its direct implementation and eliminates the PWM need. The FS-MPC is discussed widely in the literature for controlling DC-DC and AC-DC converters [12–15], multilevel converters such as packed U-cell (PUC) [9], and flying capacitor-based ANPC hybrid converters in [16]. The FS-MPC comprises finite control actions, among which the optimal control action is attained by solving optimization problem [11]. Moreover, nonlinear control schemes, such as sliding mode control (SML) is used to control the switches of the multilevel converter and reduce the THD levels [17–20]. It is a robust and dynamic scheme that offers better performance, but much more complex and harder to designed and built.

In this paper, a circuit configuration of the proposed hybrid multilevel inverter (HMLI) based on the series arrangement of a cascaded converter module in series with an H-bridge converter is analyzed. Controllers have been employed based on a simplified model of the HMLI, which comprise of voltage and current controller. Based on the controller design, the work is split into two parts. As a first control method for newly devised topology, initially, the FS-MPC as a control technique is implemented on the HMLI, and theoretical analysis is carried out in MATLAB/Simulink environment. Using the FS-MPC method, the proposed converter generates a nine-level output voltage with reduced current distortion. Later, in the real-time implementation of the HMLI topology, a hybrid control scheme, a variant of the FS-MPC method, has been proposed. The proposed method is computationally efficient and therefore has been employed to the HMLI topology to operate the converter modules switches according to their voltage stresses. In the hybrid control strategy, the H-bridge converter operates at fundamental switching frequency whereas the cascaded converter module is controlled by FS-MPC which optimally predicts the next level, and the decision is applied through the pulse width modulation (PWM) method. The inverter topology and stability of the proposed control method have been validated through simulation and experimental results. A comparative analysis of the proposed inverter with existing topologies such as NPC [21,22], HNPC with H-bridge [23,24], HNPC with cascaded module [25,26], and PWM voltage source inverter [27] is conducted to illustrate the advantages of the proposed work.

The outline of this paper is as follows. The circuit configuration and operation of the newly devised topology are explained in Section 2. The FS-MPC as a control technique is implemented on the HMLI and theoretical analysis is carried out in MATLAB/Simulink environment in Section 3. Later, in the real-time implementation of the HMLI topology, a hybrid control scheme, a variant of the FS-MPC method, has been discussed in Section 4. Simulation and experimental results are shown and discussed in Section 5, and a comparative analysis with the relevant topologies are also added in this section. Finally, Section 6 concludes this paper.

## 2. Single-Phase HMLI Configuration

The circuit configuration of the HMLI converter is based on a series arrangement of the five-level cascaded converter module with the three-level H-bridge converter presented in Figure 1. The H-bridge converter consists of four active switches ($Q_a$ – $Q_d$) and a DC source

of $2V_{dc}$. The CCM comprises three pairs of alternately connected active switches ($Q_1\bar{Q}_1$, $Q_2\bar{Q}_2$, $Q_3\bar{Q}_3$). The CCM is fed by two DC sources, each with a value of $V_{dc1} = V_{dc2} = V_{dc}$. Table 1 presents 32 switching states when combined, they produce an output voltage of nine-level.

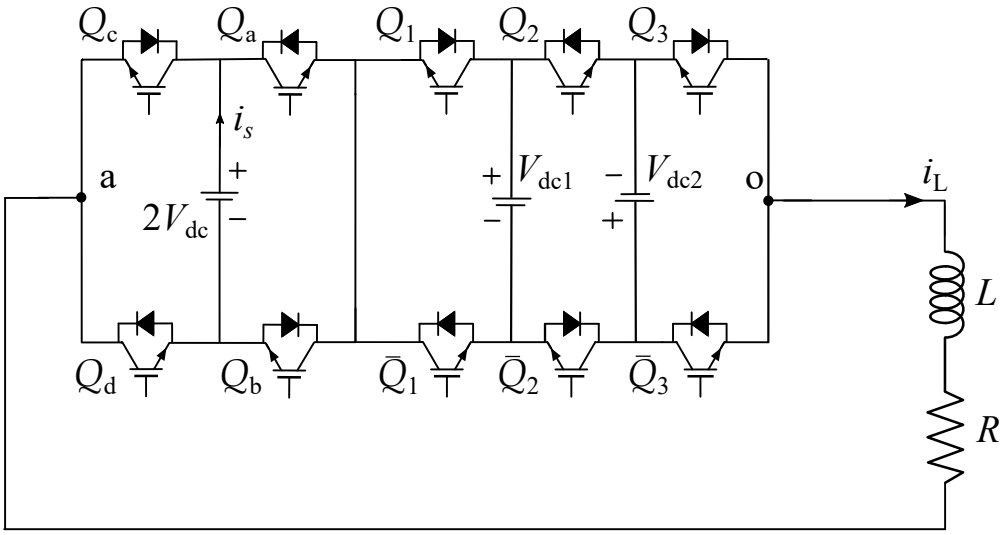


**Figure 1.** HMLI topology connected to RL load.

**Table 1.** Switching States of HMLI topology connected to RL load.

| Switching State | $Q_c$ | $Q_a$ | $Q_1$ | $Q_2$ | $Q_3$ | $v_{ao}$ |
|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 2 | 1 | 1 | 0 | 0 | 0 | 0 |
| 3 | 0 | 0 | 1 | 1 | 1 | 0 |
| 4 | 0 | 0 | 0 | 0 | 0 | 0 |
| 5 | 0 | 1 | 1 | 0 | 1 | 0 |
| 6 | 1 | 0 | 0 | 1 | 0 | 0 |
| 7 | 0 | 0 | 0 | 0 | 1 | $V_{dc}$ |
| 8 | 1 | 1 | 1 | 0 | 0 | $V_{dc}$ |
| 9 | 1 | 1 | 0 | 0 | 1 | $V_{dc}$ |
| 10 | 0 | 0 | 1 | 0 | 0 | $V_{dc}$ |
| 11 | 1 | 0 | 0 | 1 | 1 | $3V_{dc}$ |
| 12 | 1 | 0 | 1 | 1 | 0 | $3V_{dc}$ |
| 13 | 1 | 0 | 1 | 1 | 1 | $2V_{dc}$ |
| 14 | 1 | 0 | 0 | 0 | 0 | $2V_{dc}$ |
| 15 | 1 | 1 | 1 | 0 | 1 | $2V_{dc}$ |
| 16 | 0 | 0 | 1 | 0 | 1 | $2V_{dc}$ |
| 17 | 1 | 0 | 1 | 0 | 0 | $3V_{dc}$ |
| 18 | 1 | 0 | 0 | 0 | 1 | $3V_{dc}$ |
| 19 | 1 | 0 | 1 | 0 | 1 | $4V_{dc}$ |
| 20 | 1 | 1 | 1 | 1 | 0 | $-V_{dc}$ |
| 21 | 0 | 0 | 0 | 1 | 1 | $-V_{dc}$ |
| 22 | 0 | 0 | 1 | 1 | 0 | $-V_{dc}$ |
| 23 | 1 | 1 | 0 | 1 | 1 | $-V_{dc}$ |

**Table 1.** *Cont.*

| Switching State | $Q_c$ | $Q_a$ | $Q_1$ | $Q_2$ | $Q_3$ | $v_{ao}$ |
|---|---|---|---|---|---|---|
| 24 | 0 | 1 | 1 | 0 | 0 | $-3V_{dc}$ |
| 25 | 0 | 1 | 0 | 0 | 1 | $-3V_{dc}$ |
| 26 | 0 | 1 | 0 | 0 | 0 | $-2V_{dc}$ |
| 27 | 0 | 1 | 1 | 1 | 1 | $-2V_{dc}$ |
| 28 | 0 | 0 | 0 | 1 | 0 | $-2V_{dc}$ |
| 29 | 1 | 1 | 0 | 1 | 0 | $-2V_{dc}$ |
| 30 | 0 | 1 | 0 | 1 | 1 | $-V_{dc}$ |
| 31 | 0 | 1 | 1 | 1 | 0 | $-V_{dc}$ |
| 32 | 0 | 1 | 0 | 1 | 0 | $-4V_{dc}$ |

## 3. Model Predictive Control

The mathematical model of the HMLI topology connected to load is shown in Figure 1, and is given below.

$$L\frac{di_L}{dt} = S_x 2V_{dc} + S_y V_{dc1} + S_z V_{dc2} - Ri_L \tag{1}$$

where $R$ and $L$ denote the load resistor and inductor, respectively, whereas $S_x$, $S_y$, and $S_z$ are the switching functions of the overall converter which can be expressed as:

$$S_x = Q_a Q_d - Q_b Q_c \tag{2}$$

$$S_y = Q_1 \bar{Q}_2 - \bar{Q}_1 Q_2 \tag{3}$$

$$S_z = \bar{Q}_2 Q_3 - Q_2 \bar{Q}_3 \tag{4}$$

In the finite set model predictive control (FS-MPC), the switching mode for each converter level is a direct control action from MPC. In this case, the response time of MPC control action is dependent on the sampling time $T_s$. The sampling time must have a reasonable value so that the computations can be performed on time, but it should be restricted to a lower value so that the linear approximation is justified. To obtain the prediction equation for load current, the Euler formula is applied to Equation (1) in the continued section.

### *3.1. MPC Optimization*

FS-MPC comprises of finite control actions; in the case of nine-level converter, nine current predictions are calculated, which can be expressed as follows:

$$I_L^1(t+T_s) = \frac{T_s}{L}[2V_{dc} + V_{dc1} + V_{dc2} - Ri_L(t)] + i_L(t) \tag{5}$$

$$I_L^2(t+T_s) = \frac{T_s}{L}[2V_{dc} + V_{dcn} - Ri_L(t)] + i_L(t) \tag{6}$$

$$I_L^3(t+T_s) = \frac{T_s}{L}[2V_{dc} - Ri_L(t)] + i_L(t) \tag{7}$$

$$I_L^4(t+T_s) = \frac{T_s}{L}[V_{dcn} - Ri_L(t)] + i_L(t) \tag{8}$$

$$I_L^5(t+T_s) = \frac{T_s}{L}[-2V_{dc} - V_{dc1} - V_{dc2} - Ri_L(t)] + i_L(t) \tag{9}$$

$$I_L^6(t+T_s) = \frac{T_s}{L}[-2V_{dc} - V_{dcn} - Ri_L(t)] + i_L(t) \tag{10}$$

$$I_{\mathrm{L}}^{7}(t+T_s) = \frac{T_{\mathrm{s}}}{L}[-2V_{\mathrm{dc}} - Ri_{\mathrm{L}}(t)] + i_{\mathrm{L}}(t) \tag{11}$$

$$I_{\mathrm{L}}^{8}(t+T_s) = \frac{T_{\mathrm{s}}}{L}[-V_{\mathrm{dcn}} - Ri_{\mathrm{L}}(t)] + i_{\mathrm{L}}(t) \tag{12}$$

$$I_{\mathrm{L}}^{9}(t+T_s) = \frac{T_{\mathrm{s}}}{L}[-Ri_{\mathrm{L}}(t)] + i_{\mathrm{L}}(t) \tag{13}$$

A cost function $F_{\mathrm{m}}$ is calculated for each predicted current, which corresponds to a distinct voltage level $I_{\mathrm{L}}^{\mathrm{n}}(t+T_s)$ as follows:

$$F_{\mathrm{m}} = W|I_{\mathrm{L}}^{\mathrm{n}}(t+T_s) - I_{\mathrm{ref}}| \qquad for \qquad \mathrm{n} = 1, 2, .., 9. \tag{14}$$

where $W$ denotes the weighting factor, and $I_{\mathrm{ref}}$ is the converter reference current. Considering the inverter nine voltage levels and subject to Equation (1), nine current predictions are calculated. Among the nine current control actions, the optimal one is achieved by solving the optimization problem. The optimal voltage level $V_{\mathrm{optimal}}$ is subjected to the least cost function as expressed below:

$$V_{\mathrm{optimal}} = \arg\left[\min_{i_{\mathrm{L}}(t)} F_{\mathrm{m}}\right] \tag{15}$$

To track the current to its reference, the converter needs to generate the desired voltage for the required output current as presented in Figure 2. while converter operation switching frequency of 800 Hz is observed, which is not a permissible range to operate the switch with voltage stress above than 3 kV. Therefore, the study will show in a later section that the existing technique is modified. A variant of MPC known as the hybrid control scheme is proposed and employed, which is computationally efficient and hence operates the converter module switches according to their voltage stresses.

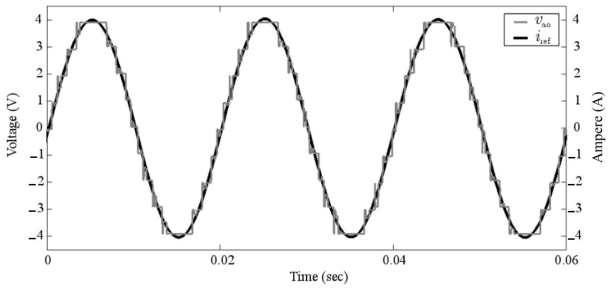


**Figure 2.** Nine-level inverter output voltage.

## 4. Real-Time Inverter Implementation

The efficiency of the HMLI topology can be improved by reducing the switching loss. Therefore, the HMLI switches are categorized in terms of their voltage stress. In the HMLI topology, the high-voltage H-bridge converter provides fundamental component support; therefore, a fundamental switching frequency (50 Hz) is selected to minimize the switching loss. The low switching frequency will cause high harmonics, which is filtered through a series active filter (cascaded converter module). With this modulation strategy, the HMLI generates a seven-level output voltage.

The HMLI topology is based on a series arrangement of a five-level cascaded converter module with the three-level H-bridge converter to form a seven-level converter presented in Figure 3. The five-level cascaded converter module circuit consists of two DC-link capacitors $C_1$ and $C_2$, which are initially charged at $V_{\mathrm{c1}} = V_{\mathrm{c2}} = V_{\mathrm{dc}}$, and three pairs of alternately connected active switches ($Q_1\bar{Q}_1$, $Q_2\bar{Q}_2$, $Q_3\bar{Q}_3$). The H-bridge converter is comprised of four active switches ($Q_{\mathrm{a}} - Q_{\mathrm{d}}$) (two half bridges), which are connected in parallel with a single DC-bus voltage $2V_{\mathrm{dc}}$. In this topology, the fundamental component is generated by the H-bridge converter with the output voltage levels of $\pm 2V_{\mathrm{dc}}$ and 0. At

the same time, the cascaded converter module (CCM) as a series active filter will produce five-level output voltage, namely $\pm 2V_{dc}$, $\pm V_{dc}$, and 0. The combined operation of the HMLI generates a seven-level output voltage. In the HMLI circuit arrangement, the active switches of an H-bridge converter are handling high-voltage stress i.e., double then DC-link capacitors voltage of the CCM.

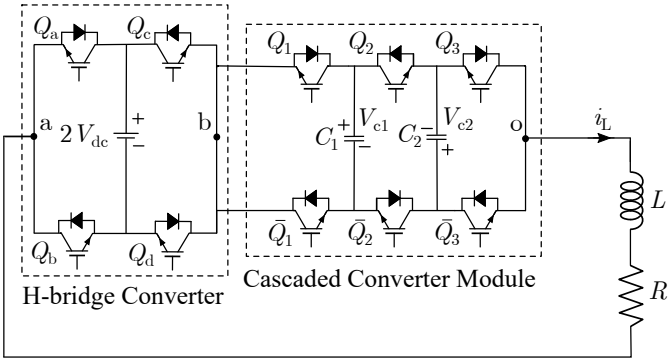


**Figure 3.** Seven-level inverter topology.

In the HMLI topology, the cascaded converter module is a vital part of circuit topology. It guarantees the seven-level output voltage of the HMLI with minimum harmonic distortion. The five-level output voltage of the cascaded converter module is ensured by the eight distinct switching modes depicted in Figure 4 when the DC-link capacitor voltage is balanced to its reference value. The cascaded converter module has redundancy for output voltage level, namely $\pm V_{dc}$ and zero levels, which ensures controllability of the capacitor; however, the $\pm 2V_{dc}$ has a unique state. The change in the $\pm 2V_{dc}$ is only determined by the direction of the current. As the cascaded converter gives harmonic component support to the HMLI, the DC-link capacitor charge is affected when the power is dissipated across the semiconductor devices during switching to attain the desired output voltage levels. Moreover, the DC-link capacitor voltage also deviates from its reference value when the output terminals are connected through any single capacitor. This happens when the output voltage level $\pm V_{dc}$ is achieved; these switching states affect the DC-link capacitor voltage by either charging or discharging it, depending on the converter's current direction as given in Table 2.

**Table 2.** Effect on DC-Link Capacitor.

| Switch Mode | Effect on Capacitor | | | |
|---|---|---|---|---|
| | When $i_s$ is from (o→a) | | When $i_s$ is from (a→o) | |
| | $C_1$ | $C_2$ | $C_1$ | $C_2$ |
| Mode 3 | Charge | by-pass | Discharge | by-pass |
| Mode 4 | Discharge | by-pass | Charge | by-pass |
| Mode 5 | by-pass | Charge | by-pass | Discharge |
| Mode 6 | by-pass | Discharge | by-pass | Charge |
| Mode 7 | Charge | Charge | Discharge | Discharge |
| Mode 8 | Discharge | Discharge | Charge | Charge |

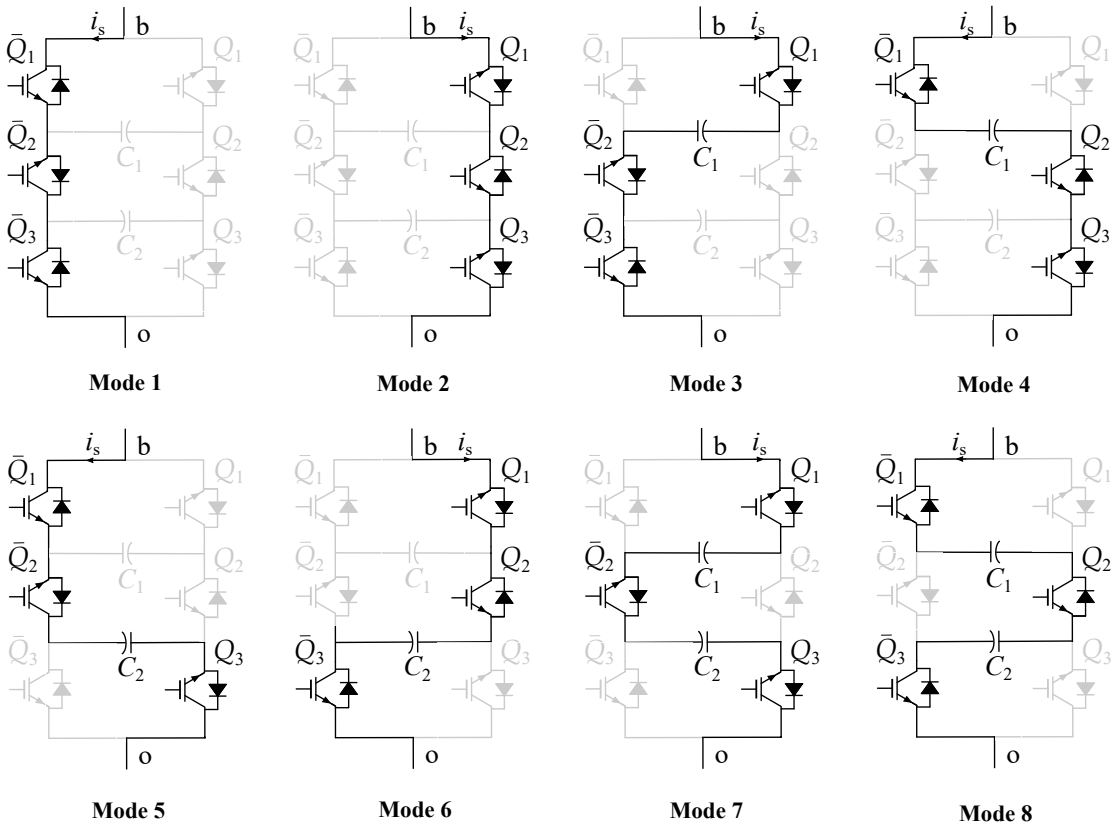


**Figure 4.** Switching modes of cascaded converter module.

### *4.1. Hybrid Modulation Strategy*

A hybrid modulation strategy is employed to HMLI topology to overcome the high-frequency switching limitation of the MPC control method, as discussed. In this strategy, the converter modules which are under higher voltage stress are operated at the low switching frequency, and switches under low-voltage stress are operated with high switching frequency. Figure 3 shows the seven-level HMLI topology connected to the RL load. The switches in the H-bridge converter are under higher voltage stress; therefore, they are modulated with a switching frequency of 50 Hz. The low switching frequency will help in reducing the switching loss of the H-bridge converter, but it will produce high harmonics. The cascaded converter module is introduced in series connection, which will filter out the high harmonics and enhanced the output voltage levels of the converter. The cascaded converter module switches are under low-voltage stress, while converter operation switching frequency of 1.6 kHz is observed.

The cascaded converter module is controlled by model predictive control (MPC), which optimally predicts the next level, and the decision is injected through the pulse width modulation (PWM) technique. The Fourier series expansion of the output voltage of a seven-level converter topology can be expressed as

$$v_{ao}(t) = v_{ab}(t) + v_{bo}(t) \tag{16}$$

$$v_{ab}(t) = \frac{4V_{dc}}{\pi} \sum_{n}^{\infty} \frac{1}{n} \cos(n\theta) \sin(n\omega t) \tag{17}$$

$$v_{bo}(t) = v_{ab}(t) - \frac{4V_{dc}}{\pi} \cos(\theta) \sin(\omega t) \tag{18}$$

where $n$ denotes the harmonic order. $\theta$ is the firing angle of the fundamental converter, which can be expressed as follows:

$$\theta = \arccos\left(\frac{\pi}{4}\frac{|V_{cj}|}{V_{dc}}\right) \qquad j = 1, 2. \tag{19}$$

4.1.1. Prediction Model

The dynamic model of a five-level cascaded converter module (CCM) shown in Figure 5 can be equated as follows

$$L\frac{di_s}{dt} = S_l V_{c1} + S_m V_{c2} - Ri_s \tag{20}$$

where $R$ and $L$ denote the load resistor and inductor, respectively, whereas $S_l$ and $S_m$ are the switching functions of the converter module, which can be computed as follows:

$$S_l = Q_1\bar{Q}_2 - \bar{Q}_1 Q_2 \tag{21}$$

$$S_m = \bar{Q}_2 Q_3 - Q_2\bar{Q}_3 \tag{22}$$

For a given switch-direction, the DC-link capacitors voltage change is the function of converter current direction ($i_s$) which are expressed as

$$\frac{dV_{c1}}{dt} = \frac{S_l i_s}{C_1} \tag{23}$$

$$\frac{dV_{c2}}{dt} = \frac{S_m i_s}{C_2} \tag{24}$$

In the finite set model predictive control (FS-MPC) switching mode for each converter level is a direct control action from MPC, and the decision is then injected through PWM. In this case, the response time of MPC control action is dependent on the sampling time of $T_s$.

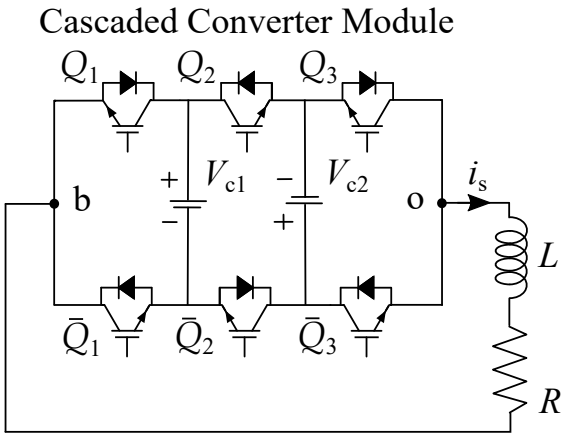


**Figure 5.** Five-level converter topology.

As the cascaded module provides high switching frequency support, the current control is implemented on this module, which will help to track the current fast and minimize the current ripple. The employed converter current control depends on the output voltage produced by the cascaded converter module. The main objective of this control scheme is to produce the desired voltage for the required output current. To obtain

the prediction equations, Euler formula is applied to converter current in Equation (25) which is given as:

$$I_s(t+T_s) = \frac{T_s}{L}[S_1 V_{c1} + S_m V_{c2} - R i_s(t)] + i_s(t) \tag{25}$$

4.1.2. Prediction Control

FS-MPC is comprised of finite control actions. Considering cascaded converter module, it has five current prediction equations, which are expressed as:

$$I_s^1(t+T_s) = \frac{T_s}{L}[V_{c1} - R i_s(t)] + i_s(t) \tag{26}$$

$$I_s^2(t+T_s) = \frac{T_s}{L}[V_{c1} + V_{c2} - R i_s(t)] + i_s(t) \tag{27}$$

$$I_s^3(t+T_s) = \frac{T_s}{L}[-V_{c1} - R i_s(t)] + i_s(t) \tag{28}$$

$$I_s^4(t+T_s) = \frac{T_s}{L}[-V_{c1} - V_{c2} - R i_s(t)] + i_s(t) \tag{29}$$

$$I_s^5(t+T_s) = \frac{T_s}{L}[-R i_s(t)] + i_s(t) \tag{30}$$

A cost function $K_n$ is calculated for each predicted current, which corresponds to a distinct voltage level $I_s^n(t+T_s)$ as follows

$$K_n = \alpha |I_s^n(t+T_s) - I_{ref}| \qquad for \qquad n = 1, 2, .., 5. \tag{31}$$

where $\alpha$ denotes the weighting factor, and $I_{ref}$ is the converter reference current. Among the five current control actions, the optimal one is achieved by solving the optimization problem. The optimal voltage level $V_m$ is subjected to the least cost function as expressed below.

$$V_m = \arg\left[\min_{i_s(t)} K_n\right] \tag{32}$$

*4.2. Voltage Balancing of DC Capacitors*

The cascaded module in the circuit arrangement of seven-level provides harmonic and high switching frequency support. Therefore, the current control is implemented in this module. To track the current to its reference, DC-link capacitors need to generate the desired voltage for the required output current. Moreover, the power dissipation across the semiconductor devices during the switching is fed by these capacitors. Therefore, the summated DC-link regulation of the DC-link capacitor is needed to ensure the safe operation of the converter. To maintain the common-mode DC-link voltage to desired voltage level, the H-bridge cell which provides fundamental component support will vary the fundamental component period to provide an amount of energy needed to the cascaded module subject to Equation (19) Figure 6 depicts the common-mode voltage regulation in which the error of the summated DC-link voltage with its reference value is compensated through PI controller and added in the reference common-mode DC-link capacitors voltage to calculate the initial angle of the H-bridge cell. This will vary the modulation signal amplitude according to the energy need to the cascaded converter module and compared further with the carriers signals of 50 Hz to attain the switching signal for the H-bridge cell.

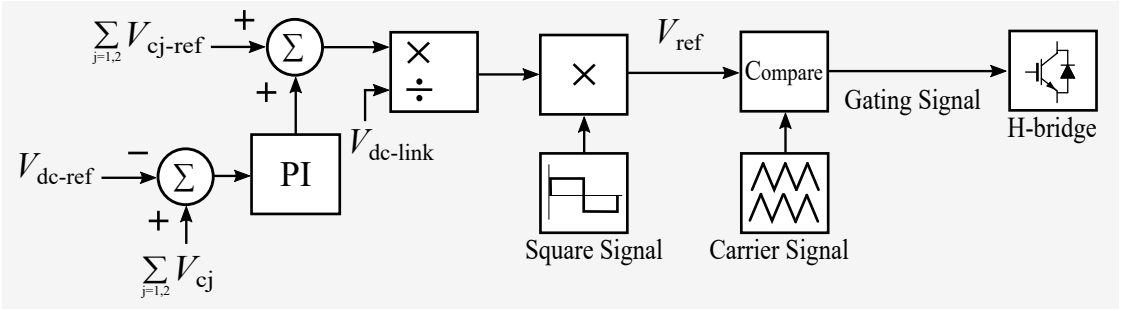


**Figure 6.** Common-mode voltage regulation.

Furthermore, due to parametric variances and switching delays, the individual DC-link capacitor voltage may deviate from its reference DC-value. The charge swapping technique by redundant switching states selection in Figure 4 is used to converge the DC-link capacitors voltage value to its desired reference. In Figure 7, a flow chart demonstrates the voltage control algorithm of the overall converter.

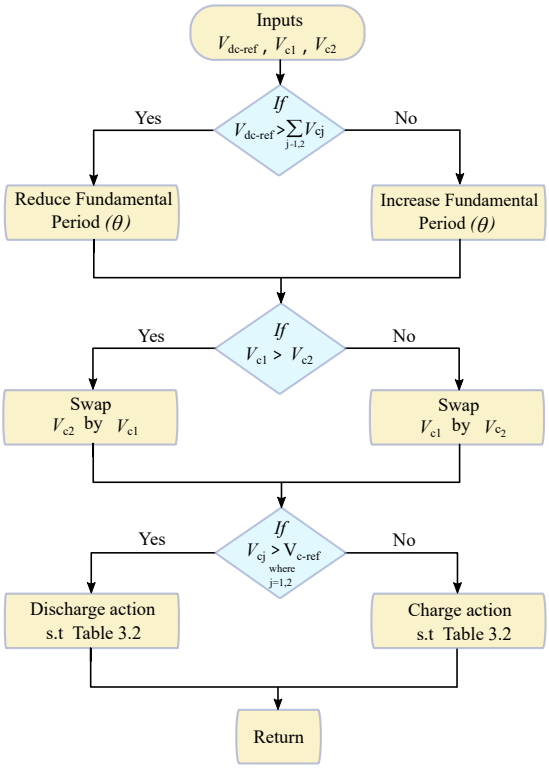


**Figure 7.** DC-link capacitor voltage balancing algorithm.

## 5. Simulation and Experimental Results

The seven-level HMLI configuration shown in Figure 3 is simulated in MATLAB sim-power environment to demonstrate the system's effectiveness and performance of the modulation and control scheme. The proposed converter and its control scheme are experimentally validated by a low-voltage laboratory prototype as depicted in Figure 8. The control algorithm is implemented on a customized control board that uses TMS320C28346 Delfino™ micro-controller unit (MCU), EPM570 ALTERA® complex programmable logic device (CPLD), and AD Conversion to realize the control in practice. To verify the converter system results, simulation results are scaled accordingly to low-voltage laboratory prototype using the system's parameters listed in Table 3. The selection of all component values is achieved with extensive simulations. The MPC algorithm is employed with a sampling frequency of 12 kHz.

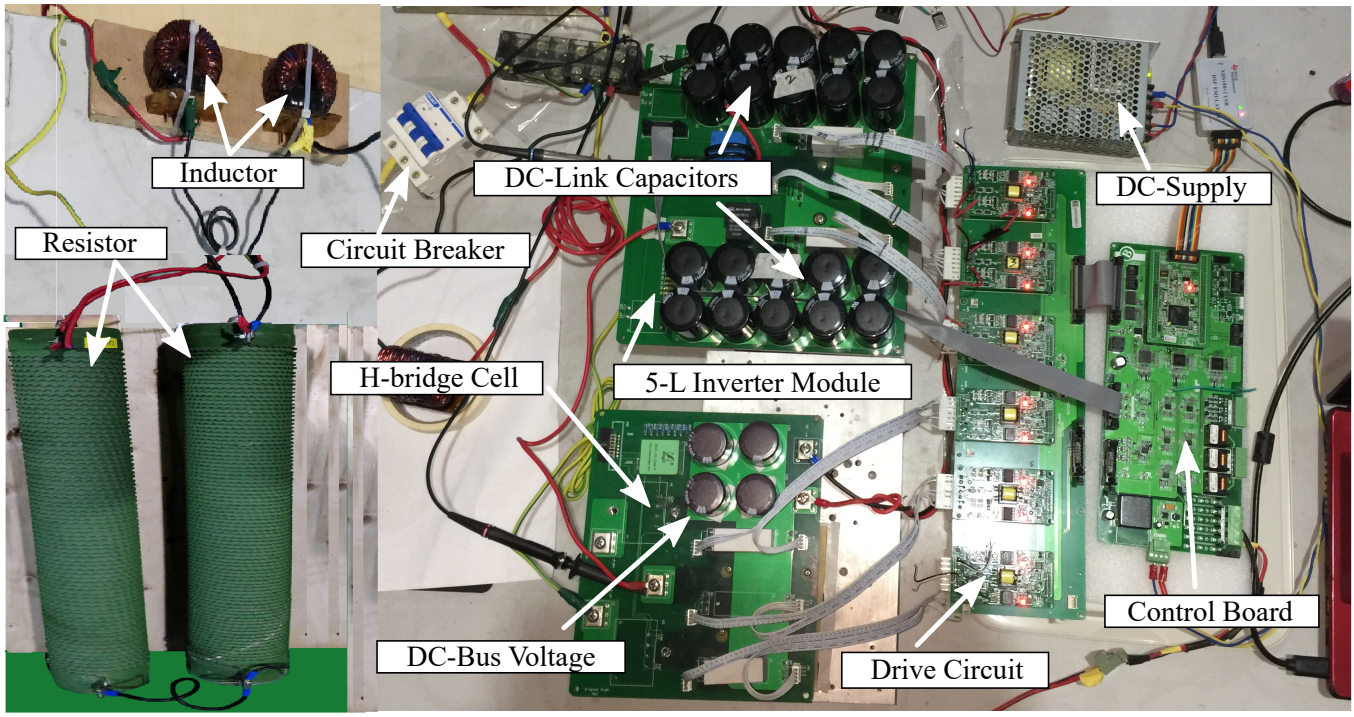


**Figure 8.** Experimental setup.

**Table 3.** System Parameters of Seven-Level Inverter.

| Parameter | Value |
|---|---|
| DC-link capacitor | 20 μF |
| CCM carrier frequency | 3.2 kHz |
| Capacitor voltage | 50 V |
| DC-bus voltage | 100 V |
| Load-A | $R$ = 44 Ω, $L$ = 2.4 mH |
| Load-B | $R$ = 22 Ω, $L$ = 2.4 mH |

Figure 9 represents the overall output voltage of the HMLI inverter ($v_{ao}$) which is the addition of H-bridge output voltage ($v_{ab}$) and CCM output voltage ($v_{bo}$) and can be equated as given in Equations (16)–(19). Figure 9 depicts the output of seven-level ±3Vdc, ±2Vdc, ±Vdc, and 0, which is achieved by operating the converter modules as per the desired switching states listed in Table 4. The h-bridge converter is connected to 2Vdc and will produce output voltage levels of ±2Vdc and 0, whereas the cascaded converter module (CCM) circuit consists of two DC-link capacitors C1 and C2, which are initially charged at Vc1 = Vc2 = Vdc and will provide harmonic component support.

**Table 4.** Seven-level HMLI output voltage.

| Angle | $v_{ab}$ | $v_{bo}$ | $v_{ao} = (v_{ab}) + (-v_{bo})$ |
|---|---|---|---|
| $0 \leq \theta \leq \alpha_1$ | 0 | 0 | 0 |
| $\alpha_1 \leq \theta \leq \alpha_2$ | 0 | $-V_{dc}$ | $V_{dc}$ |
| $\alpha_1 \leq \theta \leq \alpha_2$ | $2V_{dc}$ | $V_{dc}$ | $V_{dc}$ |
| $\alpha_2 \leq \theta \leq \alpha_3$ | $2V_{dc}$ | 0 | $2V_{dc}$ |
| $\alpha_3 \leq \theta \leq \pi$ | $2V_{dc}$ | $-V_{dc}$ | $3V_{dc}$ |

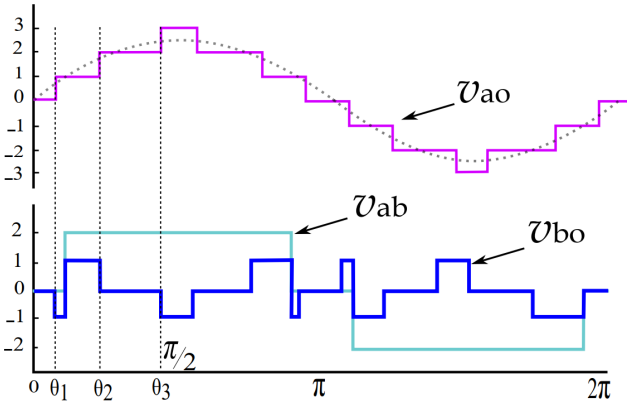


**Figure 9.** Output voltage of the proposed HMLI topology,Overall output voltage of the inverter ($v_{ao}$), H-bridge output voltage ($v_{ab}$) and CCM output voltage ($v_{bo}$).

Figure 10 depicts the simulation and experimental results of the seven-level inverter output voltage at maximum modulation index $M$ = 1.1 and converter current waveform for load-A. Figure 10a shows simulation results of individual converter cells and the overall output voltage of the converter. Active power is transferred by an H-bridge cell where high harmonics are compensated through a series active filter (CCM). Figure 10b show experimental results of the inverter, which generates the desired output voltage to track the current to its reference value for load-A. Figure 11 presents the simulation and experimental results of the studied converter, operating at $M$ = 0.9 for load-A, which results in the output voltage of five levels of the converter. Figure 11a shows simulation results of individual converter cell and the overall output voltage of the converter, whereas Figure 11b show experimental results of the inverter, which generates the desired output voltage to track the current to its reference value for load-A. It can be seen in Figures 10 and 11 that when the modulation index is reduced from $M$ = 1.1 to $M$ = 0.9, the distortion in the current waveform gets increased.

Figure 12 depicts the experimental results of the seven-level inverter output voltage at different modulation indexes and inverter current waveform for load-B. Figure 12a shows experimental results of the inverter which generates the desired output voltage to track the current to its reference value for load-B at $M$ = 1.1, whereas, Figure 12b show experimental results of the inverter which generates the desired output voltage to track the current to its reference value for load-B at $M$ = 0.9.

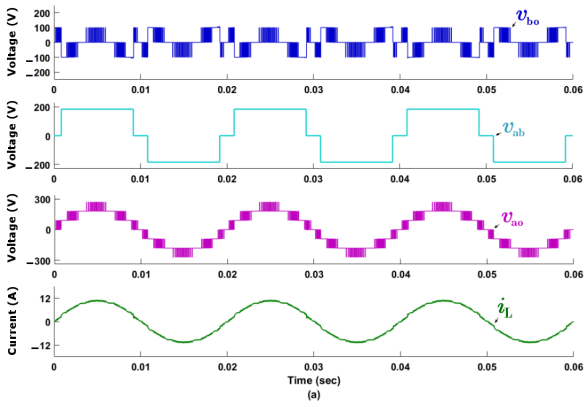


**Figure 10.** *Cont.*

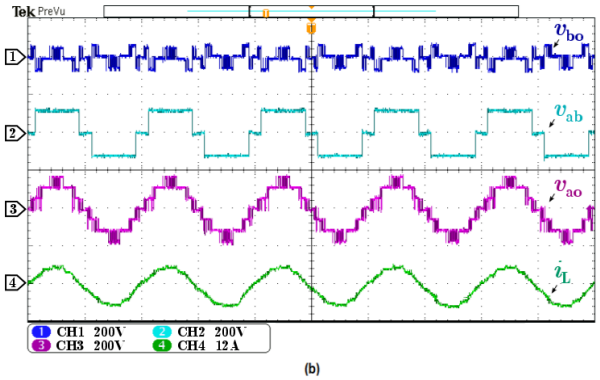


**Figure 10.** Output voltage of inverter topology for load-A at $M$ = 1.1, (**a**) simulation waveform of respective converter modules and inverter current, (**b**) experimental waveform of respective converter modules and inverter current, traces channel 1, 2, 3 (200 V/div) and 4 (12 A/div).

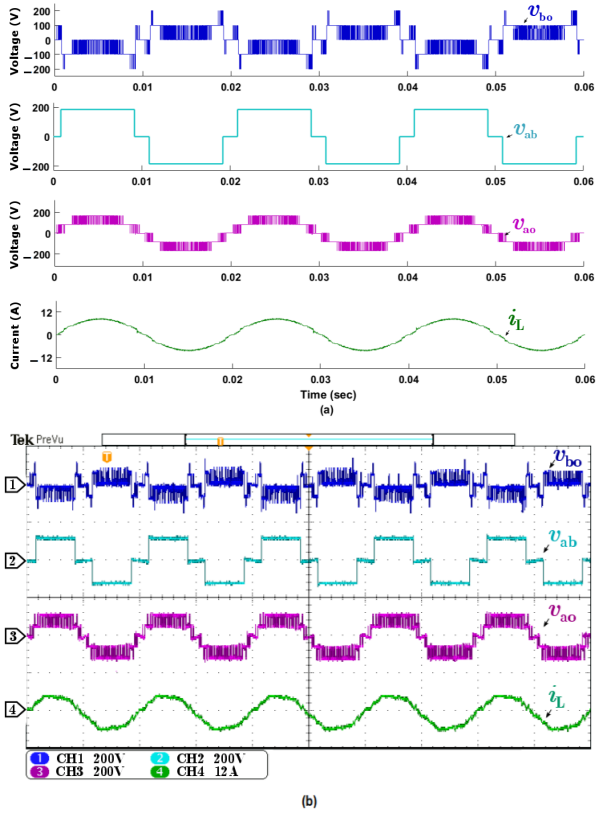


**Figure 11.** Output voltage of inverter topology for load-A at $M$ = 0.9, (**a**) simulation waveform of respective converter modules and inverter current, (**b**) experimental waveform of respective converter modules and inverter current, traces channel 1, 2, 3 (200 V/div) and 4 (12 A/div).

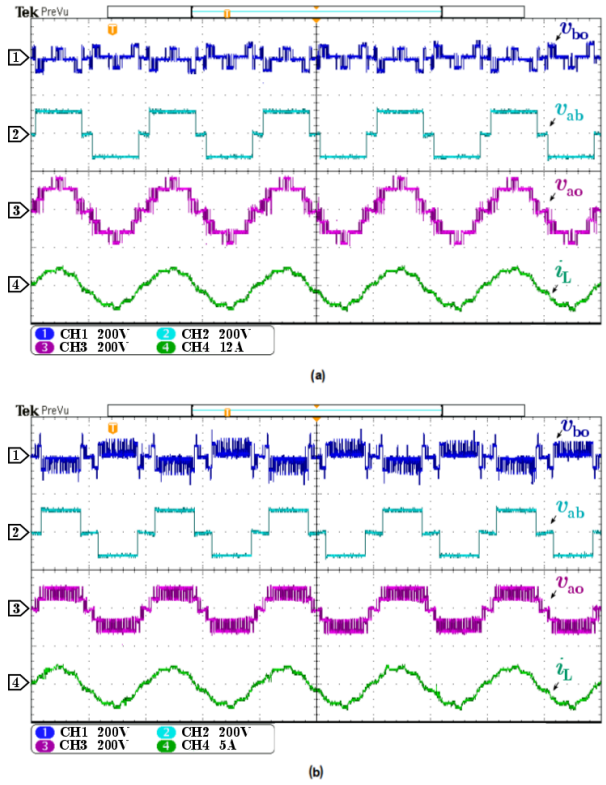


**Figure 12.** Experimental waveform of respective converter modules and inverter current at load-B, (**a**) when $M$ = 1.1, traces channel 1, 2, 3 (200 V/div) and 4 (5 A/div), (**b**) when $M$ = 0.9, traces channel 1, 2, 3 (200 V/div) and 4 (5 A/div).

Figure 13 shows experimental validation of the voltage control. The common-mode DC-link capacitors voltage is regulated to its reference value with the modification of fundamental component duty cycle subject to Figure 7. Once the common-mode voltage is regulated, the individual DC-link capacitor voltage deviates from its reference value due to the parametric variance and switching delay. To converge the individual capacitor to its reference value, the redundant states are used to swap the capacitor charge among each other, which can be seen in Figure 13. The converter performance is tested for three cases implemented in simulation and on laboratory prototype, and their respective satisfactory THD results are presented in Figure 14. The THD estimations by Fast Fourier Transform (FFT) is shown for three different cases with a simulation THD of 2.45% for load-A at $M$ = 1.1, 3.46% for load-B at $M$ = 1.1, and 4.53% for load-A at $M$ = 0.9. However, the experimental THD of 4.34% for load-A at $M$ = 1.1, 5.61% for load-B at $M$ = 1.1, and 6.81% for load-A at $M$ = 0.9 is achieved. The simulation THD is comparatively lowered than that of experimental THD because of the losses and noise.

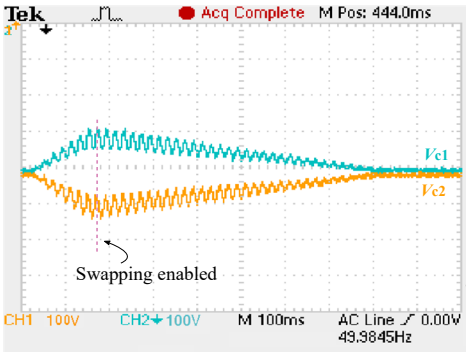


**Figure 13.** Balanced DC-link capacitor voltage, traces channel 1 and 2 (100 V/div).

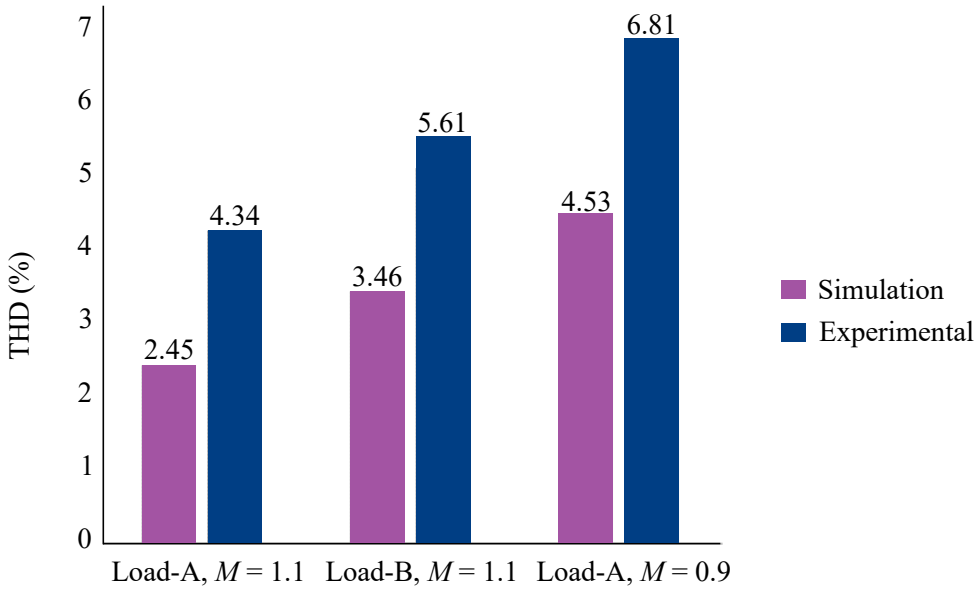


**Figure 14.** Inverter current THD at different load.

The proposed HMLI topology is compared with existing topologies such as NPC [1], HNPC with H-bridge [2], HNPC with cascaded module [3] in terms of current THD operating at different power ratings (25%, 50%, 100%). The existing topologies, NPC, HNPC with H-bridge, HNPC with cascaded module, and proposed HMLI topology at a 25% power rating have current THD of 6.59, 6.71, 5.31, and 6.55, respectively. Similarly, at 50% power rating have current THD of 2.83, 3.43, 3.39, and 3.31, respectively, likewise, at 100% power rating current THD of 1.38, 1.73, 1.71, and 1.66 are achieved, respectively. The proposed HMLI topology is compared with NPC-VSC [1] in terms of efficiency operating at different power ratings (25%, 50%, and 100%). The proposed HMLI topology has 98.2% efficiency when operating at a 25% power rating. In contrast, the NPC-VSC has 96.7% efficiency when operating at a 25% power rating. Similarly, when operating with 50% and 100% power rating the efficiency of the proposed HMLI and existing NPC-VSC have 99.2% and 98.7%, 99.5%, and 99.1%, respectively. Thus, it is concluded that the proposed topology has superior performance compared to the exiting topologies in terms of current THD and efficiency.

## 6. Conclusions

This paper presents the circuit configuration, control methods, simulation and experimental validation of the proposed HMLI topology. The converter topology is the series arrangement of the H-bridge converter and cascaded converter module. It offers several benefits in terms of low switching loss, higher efficiency, and better current THD. Initially, a finite set model predictive control (FS-MPC) was theoretically analyzed as a switching technique for HMLI. The advantages of using the FS-MPC method employed to HMLI are related to more output voltage levels and low current THD. However, the high switching frequency operation of the high-voltage stressed switches is restricted uses for the proposed lower-medium voltage converter (3–5 KV). To minimize the high switching loss, the HMLI topology modules switches are used to the high-voltage and low-voltage stressed modules, and a hybrid control scheme which is the variant of the MPC method, was proposed. This method is computationally efficient and therefore employed to the proposed topology to minimize the switching efforts of the converter. Moreover, the DC-link capacitor voltage is regulated to its reference value for stable converter operation. The performance and effectiveness of single-phase HMLI and a hybrid control scheme has been validated through simulations and experimental results using a low-voltage laboratory prototype. The main findings of this research work are that a new hybrid control scheme has been success-

fully implemented on HMLI topology, which significantly improves efficiency at different loading conditions and reduces current THD when compared with existing techniques.

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