

Article

An Embedded Half-Bridge Γ -Z-Source Inverter with Reduced Voltage Stress on Capacitors

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Abstract: In this paper, an embedded half-bridge Z-source inverter based on gamma structure is proposed. In contrast with the classical half-bridge inverter, the proposed inverter can generate zero voltage levels in output. High voltage gain and low voltage stress on capacitors are the main advantages of the proposed converter. The value of the boost factor in the proposed structure is increased by changing both the shoot-through (ST) duty cycle and turns ratio of the transformer. The operating principle of the proposed converter in four operating modes is presented. We also calculate the critical inductance and compare the proposed converter with conventional topologies. In addition, power loss and THD analysis are presented. Finally, PSCAD/EMTDC software is used to verify the correct operation of the proposed inverter and the experimental results.

Keywords: half-bridge inverter; Z-source inverter; boost factor; shoot-through; voltage stress; gamma structure



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1. Introduction

The Z-source network is one of the important networks in power electronic converters. This network can be used in dc/dc, dc/ac, ac/dc, and ac/ac power conversion. Among the four mentioned types of power conversion, the utilization of the Z-source network in dc/ac power conversion gives significant benefits; hence, the Z-source inverter (ZSI) has been discussed in [1]. The conventional ZSI has an X-shaped impedance network and its Z-source network has two inductors, two capacitors, and one diode. A quasi-Z-source inverter (QZSI) with better features has been presented in [2]. Among these benefits, one can note the reduction in voltage stress and the reduction in input current ripple. In order to decrease the inrush current of the converter in startup, the improved ZSI (IZSI) has been presented in [3]. In [4], the cascaded arrangement of several Z-source networks with low voltage stress on capacitors led to multiple-series Z-source inverters. To increase the boost factor of the presented topology in [4], several networks are required, leading to high volume and high cost.

In some of the articles, Z-source converters have been categorized based on the type of Z-source network of the converter. In general, the impedance networks of the Z-source converters are categorized as conventional Z-source networks and switched Z-source networks [5]. The main difference between these two types of Z-source networks is the existence of a power switch in the switched Z-source converters. To reduce the number of passive elements, a switched boost inverter (SBI) has been presented in [6]. The impedance network of SBI has one inductor, one capacitor, two diodes, and a power switch, and its boost factor is lower than that of ZSI [1]. In order to improve the boost factor of SBI, a current-fed switched inverter (CFSI) has been proposed in [7]. CFSI has the same boost

factor as ZSI [1] and a low input current ripple. A high boost factor has been achieved in [8] by using switched-inductor cells. Another topology for a switched Z-source inverter has been presented in [9], which has several passive and semiconductor elements. The reported topology in [9] has two inductors, two capacitors, four diodes, and one power switch in the impedance network. All proposed topologies in [1–9] can be used as a full-bridge inverter; however, the extension of the Z-source concept to a half-bridge inverter is possible. The half-bridge Z-source inverters feature the same operation as full-bridge inverters but with a two-times lower number of power switches than the full-bridge topology. In [10], a Z-source half-bridge converter with the aim of application in the electrochemical industry has been presented. In [11], a half-bridge Z-source inverter with two Z-source networks has been presented. This topology does not have a high boost factor in comparison with a conventional Z-source inverter but it features low voltage stress of the components. In [12], another topology for a half-bridge Z-source inverter has been presented, but it needs more Z-networks to achieve a high boost factor. The half-bridge switched boost inverter (HF-SBI) has been proposed in [13]. Steady-state analysis and small signal analysis of HF-SBI has been presented in [13]. With the same value of the input voltage and duty cycle, the boost factor of HF-SBI is higher than that of SBI [6] but the input current ripple of HF-SBI is still high. Two different switched half-bridge Z-source inverters have been presented in [14,15]. These topologies have a high boost factor in comparison with conventional topologies, but the use of power switches can lead to complexity in switching and modulation techniques.

Extension of half-bridge Z-source and switched Z-source inverters to a half-bridge transformer-based Z-source inverter is possible [16]. The transformer-based Z-source inverters can control the boost factor of the converter by two parameters, the shoot-through duty cycle and the turns ratio of the transformer [17,18]. A trans-Z-source neutral point clamped inverter has been presented in [19], which is composed of two impedance networks. A transformer based on the presented structures in [7,8] has been introduced in [20,21]. In [20], two types of trans-switched boost inverters have been presented with the same value of the boost factor. A variation of the presented structures in [20] has been proposed in [21]. The number of the elements in [20,21] is the same; however, in the presented structure in [21], a lower turns ratio is needed for increasing the voltage. Furthermore, the cascaded topologies for Z-source inverters based on the transformer and tapped inductors have been presented [22]. A half-bridge trans-Z-source inverter has been reported in [23]. The proposed concept features a continuous input current with a high voltage boost factor. However, comparing the counterparts, the number of components is greater and the converter features high voltage stress of the capacitors.

In this paper, a new embedded topology for the half-bridge Γ -Z-source inverter is proposed. Compared with the conventional Γ -Z-source full-bridge inverter, the input power source is connected in series with power switches instead of a series connection with diodes. The proposed concept features a high boost factor compared to the conventional Z-source inverters. Further, low capacitor voltage stresses and low switching voltage spikes are achieved with the proposed configuration. The paper is organized as follows.

In Section 2, the topology and operating principle of the proposed converter are presented. The design considerations of the magnetic components and capacitors are given in Section 3. In addition, the calculation of power losses and total harmonic distortion is provided in Section 4. A detailed comparison with the other related topologies is presented in Section 5. The power losses and efficiency are evaluated in Section 6. Section 7 validates the effectiveness of the proposed concept using simulation. The control scheme and dynamic of the proposed converter are studied in Section 8. Finally, experimental results are used to verify the correctness of the theoretical analysis in different operating modes.

2. Proposed Topology

The power circuit of the proposed topology is shown in Figure 1. The proposed topology has two transformers with a turns ratio of $N_{12} = N_1/N_2$, diodes D_1 and D_2 , and capacitors C_1 and C_2 . Similar to the classic half-bridge inverter, the proposed half-bridge

inverter has two voltage sources and two switches. In the proposed topology, the magnetizing inductances of the transformers are equal ($L_{m1} = L_{m2} = L_m$) and $C_1 = C_2 = C$. The values of voltage across primary windings in the upper and lower networks ($v_{p1} = v_{p2} = v_p$) are equal. Hence, the following summarization can be considered:

$$v_{p1} = v_{n1} = v_1 \quad (1)$$

$$v_{p2} = v_{n2} = v_2 \quad (2)$$

$$V_{C1} = V_{C2} = V_C \quad (3)$$

$$v_{D1} = v_{D2} = v_D \quad (4)$$

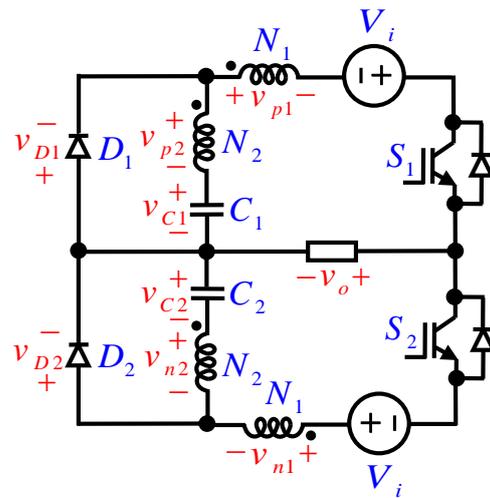


Figure 1. Power circuit of the proposed half-bridge inverter.

2.1. Operating Principle

The operating modes of the proposed inverter are specified by turning on and turning off the diodes and power switches. The number of operating modes in the proposed inverter is four. Figure 2 shows the equivalent circuit of the proposed converter in operation modes. In the first operating mode, both switches S_1 and S_2 are on; so, the proposed inverter is in shoot-through (ST) state. In the second operating mode, switch S_1 is on and switch S_2 is off; hence, the proposed inverter is in non-shoot-through state. In the third operating mode, similar to the first operating mode, both switches S_1 and S_2 are on; so, the proposed inverter is in ST state. In the fourth operating mode, switch S_1 is off and switch S_2 is on. It is important to note that, in the theoretical analysis, all of the elements are assumed to be ideal. More precisely, the following items are considered in the theoretical calculations:

- The series resistance and the voltage drop of the switches and the diodes are ignored;
- The series resistance and the capacitors and the inductors are ignored;
- The internal resistance of the input voltage is ignored;
- The switching method and the turning on and off of semiconductor elements are assumed to be ideal;
- The load of the proposed converter is pure ohmic with resistance R .

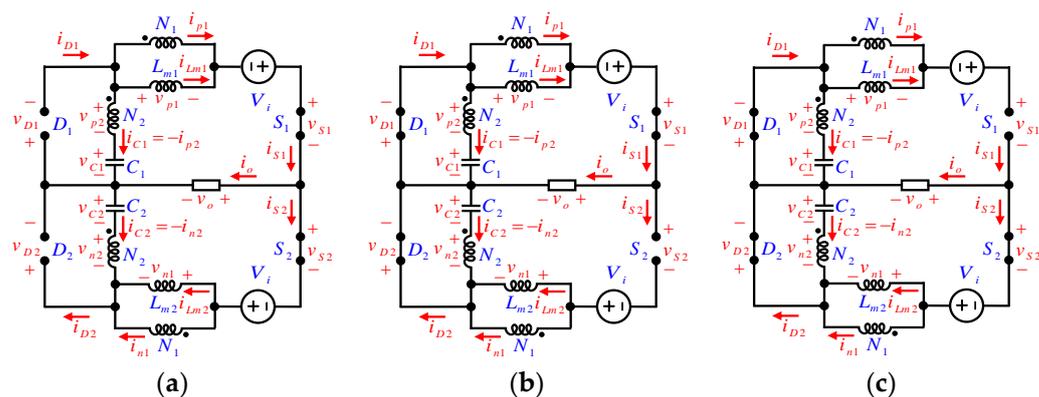


Figure 2. Equivalent circuits of the proposed inverter in different operating modes: (a) first and third operating modes; (b) second operating mode; (c) fourth operating mode.

In the following, the operating principle and detailed analyses are given.

2.1.1. First Operating Mode

The ST state occurs in the first operating mode and both switches are on but both diodes are off. By applying Kirchhoff’s voltage law (KVL) in both the upper and lower networks, the following equations are obtained:

$$V_C + v_2 - v_1 + V_i - v_o \tag{5}$$

$$V_C + v_o + V_i - v_1 + v_2 = 0 \tag{6}$$

By using Equations (5) and (6), the average voltage across the capacitors and the output voltage are obtained as follows:

$$V_C = v_1 - v_2 - V_i = \left(1 - \frac{N_2}{N_1}\right)v_1 - V_i \tag{7}$$

$$v_o = 0 \tag{8}$$

In this operating mode, due to the positive value of the voltage across the magnetizing inductor L_m , the magnetizing current linearly increases from its minimum value ($I_{L,min}$) to its maximum value ($I_{L,max}$). By considering Equation (7), the magnetizing current is obtained as follows:

$$i_{Lm} = \frac{v_1}{L_m}t + I_{L,min} = \frac{N_1 (V_C + V_i)}{(N_1 - N_2)L_m}t + I_{L,min} \tag{9}$$

By considering $i_{p1} = i_{n1} = i_1$, $i_{p2} = i_{n2} = i_2$ and Kirchhoff’s current law (KCL), the following equation can be written:

$$i_2 = i_1 + i_{Lm} \tag{10}$$

Since $i_2 = (N_1/N_2)i_1$, the current through the capacitor C_1 is calculated as follows:

$$i_{C1} = -i_2 = -\frac{N_1}{N_1 - N_2}i_{Lm} \tag{11}$$

2.1.2. Second Operating Mode

In the second operating mode, switch S_1 is on, and switch S_2 is off. The diodes are on. By using KVL, the obtained equations are as follows:

$$V_C = -v_2 = -\frac{N_2}{N_1}v_1 \quad (12)$$

$$v_o = v_{o,\max} = V_i - v_1 = V_i - \frac{N_1}{N_2}v_2 \quad (13)$$

In this operating mode, due to the negative value of the voltage across the magnetizing inductor, the magnetizing current linearly decreases from its maximum value ($I_{L,\max}$) to its minimum value ($I_{L,\min}$). By using Equation (12), the magnetizing current is obtained as:

$$i_{Lm} = \frac{v_1}{L_m}t + I_{L,\max} = -\frac{N_1}{N_2} \frac{V_C}{L_m}t + I_{L,\max} \quad (14)$$

By using KCL, the following equation is obtained as follows:

$$i_{p1} + i_{Lm} = \frac{v_{o,\max}}{R} \quad (15)$$

where R is the load resistance.

The current of capacitor C_1 is obtained by Equation (16):

$$i_{C1} = \frac{N_1}{N_2} \left(i_{Lm} - \frac{v_{o,\max}}{R} \right) \quad (16)$$

2.1.3. Third Operating Mode

In the third operating mode, both diodes are off, but both switches are on. Due to the similarity of the analysis in this operating mode to the first operating mode and to avoid prolongation, detailed analysis is omitted.

2.1.4. Fourth Operating Mode

In the fourth operating mode, switch S_1 is off, and switch S_2 is on. Both of the diodes are on. By using KVL, the following equation is obtained by Equation (17):

$$v_o = v_{o,\min} = -v_{o,\max} = v_1 - V_i \quad (17)$$

The current through the capacitor C_1 is calculated as follows:

$$i_{C1} = -i_{p2} = -\frac{N_1}{N_2}i_{p1} = \frac{N_1}{N_2}i_{Lm} \quad (18)$$

Figure 3a shows a logical diagram and waveforms of the switching pattern. Figure 3b shows waveforms of the current and voltage in the proposed inverter.

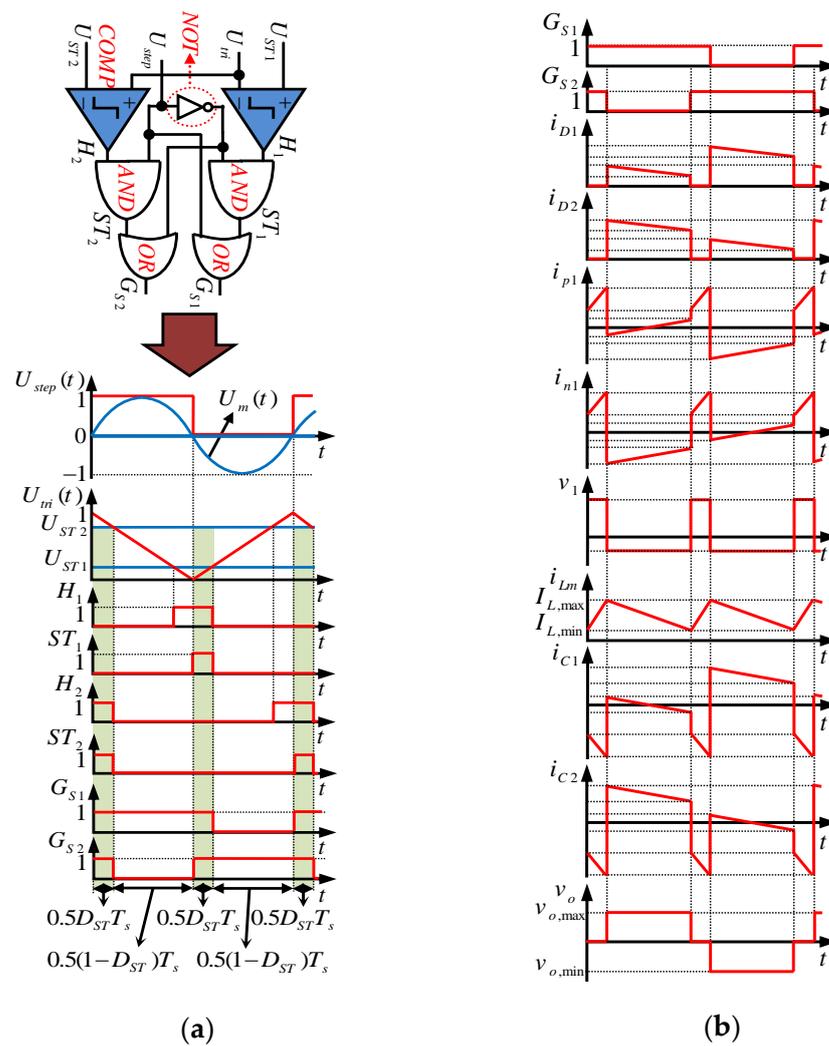


Figure 3. Switching pattern and waveforms of the proposed converter: (a) logical diagram and waveforms of switching pattern; (b) waveforms of current and voltage.

2.2. Boost Factor

The average voltage across the magnetizing inductor in steady state is zero; hence, the following equation can be written:

$$\int_0^{T_s} v_1 dt = 0 \tag{19}$$

By using Equations (7), (12), and (19), the following equation is derived:

$$\frac{N_1 (V_C + V_i)}{N_1 - N_2} D_{ST} T_s - \frac{N_1 V_C}{N_2} (1 - D_{ST}) T_s = 0 \tag{20}$$

where D_{ST} and T_s are the ST duty cycle and switching period, respectively.

From Equation (20), the average voltage across the capacitors is calculated as follows:

$$V_C = \frac{D_{ST}}{N_{12}(1 - D_{ST}) - 1} V_i \tag{21}$$

where N_{12} is equal to the ratio of N_1/N_2 and the range of the ST duty cycle is $0 \leq D_{ST} < 1 - (1/N_{12})$.

By using Equations (12), (13), and (21), the maximum output voltage is calculated as follows:

$$v_{o,\max} = \frac{N_{12} - 1}{N_{12}(1 - D_{ST}) - 1} V_i \quad (22)$$

Due to the definition of the boost factor for the proposed inverter as $B = (v_{o,\max}/V_i)$, the following equation for the boost factor is derived:

$$B = \frac{N_{12} - 1}{N_{12}(1 - D_{ST}) - 1} \quad (23)$$

3. Design Considerations

In steady state, the average value of the capacitor's current is zero; hence, the following equation can be written:

$$\int_0^{T_s} i_C dt = 0 \quad (24)$$

From Equations (11), (16), and (24), the following equation can be written:

$$-\frac{N_1}{N_1 - N_2} I_{Lm} D_{ST} + \frac{N_1(1 - D_{ST})}{2N_2} \left(2I_{Lm} - \frac{v_{o,\max}}{R} \right) = 0 \quad (25)$$

By solving Equation (25), the average current through the magnetizing inductors is obtained as follows:

$$I_{Lm} = \frac{(1 - D_{ST})(N_1 - N_2)}{2R(N_1 - N_2 - N_1 D_{ST})} v_{o,\max} \quad (26)$$

By using Equations (22) and (26), I_{Lm} is calculated as follows:

$$I_{Lm} = \frac{(1 - D_{ST})(N_{12} - 1)^2}{2R[N_{12}(1 - D_{ST}) - 1]^2} V_i \quad (27)$$

For a proper design, the ripple of magnetizing current should be calculated. By using of Equation (7), the following equation is written:

$$L_m \frac{\Delta i_{Lm}}{0.5 D_{ST} T_s} = \frac{N_1}{N_1 - N_2} (V_i + V_C) \quad (28)$$

where Δi_{Lm} is the ripple of the magnetizing current.

By using Equations (21) and (28), Δi_{Lm} is obtained as follows:

$$\Delta i_{Lm} = \frac{N_{12} D_{ST} (1 - D_{ST})}{2L_m f_s [N_{12}(1 - D_{ST}) - 1]} V_i \quad (29)$$

To calculate the voltage ripple across capacitors, Δv_C , we use:

$$\Delta v_C = \frac{N_1}{N_2 C} \int_0^{0.5(1-D_{ST})T_s} \left(\frac{v_1}{L_m} t + I_{L,\max} \right) dt \quad (30)$$

By solving Equation (30), Δv_C can be written as follows:

$$\Delta v_C = \frac{N_{12}(N_{12} - 1)^2 (1 - D_{ST})^2}{4RC f_s [N_{12}(1 - D_{ST}) - 1]^2} V_i \quad (31)$$

By defining the percentage of permissible current ripple of the magnetizing inductance ($x_{Lm}\%$) and the percentage of permissible voltage ripple for capacitors ($x_C\%$), we have:

$$x_{Lm}\% = \frac{\Delta i_{Lm}}{I_{Lm}} \times 100 \quad (32)$$

$$x_C\% = \frac{\Delta v_C}{V_C} \times 100 \quad (33)$$

By using Equations (27), (29), and (32), $x_{Lm}\%$ is derived as follows:

$$x_{Lm}\% = \frac{N_{12}D_{ST}R[N_{12}(1 - D_{ST}) - 1]}{L_m f_s(N_{12} - 1)^2} \times 100 \quad (34)$$

By using Equation (34), the value of the magnetizing inductors is obtained as follows:

$$L_m = \frac{N_{12}D_{ST}R[N_{12}(1 - D_{ST}) - 1]}{x_{Lm}\% f_s(N_{12} - 1)^2} \times 100 \quad (35)$$

By considering Equations (21), (31), and (33), $x_C\%$ is derived as follows:

$$x_C\% = \frac{N_{12}(N_{12} - 1)^2(1 - D_{ST})^2}{4RCf_sD_{ST}[N_{12}(1 - D_{ST}) - 1]} \times 100 \quad (36)$$

Hence, the value of the capacitors can be written as follows:

$$C = \frac{N_{12}(N_{12} - 1)^2(1 - D_{ST})^2}{4Rf_sx_C\%D_{ST}[N_{12}(1 - D_{ST}) - 1]} \times 100 \quad (37)$$

It is noticeable that the calculated inductance from Equation (35) should not lead to improper operating states. It should be mentioned that two operating states can occur in the proposed inverter. In the first operating state, the synchronous operation of diodes (SOD) leads to four operating modes, and D_1 and D_2 turn on and off simultaneously. Detailed analyses of these operating modes have been described in the previous sections. By selecting a small magnetizing inductance, SOD is disrupted. Asynchronous operation of diodes (AOD) in the second operating state leads to an asymmetrical output voltage with more than four operating modes. To avoid AOD, the critical inductance ($L_{m,crit}$) should be lower than the magnetizing inductance. In the boundary condition between SOD and AOD, the current through diode D_1 at the second operating mode reaches zero. Hence, by using Equation (16), the following equation is derived:

$$i_{D1} = i_{C1} + i_o = \frac{N_1}{N_2}i_{Lm} - \frac{N_1 v_{o,max}}{N_2 R} + \frac{v_{o,max}}{R} = 0 \quad (38)$$

From Equations (14) and (38), the following equation for $L_{m,crit}$ is calculated:

$$L_{m,crit} = \frac{RN_{12}^2[N_{12}(1 - D_{ST}) - 1]D_{ST}(1 - D_{ST})}{2f_s[2(N_{12} - 1)^2 - N_{12}(N_{12} - 1)^2(1 - D_{ST})]} \quad (39)$$

4. Power Loss and THD Calculation

4.1. Power Loss Calculation

In order to calculate the power loss of the proposed converter, the method that has been presented in [9,24] is used. At first, the power loss of each element is calculated and then the total power loss is obtained from the sum of them.

The power losses in semiconductor elements are divided into conduction power loss and switching power loss. The voltage and current of the switch (S_1) for a period are obtained as follows:

$$v_{S1} = \begin{cases} 0 & 0 \leq t \leq 0.5D_{ST}T_s \text{ (1st mode)} \\ 0 & 0 \leq t \leq 0.5(1 - D_{ST}T_s) \text{ (2nd mode)} \\ 0 & 0 \leq t \leq 0.5D_{ST}T_s \text{ (3rd mode)} \\ 2|v_{o,\min}| & 0 \leq t \leq 0.5(1 - D_{ST}T_s) \text{ (4th mode)} \end{cases} \quad (40)$$

$$i_{S1} = \begin{cases} \frac{N_1}{N_1 - N_2} I_{Lm} & 0 \leq t \leq 0.5D_{ST}T_s \text{ (1st mode)} \\ \frac{N_1}{N_2} \left(\frac{v_{o,\max}}{R} - I_{Lm} \right) & 0 \leq t \leq 0.5(1 - D_{ST}T_s) \text{ (2nd mode)} \\ \frac{N_1}{N_1 - N_2} I_{Lm} & 0 \leq t \leq 0.5D_{ST}T_s \text{ (3rd mode)} \\ 0 & 0 \leq t \leq 0.5(1 - D_{ST}T_s) \text{ (4th mode)} \end{cases} \quad (41)$$

According to Equation (41), the conduction power loss of the switch S_1 is calculated as follows:

$$P_{Cond,S1} = \frac{D_{ST}N_1}{N_1 - N_2} I_{Lm} \left(V_{F,S} + \frac{N_1}{N_1 - N_2} r_S I_{Lm} \right) + \frac{0.5(1 - D_{ST})N_1}{N_2} \left(\frac{v_{o,\max}}{R} - I_{Lm} \right) \left[V_{F,S} + r_S \frac{0.5N_1}{N_2} \left(\frac{v_{o,\max}}{R} - I_{Lm} \right) \right] \quad (42)$$

where r_S and $V_{F,S}$ are the series resistance and the voltage drop of the switch in conduction mode, respectively.

By considering Equations (40) and (41), the switching power loss of S_1 in $t_{on,S}$ and $t_{off,S}$ (turn-on and turn-off time) is calculated as follows:

$$P_{Sw}^{on,off} = \frac{N_1}{3(N_1 - N_2)} f_s B I_{Lm} V_i (t_{on,S} + t_{off,S}) \quad (43)$$

In order to calculate the power loss of the diodes, the voltage and current of the diode D_1 should be calculated for a period as follows:

$$v_{D1} = \begin{cases} \frac{N_{12}V_C + V_i}{1 - N_{12}} & 0 \leq t \leq 0.5D_{ST}T_s \text{ (1st mode)} \\ 0 & 0 \leq t \leq 0.5(1 - D_{ST}T_s) \text{ (2nd mode)} \\ \frac{N_{12}V_C + V_i}{1 - N_{12}} & 0 \leq t \leq 0.5D_{ST}T_s \text{ (3rd mode)} \\ 0 & 0 \leq t \leq 0.5(1 - D_{ST}T_s) \text{ (4th mode)} \end{cases} \quad (44)$$

$$i_{D1} = \begin{cases} 0 & 0 \leq t \leq 0.5D_{ST}T_s \text{ (1st mode)} \\ \frac{N_1}{N_2} \left(I_{Lm} - \frac{v_{o,\max}}{R} \right) + \frac{v_{o,\max}}{R} & 0 \leq t \leq 0.5(1 - D_{ST}T_s) \text{ (2nd mode)} \\ 0 & 0 \leq t \leq 0.5D_{ST}T_s \text{ (3rd mode)} \\ \frac{N_1}{N_2} I_{Lm} & 0 \leq t \leq 0.5(1 - D_{ST}T_s) \text{ (4th mode)} \end{cases} \quad (45)$$

The conduction and switching loss of the diode D_1 are calculated from the below equations.

$$P_{Cond,D1} = 0.5(1 - D_{ST}) \left[\frac{N_1}{N_2} \left(I_{Lm} - \frac{v_{o,\max}}{R} \right) + \frac{v_{o,\max}}{R} \right] \left\{ V_{F,D} + r_D \left[\frac{N_1}{N_2} \left(I_{Lm} - \frac{v_{o,\max}}{R} \right) + \frac{v_{o,\max}}{R} \right] \right\} + 0.5(1 - D_{ST}) \left(\frac{N_1}{N_2} I_{Lm} \right) \left(V_{F,D} + r_D \frac{N_1}{N_2} I_{Lm} \right) \quad (46)$$

$$P_{Sw,D1}^{off} = \frac{N_{12}V_C + V_i}{6(1 - N_{12})} f_s \left[2N_{12}I_{Lm} + \frac{v_{o,\max}}{R} (1 - N_{12}) \right] t_{off,D} \quad (47)$$

where r_D and $V_{F,D}$ are the series resistance and the voltage drop of the diodes in conduction mode, respectively.

According to the symmetrical operation of the proposed converter, the power loss of the switch S_2 and the diode D_2 are the same as the power loss of S_1 and D_1 , respectively.

The power loss of the capacitors is obtained as:

$$P_{rC} = \frac{1}{T_s} \int_0^{T_s} r_C i_C^2 dt \quad (48)$$

where r_C is the internal series resistance capacitors.

By considering the value of i_{C1} Equations (11), (16), and (18), the power loss of the capacitors is obtained as follows:

$$P_{C1} = P_{C2} = r_{C1} \left[\left(\frac{N_1}{N_1 - N_2} I_{Lm} \right)^2 D_{ST} + \left(0.5(1 - D_{ST}) \frac{N_1}{N_2} I_{Lm} \right)^2 \right] + 0.5r_{C1}(1 - D_{ST}) \left(\frac{N_1}{N_2} \left(I_{Lm} - \frac{v_{o,max}}{R} \right) + \frac{v_{o,max}}{R} \right)^2 \quad (49)$$

The power loss of inductors is expressed by the core loss and conduction power loss. The core power loss is calculated as follows:

$$P_{CL} = 0.33B^{1.98} f^{1.64} V_{eff} \quad (50)$$

where B is the flux density, f is the frequency in kHz, and V_{eff} is the effective core volume.

The conduction power loss of inductors is expressed by the values of resistance of inductors (r_L) and the RMS current of them as follows:

$$P_{rL1} = P_{rL2} = r_L I_{Lm}^2 \quad (51)$$

4.2. THD Calculation

In order to obtain the relation of the total harmonic distortion (THD) for the proposed converter, the Fourier series of the output voltage should be considered as follows:

$$v_o = \sum_{m=1,3,5,\dots}^{\infty} X_m \sin(m\omega t) \quad (52)$$

The value of X_m in Equation (52) is calculated from the below equation. It should be noted that because v_o is an odd function, the a_n Fourier coefficient is equal to zero.

$$X_m = \frac{2}{T_s} \int_0^{T_s} v_o \sin(m\omega t) d\omega t = \frac{2BV_i}{m\pi} \left[-\cos(m\omega t) \Big|_{\pi - 0.5\pi D_{ST}}^{0.5\pi D_{ST}} \right] \quad (53)$$

By simplifying the above equation, the following equation is obtained:

$$X_m = \frac{4BV_i}{m\pi} \cos(0.5m\pi D_{ST}) \quad (54)$$

The RMS value of the output voltage is calculated from the following equation:

$$V_{o,rms} = \sqrt{1 - D_{ST}} BV_i \quad (55)$$

Considering Equations (54) and (55), the value of THD is calculated as follows:

$$THD = \frac{\sqrt{V_{o,rms}^2 - X_{1,rms}^2}}{X_{1,rms}} = \frac{\sqrt{2V_{o,rms}^2 - X_1^2}}{X_1} \quad (56)$$

By simplifying the above equation, the value of THD is as follows:

$$THD = \frac{\sqrt{2\pi^2(1 - D_{ST}) - [4\cos(0.5\pi D_{ST})]^2}}{4\cos(0.5\pi D_{ST})} \quad (57)$$

5. Comparison

In this section, the proposed converter is compared with the literature regarding the different parameters, such as the boost factor and voltage stress on capacitors. Table 1 shows the relation among the boost factor and the maximum voltage stress across the capacitors in the proposed and the conventional structures.

Table 1. Comparison of the parameters of the proposed and conventional structures.

Structures	Boost Factor	Maximum Voltage Stress across of Capacitors
Proposed	$\frac{N_{12}-1}{N_{12}(1-D_{ST})-1}$	$\frac{D_{ST}BV_i}{N_{12}-1}$
ZSI [1]	$\frac{1}{1-2D_{ST}}$	$(1-D_{ST})BV_i$
QZSI [2]	$\frac{1}{1-2D_{ST}}$	$(1-D_{ST})BV_i$
IZSI [3]	$\frac{1}{1-2D_{ST}}$	$(1-D_{ST})BV_i$
Multiple SZSI [4]	$\frac{1}{1-(N+1)D_{ST}}$	$D_{ST}BV_i$
SBI [6]	$\frac{1-D_{ST}}{1-2D_{ST}}$	BV_i
CFSI [7]	$\frac{1}{1-2D_{ST}}$	BV_i
Switched inductor ESBI [8]	$\frac{1+D_{ST}}{1-3D_{ST}}$	BV_i
DA-SZSI [9]	$\frac{1}{1-3D_{ST}+D_{ST}}$	BV_i
Half-bridge ZSI [10]	$\frac{1}{1-2D_{ST}}$	$2BV_i$
Half-bridge SZSI [11]	$\frac{1}{1-(N+1)D_{ST}}$	$D_{ST}BV_i$
Low-stress half-bridge ZSI [12]	$\frac{1-(N-1)D_{ST}}{1-(N+1)D_{ST}}$	$\frac{2D_{ST}BV_i}{1-(N-1)D_{ST}}$
Half-bridge SBI [13]	$\frac{1-D_{ST}}{1-3D_{ST}}$	BV_i
Half-bridge qSBI [14]	$\frac{1-D_{ST}}{1-3D_{ST}}$	$\frac{2D_{ST}BV_i}{1-D_{ST}}$
Diode-assisted half-bridge ZSI [15]	$\frac{1}{1-3D_{ST}}$	BV_i
Trans ZSI [17]	$\frac{1}{1-(N+1)D_{ST}}$	$ND_{ST}BV_i$
Trans SBI [19]	$\frac{1+ND_{ST}}{1-(N+2)D_{ST}}$	BV_i

5.1. Comparison of Boost Factor

The boost factor of the proposed converter depends on two factors. The first factor is the value of the ST duty cycle, and the second factor is the turns ratio of the used transformer. Figure 4a shows the boost factor of the proposed converter for different values of N_{12} . As can be appreciated from Figure 4a, the boost factor increases by increasing the turns ratio of the transformers. In Figure 4b, the boost factor of the proposed converter with $N_{12} = 5/4$ is compared with [4,7]. Figure 4c,d show the variation in the boost factor for $N_{12} = 4/3$ and $N_{12} = 3/2$ with the presented topologies in [1–3,5,6,8–14]. As can be appreciated from Figure 4c, the proposed converter features a high boost factor. For the proposed converter, a boost factor of 10 could be achieved for an ST duty cycle around 0.2, but for the proposed converter in [13,14], it is achievable at an ST duty cycle around 0.3. It is worth mentioning that, for the same condition, the boost factor of the proposed converter could be increased by increasing the turn ratio of the transformers.

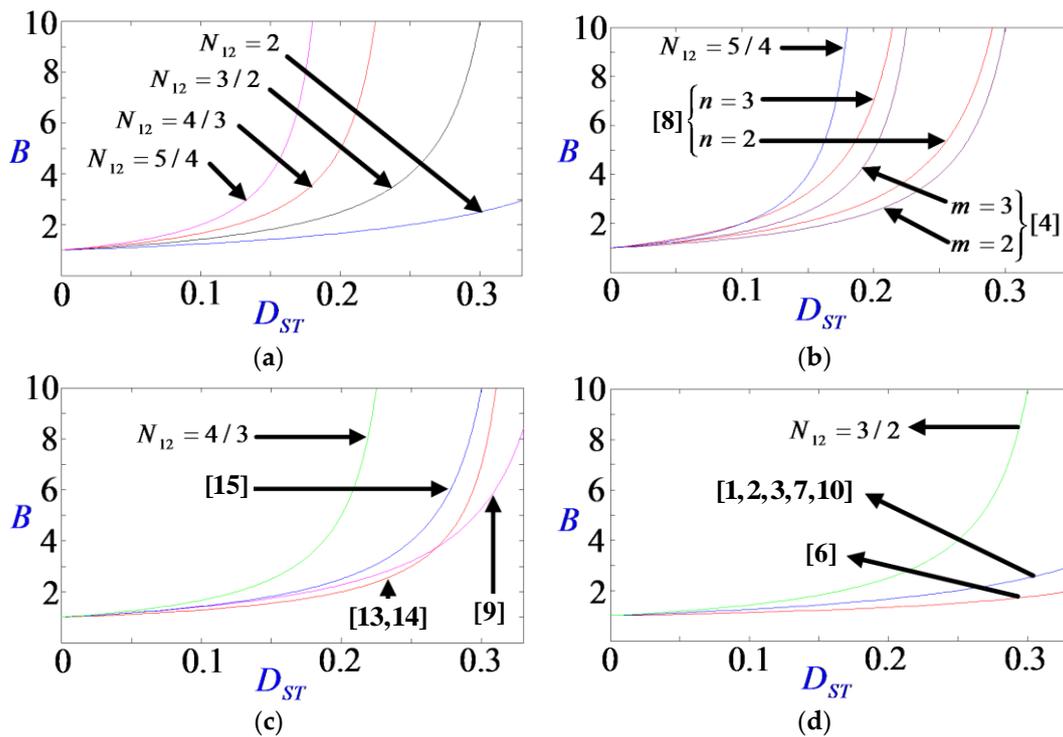


Figure 4. Comparison of boost factor of proposed converter: (a) for different values of N_{12} ; (b) for $N_{12} = 5/4$; (c) for $N_{12} = 4/3$; (d) for $N_{12} = 3/2$.

5.2. Comparison of Voltage Stress on Capacitors

The voltage stress of the capacitors is one of the parameters that could be considered for the benchmarking of the converters. This value for the proposed converter is lower than some conventional inverters for low values of the ST duty cycle. According to Equation (21), the voltage stress in $D_{ST} = 0$ is close to zero, which results in soft-start capability [25]. Figure 5a shows the normalized value of the voltage stress of the capacitors for different values of N_{12} . The voltage stress of the capacitors for the proposed and conventional inverters is compared in Figure 5b. As can be seen for the turns ratio of $N_{12} = 2$, the voltage stress of the capacitors is the lowest for the proposed converter. For the turns ratio of $3/2$, it is the lowest for ST duty cycles lower than 0.25, and it increases by increasing the D_{ST} .

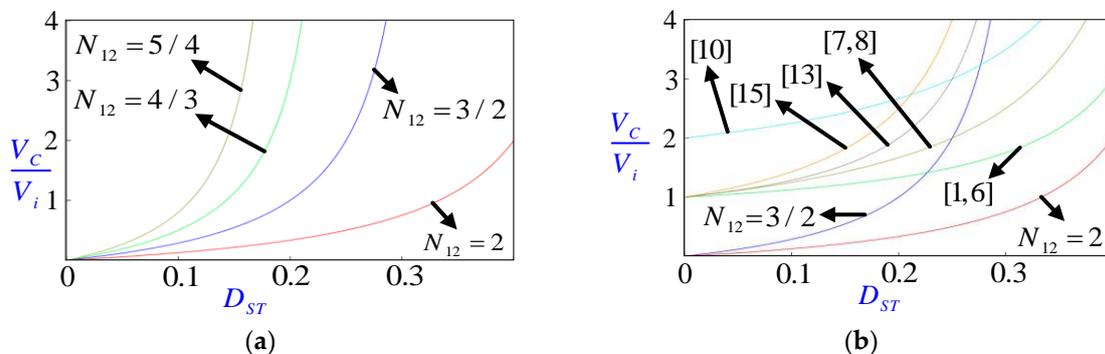


Figure 5. Voltage stress of the capacitors versus shoot-through duty cycle: (a) Different values of turns ratio; (b) Proposed converter and references.

6. Power Losses and Efficiency Evaluation

Based on the given methodology in Section 4, the power losses of the proposed converter are analyzed. Figure 6 shows the power loss distribution of the proposed converter. The estimation was carried out at the input power of 400 W for the given values in Table 4. As can be appreciated from Figure 6, the power losses of the semiconductors dominate over the power losses of the inductors and capacitors. Around 32% of the power losses are switching losses, and 37% of the dissipated power is for conduction losses in the switches. As can be seen, the switching losses are lower than the conduction losses of the switches. As the proposed converter operates at a low switching frequency, the switching losses are low compared with the conduction losses. The diodes feature a power loss that is lower than the total power losses of the switches. Most of the power losses for diodes are conduction losses, as the used diodes are Schottky barrier diodes; the conduction losses dominate over the turn-off losses of the diodes. Based on the estimated power losses, the efficiency of the proposed converter is 90.35%.

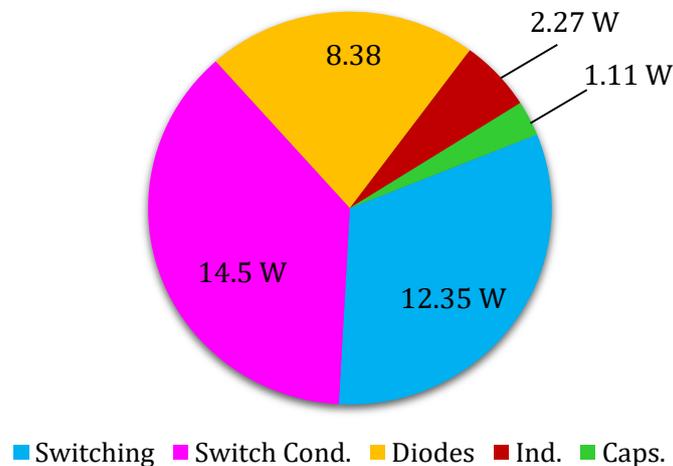


Figure 6. Distribution of power losses at the input power of 400 W.

Table 4. Selected values of parameters.

Parameter	Symbol	Value
Input voltage	V_i	48 V
Switching frequency	f_s	10 kHz
Load resistance	R	100 Ω
Turns ratio	N_{12}	4/3
Magnetizing inductance	L_m	2.5 mH
Capacitors	C	100 μ F
Shoot-through duty cycle	D_{ST}	0.2
Switches	S_1, S_2	Cree C3M0120100K
Diodes	D_1, D_2	Vishay VS-10ETS12THM3
Equivalent resistance	r_L	395 m Ω
ESR of capacitors	r_C	6 m Ω
Drain-source on-state resistance	R_{DS}	141 m Ω
Rise time	t_{on}	15 ns
Fall time	t_{off}	8 ns
Forward voltage drop	V_{FD}	1.1 V
Forward resistance	r_D	20 m Ω

Figure 7 shows the comparison of the estimated efficiency for the proposed converter and the reported converters in [11,16,26]. As can be appreciated from Figure 7, the proposed converter features the highest efficiency. The number of components is same for the proposed converter and [16]. However, the proposed configuration features a low voltage

stress in the capacitors and switches that results in high efficiency. The proposed converters in [11,26] feature a higher number of components than the proposed converter and [16]; due to this and the high RMS current of the switches, the efficiency is low for [11,26], with a difference of around 2.5% at the full-load condition. The difference for the part- and full-load conditions is higher than that for the light-load condition, as, for the full-load condition, the conduction losses dominate the switching losses. The efficiency for the proposed converter in [26] is the lowest as the number of components, especially semiconductors, is the highest.

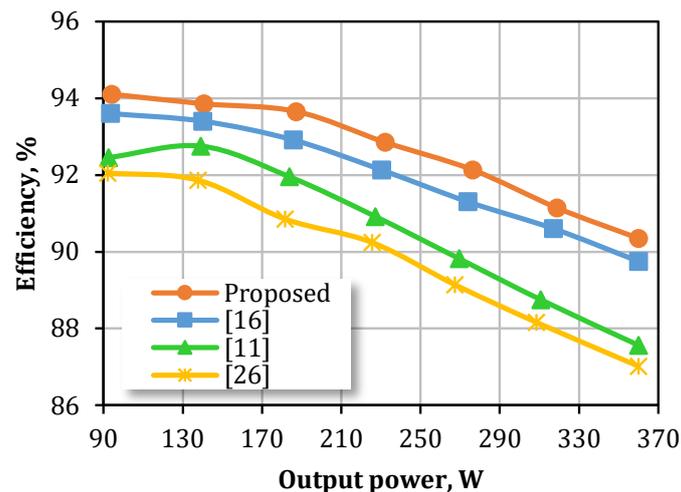


Figure 7. Comparison of estimated efficiency at the output power range of 90 W to 360 W.

7. Simulation Results

In this section, the given theoretical analysis and operation of the proposed converter are verified using PSCAD/EMTDC software. Selected values of parameters are reported in Table 4. It is noticeable that the selected value for magnetizing inductance is higher than the critical inductance, with a value of 914 μH , which is calculated from equation (39). On the other hand, $x_{Lm}\%$ and $x_C\%$ are lower than 70% and 2%, respectively.

Figure 8a shows waveforms of the current through diodes D_1 and D_2 . According to this figure, the current through diodes in the ST state is zero, which is in line with Figure 3b. Figure 8b shows the primary side current, which verifies theoretical concepts. Figure 8c shows the voltage and current of the primary magnetizing inductor. As can be observed from Figure 8c, the voltages in ST and non-ST states are 762.01 V and -190.98 V, which are close to values of 768 V and -192 V calculated from (12) and (17), respectively. The simulated average value and ripple of the magnetizing current are 4.76 A and 3.18 A, which differ slightly from the values of 4.80 A and 3.07 A calculated from (27) and (29). Figure 8d shows the waveform of the capacitors' current. These waveforms have a 180° phase degree with each other, which is in agreement with theory. Figure 9 shows the voltage across capacitors and the output voltage. According to Figure 9a, voltage ripple and average voltage values across capacitors are 2.57 V and 142.12 V, respectively. The estimated value from Equations (31) and (21) equals 2.56 V and 144 V, indicating minor differences between simulated and estimated values. According to Figure 9b, the output voltage has negative, positive, and zero levels. The maximum value of the output voltage is 237.82 V, which is in line with the value of 240 V calculated from (22). In general, the simulation results are in good agreement with the theoretical results.

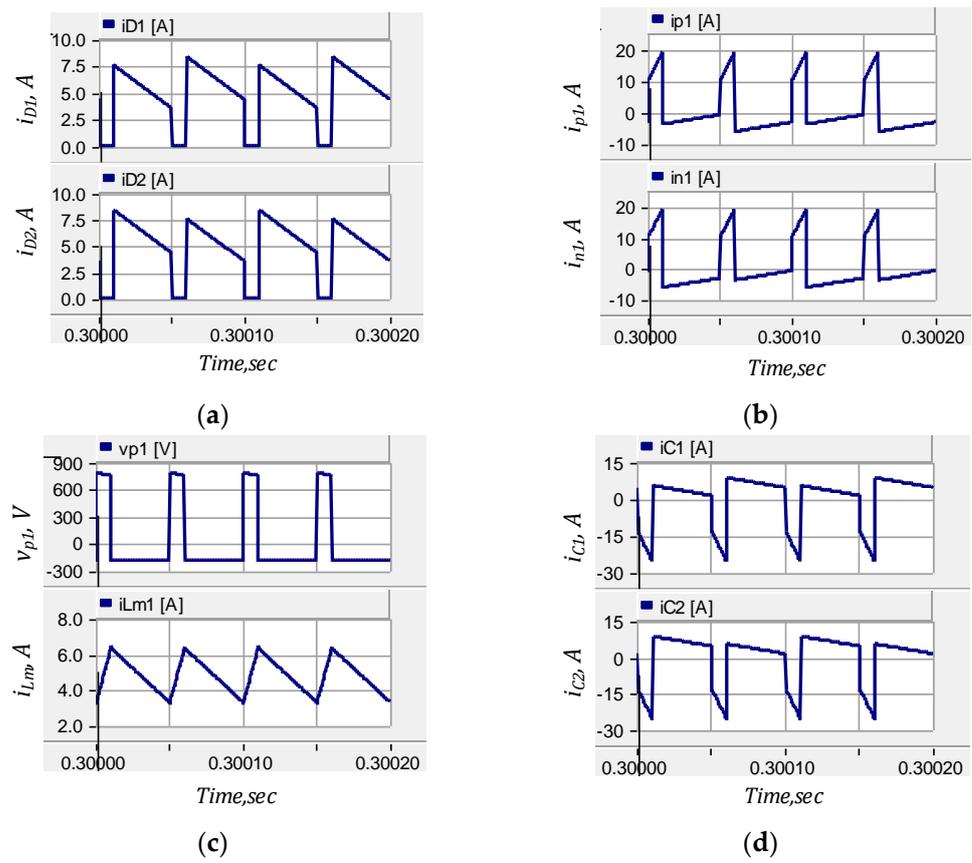


Figure 8. Simulation results: (a) current through diodes; (b) current through primary windings; (c) voltage and current of the primary magnetizing inductor; (d) current through capacitors.

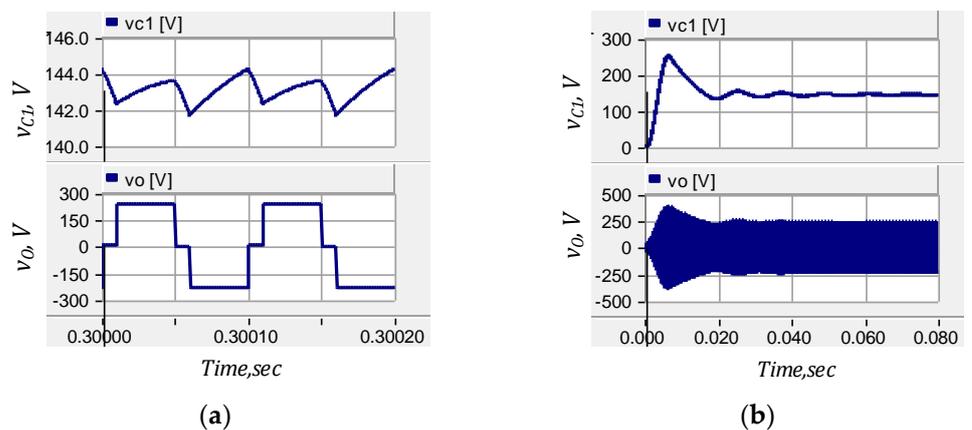


Figure 9. Simulation results of voltage of capacitors and output voltage: (a) steady state; (b) dynamic response.

Figure 10 shows the simulation results of the proposed converter during the transient state. Figure 9a shows the voltage across capacitor C_1 . As can be seen, the voltage across the capacitor reaches a steady state after 0.04 s. Figure 9b shows the output voltage waveform at the startup moment. According to this figure, the proposed inverter has stable operation, and the dynamic response is appropriate.

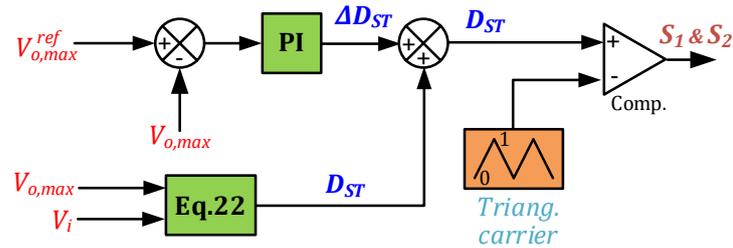


Figure 10. Implementation of control strategy.

8. Control Scheme and Dynamic Performance

Figure 10 shows the schematic of the control strategy for the proposed converter. The Pulse Width Modulation (PWM) method is used to control the switches. In order to control the maximum value of the output voltage, a PI controller is used. The maximum value of the output voltage of the proposed converter is compared with the desired value of the output voltage (V_{o,max_ref}), and if there is a difference, it is applied to the controller to produce a desirable duty ratio. The desirable duty ratio is compared with a carrier wave, and then suitable interpolated pulses are produced to the switches. The PI controller has a gain and time constant; these parameters are defined by a trade-off. In order to show the stable performance of the proposed converter, the simulated dynamic response of the output voltage for a step change in the input voltage is shown in Figure 11. As can be appreciated from Figure 11, by applying a step change in the input voltage, the converter shows stable performance. By increasing the input voltage when the converter operates in steady state, the feedback control system changes the ST duty cycle to fix the operating point at the constant output voltage, with a maximum value of 240 V when the ST duty cycle is decreased. After a short operation at an input voltage of 58 V, the voltage is step changed to 48 V and the closed-loop control system operates as the maximum value of the output voltage is fixed at 240 V by increasing the duty cycle. The stable operation of the proposed converter could be confirmed by carrying out the step change process.

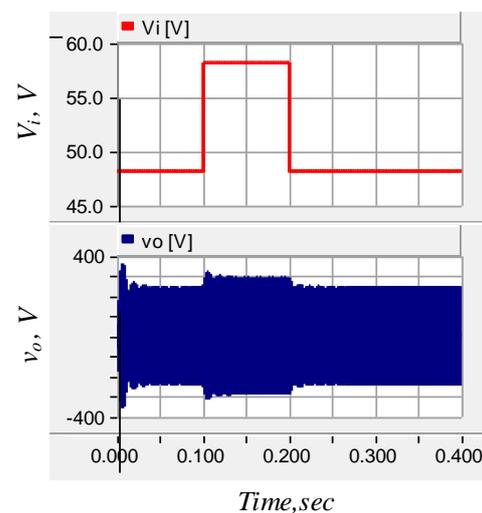


Figure 11. Dynamic response for the proposed converter due to a step change in input voltage.

9. Experimental Verification

In this section, experimental results are provided to verify the validity of the theoretical analysis and simulation results. A 400 W prototype (Figure 12) was assembled based on the main schematics of the proposed converter shown in Figure 1. The main specifications and types of semiconductor components used in the prototype are listed in Table 4. The converter was tested at the input voltage of 48 V, which was provided by the power supply EA PSI9080-60. The maximum value of output voltage was regulated to 240 V. The

converter was controlled by the microcontroller STM32F334R8T6, utilizing a Cortex-M4 core. The driver circuit consisted of an ACPL-K342 BROADCOM optocoupler and dc-dc converter PEM1-S12-D15-S. The power conversion efficiency was measured with the help of a precision power analyzer, Yokogawa WT1800. Figure 13a shows waveforms of the current through diodes D_1 and D_2 . According to this figure, the current through diodes in the ST state is zero, in agreement with Figure 3b. Figure 13b shows the primary side current of the transformers, which verifies theoretical concepts. Figure 13c shows the waveform of the current through capacitors C_1 and C_2 , respectively. These waveforms have a 180° phase degree with each other, which is in agreement with theory. Figure 14a shows the voltage of the primary magnetizing inductor. According to this figure, voltages in ST and non-ST states are 750 V and -190 V , close to the values of 768 V and -192 V estimated by (17) and (12), respectively. The measured waveform of the voltage across the capacitor and the output voltage is shown in Figure 14b,c. As can be appreciated from Figure 14b, the average value of the voltage across the capacitor is close to 137 V . The difference between 144 V calculated from (21) with the measured values is insignificant. According to Figure 14c, the output voltage has negative, positive, and zero levels. The maximum value of the output voltage is close to 231 V , which agrees with the value of 240 V calculated from (22). In general, the experimental results are in good agreement with the theoretical results.

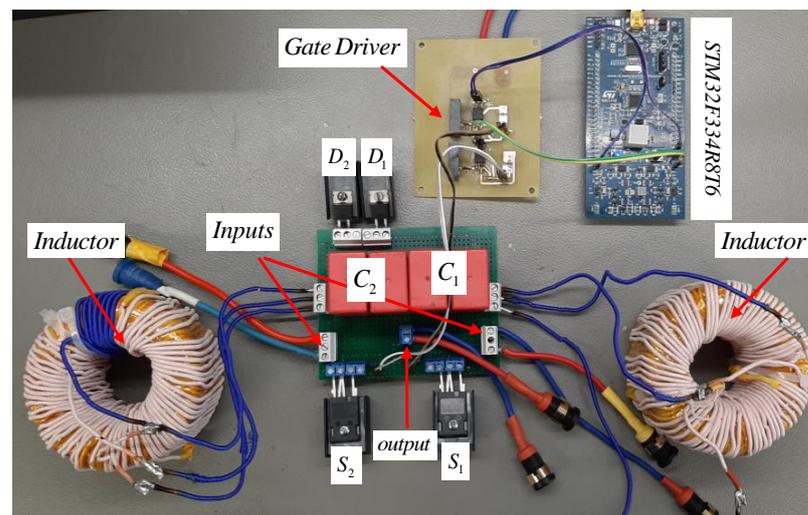


Figure 12. General view of the 400 W experimental prototype of the proposed converter.

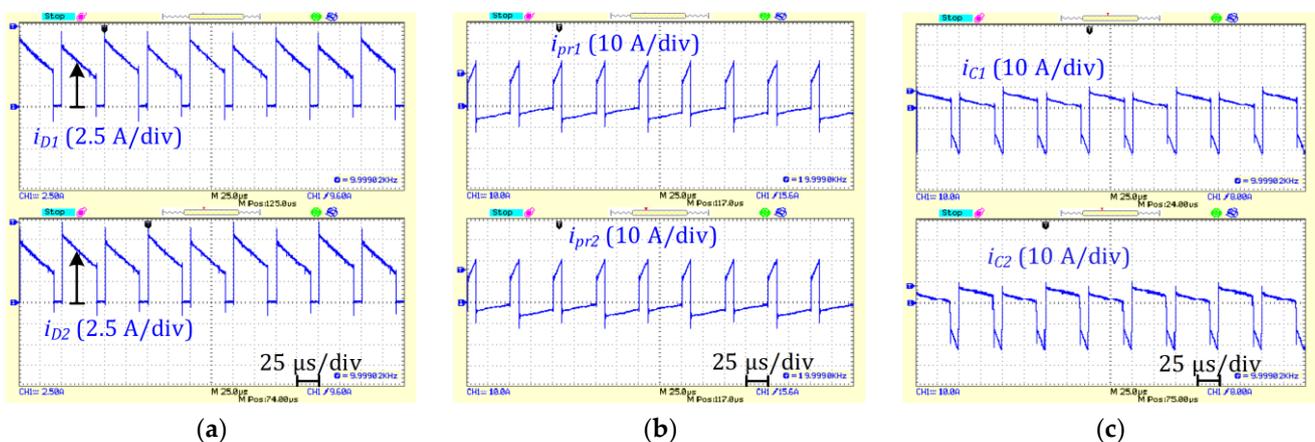


Figure 13. Experimental results: (a) current through diodes; (b) current through primary windings; (c) current through capacitors.

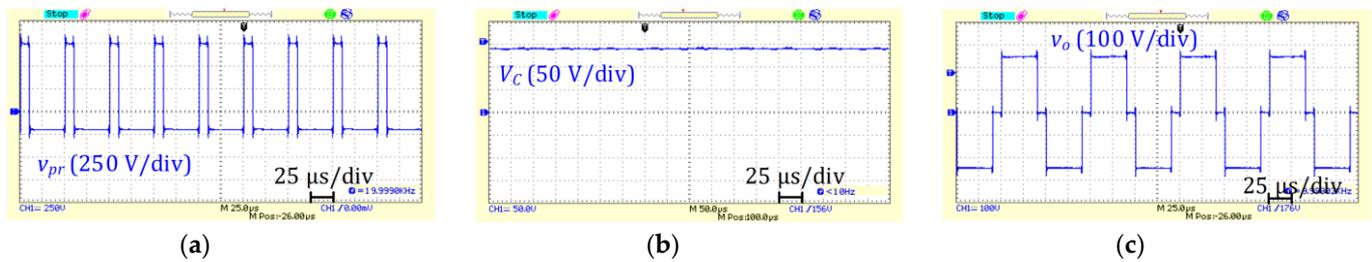


Figure 14. Experimental results: (a) voltage of primary magnetizing inductor; (b) voltage across capacitor; (c) output voltage.

Figure 15 shows the heat distribution of the prototype under the input power of 400 W. The photo was recorded with a Fluke thermal camera. As can be appreciated from Figure 15, the hottest points are the semiconductors. The average temperature for the switches is 47 °C, and it is 40 °C for the diodes. This shows that the majority of the dissipated power belongs to the semiconductors. This could be predicted from the power loss analysis described in Section 6, as the power losses of the semiconductors dominate over the power losses of the magnetics and capacitors.

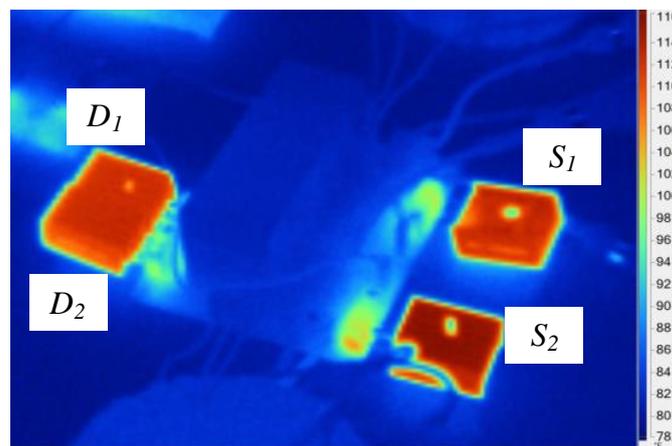


Figure 15. Heat distribution of the prototype under the test conditions at the input power of 400 W.

Figure 16 shows the comparison of the measured and estimated efficiency for the proposed converter and the reported structures in [11,16]. As can be seen, the proposed converter has the highest efficiency at the input power of 100 W and the lowest at the full-load condition. For a constant value of output voltage, the RMS current increases by increasing the input power, which results in high conduction losses and a reduction in the efficiency by around 3.5%. Comparing the measured efficiency to the estimated results, the measured efficiency follows the same trend as the estimated efficiency. The deviations between the estimated and experimental results are caused by thermal effects, which are not considered in the model: the diodes increase their resistance with temperature (0.38% per Kelvin); the on-state drain-source resistance changes with temperature (0.44% per Kelvin); the tolerance margin of datasheet parameters also has an effect (for example, 33% difference between typical and maximum on-state drain-source resistance). Figure 16b shows the comparison of the measured efficiency between the proposed concept and reported structures in [11,16]. As can be appreciated from Figure 16b, the efficiency is the highest for the proposed converter and the lowest for [11] when comparing the number of components; moreover, for the same boost factor, the RMS current of the proposed converter in [11] is higher than that of for the proposed converter, which results in a 1.38% drop in efficiency. The difference in the measured efficiency of the proposed converter and the converter presented in [16] is less as the two structures have the same number of components and the same boost factor. However, the voltage stress of the capacitors and

switches is the lowest for the proposed converter. Regarding the measured waveforms, at the full-load condition, the voltage stress of the capacitors is 150 V for the proposed converter and 198 V for the proposed structure in [16]. This demonstrates an improvement of around 25%, with almost better efficiency for the proposed converter.

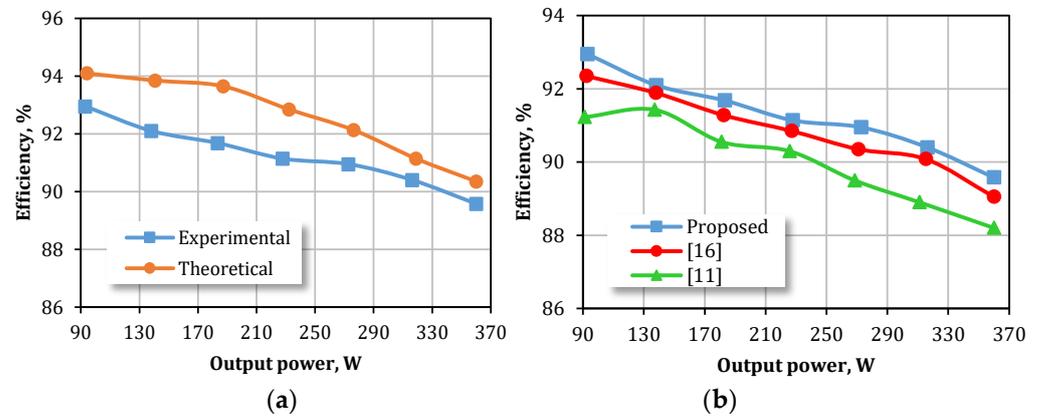


Figure 16. Comparison of efficiency: (a) measured and estimated efficiency of the proposed converter; (b) proposed converter and two reported converters in [11,16].

10. Conclusions

In this paper, an embedded topology for a half-bridge gamma-based Z-source inverter was proposed. The steady-state analysis of the proposed inverter at different operating modes was performed and design considerations have been given. The proposed converter features low voltage stress across the capacitors. In comparison with a conventional gamma-source half-bridge converter, the proposed converter improves the voltage stress of the capacitors by around 25%. The proposed half-bridge inverter could generate high voltage gain in comparison with half-bridge and full-bridge conventional Z-source inverters. Moreover, for the same boost factor, the proposed converter features a lower number of power switches than a conventional full bridge ZSI, which results in low switching losses. The estimated THD for an ST duty cycle of 0.2 equals 21.89%, which could be considered acceptable as the proposed converter features a higher boost factor than the conventional ZSI. The power loss analysis shows that the power switches dissipate the power more successfully than the other components, as around 70% of the power losses belong to the switches. Simulation results and experimental results were used to verify the given theoretical analysis. Based on the mentioned features, the proposed approach could be adopted for a full-bridge inverter. The proposed converter could be used as a grid-tied inverter to interface the dc sources to the grid; for this, it is necessary to design an output filter to filter the 50 or 60 Hz waveforms. Another application could be a front-end inverter for isolated dc-dc converters. The proposed concept can provide a boosted voltage to an isolated transformer operated at a high frequency. Depending on the boost factor of the converter, the transformer could be a step-up transformer or simply an isolated transformer.

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