Article

A Compensated Peak Current Mode Control PWM for Primary-Side Controlled Flyback Converters

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Abstract: In this paper, a feedback compensator (FBC) and a Feedforward compensator (FFC) are proposed to construct a novel compensated peak current mode control pulse width modulation (CPC-PWM) for primary-side controlled flyback converters. Using the proposed FBC, the PWM duty cycle of an abnormal operating flyback converter would be descended to limit the output current for reducing power dissipation. Using the proposed FFC, the effect of delay time would be descended to reduce the over-flow current for increasing the current accuracy. In this paper, the operating principle and mathematical model are described and analyzed. Then, the component values are well designed to satisfy the electrical specifications. Finally, a prototype is designed and realized to access system performance. The experimental results show that the proposed CPC-PWM can validate in a wide input voltage range and output short conditions, which also has good current accuracy and reduces power dissipation by about 68%.

Keywords: feedback compensator; feedforward compensator; flyback converter

1. Introduction

Because the flyback converter has a simple structure and does not require a secondary side output inductor, it has considerable advantages in size and cost. Based on the above advantages, the flyback converter is widely used in low power applications [1–16]—especially in LED lighting [8–10] and battery balancing control [11–16] to show its many advantages. With the advancement of digital technology and the cost of microcontrollers has dropped significantly. The control scheme of flyback is also moving towards digital control to obtain higher performance [17–20]. Since the flyback converter is an isolated converter, the output voltage and current are traditionally regulated by utilizing the secondary-side regulation (SSR). Usually, SSR is mainly constructed by a photocoupler. The photocoupler feedback circuit causes above 10% of the power losses at standby conditions. Recently, primary-side regulation (PSR) flyback converter (i.e., primary-side controlled flyback converter) becomes an important technology due to lower cost and standby power losses [1,17–25]. The primary-side controlled flyback converter stores energy on the transformer when the power switch is ON and releases the energy on the transformer to the load when the power switch is OFF. It is known that this topology is a constant power output. Based on the constant power output characteristics, when the output voltage of the flyback converter drops due to the load, the output current must increase. When the output voltage of the flyback converter keeps dropping, the current keeps increasing until the current is infinite, causing the problem of components burning. At the same output power, the higher input voltage results in a lower input current. On the contrary, the lower input voltage will result

in a higher input current. This means that different power losses are caused by different input voltages, so a larger rated component must be selected in the circuit design to meet the range under various conditions.

As shown in Figure 1, the conventional flyback converter has primary side peak current detection overcurrent protection. Because the primary-side peak current detection protection point voltage V_{LIMIT} is a fixed value, and the flyback converter working in Discontinuous Conduction Mode (DCM) has a constant power output as shown as [22]

$$P_O = \frac{1}{2} \cdot L_P \cdot f_{SW} \cdot I_P^2 \cdot \eta \tag{1}$$

where Lp, fsw, Ip and η are the primary side inductance, switching frequency, primary side peak current, and flyback conversion efficiency, respectively.
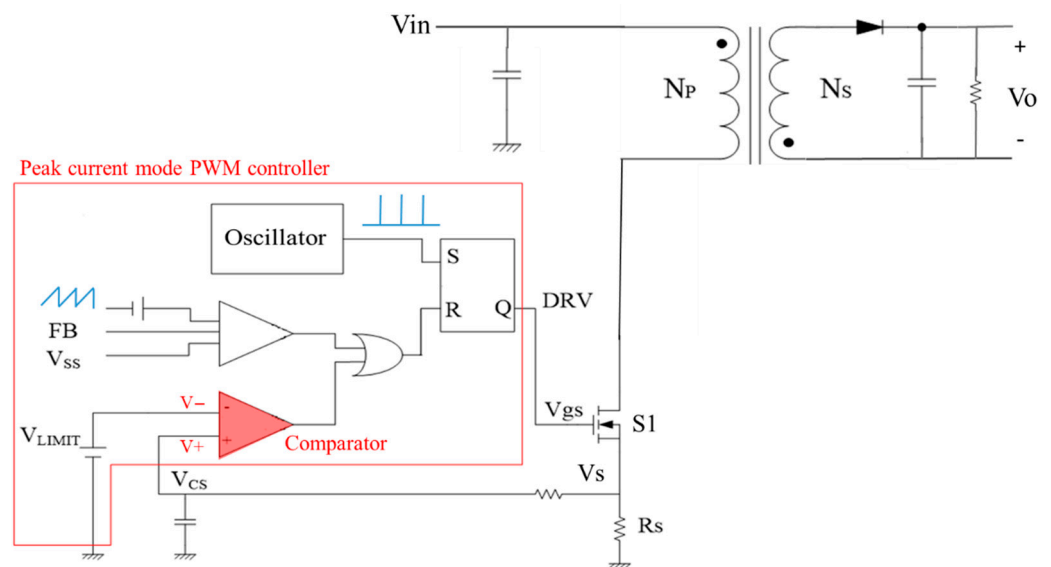

Figure 1. A typical flyback converter with primary side peak current mode control.

When the load on the output terminal becomes larger and larger, the output voltage becomes lower. At this time, the output current will still be larger and larger as shown in Equation (2). Therefore, the current rating of the part needs to be selected with a larger specification, just to meet the protection application.

$$I_O = \frac{1}{2} \cdot L_P \cdot f_{SW} \cdot I_P^2 \cdot \eta \cdot \frac{1}{V_O} \tag{2}$$

In order to overcome the above-mentioned problem, two methods were proposed and used in converters. In this first method, a current detection resistor R_{sense} is connected in series with the current loop at the output end to convert the current signal into a voltage signal. Then, use the comparison circuit or the current monitor IC to judge whether the overcurrent condition is reached. If the overcurrent condition is satisfied, turn off the synchronous rectification switch. Another method is to connect a current detection resistor R_{sense} in series with the ground current loop at the output end to convert the current signal into a voltage signal. Then, use the comparison circuit or the current detection IC to determine whether the overcurrent condition is occurring. If the condition is satisfied, the primary switch PWM duty is adjusted through the photocoupler control—to make the entire power supply achieve the functions of stability and overload protection. With these two methods, only a current detection resistor R_{sense} and comparison control circuit or current monitor IC are needed to achieve the purpose of current detection and protection. However, the current detection resistor R_{sense} is connected in series with the output main circuit. Because the current is large, in order to avoid excessive power loss, the current

detection resistor is usually very small. The current detection resistance R_{sense} is generally between several mΩ to tens of mΩ, depending on the output current. Therefore, the converted voltage signal is about tens of mV and hundreds of mV. The accuracy of such a small voltage signal is obviously insufficient for judgment and control. In addition, the power loss caused by the current detection resistor R_{sense} under heavy load is inevitable.

In a typical primary-side controlled flyback converter, a sensing resistor R_S is used to convert the current on the primary side into a voltage V_S and compares it with the reference voltage V_{LIMIT} of the controller. When the sensing voltage V_S is greater than the reference voltage V_{LIMIT}, the comparator is activated to turn off the power switch. Unfortunately, in actual applications, due to the stray capacitance inside the semiconductor device, a fixed logic drive delay is caused. When the input voltage is high, the current slope $m = \frac{V_{in}}{L_P}$ on the primary side becomes steeper. Due to the delay in the response time of the comparators, logic gates, and components, the power switch cannot be turned off immediately when the sensing voltage V_S is greater than V_{LIMIT}. As a result, the primary side current still maintains a fixed slope rise, and the overflow current ΔI_P occurs and can be shown as [22]

$$\Delta I_P = \frac{V_{in}}{L_P} \cdot t_{delay} \tag{3}$$

where t_{delay} is the delay time that is the amount delay times of the comparators, logic gates, and other components.

Figure 2 shows a schematic diagram of overflow current ΔI_P changes caused by signal delay under traditional peak current mode control. It can be seen that a higher input voltage V_{in} has a larger overflow current ΔI_P than a lower input voltage. This leads to a significant difference. When the input voltage is higher, the power that can be provided to the load is higher, and vice versa. This is one of the main reasons affecting line regulation of flyback converter.
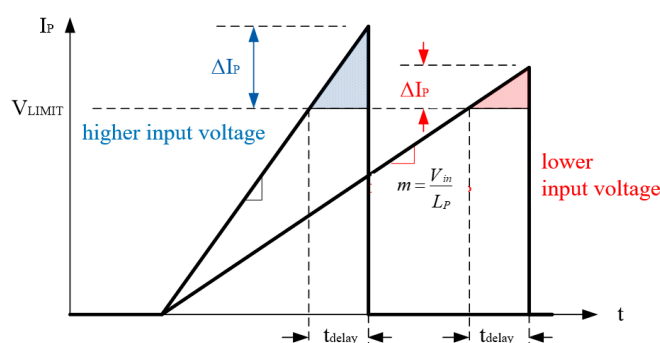

Figure 2. Overflow current with different input voltage.

In order to solve the above problem, many methods and techniques were proposed. The amount of overflow current ΔI_P can be estimated by using the change of current in the same t_{dealy} time. According to this estimated value to modify the PWM, the influence of t_{dealy} can be reduced [21]. Furthermore, the CS sample-and-hold circuit is used to measure primary side peak current I_p. Then, by calculating the average current, a compensation control method that is theoretically unaffected by t_{dealy} can be obtained [22]. Another method is to measure the mid-point current (i.e., average current) and use the average current control method, which can effectively reduce the influence of t_{dealy} and increase the accuracy of the output current [23–25]. Recently, digital technology is also used to directly measure t_{dealy}. Finally, t_{dealy} is compensated to obtain accurate output current [17,20].

Although the above methods can be used to reduce the impact of t_{dealy}. However, when an overload occurs and the output voltage is reduced, the output current cannot be suppressed. Therefore, the current rating of the components needs to be selected with a larger specification, just to meet the protection application. In order to solve this

problem, a Compensated Peak Current mode controlled PWM (CPC-PWM) for primary-side controlled flyback converters working in DCM is proposed in this paper. In the proposed CPC-PWM, the input voltage V_{in} is sensed and can be used to compensate for the control signal delay to reduce the overflow current ΔI_P to improve line regulation. In addition, the current limiting by voltage feedback scheme [26,27] is referenced. The output voltage V_{out} of flyback is sensed and be used to compensate PWM to suppress the overload current.

2. System Description

In order to suppress the output current I_o of the flyback converter during overload protection, the feedback compensator (FBC) is proposed in this paper. The inherent characteristics of the flyback converter output voltage V_{out} can be used to detect and adjust the PWM duty. Figure 3 shows the waveforms of a primary-side controlled flyback with FBC control working in DCM. As shown in Figure 3, when the output voltage V_{out} drops, the power switch duty cycle needs to be reduced to suppress the output current I_o. This means that the PWM duty cycle D_a during abnormal operation should be much smaller than the PWM duty cycle D_n during normal operation. The amount of this output voltage drop ΔV_{out} is the difference between the rated output voltage V^* and the output voltage V_{out}. Thus, the input voltage of the negative terminal of the comparator $V-$ will be compensated by the amount of this output voltage drop and written as:

$$V- = V_{LIMIT} - k \cdot \Delta V_{out} = V_{LIMIT} - k(V^* - V_{out}) \tag{4}$$

where k is a positive constant. A larger k means a smaller duty cycle D_a is obtained. Equation (4) can be rewritten as:

$$V- = k_1 \cdot V_{LIMIT} + k_2 \cdot V_{out} - k_3 \tag{5}$$

where k_1, k_2, and k_3 are positive constant. It can be seen from (5) that when the output voltage V_{out} drops more, the voltage $V-$ becomes smaller. This reduces the PWM duty cycle and achieves the purpose of suppressing the output current I_o.
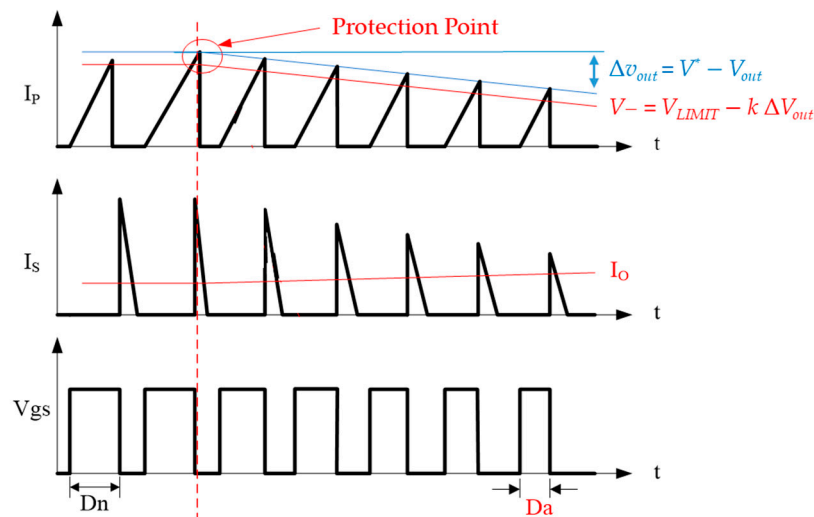

Figure 3. Waveform diagrams of a primary-side controlled flyback with FBC control working in DCM.

Figure 4 shows the theory expected V-I curves of a flyback with and without FBC. Comparing the V-I curves of the traditional method and the proposed method, the output current of the proposed method is much lower. It means that there is no need to choose a power component with a larger current rating. In this way, the power consumption

problem caused when the output load is increased or short-circuited can be suppressed, and the components with larger specifications can be avoided.
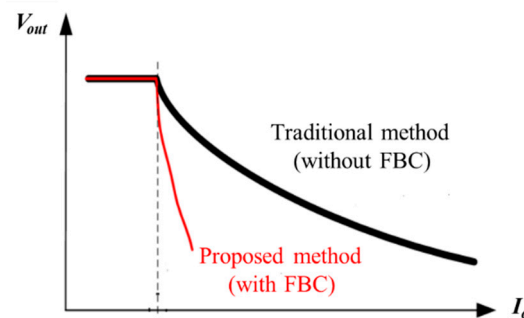

Figure 4. V-I curve of the traditional method and the proposed method.

In order to suppress the overflow current ΔI_P of the flyback converter, the FeedForward Compensator (FFC) is proposed in this paper. The input voltage V_{in} of the flyback converter is detected and used to adjust the PWM duty, since the overflow current ΔI_P is proportional to the input voltage V_{in} shown as (3). Figure 5 shows waveforms of a primary-side controlled flyback with FFC control working in DCM. As shown in Figure 5, the input voltage of the positive terminal $V+$ of the comparator is extract added by $k'V_{in}$ as written as:

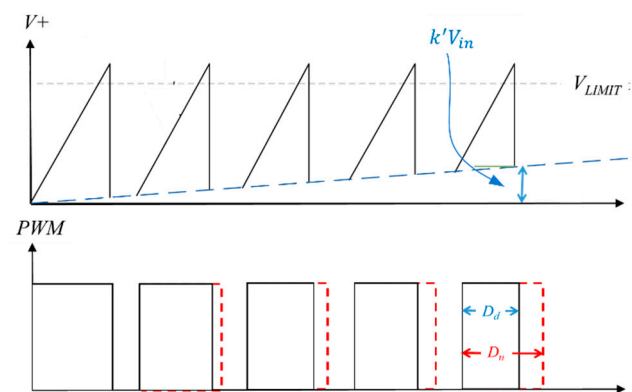$$V+ = V_S + k' \cdot V_{in} \tag{6}$$

Figure 5. Waveforms of a primary-side controlled flyback with FFC control working in DCM.

Equation (6) can be rewritten as:

$$V+ = k_4 \cdot V_S + k_5 \cdot V_{in} \tag{7}$$

where k_4 and k_5 are positive constant. It is clear that when the input voltage V_{in} increases, the voltage $V+$ becomes larger. When $V+$ becomes larger, the power switch $S1$ will be turned off early. When (8) is held, the overflow current ΔI_P caused by t_{delay} is eliminated.

$$\frac{k_5}{k_4} = \frac{t_{delay} \cdot R_S}{L_P} \tag{8}$$

Based on the above discussion, the block diagram of the proposed CPC-PWM controller mentioned in this paper can be drawn as Figure 6b. Compared with the traditional peak current mode control PWM shown in Figure 6a, we can see that the FBC is added, thereby achieving the purpose of suppressing the output protection current. On the other hand, the FFC is also added, thereby suppressing the purpose of the overflow current ΔI_P.
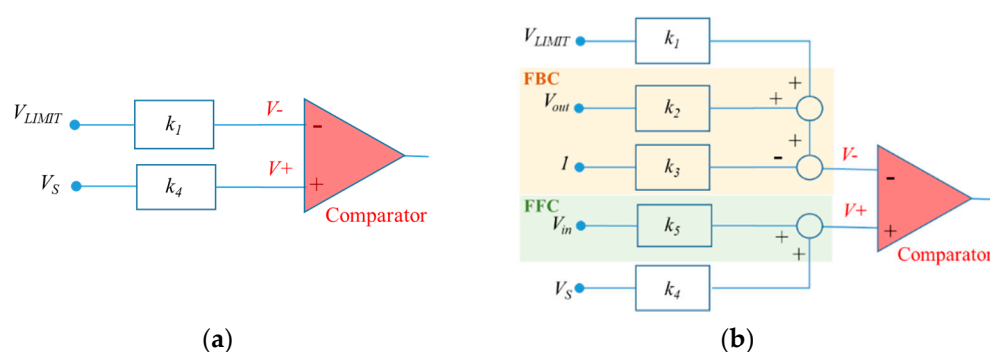
Figure 6. Control block diagrams of the traditional peak current mode control PWM (**a**) and the proposed CPC-PWM (**b**).

Design Example:

In order to verify the feasibility of the proposed CPC-PWM, a 5 W prototype is designed and realized. The specifications and circuit diagram of the prototype are listed and shown in Table 1 and Figure 7, respectively.

Table 1. Specifications of the realized prototype.

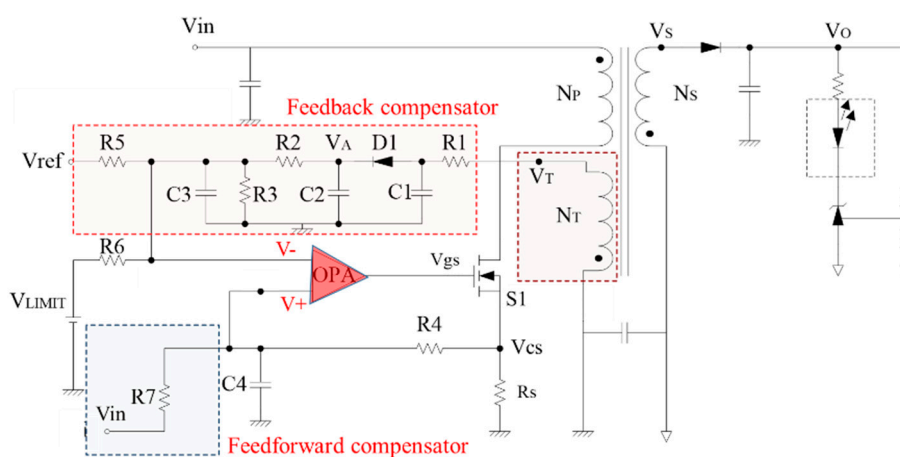| Specification	Value
Input voltage	17~34 V
Output voltage	5 V
Output current	1 A
Ripple voltage	30 mV
Output power	5 W
Overcurrent point	1.3 A $\pm$ 2%
Switching frequency	550 kHz

Figure 7. Circuit diagram of the proposed compensated peak current mode controlled PWM method.

The flyback converter proposed in this paper is mainly constructed by a transformer, an FBC, an FFB, and a power switch $S1$ as shown in Figure 7. The transformer includes a primary winding, a secondary winding, and an auxiliary winding or third winding. The output voltage of the third winding is injected into the feedback compensator circuit to adjust the PWM duty of the power switch. FBC is composed of a diode $D1$, four resistors $R1$, $R2$, $R3$, and $R5$, and three capacitors $C1$, $C2$, and $C3$, as shown as a red block in Figure 7. Due to the characteristics of the flyback converter, the energy is transferred to the secondary

side when the power switch is turned off. At the same time, the third winding is used to sample the output voltage condition to obtain the voltage V_T. Due to the transformer leakage inductance, there will be a spike voltage and the voltage V_A can be obtained only after being processed by a low-pass filter. A first-order RC filter is used and meet to (9) to filter out spike voltage

$$R1 \cdot C1 \geq t_{spike} \tag{9}$$

where t_{spike} is the period of the spike voltage.

The feedback compensator is a network circuit and can be simplified as Figure 8. The simplified circuit is composed of three voltage sources V_A, V_{ref}, and V_{LIMIT}, and four resistors $R2$, $R3$, $R5$, and $R6$. Voltage $V-$ can be obtained and shown as (10) by using KCL law. Compared with (5), parameters k_1, k_2, and k_3 can be obtained and shown as (11)–(13).

$$V- = \frac{V_{ref} \cdot G_5 + V_{LIMIT} \cdot G_6 + V_A \cdot G_3}{(G_5 + G_6 + G_3 + G_2)} \tag{10}$$

where G_X is the reciprocal of R_X, that is a conductance.

$$k_1 = \frac{G_6}{(G_5 + G_6 + G_3 + G_2)} \tag{11}$$

$$k_2 = -\frac{n_3 \cdot G_3}{n_2 \cdot (G_5 + G_6 + G_3 + G_2)} \tag{12}$$

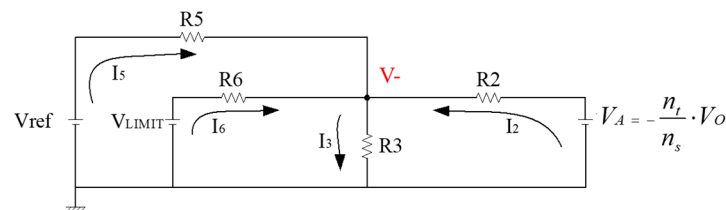$$k_3 = \frac{V_{ref} \cdot G_5}{(G_5 + G_6 + G_3 + G_2)} \tag{13}$$

Figure 8. Simplified FBC circuit.

The FFC is a network circuit composed of two voltage sources V_{in} and V_s, and two resistors $R4$ and $R7$. Voltage V+ can be obtained and shown as (14) by using KCL law. Compared with (7), parameters k_4 and k_5 can be obtained and shown as (15) and (16). In addition, the relation between resistor $R4$ and $R7$ is shown as (17).

$$V+ = \frac{V_{in} \cdot G_7 + V_S \cdot G_4}{(G_7 + G_4)} \tag{14}$$

where G_X is the reciprocal of R_X, that is a conductance.

$$k_4 = \frac{G_4}{(G_7 + G_4)} \tag{15}$$

$$k_5 = \frac{G_7}{(G_7 + G_4)} \tag{16}$$

$$R_7 = \frac{R_4 \cdot L_P}{t_{delay} \cdot R_S} - R_4 \tag{17}$$

The used components of the designed flyback converter as shown in Figure 7 are listed in Table 2.

Table 2. The used components and parameters in the design example.

Parts	Value	Parts/Parameters	Value
Resistor R1	1.1 KΩ	Capacitor C1	47 pF
Resistor R2	34 KΩ	Capacitor C2	470 pF
Resistor R3	2.43 KΩ	Capacitor C3	10 nF
Resistor R4	1 KΩ	Capacitor C4	33 pF
Resistor R5	73.2 KΩ	Volatge Vref	5.2 V
Resistor R6	100 KΩ	Volatge V_{LIMIT}	0.5 V
Resistor R7	290 KΩ	Volatge Vfault	0.385 V
Resistor RS	0.15 Ω		

3. Experimental Results

The feasibility and superiority of the proposed method are verified by discussing and comparing "overload current variation", "input power consumption during short circuit" and "overflow current variation".

Figure 9a–c shows the V-I curves obtained by using the traditional peak current control. Figure 9d–f shows the V-I curves obtained by using the proposed FBC method.

It can be seen from Figure 9a–c that the V-I curve has an obvious relationship with the input voltage V_{in}. When the input voltage V_{in} is higher, the overload point will also be higher. Figure 9d–f shows the V-I curves obtained using the proposed FBC method. It can be seen that when the input voltage V_{in} changes from 17 V to 34 V, there is no significant difference in the output current changes. It indicates that the proposed FBC method is significantly better than the traditional peak current control. From Figure 9d–f, we can also see that the output current during overload can be suppressed effectively by the proposed FBC as the theory predicted.

Figure 10a shows the comparison results of the measured overload point current using the traditional peak current control and the proposed FBC method. The variation rate of overload point current under different input voltages of the proposed FBC method is about 2% far better than the traditional 34.5%. In this design example, the traditional method requires at least a diode with a 1.7 A current stress. However, the proposed FBC method only needs a diode with 1.3 A current stress. Figure 10b shows the comparison results of the measured input power consumption using the traditional peak current control and the proposed FBC method under the output short circuit condition. Moreover, Figure 11b shows that the input power consumption of the proposed method under short-circuit protection is far superior to the traditional method. This means that there is no need to choose a power component with a larger current rating. In this way, the power consumption problem caused by the overload or short-circuited can be suppressed, and the components with larger specifications can be avoided.

Figure 11a–f shows the experimental waves under different input voltages of 17 V, 28 V, and 34 V when the flyback converter with/without FFC. In these figures, the positive terminal input voltage $V+$ of the comparator, the negative terminal input voltage $V-$ of the comparator, and the output voltage Vout waveforms of the flyback converter are shown. It can be seen from Figure 11a–c that without using FFC, the voltage $V-$ starts to climb from zero voltage under various input voltages. Until voltage $V-$ is greater than voltage $V+$, the power switch is turned off after the time t_{delay}. Observing the $V-$ waveform, it can be seen that the input voltage V_{in} is larger and the overflow current ΔI_P is larger. From Figure 11d–f, can be seen that an offset voltage is injected into $V-$, so that the overflow current ΔI_P is suppressed. The injected voltage is about 51 mV, 90 mV, and 105 mV when the input voltage is 17 V, 28 V, and 34 V, respectively. According to the experimental results, the proposed method is close to the expected theoretical result. The voltage injected by

different input voltages will also be different, which can reach the *V+* voltage early to achieve the purpose of effectively reducing the overflow current ΔI_P.
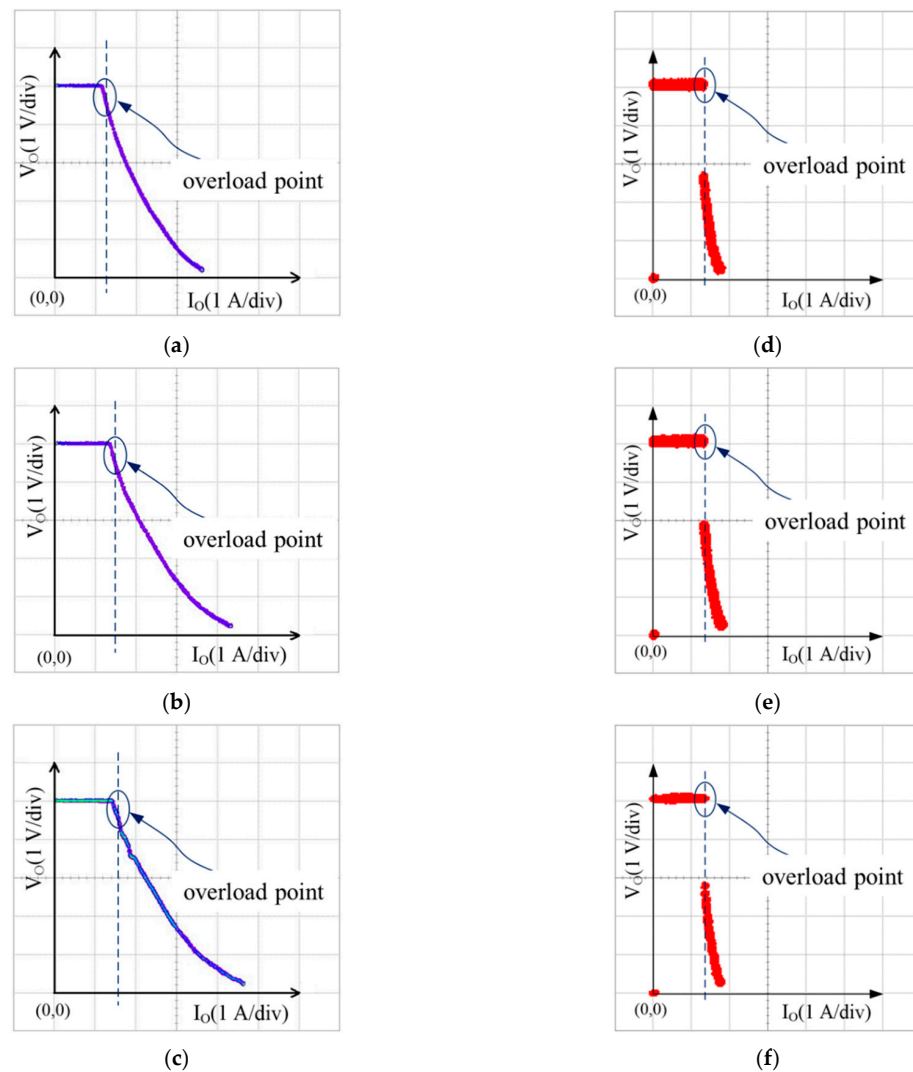

Figure 9. V-I curves obtained by using the traditional peak current detection circuit with input voltage (**a**) 17 V, (**b**) 18 V, and (**c**) 34 V, and by using the proposed FBC method with input voltage (**d**) 17 V, (**e**) 18 V, and (**f**) 34 V.
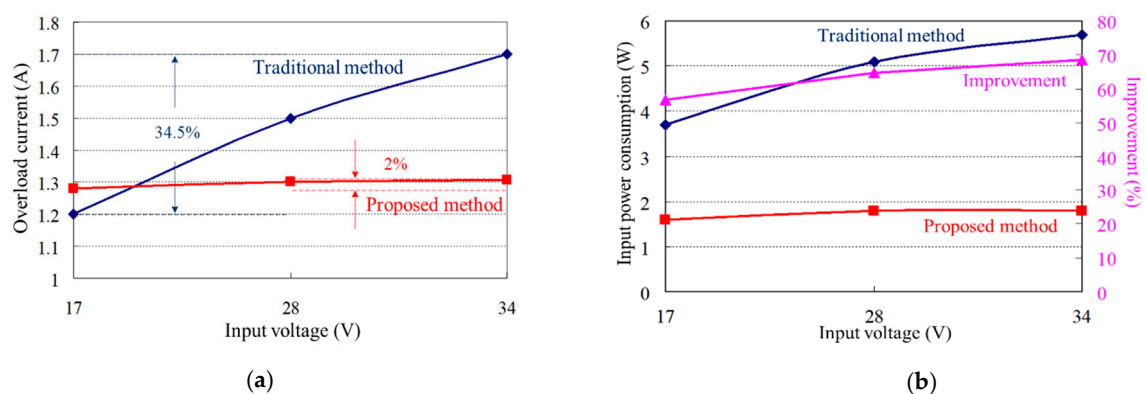

Figure 10. Experimental results (**a**) Overload current under different input voltage, (**b**) Input power consumption under different input voltage.
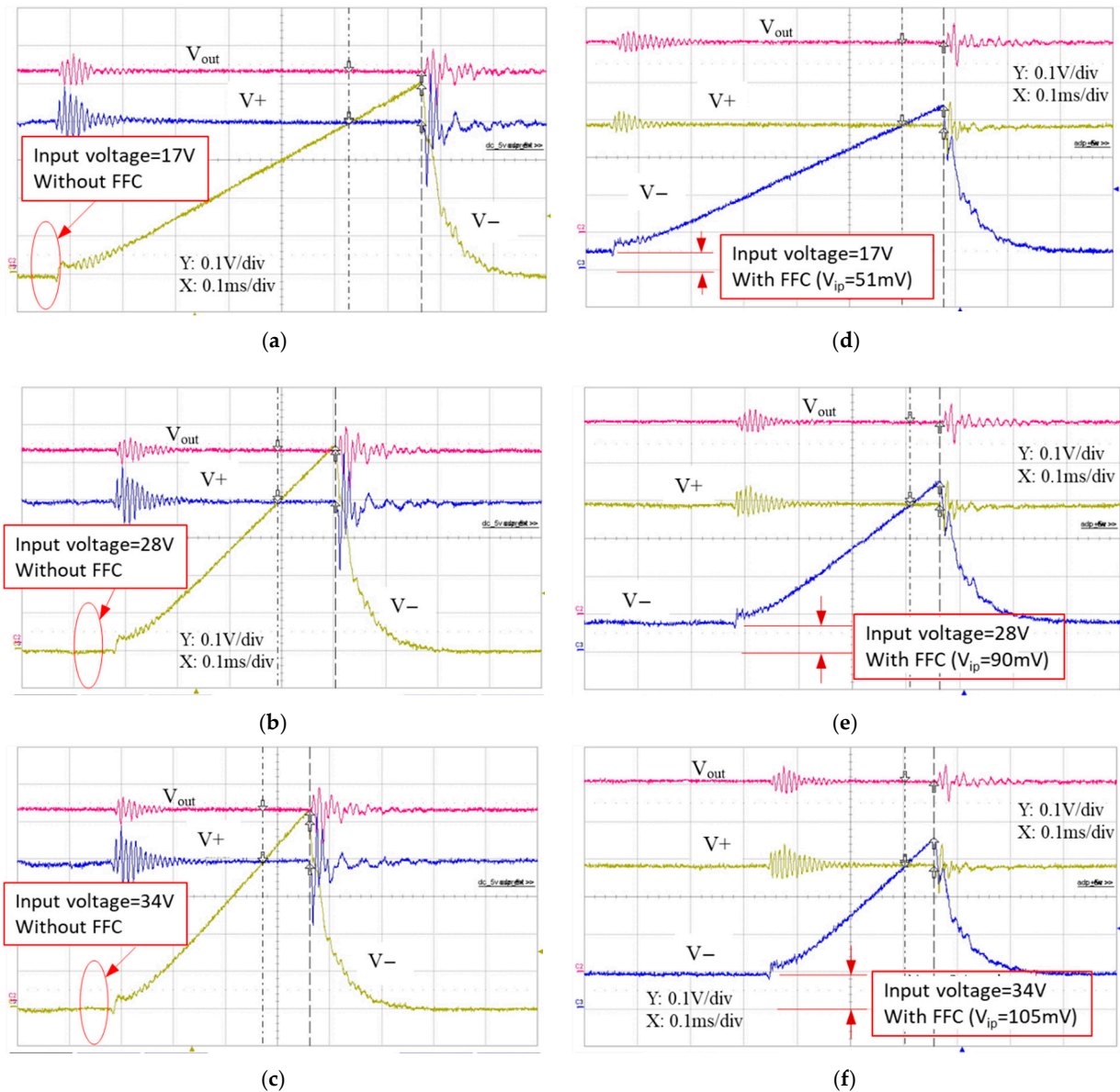
Figure 11. $V-$, $V+$, and Vout curves obtained by using the traditional peak current detection circuit with input voltage (**a**) 17 V, (**c**) 18 V, and (**e**) 34 V, and by using the proposed FFC with input voltage (**b**) 17 V, (**d**) 18 V, and (**f**) 34 V.

It is known that different voltage levels are required for different input voltages to be injected in the proposed FFC. From the experimental results, the accuracy of the V_{CS} is still not enough. If we can analyze the characteristics of the control IC, such as the t_{delay} time of different voltages, it will help the FFC to be more accurate. On the other hand, the circuits of the proposed CPC-PWM can be digitalized and simplified. For example, a small Micro-controller can be used to replace the proposed circuit, which will contribute to its simple structure, accuracy, and flexibility.

4. Conclusions

In this paper, a feedback compensator (FBC) and a feedforward compensator (FFC) were successfully proposed to construct a novel Compensated Peak Current mode control PWM (CPC-PWM) for primary-side controlled flyback converters. The relevant theories and methods proposed in this paper have been confirmed by circuit implementation. A 5 W prototype with a wide input range has been designed and realized to access system performance. Using the proposed FBC, the PWM duty of a flyback converter working in

overload can be descended to limit the current. The power consumption problem caused by the overload or short-circuited can be suppressed, and the components with larger specifications can be avoided. Using the proposed FFC, the effect of delay time can be descended to reduce the overflow current. The experimental results show that the proposed CPC-PWM can validate in a wide input voltage range and output short conditions, which also has good current accuracy and reduces power dissipation by about 68%.

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