

Article

A Study on the Distributed-Control Architecture of a DSP-Based Solid-State Transformer System with Implementation

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Abstract: This article proposes a Distributed-control Architecture (D-CA) and an operation sequence with start-up strategies for a Digital Signal Processor (DSP)-based Solid-State Transformer (SST). Although various control techniques for SSTs have been reported in earlier studies, there is still a lack of research covering comprehensive content, including hierarchical control architectures and operation sequences with start-ups considering the implementation of DSPs. Therefore, this article addresses the following factors of SST. First, the D-CA is described for the design of the hierarchy between control boards. With the D-CA, because sub-boards are in charge of their corresponding DC-link voltage balancing control individually, the computational burden on the master board can be reduced. Second, the operation sequence of the SST system is explained based on the SST with D-CA. The step of DC-link voltage balance is considered throughout the entire operation sequence for safe driving. Furthermore, the PWM start-up strategies for a Cascade H-bridge Multilevel (CHM) converter and Dual Active Bridge (DAB) converter are proposed to prevent switching pulse errors caused by DSP operating characteristics. These start-up strategies reduce the current surges. The validity of the proposed D-CA and operation sequence with start-up strategies are verified by experimental results.

Keywords: Solid-State Transformer (SST); Cascade H-bridge Multilevel (CHM) converter; Dual Active Bridge (DAB) converter; hierarchical control architecture; operation sequence; start-up strategy; Digital Signal Processor (DSP)



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1. Introduction

Recently, driven by environmental concerns and carbon dioxide regulations, industries are undergoing extensive electrification. The progress in high-capacity energy storage devices, such as batteries and supercapacitors, along with advancements in complementary technologies like sensing and lifespan prediction, is accelerating this trend [1,2].

Furthermore, powered by advancements in power semiconductor technology, traditional passive power conversion systems are being replaced by power semiconductor-based converters. Notably, among these advancements, the Solid-State Transformer (SST) stands out as a leading next-generation technology, positioned to replace conventional oil-immersed transformers. The SST has advantages, including voltage sag compensation, bidirectional power flow, and improved power quality [3–8]. Additionally, the system size and weight can be reduced compared to conventional transformers. Thanks to these advantages, the SST has found applications in diverse fields such as smart grids, transportation, and renewable energy sources [9,10].

Various SST topologies have been investigated in many studies [11]. Among the SST topologies, the system for generating DC output is applied to applications such as railways and microgrids. Moreover, the SST consisting of a Cascaded H-bridge Multilevel (CHM) converter and Dual Active Bridge (DAB) converters for the AC-DC and DC-DC

conversions, respectively, is used widely. This structure can control various output voltage levels and support bidirectional power transmission with galvanic isolation [12–14].

To configure an SST with CHM and DAB converters, proper control techniques are necessary at each power conversion stage. In a CHM converter, DC-link voltage control and grid-connected current control are performed, whereas a DAB converter is in charge of voltage control for DC output. Those control techniques for CHM and DAB converters were introduced in [15–17], individually.

In addition to the control techniques described above, assistive techniques were also reported, namely, DC-link balancing control, dead time compensation, and harmonic reduction. As voltage imbalances between DC-links of cells increase stress to the IGBTs and DC-link capacitors in a CHM converter, balancing control should be applied. DC-link balancing control can be conducted by either a CHM converter or a DAB converter. In [18], the CHM converter carries out DC-link balancing by individually adjusting the switching reference voltages of H-bridges. In contrast, in earlier work [19], another method using a DAB converter was introduced.

Modulation methods for CHM and DAB converters were also studied. The modulation methods for the CHM converter are classified into Level-Shifted Pulse-Width Modulation (LS-PWM) [20,21] and Phase-Shifted Pulse-Width Modulation (PS-PWM) [21–23]. In PS-PWM, the output voltage level for each cell is constant. In addition, losses are equally distributed for all cells, avoiding biased large losses to particular switches. DAB converter modulations were reported in [24,25]. Ref. [24] described the conventional PS-PWM controlled by the phase difference between the primary and secondary voltages, and [25] presented a hybrid modulation through the feedback-linearized controller.

The above studies dealt with the control techniques of CHM and DAB converters individually, which means that a discussion of the system operation of the SST was needed. Accordingly, a description of the overall system operation was reported in [26–31]. A comparative summary of the overall reference is available in Table 1. Refs. [26,27] presented the overall control sequence. However, the control architectures and operation sequences, which are important for the actual implementation, were not presented in detail. In particular, Ref. [26] only discussed the initial charging technique of the capacitors to protect against short-circuit accidents at the start of control. To mitigate switching pulse errors, a start-up strategy is additionally required to mitigate switching pulse errors.

Table 1. Differences between conventional methods and this article.

References	Introduction of Overall Control Sequence	Communication Structure Description	Control Hierarchical Architecture Description
[26]	Presence	None	None
[27]	Presence	None	None
[28]	None	None	Presence
[29]	None	None	Presence
[30]	Presence	None	Presence
[31]	Presence	None	Partially presence (without a balancing control)

Unlike [26,27], Ref. [28] presents a control hierarchical architecture. While Ref. [28] presents an appropriate architecture based on various SST topologies, it does not include control sequences and communication structure. Similarly, Ref. [29] shows a control hierarchical architecture. The control process of [27] is presented in detail compared to [28]. However, Ref. [29] also required an explanation of the communication structure and the control sequence. Refs. [30,31] proposed the entire operation sequence and the control hierarchical architecture. Especially, Ref. [31] indicated the output waveforms of the control sequence, but the DC-link voltage balancing control was omitted. Furthermore, data

transmission relations between control boards within the suggested control architecture were not specified in [30,31]. In other words, the controls of SST, including communication transmission between cells, are not fully organized.

As described above, although various studies on the SST have existed, there is a lack of articles covering comprehensive content, including hierarchical control architectures and operation sequences with start-up strategies considering the implementation of DSPs. Therefore, we address the following factors of SST systems based on a laboratory prototype. First, a hierarchical control architecture, the Distributed-control Architecture (D-CA), for the design of a DSP-based SST system is proposed. Unlike earlier studies where a master board is fully in charge of the entire control and sub-boards on cells exist just for PWM switching, in the D-CA, sub-boards have a dedicated DC-link voltage balancing controller individually for their corresponding cells. With this strategy, the computational burden on a master board can be reduced. Considering DSP environments, detailed figures with data transfer of communication between a master board and sub-boards are illustrated. Second, based on the designed SST with D-CA, the entire operation sequence of the SST system is described. A step of DC-link voltage balance is considered throughout the entire operation sequence for safe driving. Furthermore, the start-up strategy of CHM and DAB converters is explained, especially focusing on the aspect of the DSP. The strategies deal with the switching pulse errors associated with DSP characteristics in order to prevent a current surge.

The rest of this article is organized as follows. Section 2 explains the system configuration and control techniques of the SST. Section 3 suggests the D-CA with descriptions of DSP operation in the time domain. In Section 4, the entire operation sequence of the SST is described with start-up strategies for the CHM and DAB converters. Section 5 presents the experimental results to prove the validity of this proposal. Finally, Section 6 concludes this article.

2. SST System Configuration

In this article, all descriptions are based on the designed single-phase SST shown in Figure 1. This section explains the overall system configuration seen in the figure. The SST system consists of the 3-cell CHM converter in Figure 1a and DAB converters in Figure 1b. The CHM converter is connected to a single-phase grid (v_g), through an AC filter inductor (L). Each H-bridge of the CHM converter is connected to each DAB converter, and the DAB converters are in parallel for the generation of output voltage (v_{out}). This structure is called Input Series Output Parallel (ISOP). In front of the CHM converter, there is a pre-charge circuit to prevent inrush currents in DC-link capacitors.

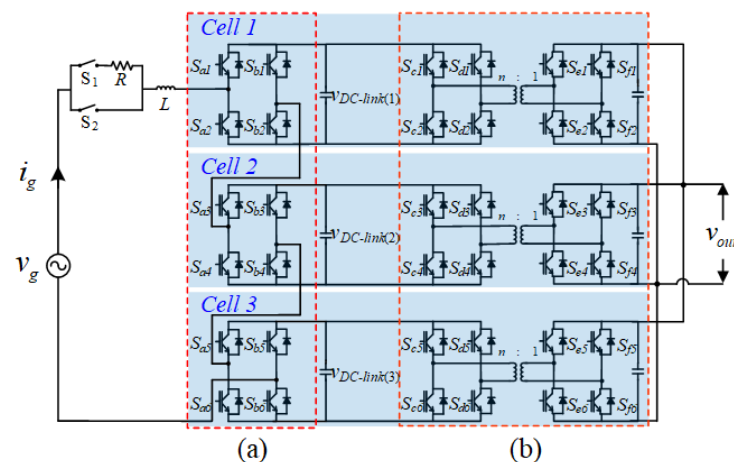


Figure 1. Topology configuration of 3-cell SST. (a) CHM converter; (b) DAB converter.

In Figure 1a, the CHM converter stacks the output voltages of each cell by connecting H-bridge converters in series. The maximum available level (m) of an output voltage of the CHM converter (v_{CHM}) is calculated as

$$m = 2H + 1 \quad (1)$$

where H is the number of H-bridge converters connected in series. As this article is described based on a three-cell topology, output voltages can be generated for up to seven levels. The output voltage level is fixed by a Modulation Index (MI), and if the MI is bigger than 0.67, a seven-level voltage is formed. The MI formula is given as

$$MI = \frac{V_g \times \sqrt{2}}{V_{dc-link(total)}} \quad (2)$$

In (2), $V_{dc-link(total)}$ means the sum of the DC-link voltage of the cells.

The DAB converter is an isolated DC-DC converter, which steps down DC-link voltage to output voltage. The DAB converter can transfer power bi-directionally and has the advantages of providing relatively low voltage stress and a low passive component rating [32]. In Figure 1b, the DAB converter is composed of H-bridge converters with a medium frequency transformer (MFTR). Input capacitors correspond to DC-link capacitors, and output capacitors are in a parallel configuration.

3. Design of D-CA for SST

This section describes the control architecture designed for the operation of the SST system in Figure 1 with a DSP. For practical fulfillment, control techniques of voltages and currents and the communication protocol with data transfer are illustrated.

3.1. Control Technique of CHM and DAB Converters

In this subsection, before describing the hierarchical control architecture of the SST, we describe the individual techniques for voltage and current controls. The control techniques are classified according to power conversion stages (i.e., CHM or DAB converter). Figures 2 and 3 depict controllers of the CHM and DAB converters, respectively.

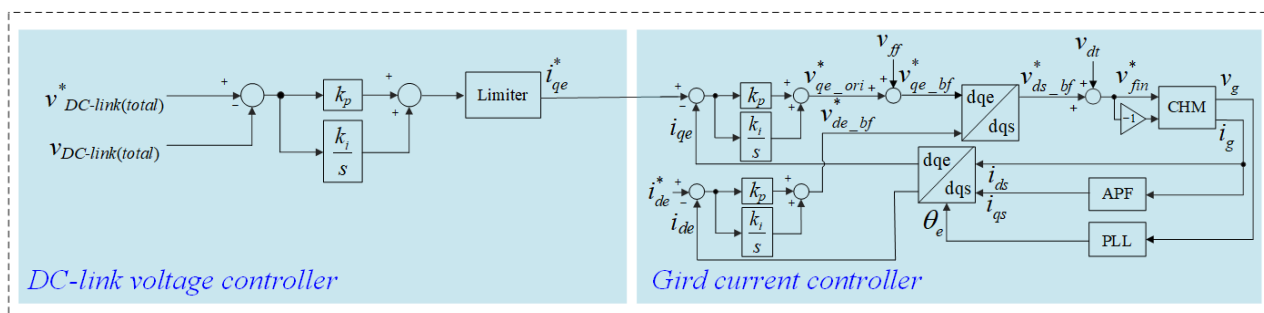


Figure 2. Control block diagram of CHM.

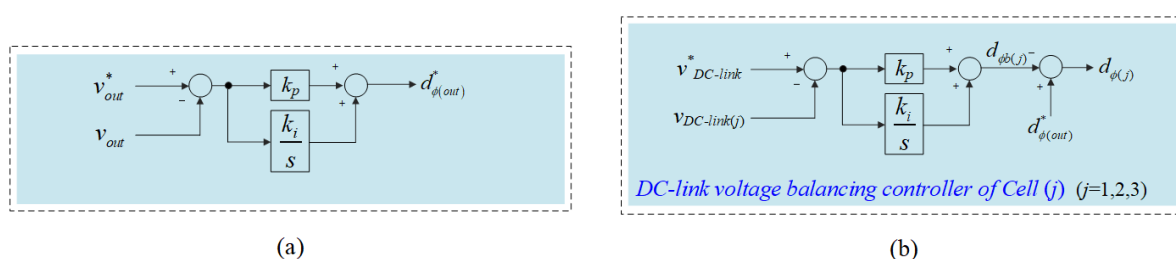


Figure 3. Control block diagram of DAB. (a) Output voltage controller; (b) DC-link voltage balancing controller.

Figure 2 is composed of a DC-link voltage controller and a grid current controller, which are the outer and inner controllers, respectively. The DC-link voltage controller operates prior to the grid current controller in order to generate the active grid current reference (i_{qe}^*) that is responsible for charging and discharging of DC-link capacitors. This process is realized by eliminating the error between the DC-link voltage reference ($v_{dc-link(total)}^*$) and $v_{dc-link(total)}$ using a Proportional-Integral (PI) controller. After the DC-link voltage control, the grid current control is conducted by PI controllers to control dq-axis currents in the synchronous reference frame (i_{dqe}), resulting in $v_{dqe_{bf}}^*$. Throughout the current control, it should be noted that the d-axis current (i_{de}) remains at zero for the unity power factor control. Subsequently, the feedforward component for grid voltage (v_{ff}) is added to $v_{qe_{bf}}^*$. The phase angle (θ_e) of the grid voltage given by the Phase-Locked Loop (PLL) using an All-Pass Filter (APF) is used to transform $v_{dqe_{bf}}^*$ to $v_{dq_{sbf}}^*$ in a reverse manner. After that, dead time compensation (v_{dt}) is added; a switching reference voltage of CHM converter (v_{fin}^*) for PS-PWM is derived. The phase shift angle (ϕ_{cr}) for the PS-PWM is calculated as

$$\phi_{cr} = \left(\frac{180}{m-1} \right)^\circ. \quad (3)$$

Therefore, based on (1) and (3), ϕ_{cr} between carriers of each cell is given as 60° in this article.

Regarding the DAB converter, the phase shift angles for PS-PWM ($d_{\phi(j)}$) are derived. The power transfer equation of the DAB converter in relation to $d_{\phi(j)}$ is expressed as

$$P = \frac{nv_{dc-link(j)}v_{out}}{2Lf_s}d_{\phi(j)}(1-d_{\phi(j)}), \quad (4)$$

where n and f_s represent a winding ratio and switching frequency, respectively. To obtain $d_{\phi(j)}$, controls are conducted by being distinguished as an output voltage controller and DC-link balancing controllers as shown in Figure 3a,b, respectively. The output voltage controller consists of a PI controller for eliminating the error between v_{out} and its reference value (v_{out}^*), with the result that $d_{\phi(out)}^*$ is generated. The DC-link balancing controller's control $v_{dc-link(1)}$ to $v_{dc-link(3)}$ to track their nominal value $v_{dc-link}^*$, forming $d_{\phi b(j)}$. Subsequently, $d_{\phi(j)}$ is calculated by subtracting $d_{\phi b(j)}$ from $d_{\phi(out)}^*$.

3.2. Distributed-Control Architecture (D-CA)

Figure 4 shows the design of the hierarchical control architecture for implementing the control techniques to the SST system configuration of Figure 1. The proposed control architecture physically has four control boards, classified into three sub-boards distributed to respective cells (Sub 1 to Sub 3) and one master board. Between the control boards, a communication line through the Controller Area Network (CAN) for data transfer and an optical fiber for synchronization is also depicted.

The master board carries out overall system controls for the generation of v_{out} , such as PLL, DC-link voltage control, grid current control, and output voltage control of the DAB converter. For these controls, actual values for v_g , i_g , and v_{out} are directly obtained through the Analog-to-Digital Converter (ADC), whereas $v_{dc-link(1)}$ to $v_{dc-link(3)}$ is received from sub-boards through the CAN. Upon finishing the entire control, the master board transmits reference values v_{fin}^* and $d_{\phi(out)}^*$ with a cell address to the sub-boards. Here, the cell address is assigned integer values according to the cell number, which is explained later in the next figure.

The sub-boards are mainly in charge of the PS-PWM for its corresponding cell, as depicted in Figure 4. However, it should be noted that the DC-link voltage balancing control is also conducted. This structure is denoted as a hierarchical control architecture with distributed control (D-CA) in this article. General control architectures where controllers are all arranged in a master board suffer from a high computational burden because the

number of DC-link voltage balancing controllers increases with the increment of cells. In contrast, the D-CA can achieve a low computational burden on the master board regardless of the number of cells due to the distribution of those controllers. Due to this mechanism, $v_{dc-link(1)}$ to $v_{dc-link(3)}$ is acquired in their corresponding sub-boards.

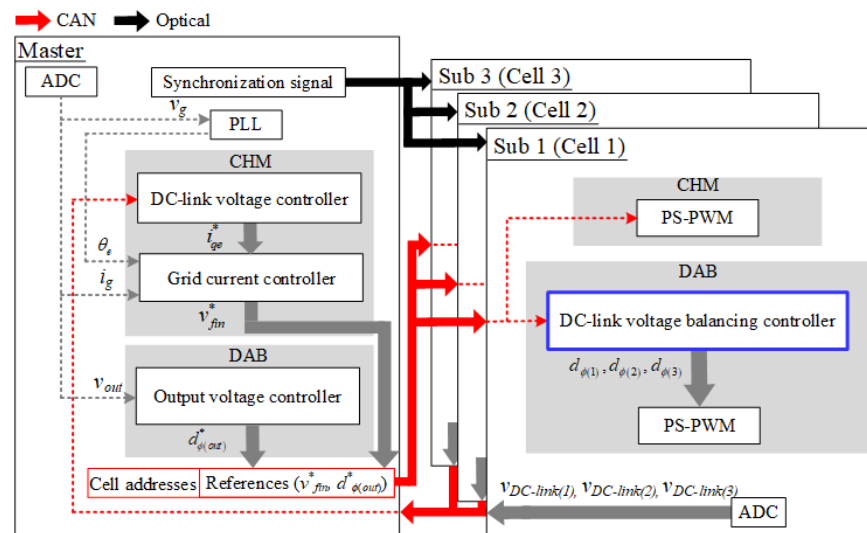


Figure 4. The disposition of controllers and data transfer of communication in D-CA.

Figure 5 shows the operation of the D-CA with respect to the aspect of the DSP in the time domain. In the figure, the control computation times, EPWM interrupt, synchronization signal (Syn_{fb}), CAN message, and triangular carriers of the CHM and DAB converters are indicated. The EPWM interrupts of the sub-boards are synchronized by Syn_{fb} generated every three cycles of the EPWM interrupt of the master board. As all controls operate every EPWM interrupt, a control period (T_{ctrl}) is identical to the interval between the present and the next EPWM interrupt. In this article, the carrier periods of the CHM and DAB (T_{CHM} , T_{DAB}) converters are set to three times and a half of the control period, respectively.

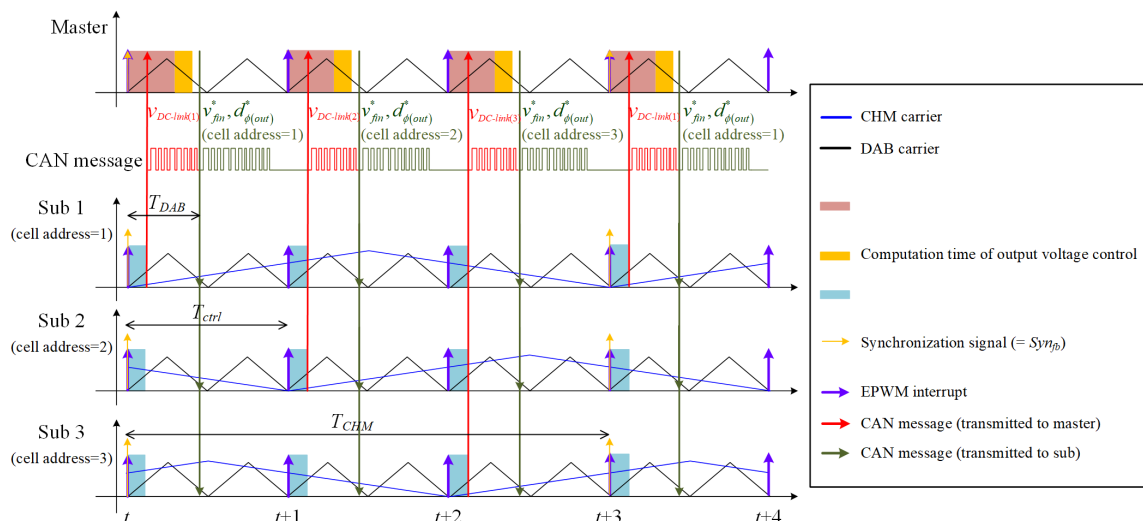


Figure 5. The operation of D-CA in the time domain with respect to DSP, including carriers, signals, computation time, and communications.

As shown in Figure 5, data transfer through the CAN between control boards starts after the controls end. One can note that data from the master board (i.e., the cell address, v_{fin}^* , and $d_{\phi(out)}^*$) are transmitted every T_{ctrl} , whereas data from the sub-boards (i.e., $v_{DC-link(j)}$)

are sent every three cycles of T_{ctrl} alternately. The sub-boards receive a cell address, which changes from one to three every control period; thus, only one cell with the same address requested by the master board sends $v_{DC-link(j)}$ to the master board. For instance, Sub 2 transmits $v_{DC-link(2)}$ at $t + 2$ because the cell address at $t + 1$ is two. This is due to the consideration of communication speed when one CAN bus is used. As the DC-link voltage controller does not require a relatively high dynamic response, this strategy is reasonable.

4. Operation Sequence with Start-Up Strategies

In this section, first, we explain the entire operation sequence for the designed SST based on D-CA for seamless and safe driving. Second, we describe the specific strategy of the start-up operation considering DSP implementation in order to prevent current surges from deteriorating the stability of the SST system. The start-up strategy described aims to eliminate switching pulse errors that are generated at the PWM operation immediately after the start of control.

4.1. Operation Sequence

The entire operation sequence of SST is explained based on Figure 6, which shows sequential output waveforms. Operation points are distinguished by the number denoted in Figure 6 (i.e., (i) to (vi)).

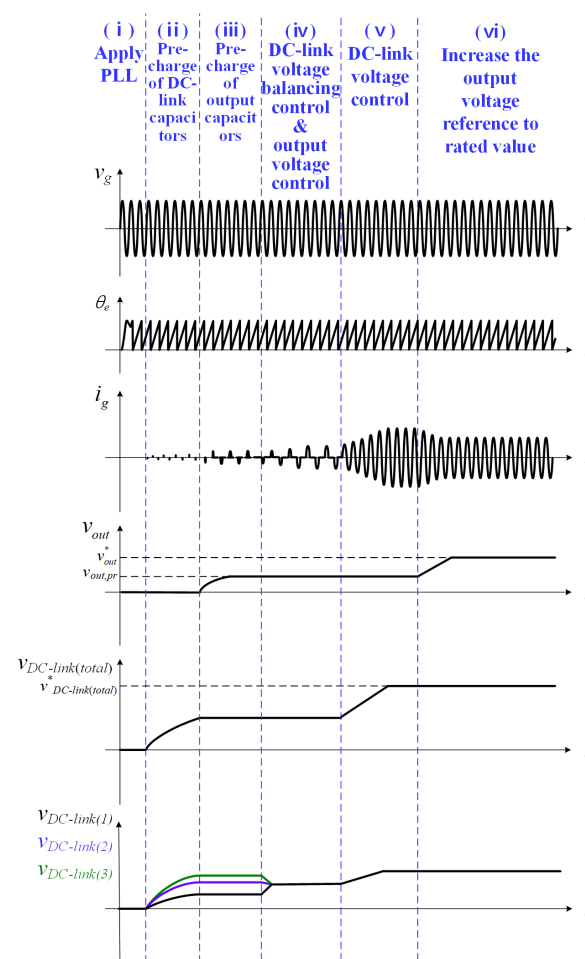


Figure 6. Waveforms of the operation sequence of designed SST based on D-CA.

In (i), the PLL is operated to estimate θ_e . Next, the pre-charge of the DC-link and output capacitors are sequentially executed in (ii) and (iii), respectively, in order to prevent capacitor failure. For the DC-link capacitors, the pre-charge circuit is given as shown in Figure 1. Switch S_1 is turned on to attach the pre-charge resistor R until the DC-link voltage

reaches a steady state. After that, S_2 is turned on to connect the CHM converter to the grid, but S_1 is detached. It can be seen that $v_{DC-link(j)}$ and $v_{DC-link(total)}$ are slowly charged in (ii) in Figure 6.

Regarding output capacitors, the pre-charge is conducted by the PWM technique without an extra pre-charge circuit. In this case, PWM with a small duty cycle is imposed on the primary side of the DAB converter; however, the PWM of the secondary side remains in an off-state; thus, v_{out} is charged slowly up to the pre-charged values ($v_{out,pr}$) determined by a turn ratio of the MFTR, as depicted in (iii) in Figure 6. A detailed explanation is given in Section 4.3.

Once the pre-charge operations in (ii) and (iii) are completed, the balancing control and output voltage control are executed in (iv). It should be noted that $v_{DC-link(j)}$ is in an unbalanced condition as shown in (ii) and (iii) due to the possibility of slight capacitance differences. This implies that DC-link voltage balancing controls should be implemented prior to the DC-link voltage control of the CHM converter in order to prevent damage to the DC-link capacitors and power semiconductors. Therefore, in (iv), it can be seen that $v_{DC-link(j)}$ becomes balanced. Regarding v_{out} , it is controlled to $v_{out,pr}$.

Subsequently, in (v), the DC-link voltage control of the CHM converter is performed and $v_{DC-link(total)}$ increases to the rated value via a ramped increase. Here, as the DC-link voltage balancing is already in operation, $v_{DC-link(j)}$ values remain the same as each other even in a transient state. Finally, in (vi), v_{out}^* increases to generate a rated DC output voltage.

4.2. Start-Up Strategy of CHM Converter

Figure 7 shows a PS-PWM of the CHM converter when (v) starts. In the figure, the start-up signal determines the start of the switching pulse output, and the point where the start-up signal becomes one is called the start-up point. At the start-up point, v_{fin}^* is calculated by grid current control. v_{fin}^* is compared to the CHM converter carriers ($Carr_{CHM}$ s) of each cell to the output PWM. The PWMs of S_{a1} , S_{a3} , and S_{a5} , which are the upper left switches for each cell, are representatively depicted.

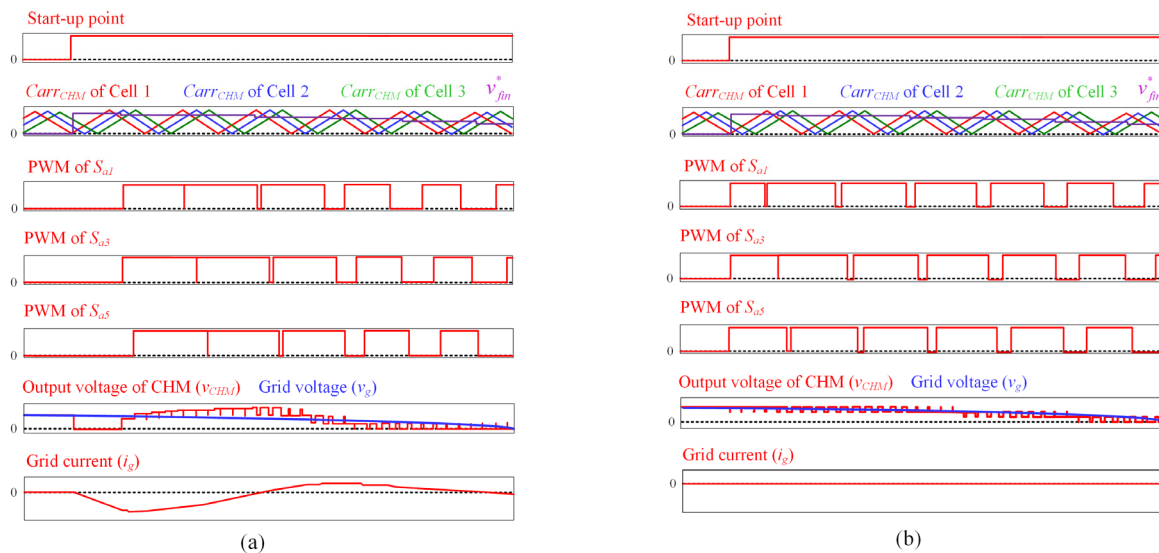


Figure 7. Omission of switching pulses in CHM with and without the applied start-up strategy. (a) Without the start-up strategy; (b) with the start-up strategy.

The PWM is implemented when v_{fin}^* and $Carr_{CHM}$ meet. According to the setting of the DSP, if the slope of $Carr_{CHM}$ is positive and equal to v_{fin}^* , a high state is derived (PWM = 1). In contrast, if the slope is negative, the PWM is converted to a low state (PWM = 0). Figure 7a,b confirm that the PWMs are output depending on the previously mentioned DSP settings.

Since the default of the PWM ($SW_{default}$) is set to low, several PWMs, which should begin at a high state, cause an error. For example, all cells must begin PWM at a high state because v_{fin}^* has a value greater than 0.66 in Figure 7a. However, since $SW_{default}$ is at a low state, PWM remains at a low state until v_{fin}^* and the negative slope of $Carr_{CHM}$ become equal. Therefore, the PWM of S_{a1} , S_{a3} , and S_{a5} does not initiate at a high state. This PWM error is referred to as a pulse omission. The pulse omission leads to an error in the DC-link voltage control and results in a surge of i_g .

To address the pulse omission in some PWMs, in this article, a start-up strategy with a $SW_{default}$ setting is given. The start-up strategy compares the magnitude of v_{fin}^* with the size of $Carr_{CHM}$ at the start-up point. If v_{fin}^* is larger than $Carr_{CHM}$, $SW_{default}$ is set to a high state to create a pulse at the start-up point. Based on the 3-cell SST, the $SW_{default}$ setting is given as

Cell 1 : $SW_{default} = \text{high}$

$$\text{Cell 2 : } \begin{cases} SW_{default} = \text{low} & (v_{fin}^* < 0.33) \\ SW_{default} = \text{high} & (v_{fin}^* > 0.33) \end{cases} \quad (5)$$

$$\text{Cell 3 : } \begin{cases} SW_{default} = \text{low} & (v_{fin}^* < 0.66) \\ SW_{default} = \text{high} & (v_{fin}^* > 0.66) \end{cases}$$

With (5), the pulse omission can be solved as shown in Figure 7b. It can be seen that switching pulses appear without omission, with the result that a surge of i_g decreases compared to that of Figure 7a.

4.3. Start-Up Strategy of DAB Converter

Figure 8 shows the waveforms of the DAB converter start-up. At the transition point where the switching signal becomes one, the operation sequence changes from (iii) to (iv), shown in Figure 6. In Figure 8, v_{pri} and v_{sec} refer to the primary and secondary voltages of the MFTR, respectively. i_{pri} and i_{sec} indicate the primary and secondary currents of the MFTR, respectively. The DAB carrier is $Carr_{DAB}$, and $v_{sw,DAB}$ means a switching reference of the DAB converter. In this article, a small duty cycle for the pre-charge of output capacitors is set to 0.05, as depicted in the PWM waveforms at the bottom of Figure 8.

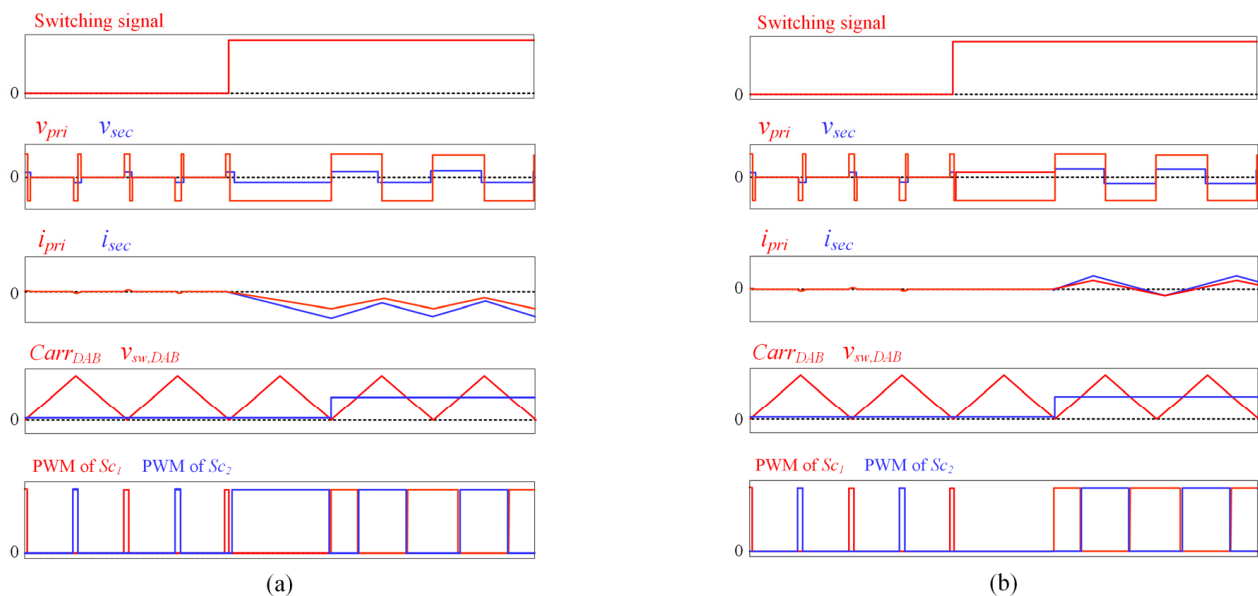


Figure 8. Difference between i_{pri} and i_{sec} in DAB with and without the applied start-up strategy. (a) Without the start-up strategy; (b) with the start-up strategy.

In Figure 8a, $v_{sw,DAB}$ is 0.5 after T_{DAB} from the transition point. This delay is caused by a shadow register of DSPs, and Figure 9 depicts this phenomenon in detail. In the shadow register, the $v_{sw,DAB}$ is applied to the PWM by reflecting the past $v_{sw,DAB}$ at each zero of $Carr_{DAB}$. Consequentially, when the point (k) is the transition point, it can be seen that $0.5 v_{sw,DAB}$ comes out from the point $(k + 1)$. While it is possible to prevent the omission of pulses by $v_{sw,DAB}$ or $Carr_{DAB}$, which change at any point, it causes the wrong PWM from (k) to $(k + 1)$.

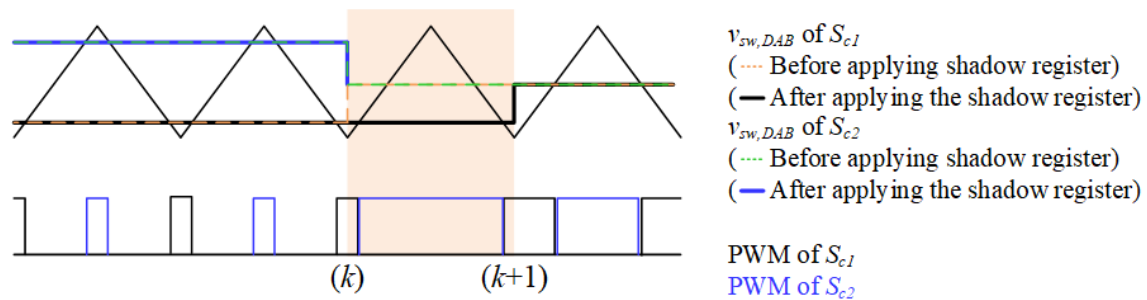


Figure 9. The PWM error caused by the delay from the shadow register.

If the wrong PWM is applied to the DAB converter because the PWM exceeds 0.5, the i_{pri} and i_{sec} lean to one polarity and increase as if with a DC offset. Therefore, all PWMs should be set to a low state for one cycle of T_{DAB} after the transition point to eliminate the wrong PWM, as illustrated in Figure 8b. This low setting of PWM is referred to as a start-up strategy of the DAB converter. It can be confirmed that 0.5 duty is output after the transition point. As a result, i_{pri} and i_{sec} can be zero on average without a DC offset.

5. Experimental Results

We conducted an experiment to prove the validity of the designed SST with D-CA and the proposed operation sequence considering the DSP implementation. The experimental setup shown in Figure 10 has the same system configuration as Figure 1 and the parameters applied are denoted in Table 2. The master board and sub-boards consisted of DSPs named TMS320F28377D.

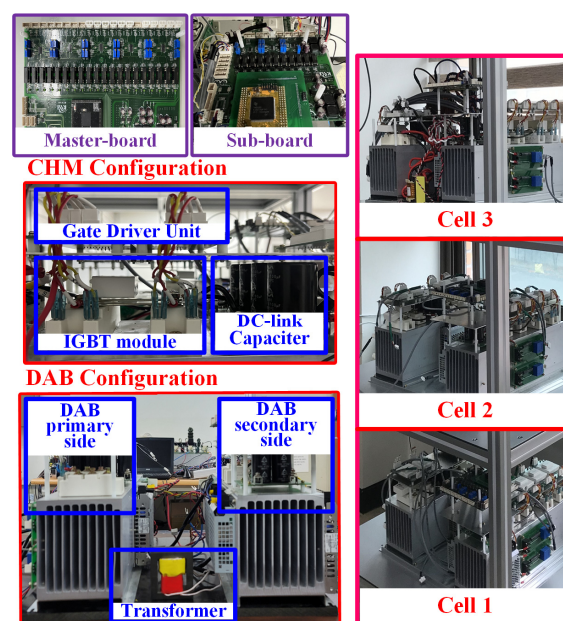


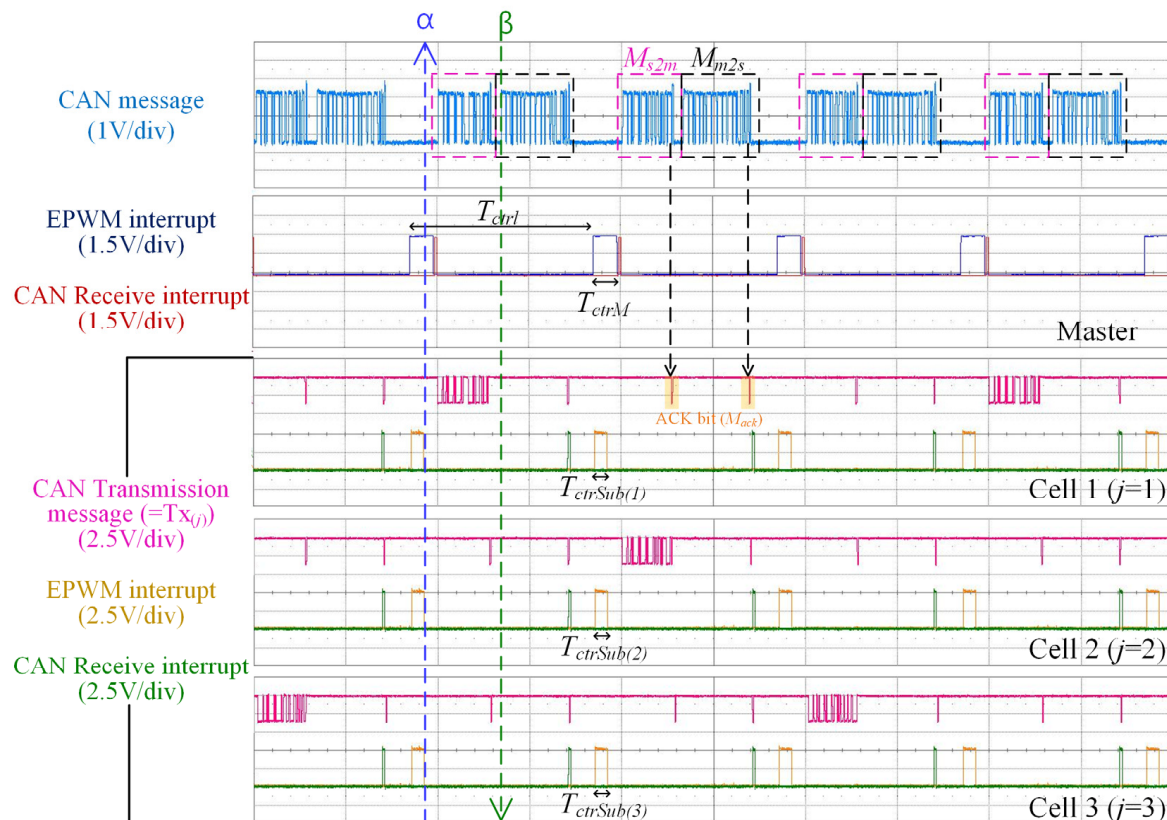
Figure 10. Experimental setup.

Table 2. Experiment parameters.

Parameter	Value
Rated power of SST	2.56 kW
Input grid voltage	220 V _{rms} , 60 Hz
DC-link voltage of CHM	390 Vdc
Output voltage of DAB	80 Vdc
Input AC filter inductor	1.9 mH
Capacitance of 1 cell DC-link	1175 μ F
Capacitance of DAB converter	2350 μ F
Switching frequency of CHM	1.67 kHz
Switching frequency of DAB	10 kHz
Control frequency	5 kHz
Turn ratio of MFTR	1.5:1
Rated output voltage	80 V

5.1. The Verification of D-CA

As illustrated in Figure 4, the D-CA with one CAN bus at 1Mbps speed was constructed in the experimental setup. Figure 11 shows the waveforms of the D-CA operation corresponding to Figure 5. The pulses in high states are the computation time of controls (T_{ctrM} , $T_{ctrSub(j)}$, $j = 1, 2, 3$) when EPWM interrupts occur, and hence the rising edge of those pulses indicates the points where EPWM interrupts are generated. It can be seen that all EPWM interrupts of the control boards are synchronized.

**Figure 11.** The waveforms of D-CA operation corresponding to Figure 5.

In the figure, the operation during a T_{ctrl} can be explained as follows. First, in the master board, as soon as an EPWM interrupt occurs, the computation of the CHM converter control (i.e., PLL, DC-link voltage control of the CHM converter, and grid current control) and the DAB converter output voltage control are conducted, as shown in T_{ctrM} . In the meantime, in the sub-boards, the computation of the DC-link voltage balancing control is performed, as depicted in $T_{ctrSub(j)}$. Subsequently, the CAN message M_{s2m} , containing data of $v_{DC-link(j)}$, is transferred from one of the sub-boards to the master board at α . Finally, the CAN message M_{m2s} , including data of v_{fin}^* , $d_{\phi(out)}^*$, is sent from the master board to all the sub-boards at β .

The pulse widths of the EPWM interrupts were the same as the computation time, as the control operation was performed by turning the EPWM interrupt on at the start of the control computation and turning it off at the end of the control computation. The division of the time axis in Figure 11 was 100 μ s, where the computational time of the master board was approximately 150 μ s, and the computation time of each sub-board was approximately 50 μ s. In other words, it can be seen that the sub-boards covered 50 μ s, which was a part of the computational burden that the master board did. As a result, it should be noted that $T_{ctrSub(j)}$ is the computation time for the DC-link voltage balancing control and is taken in every sub-board simultaneously. In addition, in the $T_{X(j)}$ waveform, the 1-bit pulse except for M_{s2m} is an ACK bit (M_{ack}) that indicates whether the message is an error or not. Mack was not sent to the master board.

5.2. The Verification of Operation Sequence and Start-Up Strategy

The experimental result of the entire operation sequence according to Figure 6 is shown in Figure 12. It can be seen that the result is as same as in Figure 6. The pre-charge of DC-link capacitors is conducted in (ii) after PLL is completed in (i); thus, $v_{DC-link(total)}$ becomes approximately 311 V_{pk}, which is the magnitude of the input grid voltage. One can notice that $v_{DC-link(j)}$ is unbalanced in this region. Next, in (iii), the output capacitors are charged to $v_{out,pr}$, which means v_{out} becomes around 69 V due to the turn ratio of the MFTR. When the output capacitors are fully charged, the DC-link voltage balancing control and output voltage control are conducted in (iv). Subsequently, the DC-link voltage control of the CHM converter starts in (v), and $v_{DC-link(total)}$ increases up to the rated value of 390 V via a ramped increase. Once $v_{DC-link(total)}$ reaches a steady state, v_{out} increases to the rated value 80 V in (vi). When v_{out} is held in a steady state, the SST is fully ready; finally, a load is connected at the output of the SST. In this experiment, a step-load is applied, and hence i_g and i_{pri} become larger immediately compared to that of (vi). It can be seen that $v_{DC-link(j)}$ and v_{out} are controlled reliably despite a step load variation.

Figure 13 shows the zoomed extractions of $v_{DC-link(total)}$ and $v_{DC-link(j)}$ from Figure 12. $v_{DC-link(j)}$ has different voltage levels in (ii) and (iii), while $v_{DC-link(total)}$ is held constant. In contrast, they become balanced in (iv) due to the DC-link voltage control. As described in Section 4, the reason for the operation of (iv) prior to (v) is to prevent the situation where one of the $v_{DC-link(j)}$ exceeds the rating of components during the ascent of $v_{DC-link(total)}$ in (v).

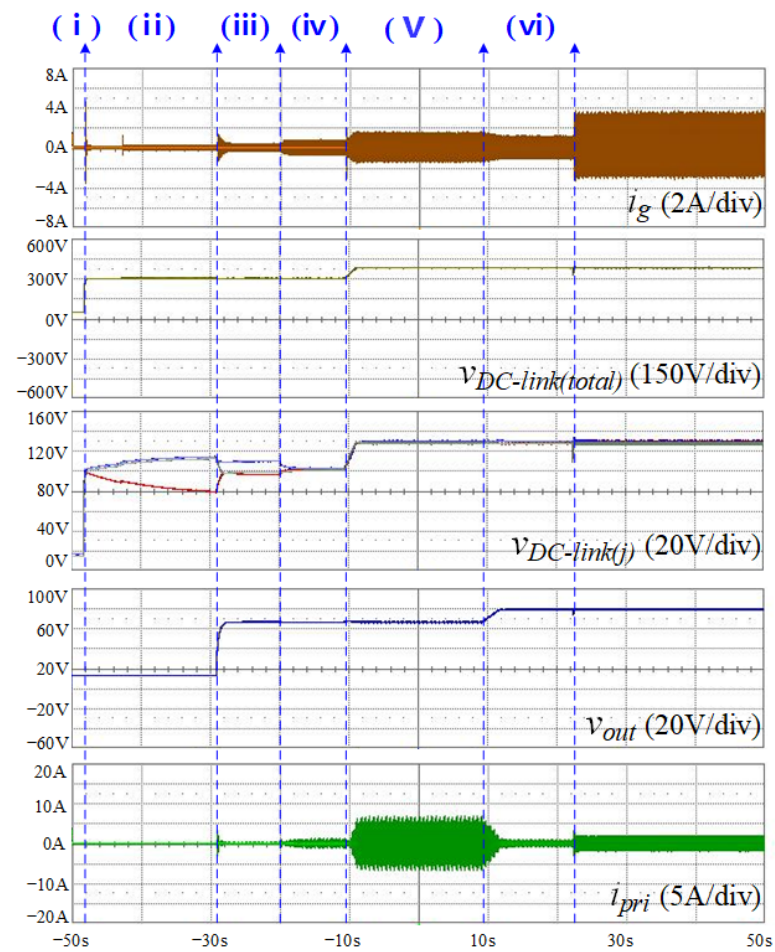


Figure 12. The experimental results corresponding to Figure 6, displaying the entire operation sequence of the designed SST. (i) PLL (ii) pre-charge of DC-link capacitors (iii) pre-charge of output capacitors (iv) DC-link voltage balancing and output voltage control (v) DC-link voltage control (vi) increase of the output voltage to rated value.

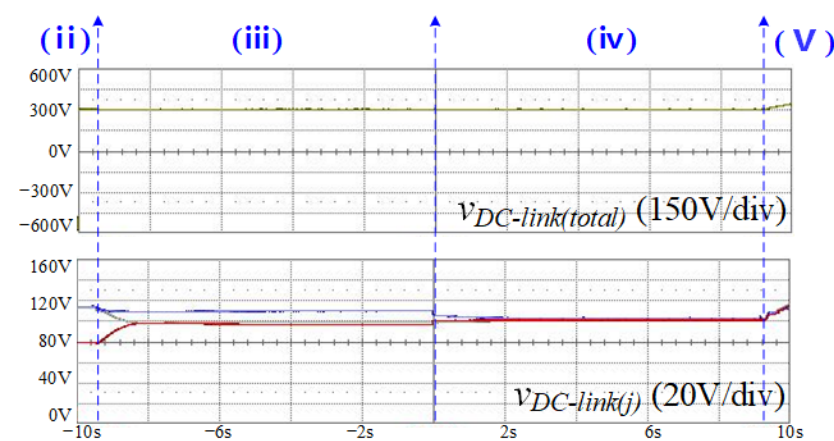


Figure 13. The enlarged waveforms of DC-link voltages in (iii) and (iv) showing the performance of the DC-link voltage balancing controller.

Figure 14 shows the experimental results when the load changes to 12.5%, 25%, and 50% of the rated load. Although the output power changes in steps, $v_{DC-link(j)}$ and v_{out} immediately track the reference values (i.e., 130 V and 80 V), indicating that the dynamic response of the designed controllers is fast enough. Furthermore, from Figure 14a–c,

displaying the zoomed extraction at respective load conditions, it can be observed that both voltages remain stable, and i_g exhibits sinusoidal waveforms.

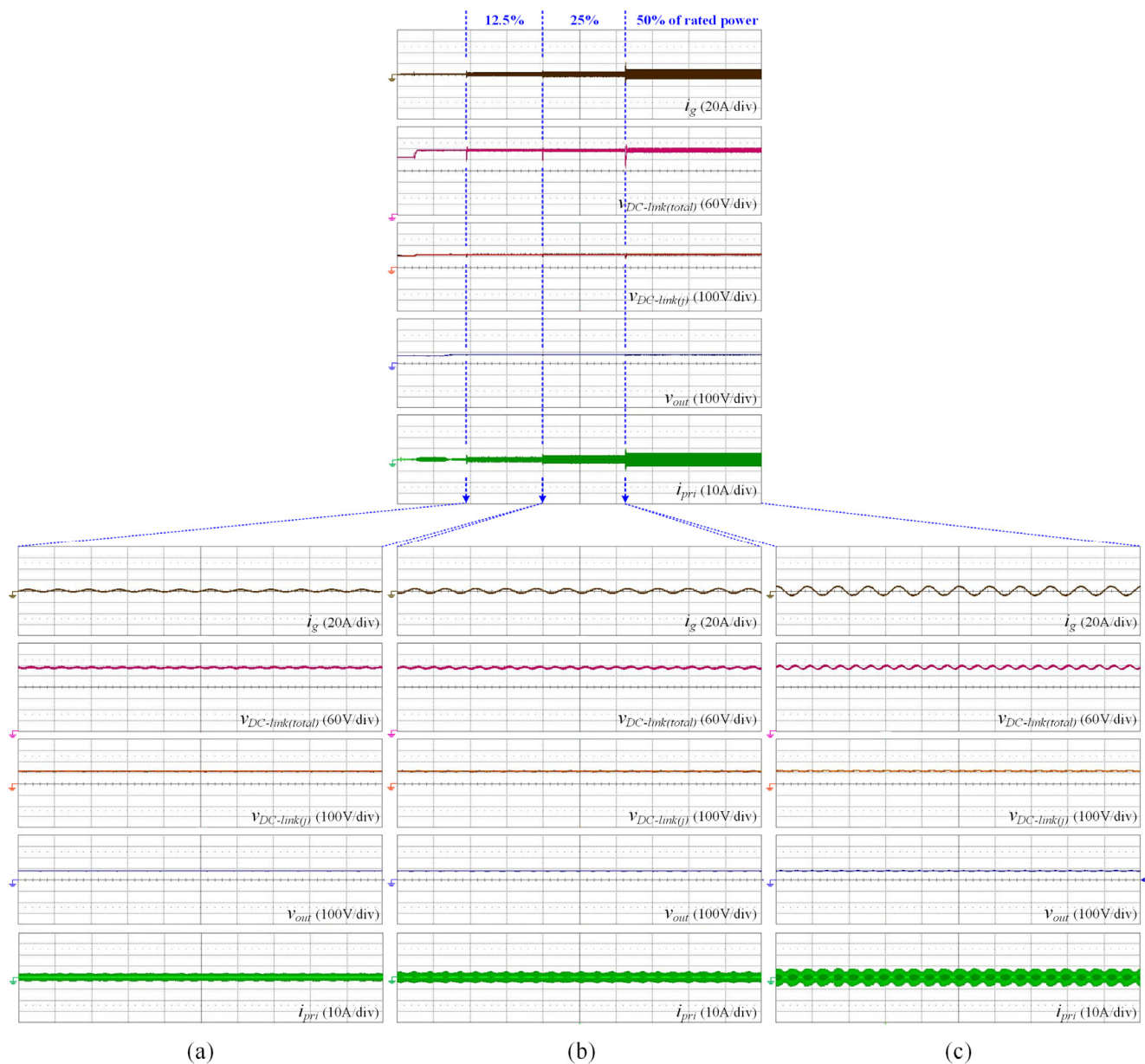


Figure 14. The experimental results of the designed SST when load changes to (a) 12.5%, (b) 25%, and (c) 50% of the rated load.

Figure 15 shows a switching pulse at the start-up operation of the CHM converter when the sequence (v) starts. Due to the application of the CHM converter start-up strategy as in B in Section 4, switching pulses are output without omissions in all cells. Therefore, it is clear that there is no high surge of i_g when (v) starts in Figure 12.

Figure 16 presents the switching pulses at the start-up operation of the DAB converter when the sequence is transferred from (iii) to (iv). In (iii), the switching pulses with a small duty cycle (0.05) are applied for the slow pre-charge of the output capacitors. Subsequently, in the transfer region from (iii) to (iv), it can be seen that the switching pulses follow those of Figure 8b due to the DAB converter start-up strategy as in Section 4.3. Therefore, at the start of (iv) in Figure 12, the magnitude of i_{pri} is not negatively biased.

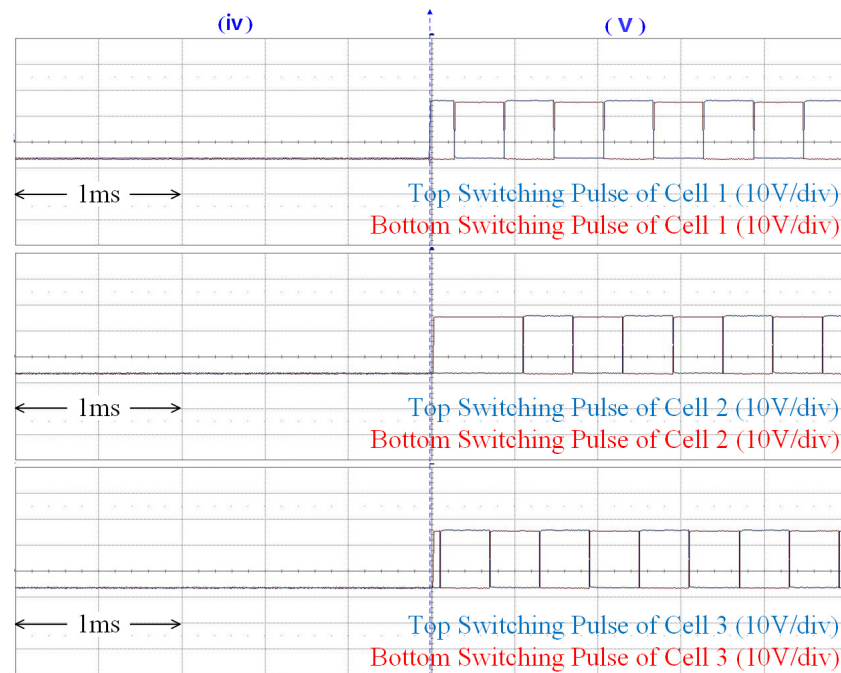


Figure 15. Experimental results: the switching pulses in the CHM validating the start-up strategy.

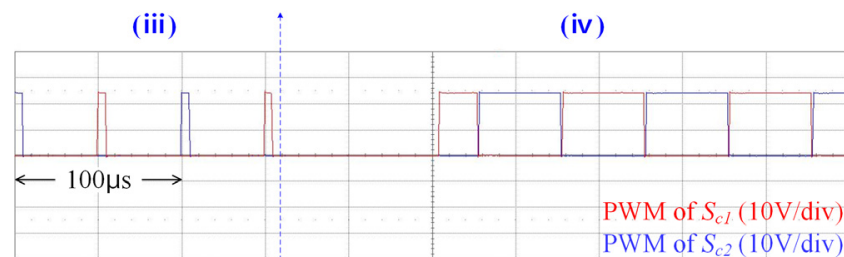


Figure 16. Experimental results: The switching pulses in the DAB primary side validating the start-up strategy. (iii) pre-charge of output capacitors (iv) DC-link voltage balancing and output voltage control.

5.3. Rated Operation of the Designed SST

Figure 17 shows the enlarged waveforms of Figure 12 when the SST is operated at the rated power. Throughout the result, v_{out} remains at 80 V and i_g is maintained as a sinusoidal waveform with approximately 16.5 A_{pk}. Furthermore, while $v_{DC-link(total)}$ is held at 390 V, $v_{DC-link(j)}$ is in a balanced condition to 130 V on average. Regarding i_{pri} , it can be noticed that a swing associated with the second order of $v_{DC-link(j)}$ appears.

Figure 18 shows the waveforms in relation to the CHM converter at the rated power. Note that v_g and v_g are in phase due to the unity power factor control. In addition, according to Table 2, since the MI is approximately 0.8, v_{CHM} has seven levels of voltage.

In terms of DAB converter operation, Figure 19 shows the waveforms of Cell 1 at the rated power. v_{pri} and v_{sec} , the square waves with a 0.5 duty cycle, have a phase shift due to the power transmission principle of the DAB converter, as described in Section 3, inducing the trapezoid shape of i_{pri} . Here, a positive phase shift means the power delivery to the output of the DAB converter. It is noteworthy that v_{out} is held constant without variation during the experiment.

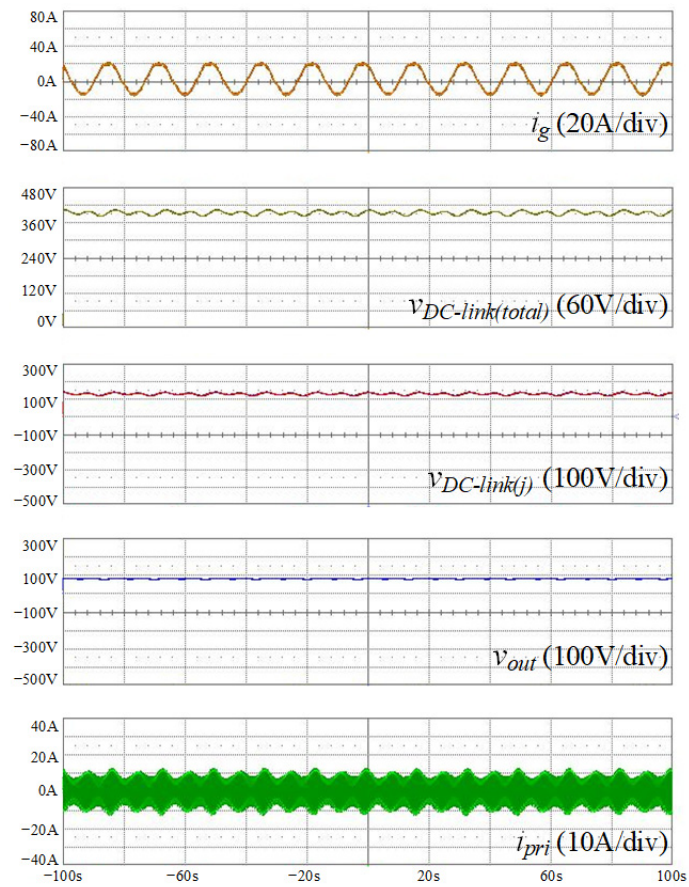


Figure 17. The experimental results of the designed SST at the rated load.

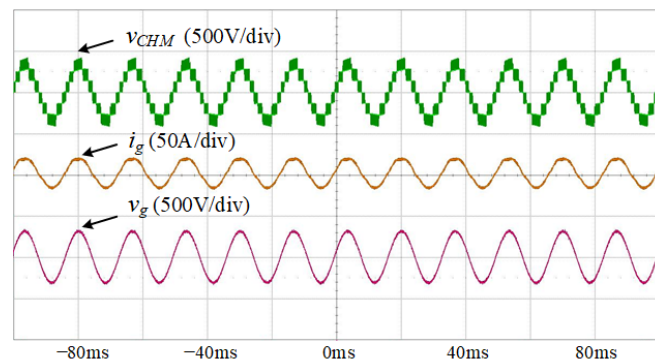


Figure 18. Experimental results showing steady state of CHM at rated load.

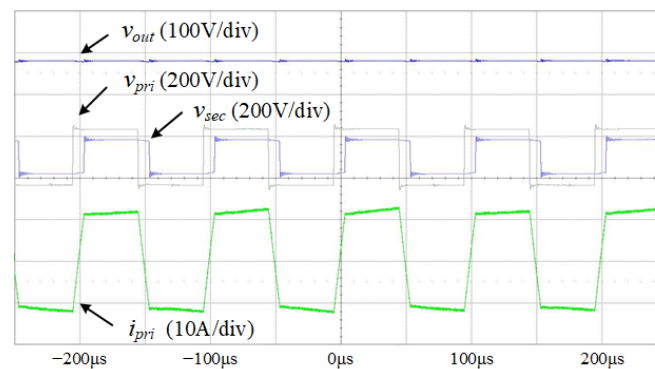


Figure 19. Experimental results showing steady state of DAB at rated load.

6. Conclusions

This article proposed a hierarchical control architecture named D-CA and an operation sequence with start-up strategies for a DSP-based SST. With the proposed D-CA, because sub-boards have a dedicated DC-link voltage balancing controller for their corresponding cells individually, the computation time was distributed, resulting in a low computational burden on the master board. We presented the controller disposition to the control boards with the communication structure and sequential operation on the DSP in the time domain. Regarding the operation sequence, by arranging a step for the DC-link voltage balance prior to the entire CHM converter control, safe driving of the SST was achieved. Furthermore, considering the implementation of the DSP, start-up strategies for the CHM and DAB converters were also designed in order to prevent unexpected damage to the SST system due to a current surge. Our experimental results verified the validity of the proposed D-CA and operation sequence with start-up strategies.

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