



Article Design of Planar Transformers for LLC Converters in High Power Density On-Board Chargers for Electric Vehicles

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Abstract: This article presents a planar transformer design and optimization method for high power density on-board chargers (OBCs) utilized in electric vehicles (EVs). Owing to considerations of electrical safety, OBCs require an isolated converter, leading to a substantial increase in volume due to the inclusion of a transformer. To address this issue and achieve high power density, a planar transformer is used, and an optimized design method is proposed for pattern arrangement, width, and core shape. The feasibility of the design is verified through the development of a 3.3 kW OBC prototype. Consequently, when compared to conventional transformers, the design method in this article results in a 27% reduction in the transformer's height and a 20% reduction in its overall volume. This reduction is advantageous for meeting the requirements of high power density OBCs.

Keywords: electric vehicle; high power density; LLC resonant converter; on-board charger; planar transformer



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1. Introduction

Nowadays, nations worldwide are strongly supporting research activity towards hybrid electric propulsion and renewable fuels both to decrease dependency on fossil fuels and to reduce dangerous air pollutants [1]. Among these, the field in which the most research is being conducted is automobiles. Recently, demand for electric vehicles (EVs) has been increasing because they have the advantage of higher energy conversion efficiency and lower greenhouse gas emissions than internal combustion engine-powered vehicles. There are many areas of research on EVs, including motors, autonomous driving, charging, and batteries. Among these, on-board chargers (OBCs) take an important role for battery charging in EVs, and to date, various circuit topologies and control algorithms have been studied to achieve reliable operation and high efficiency of OBCs [2-10]. Recently, with the aid of high switching frequency characteristics of wide band gap (WBG) devices, such as SiC and GaN, power density has been dramatically enhanced to over 4 kW/L [11–15]. As illustrated in Figure 1, a typical single-phase OBC comprises a power-factor correction (PFC) circuit and DC–DC converter. The DC–DC converter performs battery charging control while satisfying electrical isolation conditions. Among the various DC–DC converter topologies, LLC resonant converters have recently been widely utilized as strong candidates for high power density OBCs owing to the absence of an output filter [11-17]. In order to maximize the advantages of LLC converters, special attention should be paid to reducing the size of high-frequency transformers, and this leads to the design and development of planar-type transformers [16-22]. A planar transformer can achieve a low-profile design because the windings can be implemented inside a printed circuit board (PCB). However, they inherently generate parasitic capacitance, which can cause output voltage distortion, increased loss, and electromagnetic interference (EMI) [23].



Figure 1. Single-phase OBC system with planar transformer.

Therefore, previous planar transformer studies have focused on the minimization of the parasitic capacitance via the PCB pattern arrangement [10,18–23] and the control and utilization of the parasitic capacitance [24–26]. Various core shapes and matrix configurations with fractional turns for current distribution have also been researched [22–30]. In addition, recent studies applying planar transformers to achieve a high OBC power density have not addressed the optimal design of planar transformers [5,31,32]. When planar transformers are designed, insulation gaps should be installed between the multiple layers of the PCB to ensure insulation, resulting in an increase in the core window area. In the case of a transformer core with low height, the required area increases. Previous studies on planar transformer design were conducted with the goal of achieving high efficiency or improving performance rather than increasing power density.

In this paper, each design parameter is analyzed to achieve the minimum volume of the planar transformer to achieve high power density. Additionally, a design guide is proposed that allows for achieving high power density using a single PCB rather than using multiple PCBs. For this purpose, planar transformers are analyzed in detail in terms of pattern arrangement, width, core shape, size, and heat dissipation. In the pattern arrangement, the parasitic capacitance according to the arrangement is analyzed using magnetic analysis simulation, and the effect on the system is confirmed via actual fabrication. The optimal design is proposed considering the pattern width, core shape, and size considering heat dissipation conditions and performance. The validity of the proposed design guidelines is experimentally verified using a 3.3 kW LLC converter prototype for an OBC. The remainder of this paper is organized as follows: Section 2 proposes the system configuration, specifications, and optimal design method for planar transformers. Section 3 verifies the validity via experimental results, and Section 4 concludes the paper.

2. Design of the Planar Transformer

2.1. Initial Design of Planar Transformer

The specifications of the resonant converter and planar transformer parameters adopted in this study are summarized in Tables 1 and 2. Similar to general Litz wire transformers, planar transformers first select the core size using the W_aA_c product of (1), which represents the transformer capacity.

Parameters	Value
DC link voltage, V_{dc}	500 V
Battery voltage, V _{batt}	440–820 V
Rated output power, Po	3.3 kW
Switching frequency, <i>f</i> _{sw}	200–450 kHz
Resonant frequency, f_{res}	300 kHz

 Table 1. Specification of the LLC resonant converter.

Parameters	Value	
Magnetizing inductance, L_m	79.3 μH	
Leakage inductance, L_r	25.8 μH	
Resonant capacitor, C_r	10.91 nF	
Turns ratio, n	10:12	

Table 2. Parameters of the LLC resonant converter.

$$W_a A_c = \frac{P_{out} D_{cma}}{K_t B_{max} f_{max}},\tag{1}$$

 P_{out} is the output, D_{cma} is the current density, and K_t is a topology constant. The fullbridge structure uses a value of 0.0014, where B_{max} is the maximum magnetic flux density, and f_{max} is the maximum operating frequency. Furthermore, the number of primary and secondary windings is calculated such that B_{max} satisfies 300 mT via the effective cross-sectional area A_c of the core selected using (2) [33].

$$B_{\max} = \frac{L_m I_{Lm,peak}}{NA_c},\tag{2}$$

Finally, when the number of windings on the primary and secondary sides is calculated, an air gap is obtained to match the transformer parameters.

The basic planar core shape is a PEE-shaped core that is easy to manufacture, and the initial design utilizes a PEE 5821 core made of Hitachi's ML27D material that satisfies the W_aA_c design conditions. For the number of transformer turns, the primary and secondary windings are designed as two four-layer PCBs. The current density of the initial PCB pattern is designed to be 30–40 A/mm², and the initial planar transformer is shown in Figure 2. In addition, because planar transformers have low leakage inductance L_r , a separate inductor is added to satisfy the resonance parameter.



Figure 2. Initial designed planar transformer.

2.2. Pattern Design Considering Parasitic Capacitance

Because the planar transformer has multiple layers of thin copper plates of PCB with turns, various studies on parasitic capacitance in the PCB pattern have been conducted [8,16–20]. Therefore, the operating characteristics of the planar transformer of the manufactured LLC converter are examined according to the pattern arrangement. Figure 3 illustrates a conceptual diagram of the parasitic capacitance according to the pattern arrangement inside the planar transformer. Parasitic capacitor components are divided into the intra-winding capacitance generated between the same side and the inter-winding capacitance generated between the primary and secondary sides.

In this study, because the number of turns on the primary and secondary sides is not arranged to alternate, the inter-winding capacitance is very small, and the intra-winding capacitances on the primary and secondary sides are equalized with the equivalent capacitance C_{eq} , as shown in Figure 4. In this case, if the parasitic capacitance component

increases, the resonance curve of the LLC converter becomes distorted as shown in Figure 5, making it difficult to control the desired output power [10].



Figure 3. Conceptual diagram of parasitic capacitance inside the PCB pattern.



Figure 4. LLC resonant converter circuit considering equivalent parasitic capacitance.



Frequency [Hz]

Figure 5. LLC resonant converter voltage gain curve change with parasitic capacitance size.

The pattern layout of the initially designed planar transformer is shown in Figure 6a with maximum overlap between the patterns, and is illustrated in Figure 6b so that the interlayer patterns overlap to the minimum to reduce the parasitic capacitance. The parasitic capacitance is measured using JMAG, a finite element method (FEM) analysis simulation tool.

The simulation results are presented in Figure 7 and Table 3. When the patterns are arranged without overlapping, it can be observed that the parasitic capacitance is the smallest. Based on these results, planar transformers with patterns are manufactured under various conditions.







Figure 7. JMAG simulation parasitic measurement results according to PCB pattern arrangement. (a) Maximum pattern overlap. (b) Minimum pattern overlap.

Pattern Arrangement	Maximum Capacitance	Minimum Capacitance
Maximize overlap	8.14 pF	0.77 pF
Minimize overlap	2.70 pF	0.68 pF

Figures 8 and 9 illustrate planar transformer windings under various manufacturing conditions and their internal layouts. Case 1 considers the maximum pattern overlap. Case 2 minimizes the overlap of each layer, and Case 3 allows an intermediate overlap compared with Cases 1 and 2. To measure the parasitic capacitance of the manufactured PCB pattern illustrated in Figure 9, the resonance frequency is checked using an LCR meter, and the results are illustrated in Figure 10. Table 4 presents the equivalent parasitic capacitance C_{eq} of each PCB calculated using the measured resonance frequency.



Figure 8. PCB internal pattern layout under various conditions. (a) Maximum pattern overlap.(b) Minimum pattern overlap. (c) Intermediate pattern overlap.



(**a**) Case 1

(**b**) Case 2

(c) Case 3

Figure 9. Manufactured PCBs under various conditions. (**a**) Maximum pattern overlap. (**b**) Minimum pattern overlap. (**c**) Intermediate pattern overlap.



Figure 10. Impedance characteristic curve according to frequency of various PCBs. (**a**) Maximum pattern overlap. (**b**) Minimum pattern overlap. (**c**) Intermediate pattern overlap.

Table 4. Parasitic capacitance measurement results ac	ccording to PCB	pattern arrangement.
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Case	L_m	fres	C _{eq}
Case 1	78.3 μH	0.7 MHz	676 pF
Case 2	74.2 μH	1.82 MHz	103 pF
Case 3	74.0 μH	1.88 MHz	96.7 pF

Figure 11 illustrates the voltage gain curve of the LLC converter by reflecting the parasitic capacitance values calculated in Table 4. Accordingly, although the size of the parasitic capacitance affects the voltage gain curve of the LLC converter, the change in gain is negligible within the operating range of use; thus, the issue is verified via actual experiments.



Figure 11. Voltage gain curve of actual LLC resonant converter with each parasitic capacitance.

Figure 12 illustrates the LLC converter applied with the planar transformer for operation verification, and experimental verification conditions are presented in Table 5. During the verification, an additional resonant inductor is used for the same resonant frequency.



Figure 12. Experimental setup of the LLC resonant converter with planar transformer.

Table 5. Operation verification experimental condition.

Parameters	Value
DC link voltage, V_{dc}	500 V
Battery voltage, V _{batt}	600 V
Rated output power, Po	3.3 kW
Resonant frequency, <i>f</i> _{res}	300 kHz

Figure 13 illustrates the experimental waveforms and efficiencies of the conventional Litz wire and planar transformers designed for each case. The following conclusions can be drawn from the experimental results for each case:



Figure 13. Experimental waveforms and efficiency of the LLC converter with different transformer types. (a) Conventional Litz wire. (b) Case 1 planar transformer. (c) Case 2 planar transformer. (d) Case 3 planar transformer.

- (1) When using a planar transformer, the efficiency is reduced by approximately 1% compared to the conventional Litz wire transformer.
- (2) The number of turns of a planar transformer is implemented through copper on the PCB, so optimizing the pattern width is important for PCB heat dissipation and realizing the number of turns.
- (3) Because the resonant frequency caused by the parasitic capacitance of the PCB pattern differs significantly from the operating frequency in this system, it does not have a significant effect on the overall operation.
- (4) Because the difference in efficiency and operation according to the parasitic capacitance of the planar transformer of the LLC converter is insignificant, as in Case 1, which minimizes the required window area of the core, it is advantageous for achieving a high power density.

Therefore, in the remainder of this study, the pattern arrangement is designed using the Case 1 method to increase the power density.

2.3. Selection of Planar Core Shape

The core shape determines the pattern structure and overall volume of the planar transformer. Commercially utilized planar transformer cores include an E-shaped PEE core and a UI core; in this study, an additional core shape called an H core is proposed to increase the power density. The shape and characteristics of each core shape are presented in Figure 14 and Table 6, respectively.



Figure 14. Various cores for the planar transformer. (a) PEE core. (b) UI core. (c) H core.

Table 6. Characteristics of planar transformer core shape.

Planar Transformer	PEE Core	UI Core	H Core
Advantage	Low height	Wide pattern heat dissipation area	Low height
	Narrow area required	Implementing a large number of turns	Minimum volume
Disadvantage	Narrow pattern heat dissipation area	Wide area required	Difficult pattern heat dissipation
	Implementing a large number of turns	High height	Implementing a large number of turns

The PEE core can be implemented with a low profile; however, if a large number of turns are required, two or more PCBs must be utilized. In this case, heat dissipation of the planar transformer pattern becomes difficult. The UI core can implement the number of turns with two core pillars; therefore, the system can be implemented with a single PCB compared with the PEE core, and the current density can be increased owing to the large heat dissipation area. However, because the height of the core doubles compared with that of the PEE core according to the effective cross-sectional area, and the required area also increases, it is inefficient in terms of volume. The H core is a structure that can further reduce the height while reducing the PCB area exposed to the outside of the PEE core. However, heat dissipation is difficult because the entire PCB is located inside the core. Figure 15 and Table 7 present the manufactured planar transformers and their parameters, respectively. All three planar transformers have the same effective cross-sectional area, and the operation is verified by manufacturing a PCB according to each core shape.



Figure 15. Planar transformers manufactured in various core shape. (a) PEE core. (b) UI core. (c) H core.

PEE Core	UI Core	H Core
60 imes 100 imes 22	$96\times55\times41$	64 imes74 imes14
6000 mm ²	5280 mm ²	4992 mm ²
132,000 mm ³	216,480 mm ³	69,888 mm ³
78.32 μH	78.90 μH	77.56 μH
3.98 µH	0.73 μH	4.67 μΗ
	PEE Core 60 × 100 × 22 6000 mm ² 132,000 mm ³ 78.32 μH 3.98 μH	$\begin{array}{c c c c c c c c c c c c c c c c c c c $

 Table 7. Specifications for each planar transformer core shape.

Figure 16 illustrates the experimental results, system efficiency, and maximum PCB temperature. Accordingly, a slight difference in efficiency occurs depending on the core shape; however, the PCB temperature difference occurs the most. Under air-cooling conditions, it was confirmed that the PEE core increased to 112 °C, the UI core increased to 72 °C with a large dissipation area, and the H core did not dissipate heat inside the PCB; therefore, it increased to 133 °C. In general, for stable operation of the system, the temperature of the PCB is limited to 110 °C. Therefore, the PEE and UI cores, excluding the H core, are selected as cores suitable for stable operation. Consequently, the core size must be determined for an optimal design. To achieve this, the width and number of turns of the pattern must be determined before the pattern can be selected. The width of the pattern is determined as described in the following section.



Figure 16. Experimental waveforms and efficiency of the LLC converter with different transformer core types. (a) PEE core. (b) UI core. (c) H core.

2.4. Design of Pattern Width

In planar transformers, the width of the printed PCB pattern determines the size and current density of the window area of the core. As the width of the pattern increases, the size of the window area of the required core and overall volume increases. An optimal current-density design for the PCB pattern is required to design the optimal power density of the planar transformer. Accordingly, a PCB pattern with various current densities is manufactured to measure the temperature during actual operation to select an optimal pattern width. Figure 17 illustrates the system for the planar transformer water cooling.



Figure 17. Planar transformer system with water cooling. (a) Planar transformer. (b) Bottom cooling water passage.

In the previous section, the pattern width was selected based on the UI core shape because it has a large heat dissipation area. Table 8 presents the current densities based on the copper thickness and pattern width used in the PCB. Figure 18 illustrates the PCBs designed based on pattern width. The experiment is conducted under the experimental conditions of Table 5, coolant temperature is adjusted to 25 °C, and finally, the pattern width is selected considering the 65 °C coolant temperature of the actual OBC.

Table 8. Current density according to pattern width.

Parameters	Value			
Current		9.8	A _{rms}	
Thickness		3	OZ	
Width	2 mm	2.5 mm	3 mm	4 mm
Current density	46.3 A/mm ²	37 A/mm ²	30.9 A/mm^2	23.1 A/mm ²



(**a**) 2 mm





(**c**) 3 mm

(**d**) 4 mm

Figure 18. Planar transformer PCB manufactured in various pattern widths.

Figure 19 illustrates a photograph of the thermal image of the planar transformer depending on the pattern width, and Figure 20 illustrates the temperature of the PCB

pattern over time. According to the experimental results, if the current density is more than 30 A/mm^2 , the pattern temperature rises more than $110 \,^{\circ}\text{C}$ when the pattern temperature is considered the actual coolant temperature; therefore, the width of the pattern is finally selected as 3 mm, which is the current density 30 A/mm^2 . In addition, as illustrated in Figure 19, because the temperature of the core is very high, it is necessary to increase A_c for an optimal design.



Figure 19. Thermal image of the planar transformer. (a) 3 oz/2 mm. (b) 3 oz/2.5 mm. (c) 3 oz/3 mm. (d) 3 oz/4 mm.



Figure 20. Transformer pattern temperature measurement results over time. (a) 3 oz/2 mm. (b) 3 oz/2.5 mm. (c) 3 oz/3 mm. (d) 3 oz/4 mm.

2.5. Design of Core Dimension

Because the core shape, pattern arrangement, width, etc. have been determined via the previous process, a core dimension design for increasing the power density is performed. As explained in Section 2.4, because the core A_c is low, a large amount of heat is generated in the core. Increasing A_c changes the number of turns and optimal core size. In this study, when using the UI core, when A_c increases, the height is doubled compared to the PEE core. Therefore, it is determined that it is limited to increasing Ae, and finally, the planar transformer is designed using the PEE core. To reduce the loss of the existing core, B_{max} is lowered to 200 mT in (2), and the turn ratio is changed to 1 to facilitate variation in the number of turns. Table 9 presents the required A_c calculation results according to the number of turns under the B_{max} 200 mT condition, and Table 10 presents the PCB spacing to ensure insulation and distance from the core when manufacturing the planar transformer.

Parameter				Value			
N _p	4 turns	5 turns	6 turns	7 turns	8 turns	9 turns	10 turns
A _c	1250.0 mm ²	1000.0 mm ²	833.3 mm ²	714.3 mm ²	625.0 mm ²	555.6 mm ²	500.0 mm ²

Table 9. Effective area according to the number of turns.

Table 10. Spacing distance conditions for planar transformer.

Parameters	Value
Spacing distance between patterns, D_{P-P}	0.6 mm
Spacing distance between pattern and core, D_{P-C}	3 mm
Spacing distance between PCB and core, D_{PCB-C}	1 mm

The PCB utilizes a single eight-layer PCB for heat dissipation, and the windings on the primary and secondary sides are divided into four layers, respectively. For the width of the pattern, the 3 mm selected in Section 2.4 is applied. The dimensions of the PEE core utilized in the final design are illustrated in Figure 21. The PEE core is designed using (3)–(8) to satisfy all of the above conditions.



Figure 21. PEE core design dimensions.

$$A = D + E, \tag{3}$$

$$B=E+F,$$
(4)

$$C = \frac{D+E}{k},\tag{5}$$

$$D = E + 2(W_{PCB} + D_{PCB-C}),$$
 (6)

$$E = \frac{\sqrt{(W_{PCB} + D_{PCB-C})^2 + 2kA_c - (W_{PCB} + D_{PCB-C})}}{2},$$
(7)

$$F = T_{PCB} + 2D_{P-C},\tag{8}$$

$$N_{1-Layer} = \frac{N_P}{4},\tag{9}$$

$$W_{PCB} = N_{1-Layer} W_P + 2D_{P-C} + D_{P-P} (N_{1-Layer} - 1),$$
(10)

$$A:C=k:1,\tag{11}$$

 $N_{1-Layer}$ represents the number of turns per PCB layer, and the decimal point is rounded up. W_{PCB} represents the width of the actual PCB including the pattern width and PCB separation distance as illustrated in Figure 22 and is calculated using (10).



Figure 22. Parameters for planar transformer design.

In (11), k represents the horizontal-to-vertical ratio of the planar core. As k increases, the area of the PCB exiting the core widens; thus, the PCB heat dissipation area increases. In this study, k = 3 is selected via the experiments. Table 11 lists the PEE core planar transformer design results according to the number of turns calculated based on (3)–(8), and Figure 23 illustrates the area and volume analysis results based on Table 11. Finally, a planar transformer is designed based on eight turns to minimize the area and volume of the transformer while maintaining the pattern and core temperature at an operable level.

Table 11. Design results of PEE core parameters according to the number of turns.

Parameter	Value						
Np	4	5	6	7	8	9	10
A_c^r	1250.0 mm^2	1000.0 mm ²	833.3 mm ²	714.3 mm ²	625.0 mm ²	555.6 mm ²	500.0 mm^2
А	96.6 mm	92.4 mm	85.8 mm	80.6 mm	76.4 mm	77.6 mm	74.8 mm
В	46.6 mm	40.6 mm	37.3 mm	34.7 mm	32.6 mm	29.6 mm	28.2 mm
С	32.4 mm	30.8 mm	28.6 mm	26.9 mm	25.5 mm	25.9 mm	25.0 mm
D	58.6 mm	59.9 mm	56.5 mm	53.9 mm	51.8 mm	56.0 mm	54.6 mm
Е	38.6 mm	32.6 mm	29.3 mm	26.7 mm	24.6 mm	21.6 mm	20.2 mm
F	8 mm	8 mm	8 mm	8 mm	8 mm	8 mm	8 mm
Area	63 cm ²	65 cm ²	59 cm ²	54 cm^2	50 cm^2	56 cm ²	54 cm^2
Volume	294 cm^3	264 cm ³	218 cm ³	186 cm ³	162 cm ³	167 cm ³	151 cm ³



Figure 23. Transformer area and volume according to the number of turns.

3. Verification

The final system designed to verify the optimally designed planar transformer is illustrated in Figure 24. The operation is verified until temperature saturation occurs under the experimental conditions of a coolant temperature of 25 °C and a load of 3.3 kW. The time-dependent temperature measurements, as illustrated in Figure 20, are depicted in Figure 25. When compared to the existing temperature measurement results, it is evident that the temperature remains constant for up to 30 min after operation. Furthermore, there is no observable increase in pattern temperature attributed to the core. Finally, it is confirmed that the pattern temperature of the planar transformer stabilizes at approximately 72 °C, while the transformer core temperature stabilizes at approximately 89 °C.



Figure 24. Optimally designed planar transformer. (a) 3D model. (b) Manufactured transformer.



Figure 25. Transformer pattern temperature measurement results over time.

Figure 26 illustrates the operation waveform of the LLC converter for each battery voltage. The results indicate no adverse effects from parasitic capacitance, and normal operation is observed at each voltage level. This validates the feasibility of the final planar transformer design, demonstrating a 27% reduction in height and a 20% reduction in volume compared to the conventional PQ core transformer.



Figure 26. Experimental waveforms and efficiency of the LLC converter according to the battery voltage. (a) $V_{batt} = 440$ V. (b) $V_{batt} = 600$ V. (c) $V_{batt} = 820$ V.

4. Conclusions

Owing to the increasing demand for electric vehicles, the development of high power density on-board chargers is imperative to enhance vehicle mileage and fuel efficiency. In OBCs, DC–DC converters require the use of transformers for electrical safety reasons. Power density can be augmented by employing planar transformers, and this study proposes a method for designing such transformers.

For planar transformer design, analysis was conducted on pattern arrangement, pattern width, core size, and shape selection. Through simulation and production of various planar transformers, the planar transformer design method suitable for high power density was proposed. The pattern arrangement was selected based on an analysis of the actual operating frequency range and parasitic capacitance resonance frequency. The pattern width was determined considering heat dissipation conditions and actual experiments, and the final core shape and size were designed based on the previously selected parameters. Through this approach, it was confirmed that compared to conventional transformers, it was possible to reduce the height by 27% and the volume by 20%. To validate the feasibility and performance of the final planar transformer design, experiments were conducted using a prototype of the LLC converter for a 3.3 kW OBC.

The plan is to conduct experiments in the near future to confirm whether the high power density planar transformer design method proposed in this study can be mounted on an actual OBC. These experimental tests aim to verify the feasibility of implementing the design proposed in this paper, thereby demonstrating the potential for developing a high power density OBC by installing the planar transformer in the actual OBC.

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