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PV Powered High Voltage Pulse Converter with Switching Cells for Food Processing Application

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Abstract: In recent years, industries in the suburb have retrofitted their power supply units with solar power supply systems. Using solar power supply systems for various applications, such as food processing, enables energy expense saving. A promising opportunity in the food industry is solar-powered Pulsed Electric Field (PEF) used in the treatment of fruits and their by-products. For this application, a converter is proposed in this paper with a combination of a passive switched inductor cell and a switched capacitor cell. Furthermore, the derived topology possesses an extendable feature. This topology generates high voltage repetitive pulses with a single semiconductor switch and a reduced component count. Dynamic study of the converter is also performed with the derivation of the transfer function. Cost effective, reliable, and simple circuitry are the critical features of this topology. The circuit topology can generate high voltage pulses by increasing the number of switched inductors and switched capacitor cells. A correlation study on the impact of the switched inductor/capacitor cell is also performed and analyzed, which is not usually performed. A 50 W prototype is designed and tested to validate the performance of the converter

Keywords: pulsed electric field (PEF); DC–DC converters; solar PV; passive switched inductor switched capacitor (PSLSC) converter; switched capacitor cell

Citation: Sumathy, P.; Navamani, J.D.; Lavanya, A.; Sathik, J.; Zahira, R.; Essa, F.A. PV Powered High Voltage Pulse Converter with Switching Cells for Food Processing Application. *Energies* **2023**, *16*, 1010. https://doi.org/10.3390/en16021010

Academic Editor: Elyas Rakhshani

Received: 2 December 2022
Revised: 11 January 2023
Accepted: 12 January 2023
Published: 16 January 2023

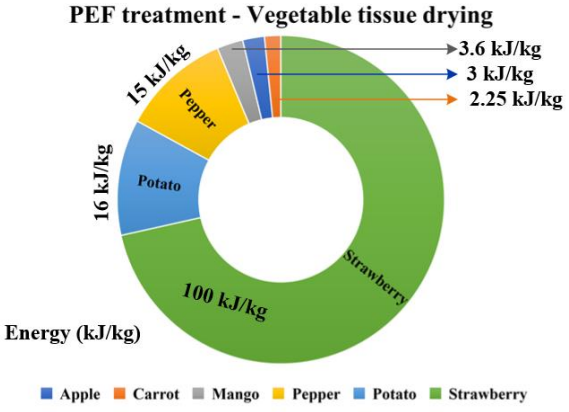
1. Introduction

Recently, modern technologies have been introduced to the food processing industries to retain the nutrients in the food when it is processed. For example, moisture extraction processes to inhibit the deterioration and dehydration of vegetables and fruits have been modernized. Thermal drying, osmotic dehydration and vacuum infusions are some of the methods of dehydration. As a substitution to traditional food processing methods, non-thermal food processing techniques have gained a wide range of popularity and serve as a potential tool in fruit preservation. As a non-thermal method in food preservation, Pulsed Electric Field technology involves short electric pulses for the inactivation of micro-organisms and the dehydration of fruits and the preservation of their vital quality and nutrition. Pulsed Electric Field (PEF) stands as a low cost and low energy technology for the cell membrane permeabilization of fruit tissues [1,2]. The PEF maintains the basic structure of food without thermal degradation and a significant temperature rise [3,4]. The benefits of PEF in large scale food industry application as a standalone process, and also as a combination with various methods for the acceleration of fermented food are discussed [1].

The PEF method of microorganism inactivation is found to increase the temperature while food processing. The selection of PEF with nano second pulses can effectively

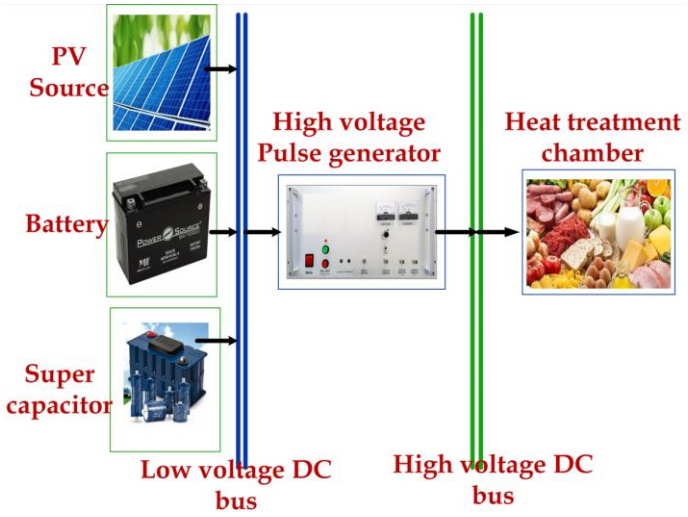
minimize the temperature rise in the food process [5]. Figure 1a illustrates the magnitude of pulses used in the treatment and preservation of various forms of food. The effects of pulse parameters are discussed in the literature, such as kV/cm, pulse frequency and pulse width in the pre-treatment of food, along with conventional methods in the preservation of pine apple, coconut milk—30 kV/cm, square wave pulses, [6]; apple juice—40 kV/cm, 100 pulses per second with 1 µs pulse width [7]; tomato peeling—7.5 kV/cm, 1 kJ/kg, 1 min at 50–70 °C [8]; juice preservation—2.7 kV/cm, 15–1000µs pulses [9]; kiwi fruit dehydration—100 v/cm, 10 µs to 100 s pulses repetitive rectangular pulses [10]; sour cherry juice, apricot and peach nectars preservation—2.4 kV/cm, 210 µs [11]; frozen dry apples—1.07 kV/cm, [12]; and frozen strawberries—850 v/cm, 100µs pulses [13] in various food processing in the industry. Similarly, the energy needed in kJ/kg for the tissue drying of strawberry [14], potato [15], pepper [16], mango [17], apple [18] and carrot [19] is presented in Figure 1b. Figure 1c shows the building blocks of PEF, the compatibility of renewable energy usage in the food processing industry as the source for converters making it a stand alone hybrid system and highlighting the significance of the high voltage converter based pulse generators.

(a)



(b)

Figure 1. *Cont.*



(c)

Figure 1. (**a**) PEF required for various process in food industry; (**b**) energy required for vegetable tissue drying; (**c**) general block diagram of PEF setup with high voltage pulse generator

Table 1. Non thermal processing methods—limitations and advantages.

Processing Kinds	Advantages	Limitations
Irradiation [20–22]	• For several foods it is very effective • Gamma rays and electron beam are the other sources available	• Public acceptance is limited • 7 kilo gray of radiation dose is sanctioned
UV radiation [6,7]	• Non thermal method • Non usage of chemicals	• Harmful to workers in industries when exposed on long term
Super critical carbon dioxide [3,22]	• Can be used in process batch (or) continuous batch	• Solid foods does not show successful results
HPP(high pressure processing) [22,23]	• Can be used of treatment of both solid and liquid samples	• Food quality changes
PEF(pulsed electric field) [20,21]	• Short duration pulses applied on short term leading to less energy usage and no heat generation	• Not suitable for foods unable to withstand higher electric fields. • Well suited for liquid samples treatment.

There are converters developed widely with applications based on renewable energy though pertaining to higher efficiencies, control strategies and switching operations. Isolated and non-isolated converters are the two main divisions of DC converters. When developing isolated DC converters, a high-frequency transformer is utilized to create an electrical isolation amid the converter's input and output. Despite having a programmable positive or negative polarity for the converter's output and being intended to safeguard sensitive loads, this feature has a severe noise interference characteristic. Table 1 gives the comparison of the PEF method of food processing with the other non-thermal methods adapted in the food processing industry to show its superiority over other non-thermal methods of food processing.

Minimum pulsed electric field voltages in the range of 0.3 kV–5 kV is effective in food processing [24–30] which implies that even a conventional single stage boost converter output without multiplier stages can be employed in food preservation directly. The low

voltage produced by the DC–DC generators generally needs high gain DC–DC converters to meet the requirements of the DC load [31,32]. Other than the conversion of renewable energy, DC–DC converters are used in varied applications such as uninterrupted power supply backup systems, discharge lamps of high intensity for head lamps in automobiles and some equipment in electric traction [33–37].Generally, the voltage stress posed on switches is equal to the output voltage in the high boost DC–DC converters conventionally used in recent years. However, to meet the stress due to high voltage, switches are selected with higher voltage ratings, resulting in high conduction loss. Also, the selection of high duty ratio switches also results in high voltage spikes, increased conduction loss and serious reverse recovery problems in diodes [38–40]. The desired high voltage gain can be achieved from various DC–DC isolated converter topologies proposed in the literature [41–43]. Saturation of the core is the problem in this type of isolated converter. Moreover, the introduced leakage inductance by the coupled inductors and transformers necessitates the need for a snubber circuit [41], voltage-clamp diode [42] and active-clamp circuit [43,44].

DC–DC converters of the non-isolated type are therefore used where the galvanized isolation is not in need. A high voltage gain is also achieved with a reduced cost and size. Quadratic boost [45], voltage shift [46], capacitor-diode voltage multiplier [47], switched-inductor and switched capacitor [48] based boost converters are some of the non-isolated boost topologies with high gain. The efficiency of a boost converter can be increased in many ways. The cascading of converter stages can increase the voltage gain. An issue of instability and control circuit complexity occurs due to an increase in the component count in cascaded cycling [49]. The gain can be increased by increasing the number of switched inductor and switched capacitor cells. Though there is an increase in the component count in this combination of switched inductor and switched capacitor, they have their own advantages. The leakage reactance stored energy can be absorbed by switched capacitors. No additional snubber circuit is required. To reduce conduction loss, MOSFET with low on-state resistor is suggested for selection [50]. A suitable converter topology efficiently boosting a low input voltage to a high output bus voltage is discussed and experimentally verified in [51,52]. To alleviate the reverse recovery problems and stress on diodes, Schottky diodes are used and a prototype designed for 40 W is experimentally verified for the converter performance [53]. With a simple topology, a high output voltage obtained with a low duty ratio can be easily obtained just by increasing the number of inductor cells of the circuit topology. The results are analyzed experimentally [54]. Another topology, applying the same gating pulses for the two switches, is proposed efficiently to obtain a high conversion ratio with a reduced loss on the converter and experimentally validated [20–23,55–59].

Substantial attention has been drawn over the past few years by high step ratio dc–dc converters due to their wide range of utilization. In this paper, a new improved converter is presented with an appreciable voltage gain for PEF. It is fed from an isolated DC source of low voltage with a switching inductor (SL) cell and switching capacitor (SC) cell. The output stage of the configuration has a high voltage switch which in turn stands as the main disadvantage of the circuit owing to its high voltage chopping functionality and capacity in turn. High voltage unipolar pulses are produced by the chopping of DC voltage elevated by the high voltage switch. The gain can be increased to a very high value by increasing the number of SL and SC cells.

The advantages of the proposed converters are as follows:

(i) Single switch topology;
(ii) Scalable;
(iii) Regulated output voltage;
(iv) High efficiency;
(v) Less stress on semiconductor devices;
(vi) High voltage output.

The above advantages are verified suitably using simulation results, mathematical derivations and a prototype. The simulation and hardware specifications are tabulated and the results are provided in the following sections.

2. Passive Switched Inductor Switched Capacitor (PSLSC) Converter

The boosted voltage level is achieved by combining a switched inductor cell and a switched capacitor cell, as shown in Figure 2a,b. The boost converter proposed is a combination of switched inductor and switched capacitor cells, as shown in Figure 2c. The proposed converter comprises of a dynamic switch (SW), an output capacitor ($C_{0)}$, output inductor (L_0), load resistance (R_L), a switched inductor cell and a switched capacitor (SC) cell.

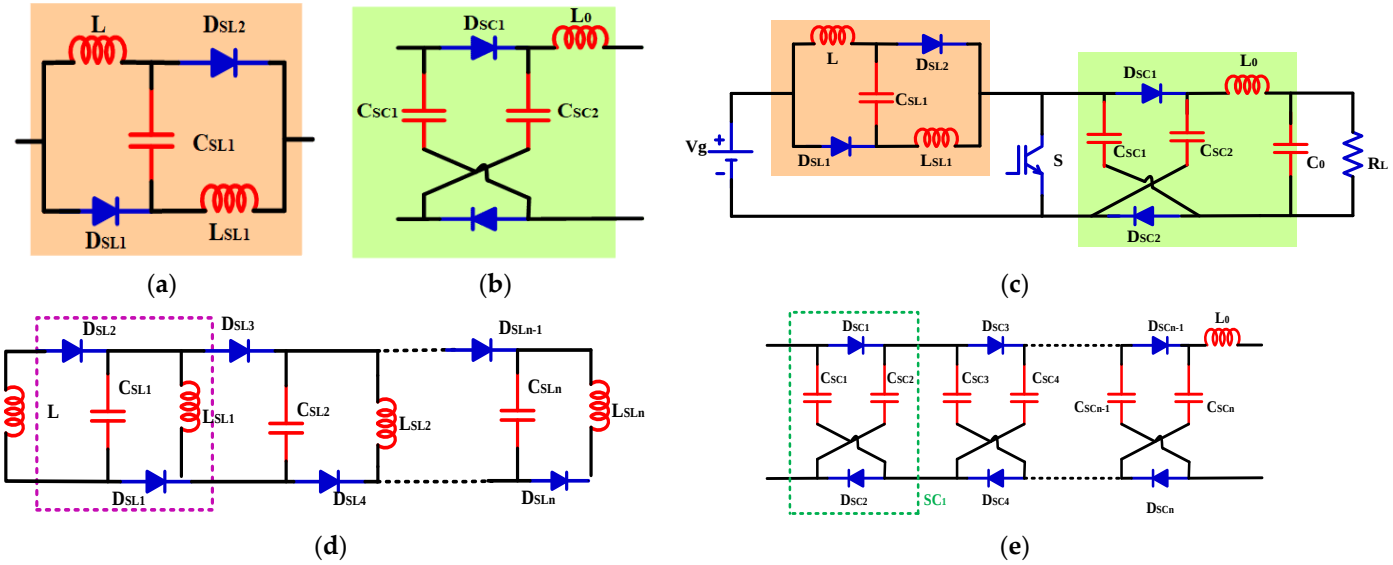


Figure 2. (**a**) SLcell; (**b**) SC cell; (**c**) PSLSC converter topology with single SL and SC cell; (**d**) Cascaded structure of Switched Inductor cell; (**e**) Cascaded structure of Switched Capacitor cell.

3. PSLSC Converter CCM Analysis

In this segment, the operating principle of a PSLSC converter with a SL and SC cell is discussed. The proposed converter shown in Figure 3 is effective in food processing applications. Figure 3 depicts the circuit of the PSLSC converter and further analysis will be carried out with this circuit. The switched inductor (SL) cell consists of two diodes (D_{SL1} and D_{SL2}), an inductor (L and L_{SL1}) and a capacitor (C_{SL1}). The SC cell consists of two diodes (D_{SC1} and D_{SC2}) and two capacitors (C_{SC1} and C_{SC2}). The SL cell charges during the ON period and discharges to the load during the OFF condition of the dynamic switch.

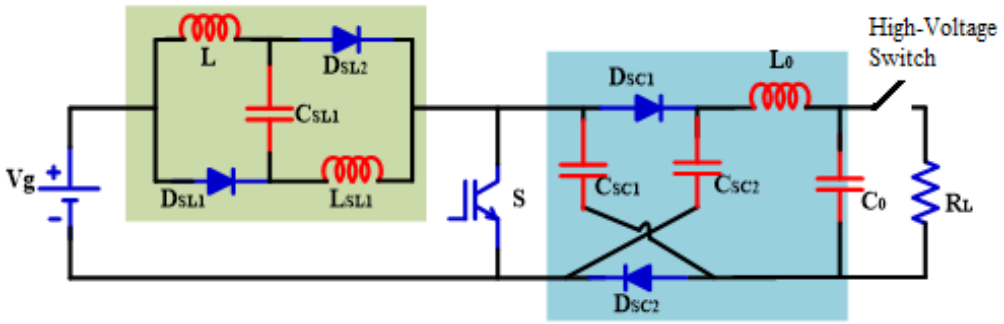


Figure 3. Proposed PSLSC converter.

3.1. Operating Modes of Converter Proposed in CCM

Mode 1:

The switch 'SW' conducts at t = t0. Diodes D_{SL1} and D_{SL2} are forward biased. The inductors 'L' and 'L_{SL1}' are excited by the input DC source Vg. The inductors 'L' and 'L_{SL1}' are connected in parallel with capacitor C_{SL1}. The DC energy source is transferred to the

inductor 'L'. The current Ig is equal to the accumulation of the currents I_L, I_{LSL1} and I_{CSL1}. The capacitors C_{SC1} and C_{SC2} are connected in series with inductors L_0 as the two diodes D_{SC1} and D_{SC2} are reverse biased and supply the load resistance R_L. Figure 4 shows the flow of current in the converter circuit during this interval.

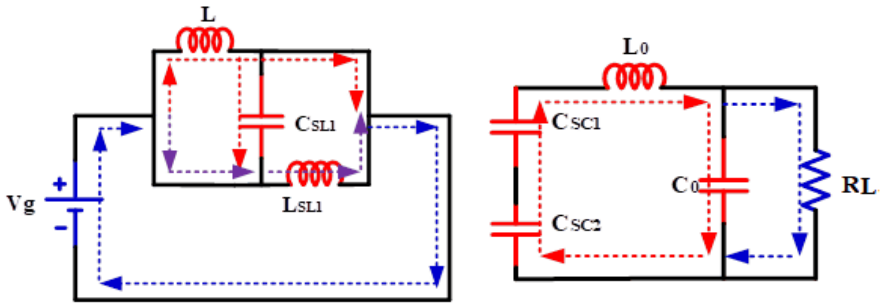


Figure 4. Current flow path of the converter circuit during the interval t_{on}.

Considering the 'ON' stage of the switch 'SW' in the main circuit and applying the principle of inductor voltage-second balance, the following equations are obtained:

$$\int_0^{DT_s} V_L dt = \int_0^{DT_s} V_{SL1} dt = \int_0^{DT_s} V_{CSL1} dt = \int_0^{DT_s} V_g dt \quad (1)$$

$$\int_0^{DT_s} V_{LO} dt = \int_0^{DT_s} (2V_{CSC1} - V_0) dt \quad (2)$$

On the application of the principle of capacitor current-second balance to the main circuit while the switch 'SW' is in ON state, the following relationships are obtained:

$$\int_0^{DT_s} I_{CSL1} dt = \int_0^{DT_s} \frac{I_g}{3} dt \quad (3)$$

$$\int_0^{DT_s} I_{CSC1} dt = \int_0^{DT_s} I_{CSC2} dt = -\int_0^{DT_s} I_{L0} dt \quad (4)$$

$$\int_0^{DT_s} I_{C0} dt = \int_0^{DT_s} (I_{L0} - I_0) dt \quad (5)$$

Mode 2:

During the instant the switch 'SW' is turned off, the inductor 'L' capacitor C_{SL1} and inductor L_{SL1} are connected in series as the diodes D_{SL1} and D_{SL2} are reverse biased. The diodes D_{SC1} and D_{SC2} are forward biased and they connect the capacitors C_{SC1} and C_{SC2} in parallel. This makes the voltage boosted to a high value and available across C0 and RL. The current flow path of the converter circuit during this interval is shown in Figure 5.

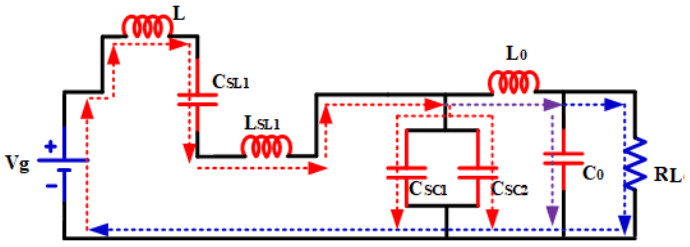


Figure 5. Current flow path of the converter circuit during the interval t_{off}.

On the application of the principle of inductor voltage-second balance, to the PSLSC circuit while the switch 'SW' is in OFF state, the following relationships are obtained:

$$\int_{DT_s}^{T_s} V_L dt = \int_{DT_s}^{T_s} \frac{(V_g - V_{CSC1})}{3} dt = \int_{DT_s}^{T_s} VL_{SL1}\, dt \quad (6)$$

$$\int_{DT_s}^{T_s} V_{L0}dt = \int_{DT_s}^{T_s} (V_{CSC1} - V_{CO})dt \quad (7)$$

On the application of the principle of capacitor current-second balance to the PSLSC circuit while the switch 'SW' is in OFF state, the following relationships are obtained:

$$\int_{DT_s}^{T_s} I_{CSL1}dt = -\int_{DT_s}^{T_s} I_L dt \quad (8)$$

$$\int_{DT_s}^{T_s} I_{CSC1}dt = \int_{DT_s}^{T_s} I_{CSC2}dt = \int_{DT_s}^{T_s} \frac{I_L - I_{L0}}{2}dt \quad (9)$$

$$\int_{DT_s}^{T_s} I_{C0}dt = \int_{DT_s}^{T_s} (I_{LO} - I_0)dt \quad (10)$$

3.2. Derivation of PSLSC Converter Voltage Gain

The waveforms related to the voltage and the current of active and passive components of the PSLSC converter in CCM mode are given in Figure 5. On simplifying (1), (2), (6) and (7) the following voltage equations are obtained.

$$V_{CSL1} = V_g \quad (11)$$

$$V_{CSC1} = V_{CSC2} = V_g \frac{(1+2D)}{(1-D)} \quad (12)$$

The voltage gain ratio of PSLSC converter is

$$\frac{V_0}{V_g} = \frac{(1+2D)(1+D)}{(1-D)} \quad (13)$$

On simplifying (3), (4), (5), (8), (9) and (10) the following current equations are obtained.

$$I_L = I_{LSL1} = \frac{I_0(1+D)}{1-D} \quad (14)$$

$$I_{LO} = I_O \quad (15)$$

Equation (13) is the voltage ratio of the proposed converter. When the numbers of SL and SC cells are increased, the gain of the converter increases. The increase in the number of switched inductor cell increases the voltage ratio and makes no change with respect to the gain ratio with respect to odd (or) even numbers of switched inductor cells. Whereas the addition of switched capacitor cells in odd (or) even numbers makes considerable changes of the voltage boost ratio. The generalized voltage boost ratio with 'M' number of cells added is given below.

$$G_{V(M=1,3,5,.....)} = \frac{V_0}{V_g} = \frac{[1+2M_{SL}D][M_{SC}+D]}{[1-D]} \quad (16)$$

$$G_{V(M=2,4,6,.....)} = \frac{V_0}{V_g} = \frac{[1+2M_{SL}D][M_{SC}+1]-D]}{[1-D]} \quad (17)$$

The proposed topology waveforms are given in Figure 6a,b. Figure 6a shows the wave forms of voltages depicting the gate pulse of switch 'SW', V_{CSL1}, V_{DSL1}, V_{DSL2}, V_{CSC1}, V_{CSC2} and V_{SW} from top to bottom. Figure 6b shows the wave forms of currents that are related to gate pulse of switch 'SW', I_{LSC1}, I_{L0}, V_g and V_{OUT} from topmost to bottom.

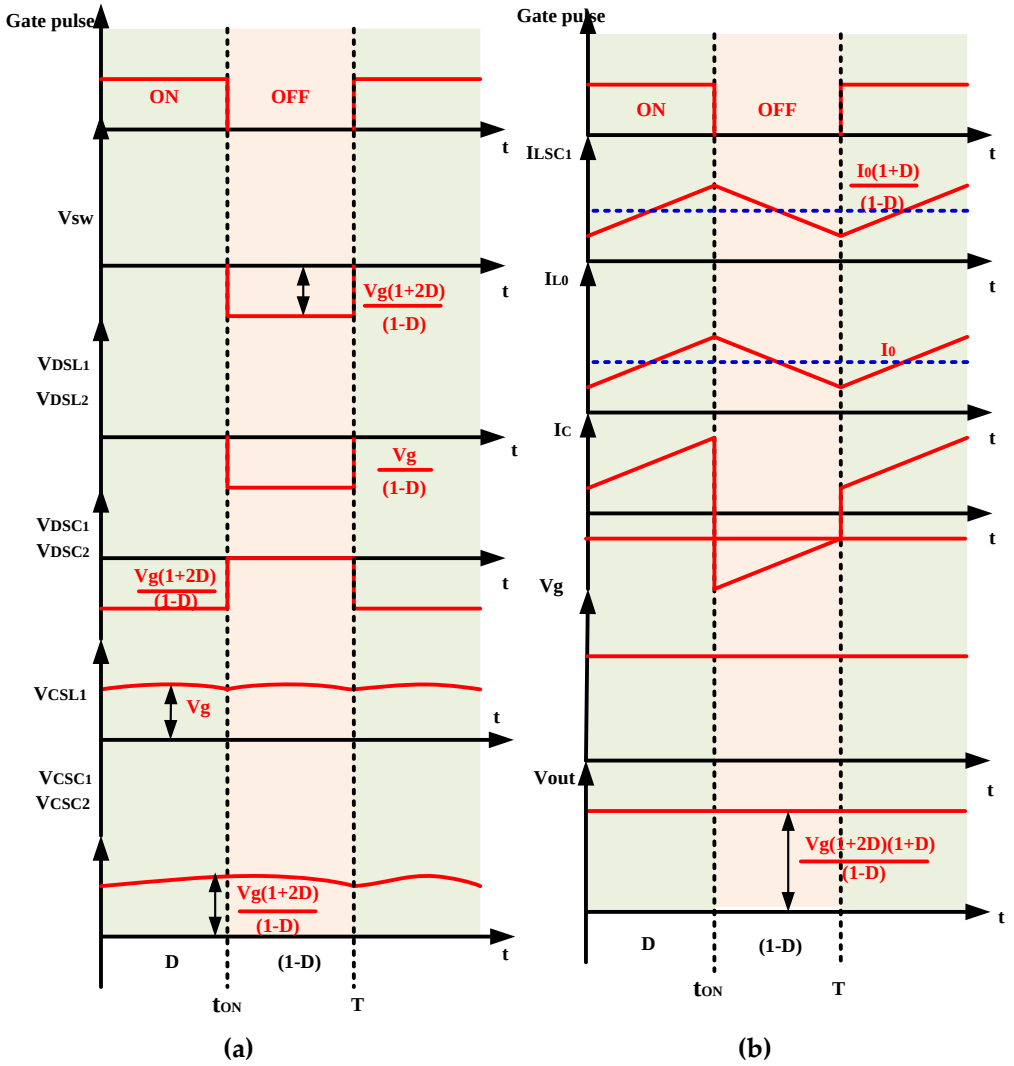


Figure 6. The proposed PSLSC converter waveforms (**a**) voltage waveforms; (**b**) current waveforms along input and output voltage waveforms.

A correlation table is made with the increase in odd and even number of switched inductor and switched capacitor cells and is shown in Tables 2 and 3.

Table 2. Correlation for 1, 2 . . . M_{SLn} switched-inductor cell (M_{SL}) with single Switched-capacitor cell.

Switched-inductor ell (M_{SL})	Number of SL Cell	Voltage Ratio	Switch Stress in Terms of Vg	Switch Stress in Terms of Vo
	1	$\frac{(1+2D)(1+D)}{1-D}$	$\frac{V_g(1+2D)}{1-D}$	$\frac{V_O}{1+D}$
	2	$\frac{(1+4D)(1+D)}{1-D}$	$\frac{V_g(1+4D)}{1-D}$	
	3	$\frac{(1+6D)(1+D)}{1-D}$	$\frac{V_g(1+6D)}{1-D}$	
	N	$\frac{(1+2M_{SL}D)(1+D)}{1-D}$	$\frac{V_g(1+2M_{SL}D)}{1-D}$	

Table 3. Correlations for 1, 2 . . . M_{SCn} Switched-capacitor cell (M_{SC}) with single Switched-inductor cell.

Switched-capacitor cell (M_{SC})	Number of SC Cell	Voltage Gain	Switch Stress in Terms of Vg	Switch Stress in Terms of Vo
	1	$\frac{(1+2D)(1+D)}{1-D}$		$\frac{V_O}{1+D}$
	2	$\frac{(1+2D)(3-D)}{1-D}$		$\frac{V_O}{3+D}$
	3	$\frac{(1+2D)(3+D)}{1-D}$	$\frac{V_g(1+2D)}{1-D}$	$\frac{V_O}{3+D}$
	n odd	$\frac{(1+2D)(M_{SC}+D)}{1-D}$		$\frac{V_O}{M_{SC}+D}$
	n even	$\frac{(1+2D)((M_{SC}+1)-D)}{1-D}$		$\frac{V_O}{(M_{SC}+1)-D}$

It is observed from Tables 2 and 3 that the increase in switched capacitor cells gives more gain when compared with the gain obtained with an increase in switched inductor cells. The increase in odd or even numbers of switched capacitor cells poses no change in switch stress in terms of V_g as can be found from Table 3. Increase in number of switched capacitors further decreases the switch stress in terms of V_0. The voltage stress on switch in terms of V_0 remains constant irrespective of the increase in switched inductor cells in odd (or) even numbers as can be observed from Table 2. The voltage stress on the switch in terms of V_g is considerably high with an increase in the number of cells of the switched inductor. A proper selection of M_{SC} and M_{SL} can give a very high voltage gain suitable for the generation of high voltage pulses with minimal stress on the switch.

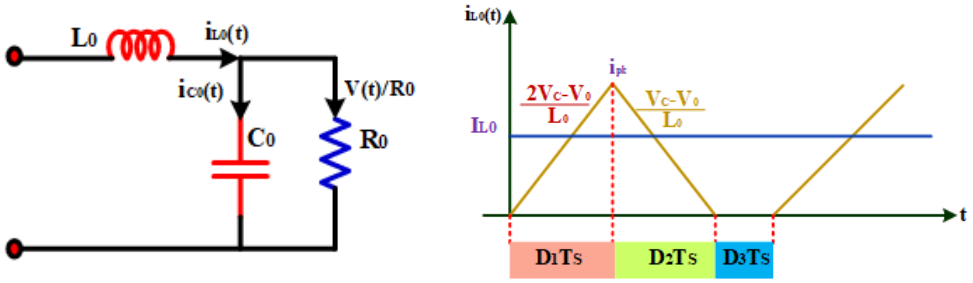
4. Analysis of PSLSC Converter in DCM (Discontinuous Conduction Mode)

When a converter is designed for an application, it is necessary to study the operation of the converter in DCM and BCM conditions. This section elaborates on the operation of the proposed PSLSC converter in discontinuous conduction.

Figure 7b shows the current flow in inductor during D_1T_S, D_2T_S and D_3T_S. The average current through the inductor L_0 is found. From Figure 7a, the current in inductor is obtained as

$$i_{L0}(t) = i_{C0}(t) + \frac{v(t)}{R_0} \tag{18}$$

$$\text{Average current} = \langle i_{L0} \rangle = \frac{1}{T}\int_0^{T_S} i_{L0}(t)dt = \frac{V_0}{R_0} \tag{19}$$



(**a**) (**b**)

Figure 7. (**a**) Proposed Converter configuration in DCM; (**b**) Proposed converter DCM waveforms illustrated.

The area of the triangle also gives the average current through the inductor L_0.

$$\text{Area of Triangle} = \frac{1}{2}\left[\frac{2V_C - V_0}{L_0}\right] D_1 T_S * [D_1 + D_2] \tag{20}$$

Equating (19) and (20), the (21) is obtained.

$$\frac{V_0}{R_0} = \frac{1}{2}\left[\frac{2V_g - V_0}{L_0}\right] D_1\, T_S[D_1 + D_2] \tag{21}$$

Considering Figure 7b, the gain of the converter is determined. The volt-second balance expression in ON mode is obtained as

$$V_g D_1 T_S + \frac{(V_g - V_C)}{3} D_2 T_S = 0 \tag{22}$$

Simplifying (22), the following expression is obtained as

$$V_C = \left[1 + \frac{3D_1}{D_2}\right] V_g \tag{23}$$

Similarly, the volt-second balance law is applied on the non-conducting period of the converter in DCM mode and the obtained expression is

$$2V_C D_1 - V_0 D_1 + V_C D_2 - V_0 D_2 = 0 \tag{24}$$

After simplifying the gain of the converter under DCM is given as

$$V_0 = \left[1 + \frac{3D_1}{D_2}\right]\left[\frac{2D_1 + D_2}{D_1 + D_2}\right] V_g \tag{25}$$

where $K = \frac{2L_0}{R_0 T_S}$.

5. Analysis of PSLSC Converter Topology in BCM (Boundary Conduction Mode)

The boundary between CCM and DCM is BCM. While the converter proposed operates in BCM, the gain of CCM and DCM are equal. The critical value of 'K' obtained is given in Equation (29). Figure 8 shows the curve of 'Kcrit' in terms of 'D'. At the boundary of DCM and CCM, the converter operates in a condition where K=Kcrit. When K>Kcrit, the converter functions in CCM ($I_L > \Delta i_L$) and when K<Kcrit the converter functions in DCM ($I_L < \Delta i_L$).

Figure 8. Proposed converter Boundary condition.

The inductor current ripple is given as

$$\Delta i_L = \Delta i_{LSL1} = \frac{V_g D T_S}{2L} \tag{26}$$

Considering the operation of the converter at the boundary condition

$$\frac{I_0(1+D)}{1-D} > \frac{V_g D T_S}{2L} \tag{27}$$

On substituting (26) in (27) and rearranging the Kcrit value is obtained as

$$\frac{2Lf_s}{R_0} > \frac{(1-D)D}{G_{VCCM}} \tag{28}$$

$$K_{crit}(D) = \frac{D(1-D)}{G_{VCCM}} \tag{29}$$

From Figure 8 it is observed that at D = 0.2, the value of Kcrit is 0.07619. When K > 0.07619, the PSLSC functions in CCM and when K < 0.07619 it functions in DCM.

6. Design of PSLSC Converter and Stress Analysis

a Inductors Design

The input inductor 'L' of the converter proposed is calculated in the CCM as follows:

$$L = \frac{R_L\,(1-D)^2 D}{2(2D^2+3D+1)(1+D)f_s} \tag{30}$$

The inductor of switched inductor cell is found to be same as that of input inductor. It is expressed as

$$L_{SL1} = \frac{R_L\,(1-D)^2 D}{2(2D^2+3D+1)(1+D)f_s} \tag{31}$$

whereas the fs represents the switching frequency and R0 is the load resistance. The input inductor is also a function of frequency, load resistance and duty ratio. It is expressed as

$$L_0 = \frac{R_L(1-D)D}{2(1+D)f_s} \tag{32}$$

b Capacitor Design

The average current passing through the capacitors during their conduction period is considered and the relationship of the capacitors is obtained as follows using the Equations (11) and (12). The ripple voltage is considered as 10% of the capacitor voltage. The various capacitor expressions are as follows:

$$C_{SL1} = \frac{\left(2D^2+3D+1\right)I_0 D}{\Delta V_{cSL1} f_s (1-D)} \tag{33}$$

$$C_{SC1} = C_{SC2} = \frac{I_0 D}{\Delta V_{CSC1} f_s} \tag{34}$$

$$C_0 = \frac{I_0 D}{\Delta V_{C0} f_s} \tag{35}$$

c PSLSC converter Switch Stresses

Based on the analysis of the PSLSC converter in CCM, the switch stresses on the components are calculated and tabulated in Table 4. The parasitic factors are ignored for the convenience of calculating the voltage current stress. All the stress depends on the duty

ratio and by the proper selection of the duty ratio the efficiency can be maintained high with nominal stress on the components.

Table 4. Switch stresses of PSLSC converter.

Parameters		PSLSC Converter
Voltage stress of the diodes in switched inductor cell	D_{SL1} D_{SL2}	$\frac{V_g}{(1-D)}$
Voltage stress of the diodes in switched capacitor cell	D_{SC1} D_{SC2}	$\frac{V_g}{(1-D)^2}$
Voltage stress on switch	SW	$\frac{V_g}{(1-D)^2}$
RMS current of diodes in SL cell	D_{SL1} D_{SL2}	$\frac{I_0[1+2D][1+D]}{3[1-D]} .\sqrt{D}$
RMS current of the diodes in SC cell	D_{SC1} D_{SC2}	$\frac{2I_0}{\sqrt{1-D}} .D$
RMS current of the switch	SW	$\frac{I_0[1+2D][1+D]}{[1+D]} .\sqrt{D}$
RMS value inductor current of the PSLSC topology	L L_{SL1}	$\frac{I_0[1+D]}{[1-D]}$
	L_0	$\frac{(1-D)I_g}{[2D^2+3D+1]}$
RMS value capacitor current of the PSLSC topology	C_{SL1}	$I_0 \frac{(1+2D)}{(1+D)(1-D)} \sqrt{\frac{3-2D}{3}}$
	C_{SC1} C_{SC2}	$I_0 \sqrt{\frac{D}{1-D}}$
	C_0	$I_0 \sqrt{D}$
Average load current	R_L	$\frac{(1-D)I_g}{[2D^2+3D+1]}$

7. Dynamic Analysis of PSLSC Converter

The state space equations are used to obtain a piecewise linear model in order to describe the behavior of the converter proposed. State space equations are obtained resulting in electrical trajectories, owing to the turn ON/OFF conditions of switch and diodes. V_g and V_0 are the input and output variables, respectively. The inductor currents i_L, i_{LSL1} and i_{L0} and capacitor voltages V_{CSL1}, V_{CSC1}, V_{CSC2} and V_{C0} form the variables of the state space equations. The inductors L and L_{SL1} are selected to be of the same value while all the capacitors in the circuit are selected to be of the same value. The same value components usage results in same voltage and current across them when they are connected in series and parallel with respect to the ON/OFF condition of the switch. The inductor currents and capacitor voltages are treated as single variable with the assumption that there is no generality loss. From Figure 5, it can be observed that the inductors L and L_{SL1} are in series and capacitors C_{SC1}, C_{SC2} and C_0 are in parallel, which means the currents through L and L_{SL1} are equal and the voltages of C_{SC1}, C_{SC2} and C_0 are same. Therefore, the state variables V_{CSC1}, V_{CSC2} and i_{LSL1} are invalid, while the state variables i_L, i_{L0}, V_C and V_{C0} are considered. Similarly, the voltages in capacitors C_{SC1}, C_{SC2} and C_0 are equal and the currents through L and L_{SL1} are equal as shown in Figure 4. The state variables V_{CSC1}, V_{CSC2} and i_{LSL1} are invalid, the variables i_L, i_{L0}, V_C and V_{C0} are considered. The PSLSC system is represented in a steady state with state variables i_L, i_{L0}, V_C and V_{C0} and the input-output variables V_g and V_0.

The steady-state representation of a system in general is given by

$$\dot{x(t)} = Ax(t) + Bu(t) \tag{36}$$

$$y(t) = Cx(t) + Du(t) \tag{37}$$

During the ON and OFF conditions, the state equation of the system in general form is given as follows:

$$\dot{x(t)} = A_1 x(t) + B_1 u(t) \tag{38}$$

$$y(t) = C_1 x(t) + D_1 u(t) \tag{39}$$

$$\dot{x(t)} = A_2 x(t) + B_2 u(t) \tag{40}$$

$$y(t) = C_2 x(t) + D_2 u(t) \tag{41}$$

The proposed PSLSC converter state equations during the ON and OFF conditions are given as follows:

During 'ON' condition of the switch

$$\begin{bmatrix} \dot{i_L} \\ \dot{i_{L0}} \\ \dot{v_C} \\ \dot{v_{C0}} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{2}{L_0} & \frac{-1}{L_0} \\ 0 & \frac{-1}{C} & 0 & 0 \\ 0 & \frac{-1}{C_0} & 0 & \frac{-1}{R_L C_0} \end{bmatrix} \begin{bmatrix} i_L \\ i_{L0} \\ v_C \\ v_{C0} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \\ 0 \end{bmatrix} \begin{bmatrix} v_g \end{bmatrix} \tag{42}$$

during 'OFF 'condition of the switch

$$\begin{bmatrix} \dot{i_L} \\ \dot{i_{L0}} \\ \dot{v_C} \\ \dot{v_{C0}} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-1}{3L} & 0 \\ 0 & 0 & \frac{1}{L_0} & \frac{-1}{L_0} \\ \frac{-1}{2C} & \frac{-1}{2C} & 0 & 0 \\ 0 & \frac{1}{C_0} & 0 & \frac{-1}{R_L C_0} \end{bmatrix} \begin{bmatrix} i_L \\ i_{L0} \\ v_C \\ v_{C0} \end{bmatrix} + \begin{bmatrix} \frac{1}{3L} \\ 0 \\ 0 \\ 0 \end{bmatrix} \begin{bmatrix} v_g \end{bmatrix} \tag{43}$$

the output voltage is given as

$$[V_0] = \begin{bmatrix} 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_L \\ i_{L0} \\ v_C \\ v_{C0} \end{bmatrix} + [0] \begin{bmatrix} v_g \end{bmatrix} \tag{44}$$

The generalized input to output transfer function is given as

$$\frac{V_0(S)}{V_g(S)} = C[SI - A]^{-1} B \tag{45}$$

On substituting the values for A, B, C and D matrices, the gain expression under dynamic analysis is as follows:

$$\frac{V_0(S)}{V_g(S)} = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix} \left[\begin{bmatrix} S & 0 & 0 & 0 \\ 0 & S & 0 & 0 \\ 0 & 0 & S & 0 \\ 0 & 0 & 0 & S \end{bmatrix} - \begin{bmatrix} 0 & 0 & \frac{-D'}{3L} & 0 \\ 0 & 0 & \frac{1+D}{L_0} & \frac{-1}{L_0} \\ \frac{D'}{2C} & \frac{-(1+D)}{2C} & 0 & 0 \\ 0 & \frac{1}{C_0} & 0 & \frac{-1}{R_0 C_0} \end{bmatrix} \right]^{-1} \cdot \begin{bmatrix} \frac{1+2D}{3L} \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{46}$$

where

$$A = \begin{bmatrix} 0 & 0 & \frac{-D'}{3L} & 0 \\ 0 & 0 & \frac{1+D}{L_0} & \frac{-1}{L_0} \\ \frac{D'}{2C} & \frac{-(1+D)}{2C} & 0 & 0 \\ 0 & \frac{1}{C_0} & 0 & \frac{-1}{R_0 C_0} \end{bmatrix} \tag{47}$$

$$B = \begin{bmatrix} \frac{1+2D}{3L} \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{48}$$

$$C = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix} \tag{49}$$

$$D = [0] \tag{50}$$

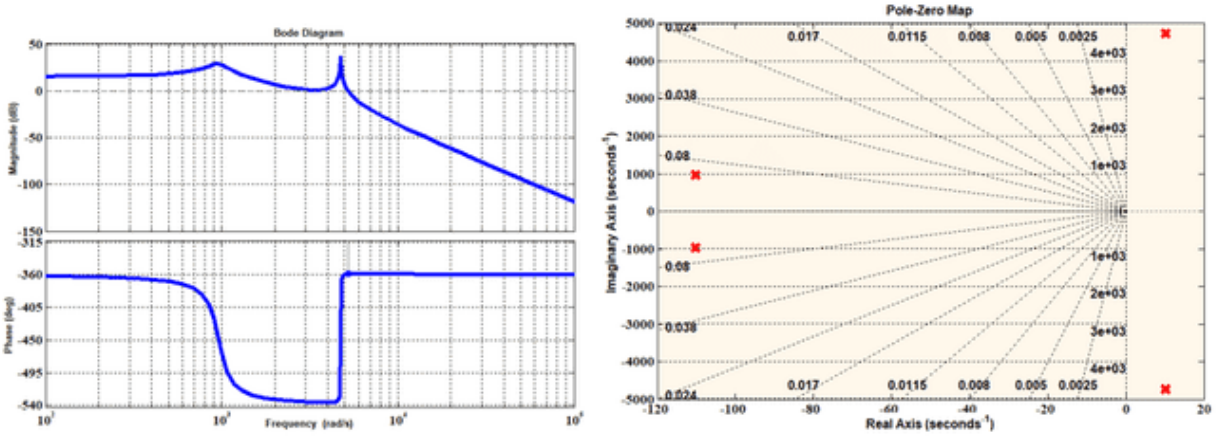
By simplifying and rearranging, the input to output transfer function is obtained as

$$\frac{V_0(s)}{V_g(s)} = \frac{\frac{(1-D)(1+2D)D'}{6LL_0CC_0}}{\frac{S^4 6LL_0CC_0R_0 + S^3 6LL_0C + S^2\left[D'^2L_0C_0R_0 + (1+D)^2 3LC_0R_0 + 6LCR_0\right] + S\left[D'^2L_0 + (1+D)^2 6L\right] + R_0D'^2}{6LL_0CC_0R_0}} \tag{51}$$

On further simplification, the transfer function of the PSLSC converter is finally obtained as

$$\frac{V_0(S)}{V_g(S)} = \frac{\frac{(1+2D)(1+D)}{(1-D)}}{\left[1 + S\left[\frac{L_0}{R_0} + \frac{6(1+D)^2L}{D'^2R_0}\right] + S^2\left[L_0C_0 + \frac{3LC_0(1+D)^2}{D'^2} + \frac{6LC}{D'^2}\right] + S^3\frac{6LL_0C}{D'^2R_0} + S^4\frac{6LL_0CC_0}{D'^2}\right]} \tag{52}$$

The transfer function in Equation (52) is used to design the voltage feedback compensation. To determine the stability of the system, the following parameters are used. *Vg* = 300 V, *Vo* = 1.8 kV, R_o = 500 Ω, D = 0.5 and f_s = 50 kHz. The reason for this operating voltage for the proposed converter is that the converter is designed for food processing applications. The power rating of this application is around 50–100 W. The bode plot and pole-zero map of the transfer function given in Equation (52) is given in Figure 9. It can be found from the plot and map that the system is not stable and the selection of a suitable converter can make the system stable. Red cross denotes the poles in the map.



(**a**) (**b**)

Figure 9. Dynamic analysis (**a**) bode plot of input to output transfer function; (**b**) pole-zero map of input to output transfer function.

8. Efficiency Analysis

This section discusses the proposed converter efficiency. Figure 10 shows the equivalent circuit of the proposed converter. The internal resistances of the diodes DSL1, D_{SL2}, D_{SC1} and D_{SC2} are represented as R_{fDSL1}, R_{fDSL2}, R_{fDSC1} and R_{fDSC2}, respectively. The ESR of the inductors L, L_{SL1} and L_0 are represented as R_L, R_{LSL1} and R_{L0}. Similarly, ESR of capacitors C_{SL1}, C_{SC1}, C_{SC2} and C_0 are represented as R_{CSL}, R_{CSC1}, R_{CSC2} and R_{C0}, respectively. The 'ON' state resistance of the switch is denoted as R_{SW}.

The power loss on the switch is denoted as PSW and it is given as

$$P_{SW} = P_{SW(conduction)} + P_{SW(switching)} \tag{53}$$

$$P_{SW(conduction)} = \frac{I_0^2(1+2D)^2(1+D)^2DR_{DS(on)}}{(1-D)^2} \tag{54}$$

$$P_{SW(switching)} = \frac{f_s C_0 V_{max}^2}{2} = \frac{f_s C_0 V_g^2 (1+2D)^2}{2(1-D)^2} \quad (55)$$

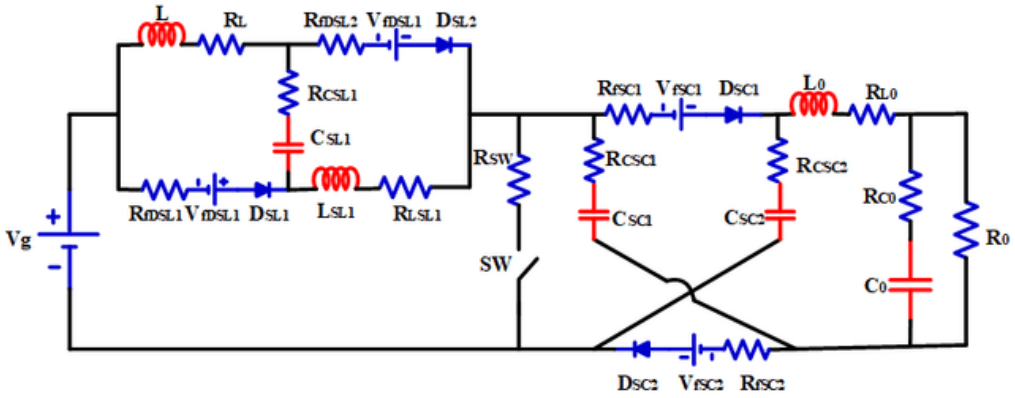


Figure 10. Equivalent circuit of PSLSC converter.

The power losses on the diodes are given as PD and PD as follows:

$$P_D = \frac{2I_0(1+2D)(1+D)DV_F}{3(1-D)} + 4I_0\,DV_F + \frac{2I_0^2(1+D)^2(1+2D)^2}{9(1-D)^2}DR_F + \frac{4I_0^2D^2}{1-D}R_F \quad (56)$$

P_L and P_C denotes the inductor and capacitor loss and is given as

$$P_L = \frac{2[I_0\,(1+D)]^2 R_L}{(1-D)^2} + I_0^2 R_L \quad (57)$$

$$P_C = \left[\frac{I_0^2(1+2D)^2(1+D)^2(3-2D)(1+D)DV_F}{3(1-D)^2} + \frac{2I_0^2 D}{(1-D)} + I_0^2\,D\right]R_C \quad (58)$$

The total power loss (PLOSS) in the converter is given as

$$P_{LOSS} = P_{SW} + P_D + P_L + P_C \quad (59)$$

The efficiency (η) of the proposed high step-up converter is given by

$$Efficiency = \eta = \frac{P_0}{P_{in}} = \frac{1}{1+(\frac{P_{LOSS}}{P_0})} \quad (60)$$

9. Comparative Study

Table 5 presents the comparison of the proposed converter and other DC–DC converters developed recently in terms of voltage gain, component count, extendibility and switch count. Figure 11 demonstrates the voltage ratio versus the duty cycle for the converters in [51–56]. It is clear that the boost ratio of the converter PSLSC is higher when compared with the converters in [52–56]. This characteristic feature makes the converter PSLSC much more suitable for step-up application in a higher range. At the expense of a higher component quantity, the converters [51–56] are shown to have a high voltage gain compared with the proposed topology. For instance, the [53] has a single switch topology as that of the proposed one but the extendibility and boost ratio is less when compared with the proposed converter. Though a converter [54] offers extendibility, it has more switch counts and switch stresses than the PSLSC converter.

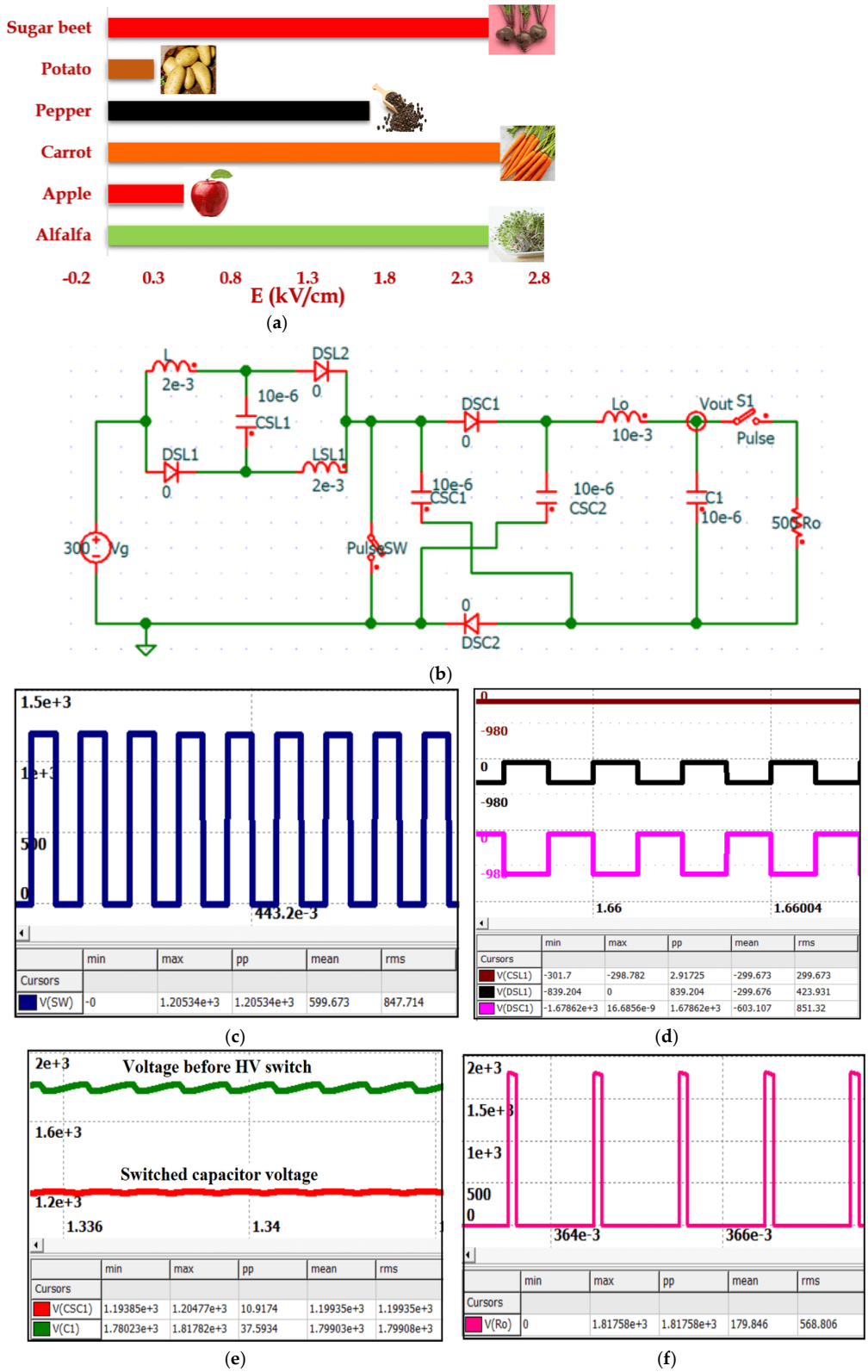


Figure 11. (**a**) Required electric field in kV/cm for food processing; (**b**) simulation circuit of PSLSC converter; (**c**) voltage across the switch; (**d**) voltage across the capacitor of the switched inductor cell (VSCL1), voltage across the diode of the switched inductor cell (VDSL1), voltage across the switched capacitor diode (VDSC1); (**e**) the voltage before the high voltage switch (SW) and voltage across the switched capacitor cell (VCSC1); (**f**) high voltage pulse across the load (RL).

Table 5. Comparison of PSLSC converter and existing high gain converters.

Converter	Voltage Gain	Component Count				Extendable	Single Switch Topology
		Sw	D	L	C		
Proposed converter	$\frac{(1+2M_{SL}D)(1+M_{SC}D)}{1-D}$	1	$2(M_{SL} + M_{Sc})$	$M_{SL} + 2$	$1 + M_{SL} + 2M_{Sc}$	Yes	✓
APIC converter [54]	$\frac{1+(n+1)D}{1-D}$	n + 2	2n	n + 2	1	Yes	X
ASLPSC converter [55]	$\frac{1+3D}{1-D}$	2	2	3	3	No	X
Modified sepic [52]	$\frac{1+3D}{1-D}$	2	2	3	3	No	X
SH-SLC converter [56]	$\frac{1+3D}{1-D}$	2	7	4	1	No	X
Switched inductor [51]	$\frac{3-D}{1-D}$	2	3	2	3	No	X
Boost with VM cell [53]	$\frac{2+D}{1-D}$	1	4	2	5	No	✓

10. Simulation Results

A simulation circuit is designed with the rating of 65 W and 1.8 kV output voltages. From the Expressions (34)–(39), the values of inductors and capacitors are calculated as given in Table 6. Table 6 gives the chosen design specifications of the proposed converter. This simulation analysis is performed to validate that the PSLSC converter is suitable for pulsed electric field (PEF) in the food industry. For vegetable tissue drying, the required pulsed electric field is 0.5–5 kV/cm. In this aspect, we have assumed the distance between the electrode as 1 cm and the area of the plate as 1 cm^2. With these specifications, the equivalent resistance of the sample to be dried is calculated as 500 Ω (1 cm/(2000 μs/cm × 1 cm^2)).

Table 6. Design parameters of PSLSC converter.

Sno	Parameters	Values
High gain converter-Specifications		
1	Input voltage	300 V
2	Output voltage	1.8 kV
3	Duty cycle	0.5
4	Switching frequency	50 kHz
5	Gain	6
6	Inductor	2 mH, 10 mH
7	Capacitor	10 μF
8	Load resistance	500 Ω
HV switch specification		
9	Switching frequency	300 V
10	Pulse width	1.8 kV
11	Repetitive pulse rate	0.5
12	Duty cycle	50 kHz

The simulation is carried out in an nl5 simulator. The reason for choosing the output voltage of the converter as 1.8 kV is illustrated in Figure 11a. For vegetable and fruit juice expression and tissue drying, the required high voltage pulses ranges from 0.3 to 5 kV. Figure 11b shows the simulation circuit with the design values of each of the components exactly as used in the simulator. The obtained output voltage, switch and diodes' stress in terms of voltage are given in Figure 11c–f.

Figure 11e presents the regulated voltage obtained from the PSLSC converter with 300 V input voltage and a gain of six. A high voltage switch is used to chop this regulated

dc voltage with a 10% duty cycle and a switching frequency of 1 kHz. The repetitive high voltage pulse is presented in Figure 11f.

Table 7 presents the comparative result which depicts the validation of theoretical study with the simulation results. From this table, it is clear that the voltage rating of the components in the converter is lesser than the output voltage with the single SL and SC cells. In this case, if the SL and SC cells are extended to generate high voltage pulses then the voltage rating of the components will be further reduced due to the division of the voltage in the components. The efficiency of the converter is noted to be 93% for this rating. Figure 12 shows the comparison of the proposed PSLSC converter with the converters in [33,58] to highlight the advantage of the converter.

Table 7. Comparison of simulation and theoretical results.

Sno	Parameters	Theoretical Formulae	Theoretical Results	Simulation Result
1	Output voltage	$\frac{V_g(1+2D)(1+D)}{1-D}$	1.8 kV	1.8 kV
2	Switched capacitor voltage	$\frac{V_g(1+2D)}{1-D}$	1.2 kV	1.19 kV
3	Switch voltage	$\frac{V_g(1+2D)}{1-D}$	1.2 kV	1.19 kV
4	Capacitor in switched inductor cell	V_g	300 V	299.6 V
5	Average diode voltage in switched inductor cell	$\frac{V_g(D)}{1-D}$	300 V	299.6 V
6	Average diode voltage in switched capacitor cell	$\frac{V_g(1+2D)D}{1-D}$	600 V	603 V

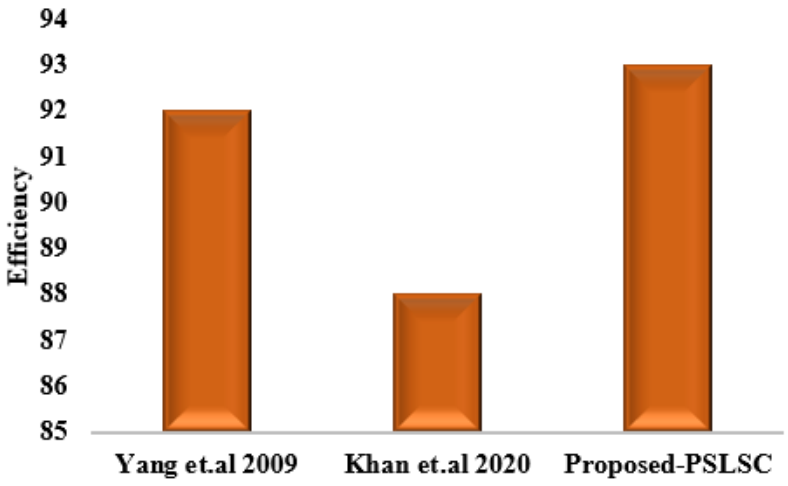


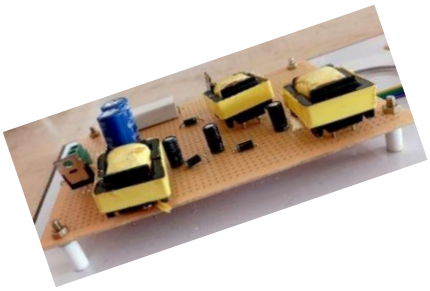
Figure 12. Efficiency comparison at the rated power [33,57].

11. Experimental Results

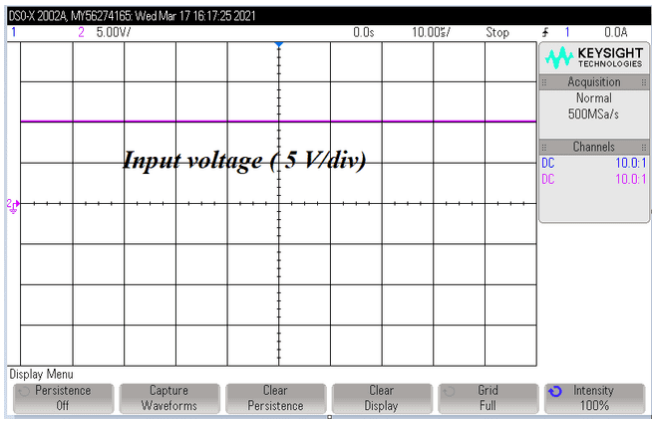
The proposed PSLSC converter is tested for its design effectiveness for a 10 V input voltage and a 42 V output with 50 W to verify the theoretical analysis in CCM mode of the operation. The list of hardware components taken for the construction of prototype is given in Table 8. The prototype is scaled down and tested to confirm the potential ability of the proposed PSLSC high voltage pulse generator. The photograph of the experimental setup with the results obtained is presented in Figure 13a–h. the pulse generator is fed with the input voltage of 10 V and it operates with the duty cycle of 0.4 to generate the output voltage of 42 V. Pulsed output voltage is obtained with a 10-microsecond pulse width and the obtained data are presented in Figure 13b.

Table 8. Hardware Specifications of PSLSC converter.

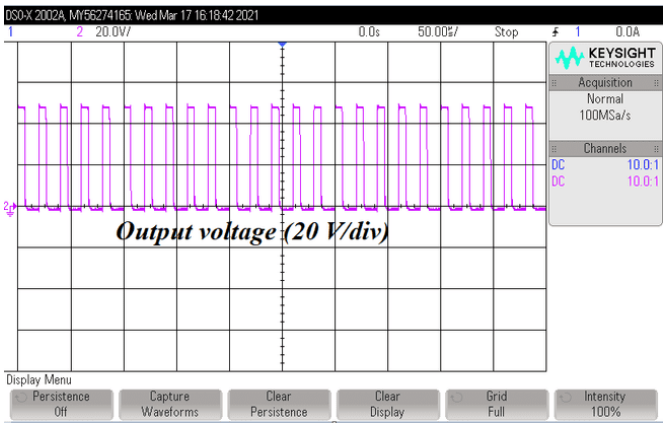
Sl.no	Parameters	Values	Prototype Tested
	PSLSC converter-Specifications		
1	Input voltage	10 V	
2	Output voltage	42 V	
3	Duty cycle	0.4	
4	Switching frequency	50 kHz	
5	Gain	4.2	
6	Inductor	15 µH, 50 µH	
7	Capacitor	10 µF	
8	Power rating	40 W	
	HV switch specification		
9	Switching frequency	50 kHz	
10	Pulse width	10 µs	
11	Repetitive pulse rate	50,000/s	



From the results obtained from the prototype, it is more obvious that the scaled down prototype generates the desired voltage required for the mentioned application. It generates the pulse with the width of 10 µs and a repetition rate of 500 per second. The operation of switched inductor cell is validated with the results obtained across the L and LSL1. This is verified with the results illustrated in Figure 13e,f. These two inductors are parallelly charged and discharged serially at the ON and OFF conditions of the switch.



(**a**)



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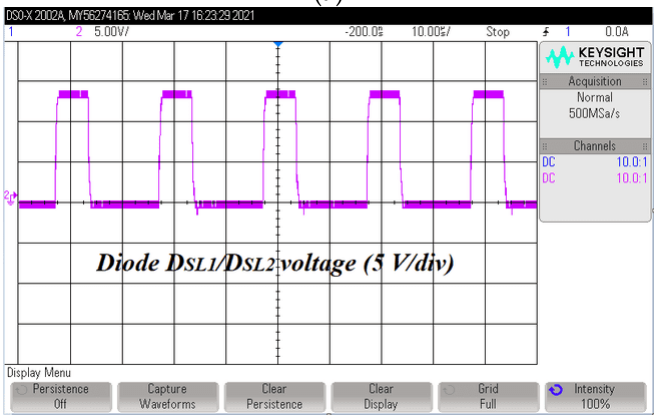
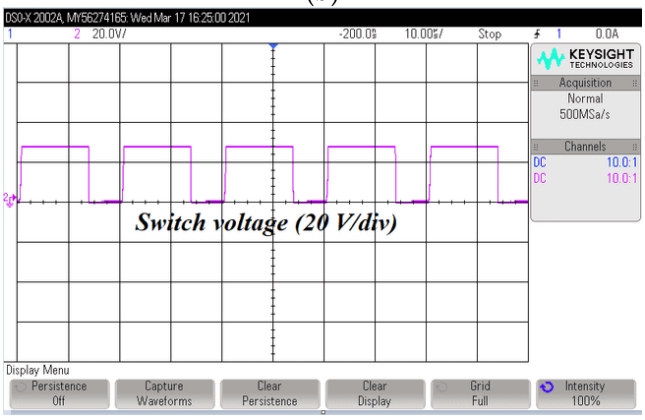
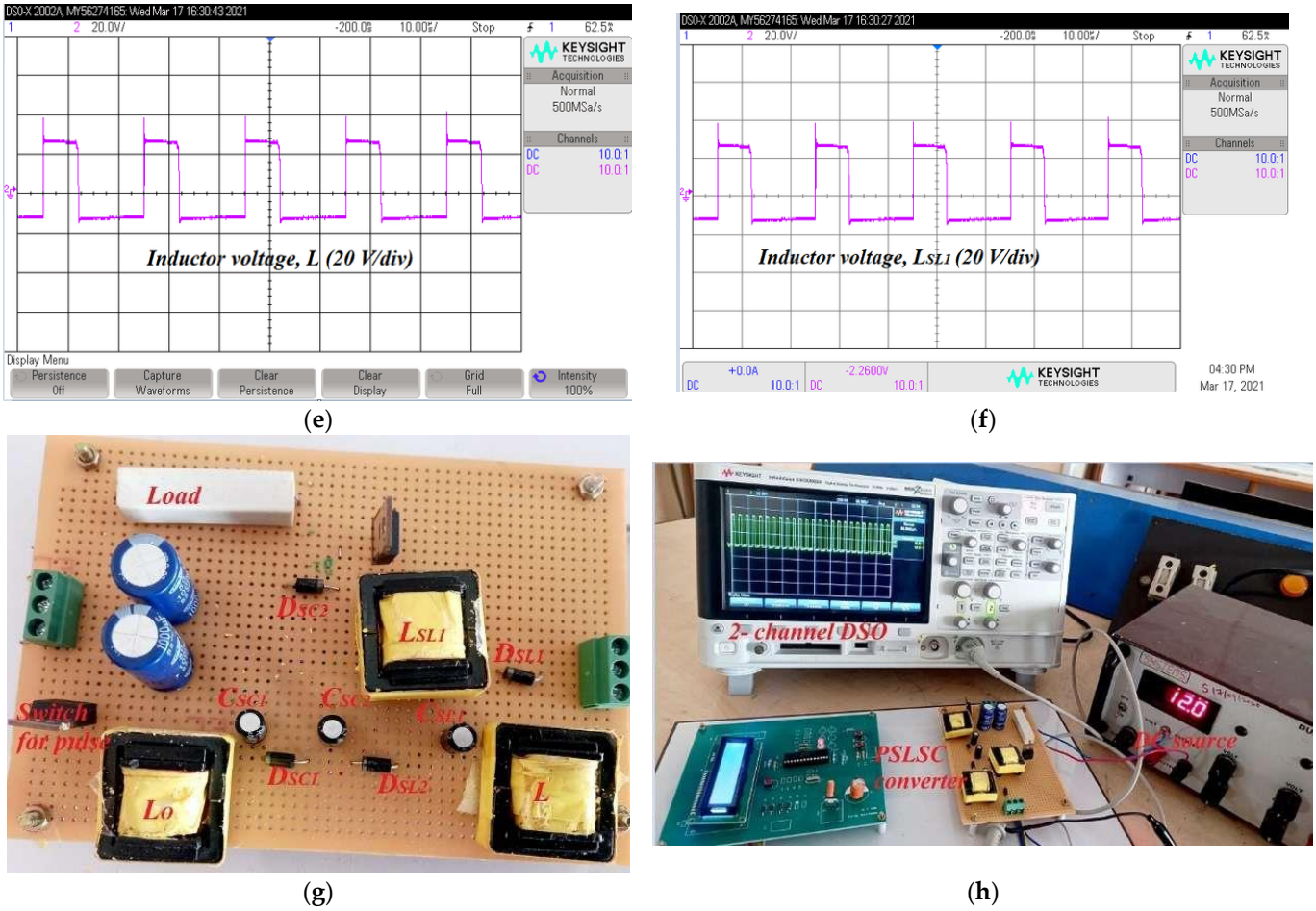


(**c**)



(**d**)

Figure 13. *Cont.*



(**e**) (**f**)

(**g**) (**h**)

Figure 13. (**a**) input voltage; (**b**) output voltage; (**c**) diode voltage; (**d**) switch voltage; (**e**) inductor L voltage; (**f**) inductor LSL1 voltage; (**g**) converter setup; (**h**) entire setup.

12. Conclusions

In this paper, a high voltage pulse generator is proposed for food processing which can be used for mechanical extraction, solid-liquid extraction, dehydration, freezing, etc. The design steps involved in this topology are presented. Steady-state and dynamic study is performed in a continuous conduction mode and the necessary waveforms are presented. It is noted that the topology has an attractive feature of extendable capability for increasing the voltage gain. This topology is also more suitable to domestic use if it is presented with multiple SL and SC cells and it can be integrated with the available standard voltage source in the domestic location. Furthermore, the converter can employ lower rating components with the integration of multiple cells with the feature of extendibility. This feature allows us to generate high voltages in a kV range with low voltage components. To meet up to the high voltage need of practical food processing applications, the number of multiplier stages need to be increased. This increases the number of components, cost and thereby the weight of the converter. However, the operation of the circuit is simple as it is a single switch topology. High rated switches need to be selected when the numbers of converter stages are increased for higher voltage applications and operations.

Dynamic study is performed using state–space analysis and the inference from the frequency response is discussed. The efficiency of the converter is observed to be 93%. A simulation study is performed with 1.8 kV, 65 W rating to generate a repetitive high voltage pulse at 500 pulses/second with a 100 µsec pulse width. Finally, a scaled down prototype is tested with a 50 W rating and the repetitive pulse is obtained with 42 V. The way to perform the MPPT action for the proposed converter is the future scope.

Author Contributions: Conceptualization, P.S., J.D.N., A.L. and J.S.; methodology, J.D.N., P.S.; software, J.D.N. and A.L.; validation, J.D.N. and P.S.; formal analysis, A.L., R.Z., F.A.E. and J.S.; investigation, J.D.N., R.Z. and F.A.E.; resources, P.S., J.D.N., A.L. and J.S.; data curation, J.D.N., A.L. and J.S.; writing—original draft preparation, J.D.N., R.Z., F.A.E. and A.L.; writing—review and editing, P.S. and J.D.N.; supervision, J.D.N.; project administration, J.D.N. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Data Availability Statement: All data generated or analyzed during this study are included in this article.

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

V_g	Input Voltage
V_O	Output Voltage
V_L	Inductor Voltage
V_C	Capacitor Voltage
ΔV_C	Capacitor Voltage Ripple
ΔI_L	Inductor Current Ripple
R_L	Load Resistance
D	Duty Ratio
P_{in}	Input Power
P_O	Output Power
P_{LOSS}	Power Loss
P_{SW}	Power Loss on switch
P_D	Power Loss on diode
P_L	Power Loss on inductor
P_C	Power Loss on capacitor
SC	Switched capacitor
SL	Switched inductor
R_{fDSL1}, R_{fDSL2}, R_{fDSC1}, R_{fDSC2}	Parasitic resistance of inductor
R_{LSL1},R_{L1}, R_{L0}	Parasitic resistance of capacitors
R_{CSC1}, R_{CSC2}, R_0	Parasitic resistance of diodes
H	Efficiency

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