Energies **2013**, *6*, 4246-4268; doi:10.3390/en6084246

OPEN ACCESS

energies

ISSN 1996-1073

www.mdpi.com/journal/energies

Article

Analysis and Simulation of Fault Characteristics of Power Switch Failures in Distribution Electronic Power Transformers

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Received: 5 June 2013; in revised form: 17 July 2013 / Accepted: 9 August 2013 / Published: 19 August 2013

Abstract: This paper presents research on the voltage and current distortion in the input stage, isolation stage and output stage of Distribution Electronic Power transformer (D-EPT) after the open-circuit and short-circuit faults of its power switches. In this paper, the operational principles and the control methods for input stage, isolation stage and output stage of D-EPT, which work as a cascaded H-bridge rectifier, DC-DC converter and inverter, respectively, are introduced. Based on conclusions derived from the performance analysis of D-EPT after the faults, this paper comes up with the effects from its topology design and control scheme on the current and voltage distortion. According to the EPT fault characteristics, since the waveforms of relevant components heavily depend on the location of the faulty switch, it is very easy to locate the exact position of the faulty switch. Finally, the fault characteristics peculiar to D-EPT are analyzed, and further discussed with simulation on the Saber platform, as well as a fault location diagnosis algorithm.

Keywords: electronic power transformer (EPT); open-circuit fault; short-circuit fault; cascaded H-bridge rectifier; DC-DC converter; inverter; fault characteristics

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1. Introduction

The electronic power transformer (EPT), usually referred to as power electronic transformer (PET) or solid state transformer (SST), is a new sort of power transformer, which is based on power electronic converters. The concept of EPT was first mentioned in 1970s [1], and it has attracted more and more attention in recent decades with the development of power electronic technology. In fact, a significant advantage of EPT is that the magnitude and phase angle of voltages in both the primary side and the secondary side of EPT can be controlled in real-time through power electronic converters to achieve flexible regulation of the current and power. As a result, EPT can be regarded as a power transformer with the functions of a FACTS (Flexible Alternative Current Transmission System) or DFACTS (Distribution Flexible Alternative Current Transmission System) device. It can be applied in generation, transmission and distribution systems. A unique characteristic of EPT is that the output voltage and frequency are adjustable; hence they can be set up for all kinds of applications. This means that EPT can offer a customized power supply with a particular voltage level and particular frequency without additional power transformers and frequency conversion equipment [2].

Due to the fact that an EPT consists of power electronic converters, the reliability of EPT which is always of special significance for the electric power system is dependent on those power electronic converters and power switches. Hence the fault characteristics, fault detection and protection of those power electronic converters and power switches are of great importance for EPT, whose failure could result in damage to the whole power system and loss to end user.

Faults occurring in power switches can be generally classified into short-circuit and open-circuit faults [3]. In the short-circuit fault, the fault detection and protection should be very fast and based on a hardware circuit as time between fault initiation and failure is very short [4,5]. Therefore, the protection circuits against the short-circuit fault of power switches have become a standard part integrated in the gate driver for practical industrial applications. Meanwhile, the open-circuit fault has not received so much attention yet, in spite of the fact that some methods were proposed for the diagnosis of the open-circuit fault in several power converter topologies and electric machines [6–21].

The open-circuit fault may be caused by the lifting of the bonding wires due to the thermal cycling, a driver failure, or a short-circuit fault-induced rupture [6–12]. In comparison with the short-circuit fault, the open-circuit fault will not cause the immediate shut down of the whole system, and the converter can still work in an abnormal but steady situation. Moreover, the abnormal state resulting from an open-circuit fault can lead to overstresses on the healthy switches as well as pulsating currents. This can in turn lead to failures of other components.

There have been many researches on the configuration design for EPT [22–25] and many literatures have also been studying the EPT applications in electric power system [26–30] in the past decade. Some researchers have published technical papers to address the power switch fault diagnosis problem for inverters and converters [6–12], in which some of the studies are for inverter motor drive system [7,8] and the others are for matrix converters [9–12]. However, little effort has been undertaken on analyzing the issues of fault detection, fault characteristics and protection of EPTs. A hierarchical section protection based on EPT for the Future Renewable Electric Energy Delivery and Management (FREEDM) system is proposed in [31,32]. Although the protection method is more appropriate than the conventional differential protection scheme, it only focuses on the whole micro-grid system rather

than the EPT device. So far, there are no studies conducted specially for the protection of EPTs based on their power switches.

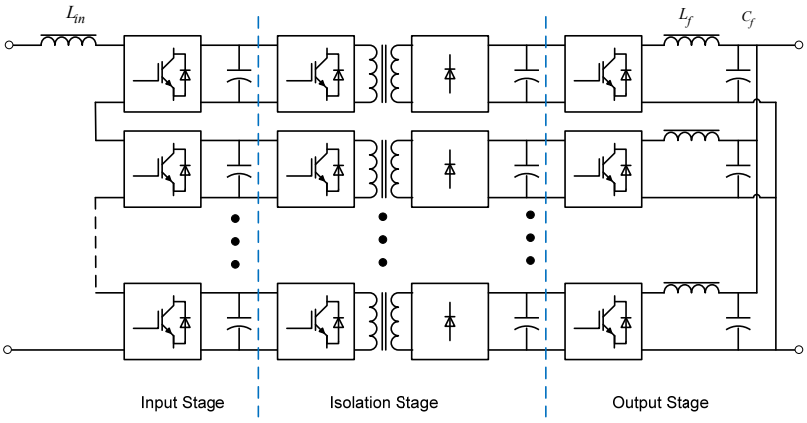
In this paper, the fault characteristics based on the power switches of EPT are proposed for fault detection and EPT protection.

Section 2 gives the topology and operational principles of the EPT, and Section 3 gives the basic control scheme of the EPT. The possible faults of EPT power switches are systematically analyzed and summarized in Section 4. In Section 5, the analysis of the possible faults is verified and further discussed with simulation in Saber. Based on the simulation results, the protection design is discussed in Section 6. Conclusions are given in Section 7.

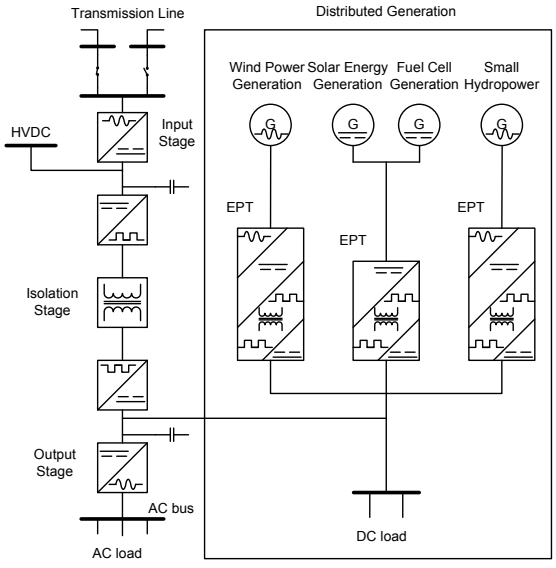
2. Configuration and Operation Principle of D-EPT

The proposed Distribution Electronic Power Transformer (D-EPT) is designed as a 3-phase and 4-wire transformer, and the basic schematic of proposed D-EPT is shown in Figure 1a. As can be seen from Figure 1a, the proposed D-EPT is composed of three main stages: an input stage, an isolation stage and an output stage.

Figure 1. (**a**) Basic schematic of proposed D-EPT and (**b**) substation based on EPT.



(**a**)



(**b**)

The input stage has multiple H-bridge rectifiers connected in cascade, which convert the input AC voltage to the DC voltages in multiple Input Stage DC buses.

The isolation stage consists of a front-end H-bridge, a High Frequency Isolation Transformer (HFIT) and a diode bridge. The DC voltage from each Input Stage DC Bus is modulated to a high frequency AC wave by a front-end H-bridge chopper, and then the high voltage and high frequency square wave is transformed through a HFIT to the low voltage high frequency square wave on the secondary side of the HFIT. The low voltage square wave is rectified as DC voltage by a diode bridge at the end of isolation stage. In other words, the isolation stage acts like an isolated DC-DC converter.

The output stage has multiple H-bridge inverters connected in parallel, which invert the DC voltage of the Output Stage DC Bus (OSDCB) to an AC sinusoidal voltage.

Figure 1b shows the EPT-based substation which can manage both AC and DC sources; hence the transmission system can connect distributed generation which includes wind power, solar energy and hydro-power. It can be seen from the block diagram that EPT has both AC links and DC links, which would reduce the room and cost of the substation by connecting them in a same substation.

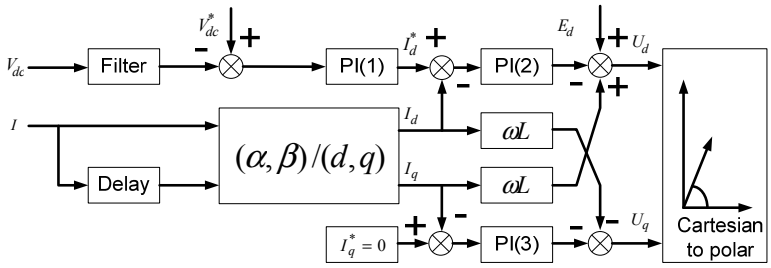
3. Basic D-EPT Control Method

The control strategy determines the performance and the fault characteristic of D-EPT due to the application of power electronic components. In this section, the control strategies of input stage, isolation stage and output stage will be discussed in detail.

3.1. Control Scheme for Input Stage

The D-EPT input stage is directly connected to the distribution power system. The input stage is also shown in Figure 1b, which is between the transmission line and HVDC bus; and its control strategy is shown in Figure 2. The main task of the control scheme is to keep the input current sinusoidal and in phase with the input phase voltage to prevent it from injecting harmonics into the grid. Hence the input power factor of D-EPT is unity, or adjustable. Furthermore, the control scheme is designed to stabilize the DC bus voltage at the desired value against the input voltage, which is always variable.

Figure 2. The input stage control strategy.



The mathematic model of the input stage can be presented in stationary *a-b-c* reference frame or synchronous rotating *d-q* reference frame, and can be given by:

$$\left[\begin{cases} L\dfrac{dI_d}{dt} = E_d - U_d + \omega L I_q \\ L\dfrac{dI_q}{dt} = -U_q + \omega L I_d \end{cases}\right] \tag{1}$$

where L is the input inductor; and ω is the synchronous angular velocity. Equation (1) indicates that there is a cross coupling between the d axis and the q axis, which would affect the dynamic performance of the system.

Figure 2 shows the control diagram of the input stage of the D-EPT, which illustrates an outer voltage loop and an inner current loop to sinusoid the input current and stabilize the DC bus voltage. It is important to mention that the DC bus voltage V_{dc} sampled for the feedback to the rectifiers is the Output Stage DC Bus (OSDCB) voltage in the isolation stage, rather than the Input Stage DC Bus (ISDCB) voltage in the input stage, and its value is the average of all the DC bus voltages of the cascaded H-bridge in one phase. Hence the isolation voltage to the DC by voltage sensors will be reduced from 10 to 400 V, which can greatly reduce the cost.

3.2. Control Scheme for Isolation Stage

The DC bus voltage in the input stage is modulated to a high frequency square wave by the chopper circuit of the isolation stage. The high voltage high frequency square wave is then demodulated to a low voltage high frequency square wave on the secondary side of the HFIT, and finally rectified to DC voltage in Output Stage DC Bus by the diode bridge.

To simplify the design of the control system, open-loop PWM (Pulse Width Modulation) control is applied to the front-end H-bridge chopper. Therefore, the isolation stage can be taken as a proportional amplifier without close-loop control. And the simplified model of the isolation stage can be shown by:

$$V_{dc2} = k \times V_{dc1} \tag{2}$$

where k is the transformer ratio; V_{dc1} and V_{dc2} are the voltages of ISDCB and OSDCB, respectively.

3.3. Control Scheme for Output Stage

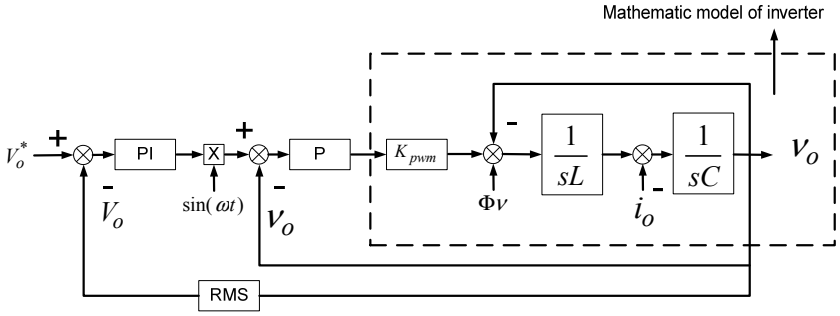
As mentioned before, there are multiple inverters connected in parallel in the output stage, and all inverters share the same triggering signal which is to meet the requirement of the loads. Hence the mathematic model for single phase can be given by:

$$\begin{cases} C_f \times \dfrac{dv_o}{dt} = i_L - i_o \\ L_f \times \dfrac{di_L}{dt} = v_i - v_o \end{cases} \tag{3}$$

where C_f and L_f are the capacitor and inductor of the output filter; v_i and i_L as well as v_o and i_o are the voltage and current at the input as well as output of the output filter, respectively.

As the loads to the distribution system are always regarded as a passive system, a constant AC voltage control based on instantaneous value feedback is applied. The control strategy of one phase of the output stage is shown in Figure 3.

Figure 3. The output stage control strategy.



4. Multiple Faults in D-EPT

This section discusses the effects to the electric circuit under various fault conditions for EPT which is shown in Figure 1a. Figure 4 illustrates the most common faults associated with the power electronic components and load, including open-circuit and short-circuit faults of IGBT to the H-bridge with its anti-parallel diode and rectifier diode.

Figure 4. Possible faults of power switches of the EPT.

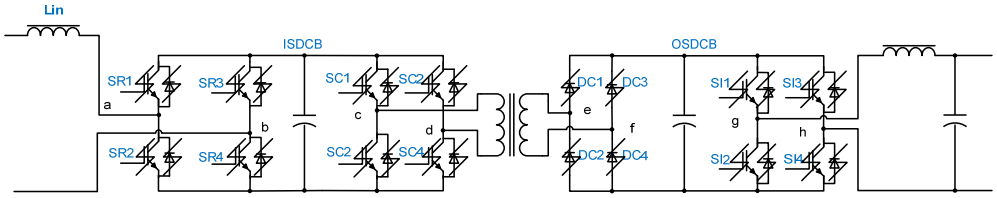
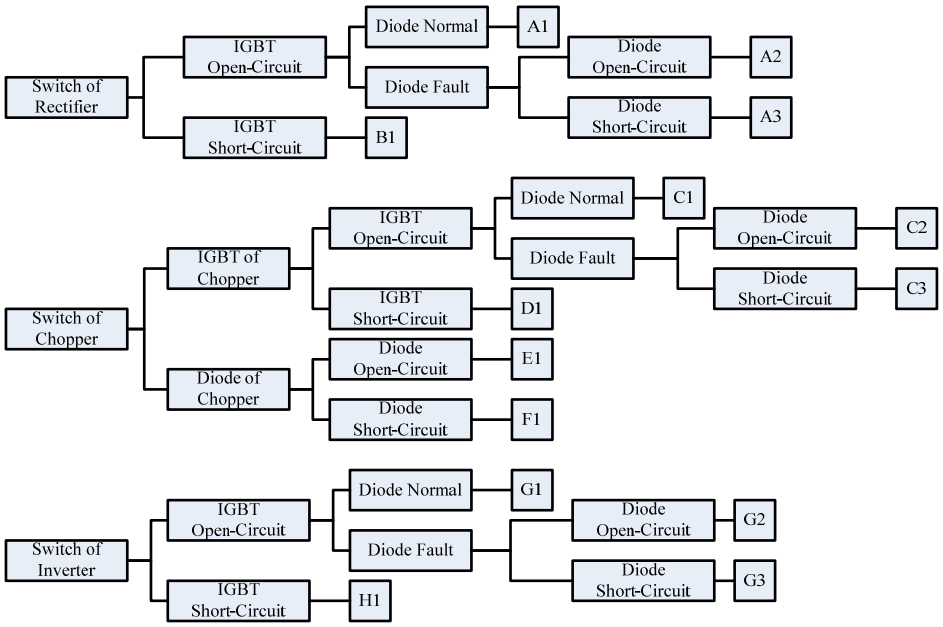


Figure 5 lists all kinds of faults of the power switches of EPT including IGBT and diodes of the rectifiers (input stage), choppers (isolation stage) and inverters (output stage). The fault cases are numbered with A1, A2, ..., H1, and their details discussed below.

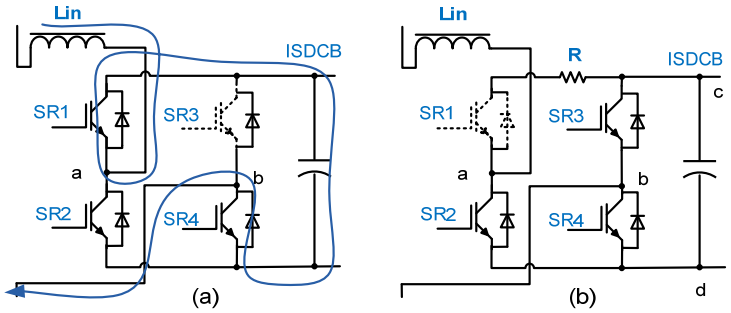
Figure 5. Catalogue of fault cases.



A1. Rectifier IGBT Open-Circuit with Anti-Parallel Diode Normal

By applying unipolar PWM to the rectifier, the fault to any single IGBT will lead to same consequence. If the open-circuit fault happens on the IGBT (such as SR3) with its anti-parallel diode normal, the current could pass through the anti-parallel diode of SR3 from b point to the ISDCB, although blocked from ISDCB to b point. Hence the current could not pass in the input inductor Lin through SR1 and SR3 in the positive half-cycle of source voltage; instead, the current will charge ISDCB capacitor through the anti-parallel diodes of SR1 and SR4, shown in Figure 6a. As a result, the failure rectifier will work differently compared to the three other rectifiers, which results in an unbalance in the ISDCB voltage.

Figure 6. Schematic diagrams of input stage for (**a**) Fault A1 (IGBT SR3 open-circuit) and (**b**) Fault A2 (IGBT SR1 and its body diode open-circuit).



A2. Rectifier IGBT and Its Anti-Parallel Diode both Open-Circuit

First of all, if the open-circuit fault happens on both SR1 and its anti-parallel diode, which is shown in Figure 6b, the current is neither able to charge the ISDCB capacitor nor to flow in the input inductor Lin through SR1. As the energy transferred to the ISDCB capacitor is reduced, the OSDCB voltage will be reduced simultaneously.

Moreover, according to Kirchhoff's Voltage Law (KVL), when no fault happens, the voltage across the SR2 can be shown by:

$$V_{SR2} = V_{da} = V_s + L_{in}\frac{di}{dt} = V_{ISDC} \tag{4}$$

where V_s is the source voltage; $L_{in}\frac{di}{dt}$ is the voltage of the input inductor; and V_{ISDC} is the ISDCB voltage, which equals the voltage across the IGBT SR2.

When the open-circuit fault happens, the loop of the current to charge the inductor and ISDCB capacitor are both incomplete. As the open-circuit model for an IGBT is a normal IGBT in series with a resistor, which can be seen from Figure 6b, the voltage across the SR2 can be shown by:

$$V_{SR2} = V_{da} = V_s + L_{in}\frac{di}{dt} = V_{ISDC} + V_R \tag{5}$$

where V_s is the source voltage; $L_{in}(d_i/d_t)$ is the voltage of the input inductor; V_R is the voltage across the equivalent resistor of the failure IGBT SR1; and V_{ISDC} is the ISDCB voltage. Due to the effect of the

equivalent resistor of the failure IGBT SR1, the current through the SR1 is greatly reduced, hence the voltage of the input inductor $L_{in}(d_i/d_t)$ is greatly increased. As a result, the voltage across the IGBT SR2 is much higher than the ISDCB voltage, which will cause over voltage on the IGBT SR2.

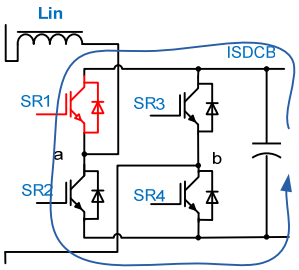
A3. Rectifier IGBT Open-Circuit with Its Anti-Parallel Diode Short-Circuit

The diode short-circuit fault equals to IGBT short-circuit one, and its details are discussed in fault B1.

B1. Rectifier IGBT Short-Circuit with Anti-Parallel Diode Normal

If SR1 is short-circuited, the ISDCB capacitor will be short-circuited through SR1 and SR2, as SR2 is turned on and SR1 is short-circuited, which is shown in Figure 7. Hence the SR1 and SR2 will both be over current. As a result, the ISDCB voltage will greatly decrease like the OSDCB voltage, as no energy would have been transferred to the DC bus capacitor.

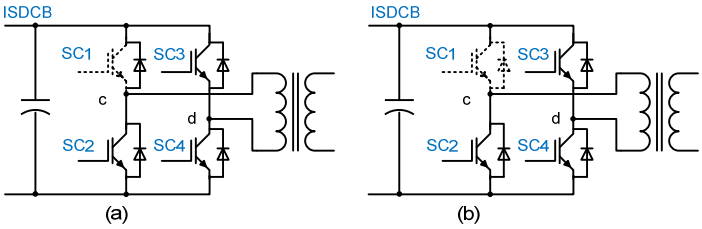
Figure 7. Schematic diagrams of input stage for fault B1 (IGBT SR1 short-circuit).



C1. Chopper IGBT Open-Circuit with Anti-Parallel Diode Normal

If SC1 is open-circuited, the energy cannot be transferred through SC1 and SC4 to the secondary side of the HFIT, which is shown in Figure 8a. However, the circuit can work as a two-switch forward converter that the anti-parallel diodes of SC1 and SC4 work as free-wheeling diodes when SC2 and SC3 are turned off. Hence the anti-parallel diodes prevent the magnetic flux build-up from one cycle to next. As a result, the full-bridge chopper becomes a half-bridge chopper.

Figure 8. Schematic diagrams of isolation stage for (**a**) Fault C1 (IGBT SC1 open-circuit) and (**b**) Fault C2 (IGBT SC1 and its body diode open-circuit).



C2. Chopper IGBT and Its Anti-Parallel Diode both Open-Circuit

As shown in Figure 8b, with the fault C2, the circuit will not work properly since its magnetizing current will not be allowed to reset to zero, as the magnetizing current has no place to discharge its

value when SC1 and its anti-parallel diode are both open-circuit. Hence, it will cause the magnetizing current to continuously increase linearly until it finally saturates the core.

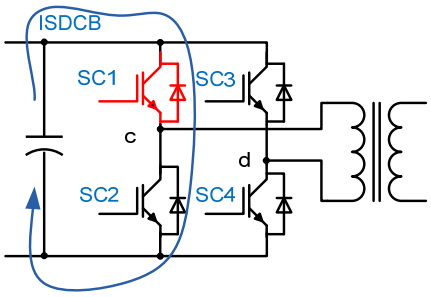
C3. Chopper IGBT Open with Its Anti-Parallel Diode Short-Circuit

The diode short-circuit fault equals to IGBT short-circuit one, and its details ARE discussed in fault D1.

D1. Chopper IGBT Short-Circuit

If SC1 is short-circuited as shown in Figure 9, the ISDCB capacitor will be shorted through SC2 and the shorted SC1. Hence the SC1 and SC2 will be over current and the ISDCB voltage will decrease greatly. As the circuit could not transfer energy through the HFIT, the OSDCB voltage will also decrease greatly. The primary side of HFIT may also fail if its coil is shorted, and the consequence is as same as the Chopper IGBT short-circuit fault.

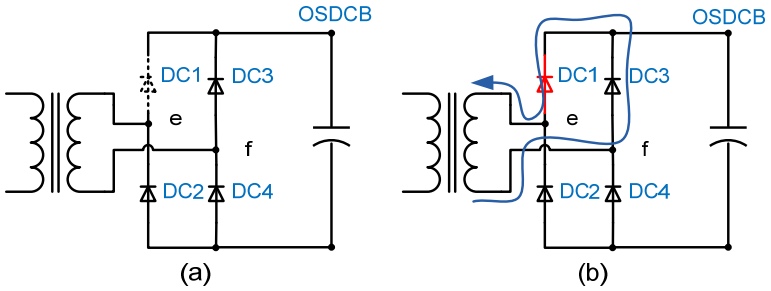
Figure 9. Schematic diagrams of isolation stage for fault D1 (IGBT SC1 short-circuit).



E1. Chopper Rectifier Diode Open-Circuit

If DC1 is open-circuited as shown in Figure 10a, the HFIT current could not charge the OSDCB capacitor through DC1 and DC4, which changes the full-bridge diode rectifier into a half-bridge diode rectifier. As a result, the current which is supposed to pass through DC1 and DC4 will go through DC2 and DC3 instead. The additional current to DC2 and DC3 might cause over current on them, as well as IGBTs of the chopper at the primary side of the HFIT.

Figure 10. Schematic diagrams of isolation stage for (**a**) Fault E1 (diode DC1 open-circuit) and (**b**) Fault F1 (diode DC1 short-circuit).



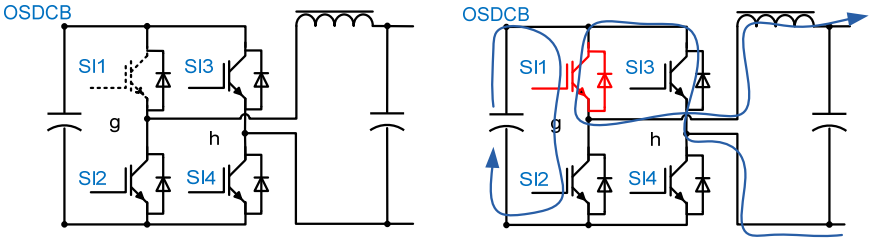
F1. Chopper Rectifier Diode Short-Circuit

If DC1 is short-circuited as shown in Figure 10b, the secondary side of the HFIT will be short-circuit through DC3 and the shorted DC1, as well as the primary side of the HFIT. Hence the OSDCB voltage will decrease as no energy will be transfer during that interval. Moreover, the DC1 and DC3 will be over current due to the short-circuit fault, as well as IGBTs of the chopper at the primary side of the HFIT. The secondary side of HFIT may also fail if its coil is shorted, and the consequence is as same as Chopper diode short-circuit fault.

G1. Inverter IGBT Open-Circuit with Its Anti-Parallel Diode Normal

If SI1 is open-circuited, the inverter could not generate positive pulses for the output voltage, shown in Figure 11a. Due to the fact that all four inverters in parallel share the gate drive signal and control system, the output current of failure inverter will be different from the remaining three ones.

Figure 11. Schematic diagrams of output stage for (**a**) Fault G1 (IGBT SI1 open-circuit) and (**b**) Fault H1 (IGBT SI1 short-circuit).



G2. Inverter IGBT and Its Anti-Parallel Diode Are both Open-Circuit

If SI1 and its anti-parallel diode are both open-circuit, the consequence is similar to the G1 fault.

G3. Inverter IGBT Open-Circuit with Its Diode Short-Circuit

The diode short-circuit fault equals to IGBT short-circuit one, and its details is discussed in the H1 fault.

H1. Inverter IGBT Short-Circuit

If SI1 is short-circuited, the OSDCB capacitor will be short-circuited with the short-circuit current flowing through SI2 and shorted SI1. Hence the OSDCB voltages of all four inverters will decrease greatly, as their current will flow through the anti-parallel diodes of SI2 and SI3 by the output filter, as shown in Figure 11b. In other words, all four OSDCB capacitors will be short-circuited and the IGBTs including SI1, SI2, SI3 and SI4 will all be over current.

5. Simulation Results

Simulation is performed on the Saber simulation platform (The Synopsys, Mountain View, CA, USA). An EPT shown in Figure 1a boosts 5774 V input voltage (line voltage 10 kV) to 9000 V DC

voltage. The input stage has four cascaded H-bridges, with DC bus voltages of 2250 V each. The isolation stage transforms the ISDCB voltage (2250 V) to OSDCB voltage (375 V), then inverts it to a 230 V (line voltage 400 V) load voltage at the output stage. The input inductor is 30 mH, and the ISDCB capacitor and OSDCB capacitor of one module are 3 mF and 22.4 mF, respectively. With a 230 V output voltage, the load resistor is 2 ohm, hence the output power for single phase and three phase are 26.45 kW and 79.35 kW. The simulation results are summarized in Table 1, where the abbreviations "UV", "OV" "OC" and "UB" are used to indicate the under voltage, over voltage, over current, and output currents unbalance, respectively. The faults are generated by a timer which is set to be 0.8 s in the simulation, and the failure IGBTs and diodes are selected as same as in Section 3 in order to verify the analysis above. During the simulation, the selected failure IGBT will work normally from 0 to 0.8 s, and then set to be open or shorted after 0.8 s according to the timer.

Table 1. Fault case study with power switches to D-EPT.

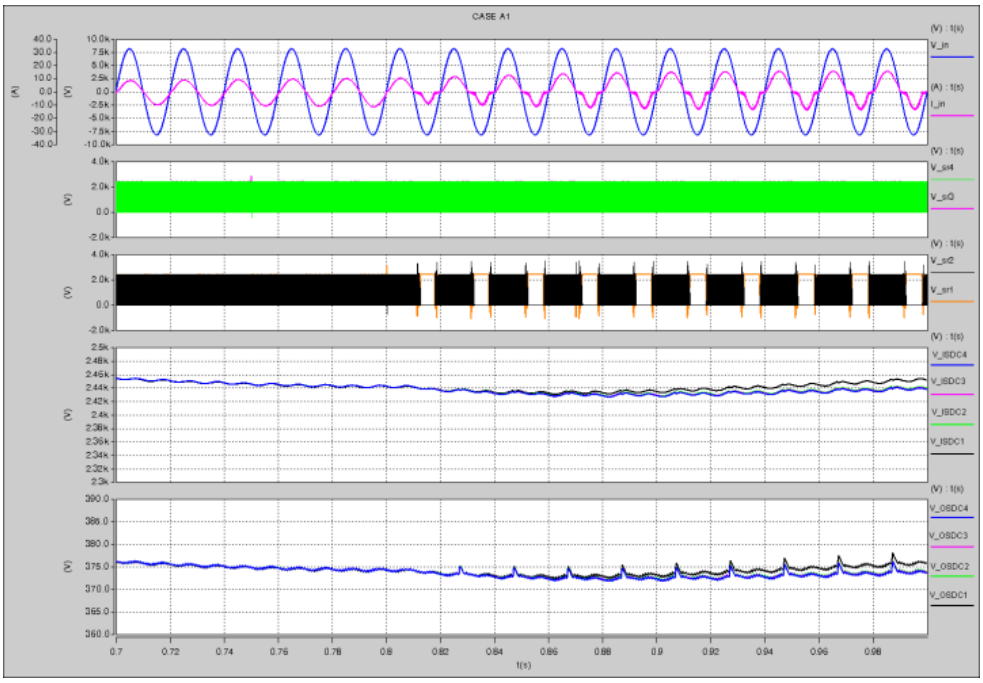
Input Stage	**A1**	**A2**	**B1**	**Isolation Stage**	**C1**	**C2**	**D1**	**E1**	**F1**	**Output Stage**	**G1**	**H1**
Input PF	<0.99	<0.99	<0.99	Input PF	0.99	0.99	<0.99	0.99	<0.99	Input PF	0.99	<0.99
I_in			OC	I_in			OC		OC	I_in		OC
ISDC1	UV	UV	UV	ISDC1			UV		UV	ISDC1		UV
ISDC2	UV	UV	OV	ISDC2			OV		OV	ISDC2		UV
ISDC3	UV	UV	OV	ISDC3			OV		OV	ISDC3		UV
ISDC4	UV	UV	OV	ISDC4			OV		OV	ISDC4		UV
OSDC1	UV	UV	UV	OSDC1			UV		UV	OSDC1		UV
OSDC2	UV	UV	OV	OSDC2			OV		OV	OSDC2		UV
OSDC3	UV	UV	OV	OSDC3			OV		OV	OSDC3		UV
OSDC4	UV	UV	OV	OSDC4			OV		OV	OSDC4		UV
SR1		OV	OC	SC1			OC		OC	SI1		OC
SR2		OV	OC	SC2			OC			SI2		OC
SR3				SC3	OC	OC		OC	OC	SI3		OC
SR4				SC4	OC	OC		OC		SI4		OC
				It_1		OC			OC	Io_1	UB	UB
				It_2						Io_2	UB	UB
				It_3						Io_3	UB	UB
				It_4						Io_4	UB	UB

A1. Rectifier IGBT Open-Circuit with Anti-Parallel Diode Normal

Figure 12 shows the A1 fault simulation results of the input voltage (V_in), input current (I_in), the voltage across the IGBTs of the failure H-bridge (V_sr1 to V_sr4), four ISDCB voltages (V_ISDC1 to V_ISDC4) and four OSDCB voltages (V_OSDC1 to V_OSDC4).

It can be observed that the V_ISDC1 and V_OSDC1 increase continuously since the IGBT fault A1 happens on 0.8 s, as well as their ripple voltages. Moreover, I_in is not sinusoidal because it could not follow the V_in due to the fault A1. However, the sum of the DC bus voltage which is the feedback to input stage control scheme remains at 9000 V.

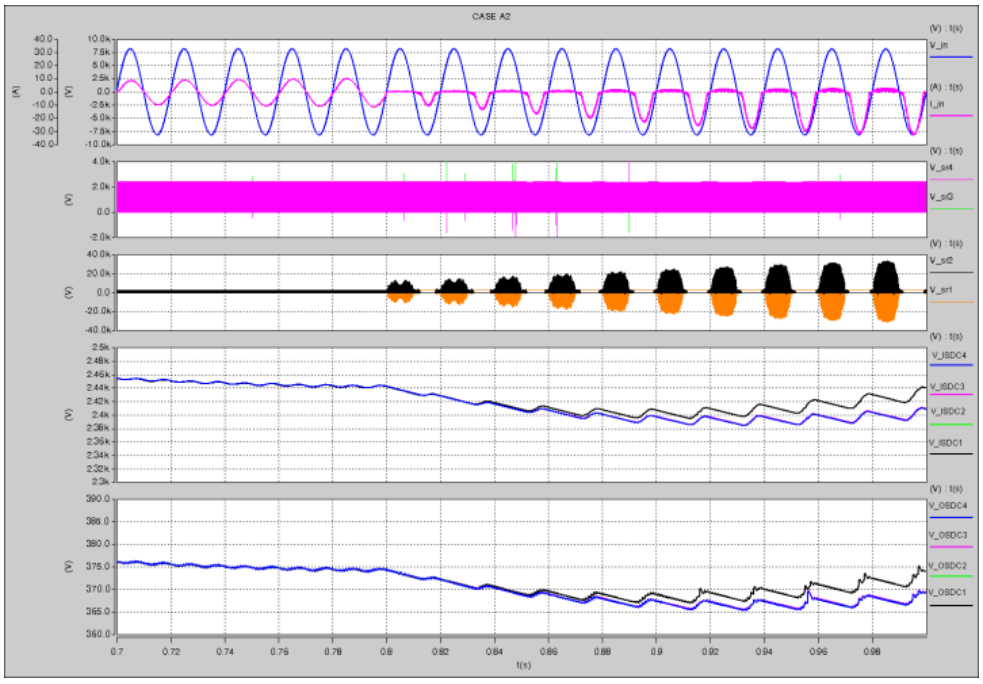
Figure 12. Simulation results of fault A1.



A2. Rectifier IGBT and Its Anti-Parallel Diode both Open-Circuit

Figure 13 shows the A1 fault simulation results of the input voltage, input current, voltage across the IGBTs of the failure H-bridge, 4 ISDCB voltages, and four OSDCB voltages.

Figure 13. Simulation results of fault A2.



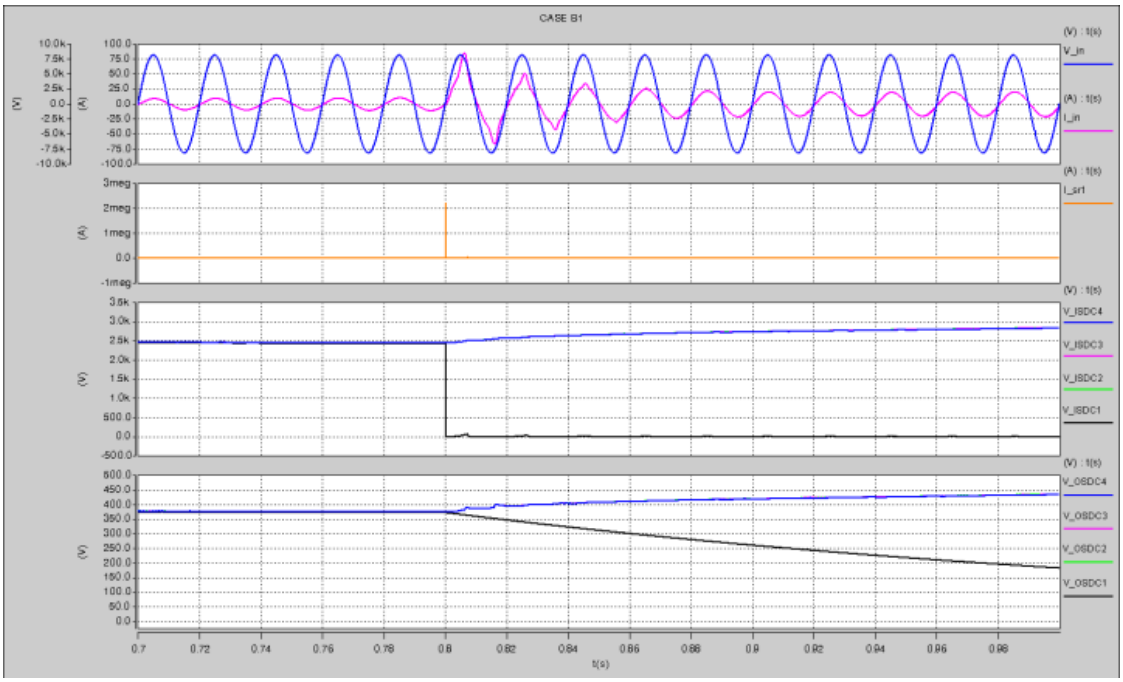
It can be seen that V_sr1 and V_sr2 are up to 50 kV and −50 kV for the maximum, which are supposed to be 2450 V such as V_sr3 and V_sr4. Hence it will cause over voltage on SR1 and SR2. At the same time, I_in is blocked at the positive half cycle of the source voltage; hence it will be

distorted from V_in, which is also shown in Figure 12. V_ISDC1 and V_OSDC1 keep on increasing after the fault happens, as well as the ripple voltages, which will cause over voltage on the ISDCB and OSDCB capacitors.

B1. Rectifier IGBT Short-Circuit with Anti-Parallel Diode Normal

Figure 14 shows the B1 fault simulation results of the input voltage, input current, the currents through the IGBTs SR1 (I_sr1), four ISDCB voltages and four OSDCB voltages. It can be seen from Figure 14 that the current I_sr1 through SR1 at the IGBT failure moment 0.8 s are almost 1 MA, which is because the ISDCB capacitor of the failure H-bridge is shorted by SR2 and shorted SR1. Meanwhile, I_in rises rapidly with its peak value approximately 400 A. Due to the short-circuit fault, V_ISDC1 decreases to 0 V immediately, which will cause ISDCB under voltage. Moreover, V_OSDC1 decreases rapidly as well, as no current will charge the OSDCB capacitor.

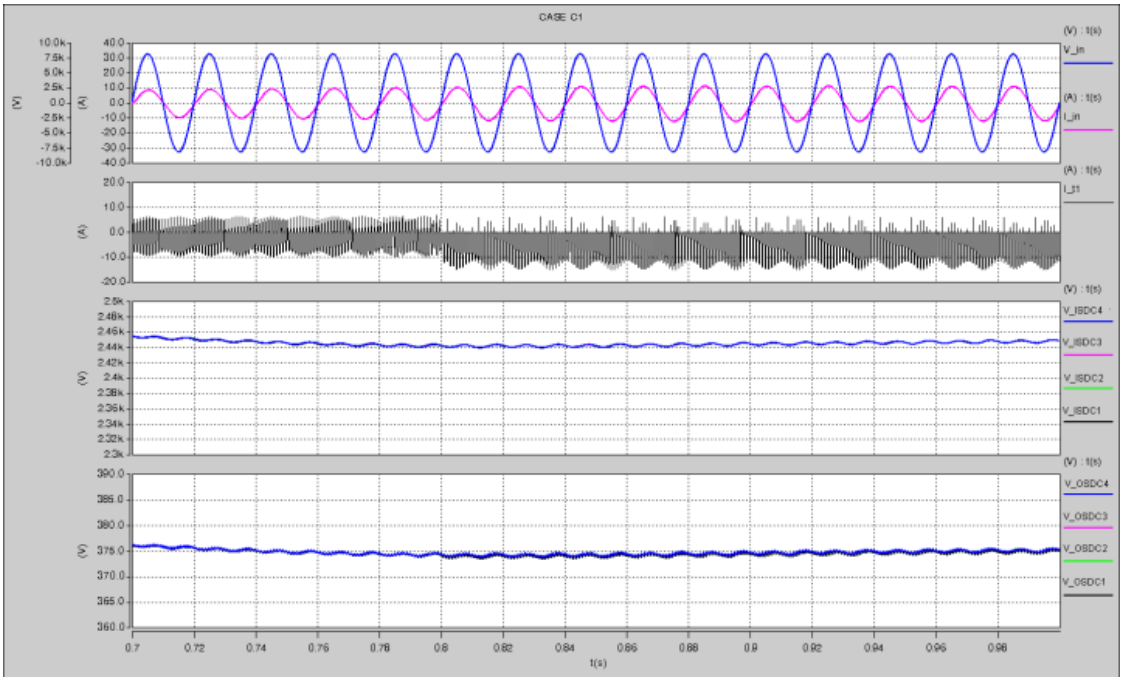
Figure 14. Simulation results of fault B1.



C1. Chopper IGBT Open-Circuit with Anti-Parallel Diode Normal

Figure 15 shows the C1 fault simulation results of the input voltage, input current, the current through the primary side of the HFIT to the failure chopper (I_t1), four ISDCB voltages, and four OSDCB voltages. It can be observed that I_t1 can only flow in one direction since the C1 fault happens at 0.8 s, as the full-bridge chopper becomes a half-bridge chopper. As the HFIT current I_t1 increases as the fault happens, it may cause over current on the IGBT.

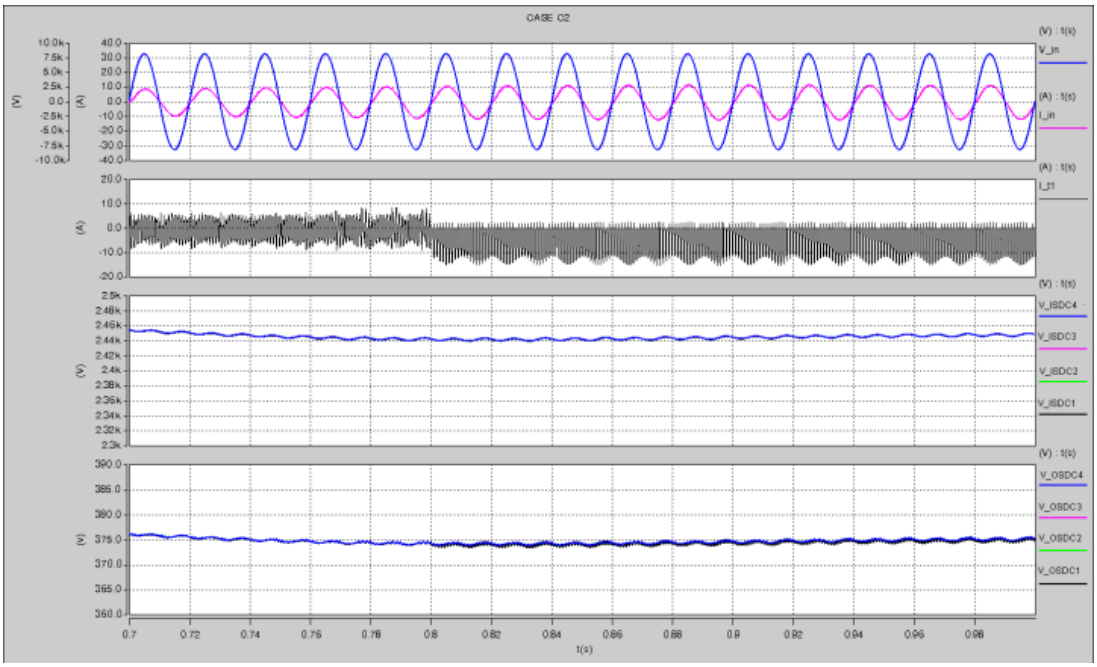
Figure 15. Simulat0ion results of fault C1.



C2. Chopper IGBT and Its Anti-Parallel Diode both Open-Circuit

Figure 16 shows the C2 fault simulation results of the input voltage, the input current, the current through the primary side of the HFIT to the failure chopper, four ISDCB voltages, and four OSDCB voltages. It can be observed that I_t1 can only flow in one direction due to the fact the C2 fault happens at 0.8 s. Unlike the C1 fault, the C2 fault left no path for the magnetizing current to discharge its value when SC1 and its anti-parallel diode are both open-circuit. Hence, I_t1 will continuously increase linearly until it finally saturates the core.

Figure 16. Simulation results of fault C2.

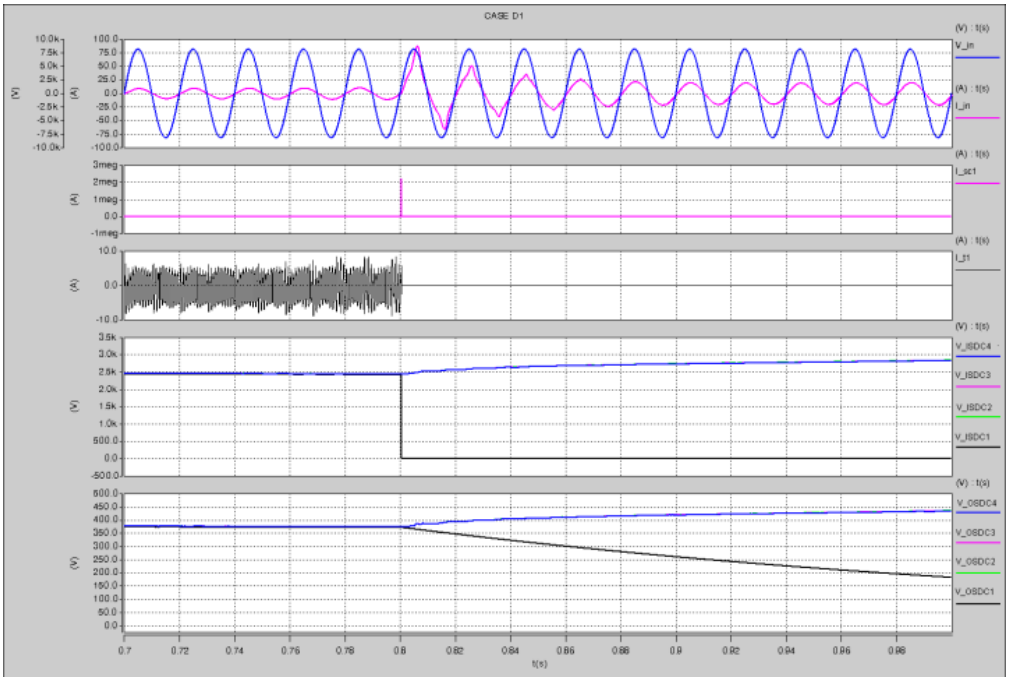


D1. Chopper IGBT Short-Circuit

Figure 17 shows the D1 fault simulation results of the input voltage, input current, the current through the shorted IGBT (I_sc1) and the one through the primary side of the HFIT to the failure chopper H-bridge, four ISDCB voltages and four OSDCB voltages.

It can be observed that I_sc1 is almost 2 MA at the moment of failure at 0.8 s, which is because the ISDCB capacitor of the failure H-bridge is shorted by SC2 and SC1 is shorted. At the same time, the I_in rises rapidly, with its peak value being approximately 75 A. Due to the short-circuit fault, V_ISDC decreases to 0 V when the fault happens, which will reduce I_t1 to 0 A. Moreover, V_OSDC1 will decrease rapidly as well, as no current will charge the OSDCB capacitor due to the short-circuit fault.

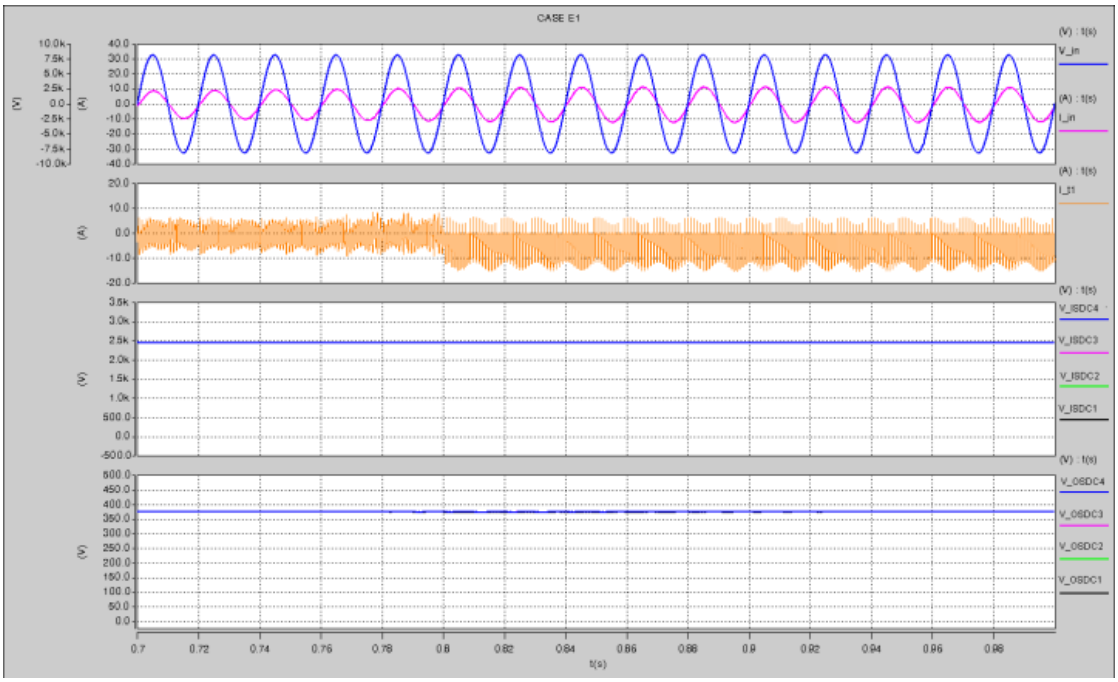
Figure 17. Simulation results of fault D1.



E1. Chopper Rectifier Diode Open-Circuit

Figure 18 shows the E1 fault simulation results of the input voltage, input current, the current through the primary side of the HFIT to the failure chopper, four ISDCB voltages, and four OSDCB voltages. It can be observed that I_t1 can only flow in one direction when the fault E1 happens at 0.8 s. The peak current of the HFIT increases as the full-bridge diode rectifier becomes a half-bridge diode rectifier, which may cause over current on the diode and IGBTs on the primary side of the HFIT.

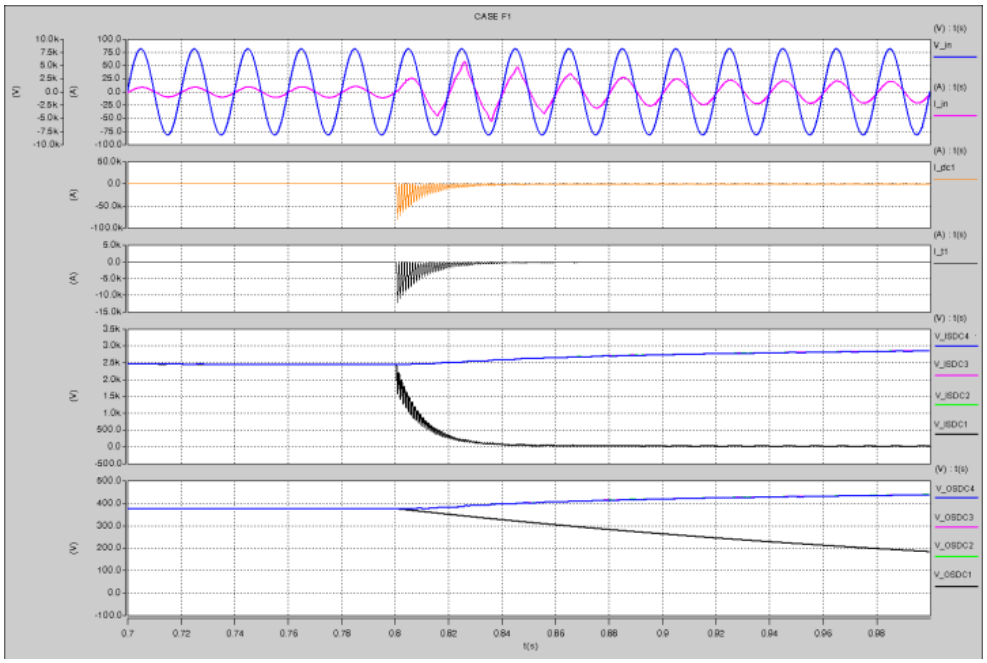
Figure 18. Simulation results of fault E1.



F1. Chopper Rectifier Diode Short-Circuit

Figure 19 shows the F1 fault simulation results of the input voltage, input current, the current through the primary side of the HFIT, and the current through the shorted diode of the failure chopper (I_dc1), four ISDCB voltages and four OSDCB voltages,. It can be observed that I_dc1 and I_t1 at the failure moment are approximately 100 kA and 15 kA, respectively, which are seriously over current. V_ISDC1 decreases to 0 V within 40 ms and V_OSDC1 decreases to 200 V at 1.0 s due to the shorted diode, which are serious under voltages for both DC buses.

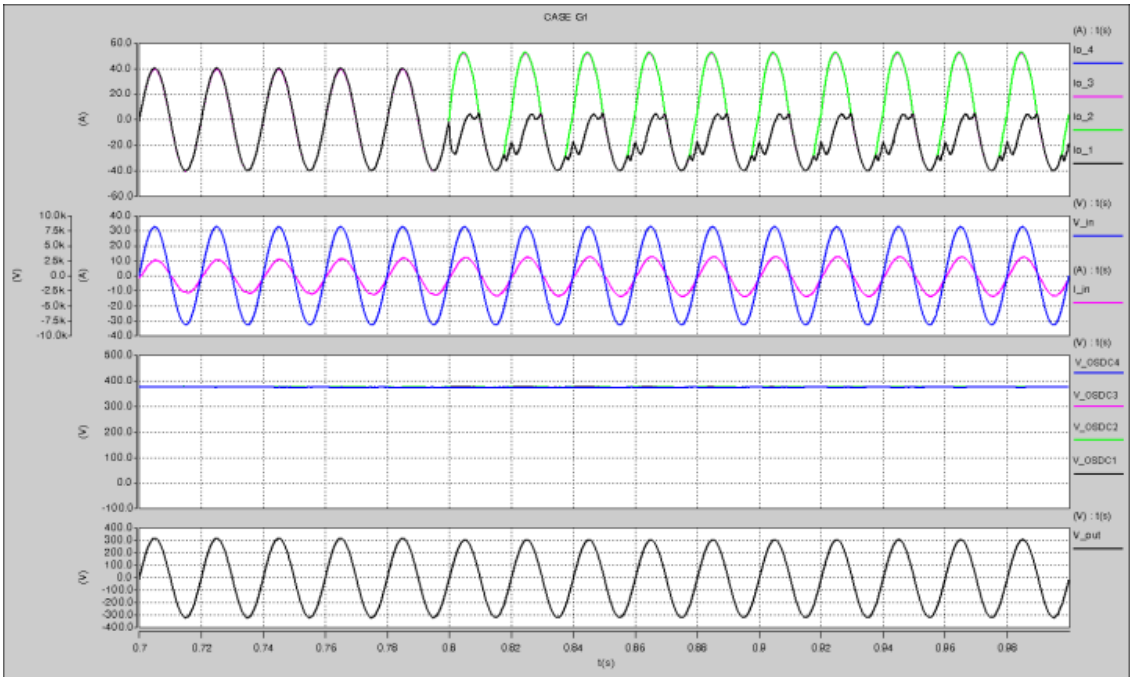
Figure 19. Simulation results of fault F1.



G1. Inverter IGBT Open-Circuit with Its Anti-Parallel Diode Normal

Figure 20 shows the G1 fault simulation results of the output currents of output stage modules (Io_4 to Io_1) which are in parallel with each other, the input voltage, input current, four OSDCB voltages, and the total output phase current (I_out). It can be observed that Io_1 can only flow in one direction since the fault happens, which makes Io_2, Io_3 and Io_4 increase in the same direction to cover the loss of Io_1, hence containing a dc component. The G2 fault case is similar to a G1 fault.

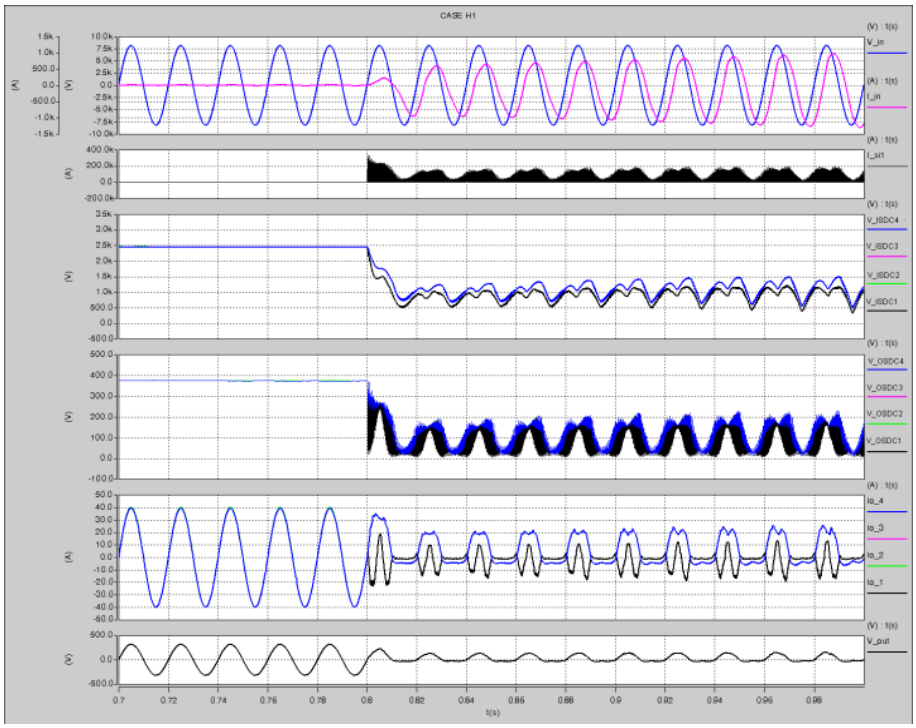
Figure 20. Simulation results of faults G1 and G2.



H1. Inverter IGBT Short-Circuit

Figure 21 shows the H1 fault simulation results of the input voltage, input current, the current through the shorted IGBT SI1 (I_si1), four ISDCB voltages, four OSDCB voltages, the output currents of output stage modules, and the total output phase current. It can be seen from the Figure 21 that I_si1 increases to 200 kA at the moment of failure due to the shoot-through fault, hence resulting in a reduction on V_OSDC1. Meanwhile, the short-circuit path is shared by the output filter to the rest of OSDCB capacitors; hence all four OSDCB voltage will be reduced, as well as the four ISDCB voltages. Due to the abnormal OSDCB voltage, the output voltage is distorted as well.

Figure 21. Simulation results of fault H1.



6. Protection and Fault Diagnosis Strategy

For short-circuit fault, the fault detection and protection should be very fast and based on the gate driver circuit of the power switch as the time between fault initiation and failure is very short. Take the IGBT driver 2SC0535T of CONCEPT (CT-Concept Technologie AG, Biel/Bienne, Switzerland) as an example, whose turn-on characteristics are shown in Figure 22.

Each channel of the 2SC0535T driver is equipped with a Collector-Emitter-Voltage (V_{ce}) monitoring circuit. The IGBT Collector-Emitter-Voltages are measured individually, and are checked after the response time at turn-on to detect a short circuit or over current. If the measured V_{ce} at the end of the response time is higher than the dynamic threshold V_{cethx}, the driver detects a short circuit or over current. Then the driver turns the corresponding power switches off immediately, hence the consequent damages of the faults to the D-EPT are prevented. At the same time, the fault status is immediately transferred to the corresponding SO_x output of the affected channel, which is usually connected to the I/O pins of DSP so that DSP would be aware of the faults. The power switch is kept in the off state (non-conducting) and the fault is shown at pin SO_x as long as the blocking time is over or the fault is clear. Hence the short circuit fault protection based on hardware circuit is realized.

Based on the simulation results and Table 1, the fault location algorithm of the power switches faults is shown in Figure 23. As can be seen from this Figure, by monitoring the state of input current (I_in), the B1, D1, F1 and H1 faults which are all short-circuit faults, can be easily indicated, as short-circuit faults always reduce the resistance to the relevant part hence increasing the input current. By identifying the abnormal IGBT state which includes over voltage and over current, one can locate the failure part of the EPT easily.

Figure 22. Turn-on characteristics of an IGBT.

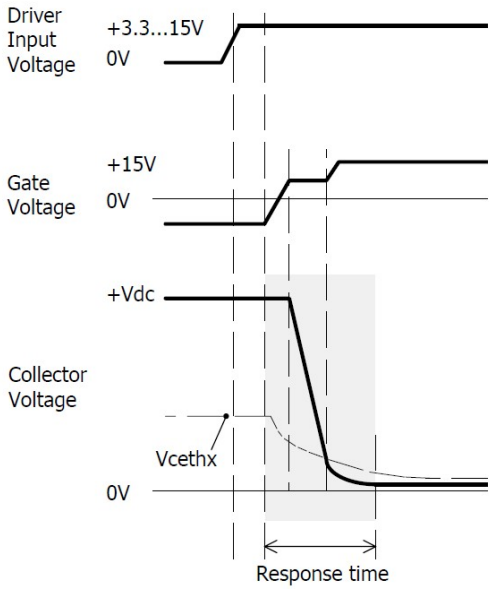
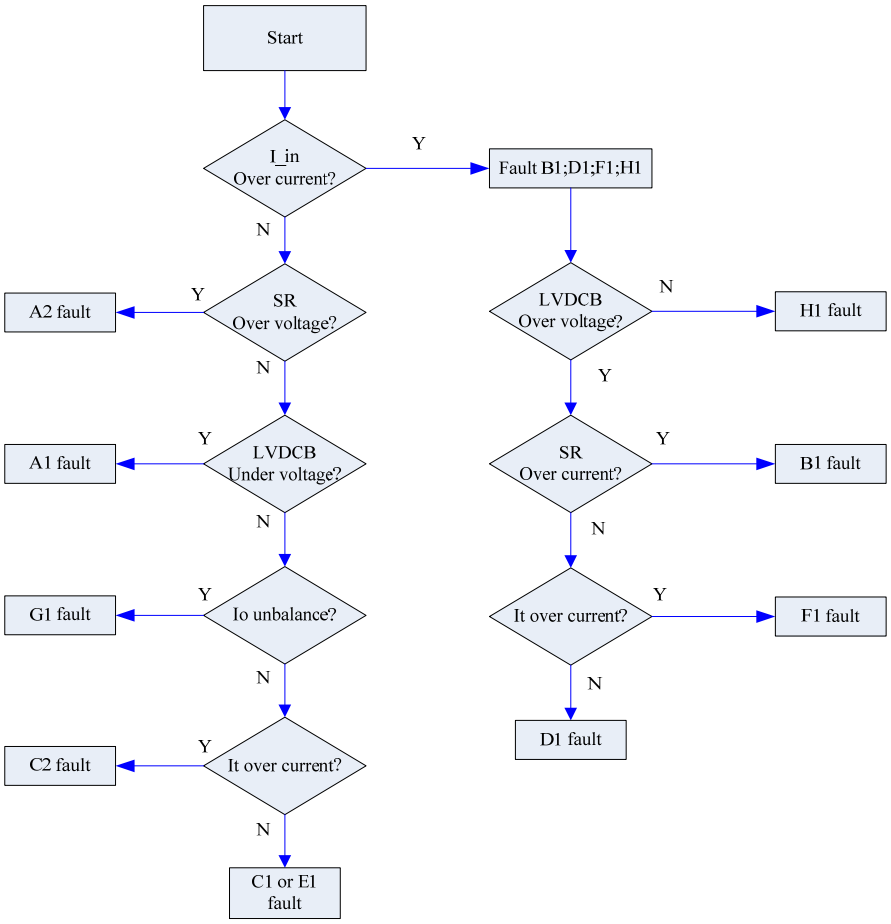


Figure 23. Flowchart for fault location algorithm.



As for open-circuit faults, a simple but effective way to identify the fault location from input stage (A1 and A2 faults), isolation stage (C1, C2, E1 and F1 faults), and output stage (G1 fault) is to monitor the abnormal states of relevant components. By applying current sensors and voltage sensors, these

states of relevant components such as module output currents, transformer currents can be monitored. However, it is difficult to distinguish the C1 fault and E1 fault as the working power switches and working modes during those faults are exactly the same, hence with similar shapes of the waveforms.

Voltage and current sensors are needed to detect the abnormality of voltages and currents when faults occur. Based on Table 1 which is concluded from the simulation results of Section 5, the listed voltages and currents must be kept under monitoring, and treated in different ways.

First of all, the current sensor for input phase current (I_in) is needed, not only for input current over current, but also for the input factor abnormality. Hence a program should be applied not only to calculate the RMS value of input current, but also the input power factor.

Due to the EPT control scheme, only OSDCB voltages need to be monitored, hence reducing the cost and complexity which will increase greatly when it comes to the ISDCB voltages. The voltage sensors need to monitor the amplitudes of the DC voltages as well as their ripples. Moreover, some consequences of the faults will cause DC bus voltages to unbalance first, such as the case of the A1 or A2 faults, rather than under voltage and over voltage which are the worst case results. Hence the monitoring program needs to detect the amplitude and ripple voltage of each OSDCB voltage, and then check whether it is over voltage, under voltage, or unbalanced.

In the short-circuit fault, the fault detection and protection should be very fast and based on a hardware circuit as time between fault initiation and failure is very short. Therefore, the fault detection circuit should be embedded in each IGBT driver to detect the over voltage and over current faults for each IGBT.

The transformer currents are needed in order to detect the faults happening in the isolation stage of EPT, each one of which will cause transformer current abnormality including C1, C2, D1, E1, and F1 faults. The protection based on the RMS value is sufficient in many fields; however it is not enough for the detection of an isolation fault. According to the simulation results, the RMS value of transformer current is normal; however the amplitude of the current is already over the limit. Furthermore, the average current needs to be calculated to detect the transformer saturation problem. Hence the amplitude, RMS value and average value of transformer current are all needed.

In the output stage, the average value of each module output current is not zero after the G1 fault according to the simulation. Hence the output current of each module is also needed to calculate the amplitude, RMS value, and average value.

Finally, one needs to monitor the output voltage for its amplitude, RMS value and average value according to the simulation of the H1 fault.

The computational needs of DSP are RMS, amplitude and average values of voltage and current. The protection scheme would then compare them with the rated values to detect the faults, and the computational burden of all this s quite light for a 96 MHz TMS320F28335 DSP from Texas Instruments.

7. Conclusions

The fault characteristics are important evaluation indicators of the Distribution Electronic Power Transformer (D-EPT). In this paper, the fault characteristics based on power switches failures to D-EPT are presented, analyzed and then verified by Saber simulation. The possible faults for power switches such as IGBTs and diodes including open-circuit faults and short-circuit faults which

mainly focus on the distortions to input current, ISDCB voltages, OSDCB voltages and currents through relevant power electronics components are thoroughly categorized and illustrated in detail. Based on the simulation results, the protection design is introduced, and one can identify the exact location of the faulty switches, and take remedies to prevent the consequent damages of most of the faults (open-circuit faults) to D-EPT and the whole power system as well as the losses to an end user when the fault location algorithm according to aforementioned analysis is employed. For short-circuit faults, the driver would turn the corresponding power switch off while transferring the fault status to the DSP at pin SO_x.

Conflicts of Interest

The authors declare no conflict of interest.

Acknowledgments

This work was supported in part by the Project of National Natural Science Foundation of China (51277083) and the National Basic Research Program of China (2009CB219702).

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