

## Article

# Novel Interleaved Converter with Extra-High Voltage Gain to Process Low-Voltage Renewable-Energy Generation

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**Abstract:** This paper presents a novel interleaved converter (NIC) with extra-high voltage gain to process the power of low-voltage renewable-energy generators such as photovoltaic (PV) panel, wind turbine, and fuel cells. The NIC can boost a low input voltage to a much higher voltage level to inject renewable energy to DC bus for grid applications. Since the NIC has two circuit branches in parallel at frond end to share input current, it is suitable for high power applications. In addition, the NIC is controlled in an interleaving pattern, which has the advantages that the NIC has lower input current ripple, and the frequency of the ripple is twice the switching frequency. Two coupled inductors and two switched capacitors are incorporated to achieve a much higher voltage gain than conventional high step-up converters. The proposed NIC has intrinsic features such as leakage energy totally recycling and low voltage stress on power semiconductor. Thorough theoretical analysis and key parameter design are presented in this paper. A prototype is built for practical measurements to validate the proposed NIC.

**Keywords:** photovoltaic (PV) panel; fuel cells; high step-up converter; interleaved converter; low voltage stress

## 1. Introduction

Since fossil fuels will be depleted in the next decades, development of green energy power generation systems becomes urgent. Among renewable energy generation systems, photovoltaic (PV), wind turbine, energy storage systems, and fuel cells attract a lot of attention [1–4]. Nevertheless, low output voltage is their common shortcoming, especially in grid connection or electric vehicle (EV) applications. Therefore, a step-up converter to achieve high voltage gain is required. Conventional boost-type converters, like boost, buck-boost, and flyback, are able to step-up input voltage. However, in order to meet high-voltage gain requirements, they have to operate in heavy-duty ratio or adopt a high turns ratio transformer, which will decrease the conversion efficiency dramatically. Cascading more boost-type converters can avoid the above problem but issues of volume, cost, and efficiency emerge. Therefore, the high step-up DC/DC converter is the current design trend.

High step-up converters can be mainly classified into two categories: single-stage and interleaved structure. Single-stage topology incorporates coupled inductors and/or switched capacitors to complete high voltage gain. Even though its input voltage is boosted, a large magnitude of input current ripple occurs, limiting the converter power rating significantly [5–8]. The interleaved converter has the ability of suppressing input current ripple by means of adding a parallel current path, which is a better choice for high power applications [9–11]. However, the conventional interleaved converters have voltage gain limitation, which confines their applications in grid-tied systems. To overcome the aforementioned disadvantages, various high step-up interleaved converters were proposed in [12–16]; nevertheless, the shortcomings of lower voltage gain, higher voltage stress, and large component

count still exist. An interleaved Boost converter combining voltage doubler is introduced in [12], while a coupled inductor is examined in [13]. In order to achieve high voltage gain, the converters in [12,13] have to be operated at heavy-duty ratio or adopt a magnetic transform with high turns ratio, which results in low conversion efficiency or high voltage stress. Even though Lai et al. [14] proposed another high step-up converter, incorporating coupled inductor and switched capacitor, into an interleaved Boost configuration, the converter intrinsically has the demerits of higher voltage stress and sophisticated structure. An interleaved step-up converter with winding-cross-coupled inductors and voltage multiplier cells is presented in [15]. This converter is composed of eight semiconductor devices and two three-winding coupled inductors. That is, a large number of power devices must be used. Tseng et al. [16] utilized the characteristics of forward, flyback, and interleaved converters to boost input voltage, but voltage gain still is limited.

This paper proposes a novel interleaved converter (NIC), which can accomplish a high voltage conversion ratio and is capable of processing low voltage, high power distributed resources. Its power stage is depicted in Figure 1. The proposed NIC mainly includes three parts: one interleaved-boost converter cell and two voltage multipliers. The interleaved-Boost converter cell is in charge of lowering input current ripple, increasing current rating, and primarily stepping input voltage. The two voltage multipliers can further stack up voltage level. The series voltage of the three parts determines the magnitude of output voltage. Since the proposed converter only uses two coupled inductors, three capacitors, four diodes, and two active power switches, it has a lower component count and a simple circuit structure. The advantages of the proposed NIC are summarized as follows:

- (1) The NIC can suppress input current ripple.
- (2) The energy stored in leakage inductance can be recycled.
- (3) The voltage stress of the semiconductor device is low enough so that a power switch with lower on-state resistance and smaller parasitic capacitance can be chosen.
- (4) As compared with a conventional interleaved high step-up converter, the proposed NIC can achieve a much higher voltage gain under the same power component count.

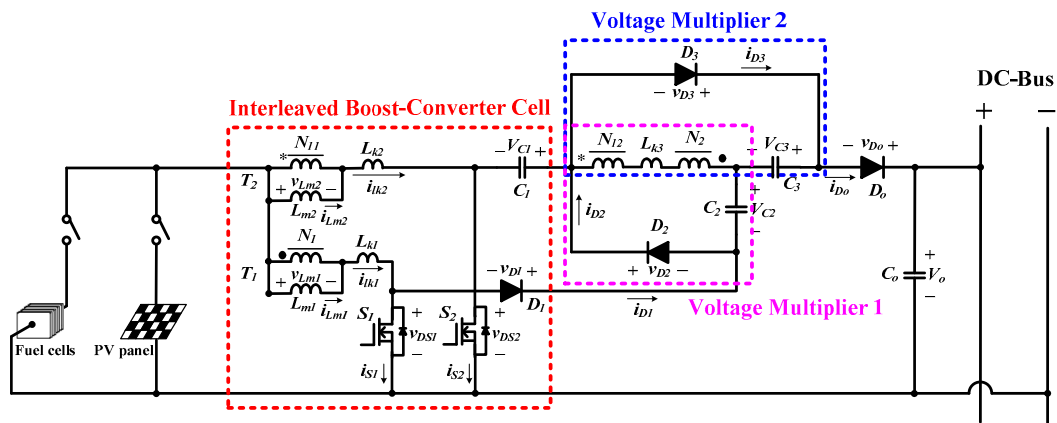


Figure 1. The main power circuit of the proposed novel interleaved converter (NIC). PV: photovoltaic.

## 2. Operation Principle of the Proposed Converter

In Figure 1,  $L_{m1}$  and  $L_{m2}$  denote the magnetizing inductances of the coupled inductors  $T_1$  and  $T_2$ , respectively. The  $L_{k1}$  and  $L_{k2}$  represent the primary leakage inductances of  $T_1$  and  $T_2$ , in turn, while  $L_{k3}$  stands for the total leakage inductance at the secondary windings of both coupled inductors. Turns ratios of primary to secondary of  $T_1$  and  $T_2$  are denoted as  $n_1$  and  $n_2$ , respectively.  $C_1$ ,  $C_2$ , and  $C_3$  are the main capacitors employed in the circuit. It is supposed that the NIC operates in continuous conduction mode (CCM) and the two active switches  $S_1$  and  $S_2$  are controlled in interleaved manner. Accordingly, the operation of the NIC can be divided into ten operation modes over one switching cycle. The corresponding equivalents are illustrated in Figure 2, while Figure 3 depicts key waveforms. Analysis of the proposed NIC begins by making these assumptions:

- (1) All parasitic capacitances and internal resistances are neglected. Moreover, all diodes are ideal.
- (2) The voltages across capacitors  $C_1$ ,  $C_2$ ,  $C_3$ , and  $C_o$  are time-invariant.
- (3) Magnetizing inductances,  $L_{m1}$  and  $L_{m2}$ , are much larger than the leakage inductances  $L_{lk1}$ ,  $L_{lk2}$  and  $L_{lk3}$ .
- (4) The switching period is  $T_s$ . Both switches are closed for time  $DT_s$  and open for  $(1 - D)T_s$ .

**Mode 1 ( $t_0-t_1$ ) (Figure 2a):** This mode is the initial mode of the all operation procedures. During this time interval, both active switches  $S_1$  and  $S_2$  are closed. Diodes  $D_1$ ,  $D_3$  and  $D_o$  are in reverse-bias, but  $D_2$  is forward-biased. Input voltage  $V_{in}$  is across the primaries of  $T_1$  and  $T_2$  directly. Then, the current flowing through  $S_2$  starts increasing linearly from zero, while the switch current  $i_{S1}$ , having an initial value determined by the end of Mode 10, also increases linearly. In addition, the energy remained in  $L_{k3}$  will be recycled to  $C_2$  via  $D_2$ . At the time that the diode current  $i_{D2}$  drops to zero, and this mode ends.

**Mode 2 ( $t_1-t_2$ ) (Figure 2b):** During this time interval, active switches  $S_1$  and  $S_2$  are still closed, and  $V_{in}$  remains across the two coupled inductors. Thus, the current  $i_{Lm1}$  and  $i_{Lm2}$  are continuously increasing. In this mode, the current flowing through leakage inductances  $i_{lk1}$  and  $i_{lk2}$  are equal to magnetizing-inductance currents  $i_{Lm1}$  and  $i_{Lm2}$ , respectively. This mode ends when the switch  $S_1$  is turned off.

**Mode 3 ( $t_2-t_3$ ) (Figure 2c):** In this mode,  $S_2$  remains in on state but  $S_1$  becomes off. Diodes  $D_2$ ,  $D_3$  and  $D_o$  are reversely-biased but  $D_1$  is in forward-bias. The  $V_{in}$ ,  $L_{m1}$ ,  $L_{k1}$  and  $C_2$  dump energy to  $L_{k3}$  and  $C_1$  via  $D_1$  and  $S_2$ , so the current flowing through  $D_1$  and  $S_2$  increases. This mode finishes when  $D_3$  becomes forward-biased and  $L_{k3}$  starts to release energy.

**Mode 4 ( $t_3-t_4$ ) (Figure 2d):** Over the whole interval of Mode 4,  $S_2$  is still kept in on state while  $S_1$  is in off state. The  $D_1$  remains forward-biased and  $D_3$  becomes closed. Meanwhile, both diodes  $D_2$  and  $D_o$  continue the off status. Magnetizing-inductance  $L_{m1}$  pumps energy to  $C_3$  via the coupled inductor. Capacitor  $C_1$  is charged continuously, the circuit behavior of which is the same as in the previous mode. When the leakage-inductance  $L_{k1}$  releases over its stored energy,  $i_{D1}$  will drop to zero. That is, diode  $D_1$  becomes reversely-biased and this mode ends.

**Mode 5 ( $t_4-t_5$ ) (Figure 2e):** During this time interval,  $S_2$  is still closed and  $S_1$  is open. Diodes  $D_1$ ,  $D_2$  and  $D_o$  are reversely-biased but  $D_3$  is in forward-bias.  $V_{in}$  and  $L_{m1}$  supply energy to  $C_3$  simultaneously by the  $T_1$  and  $T_2$  in turn. This mode finishes as  $S_1$  is turned on.

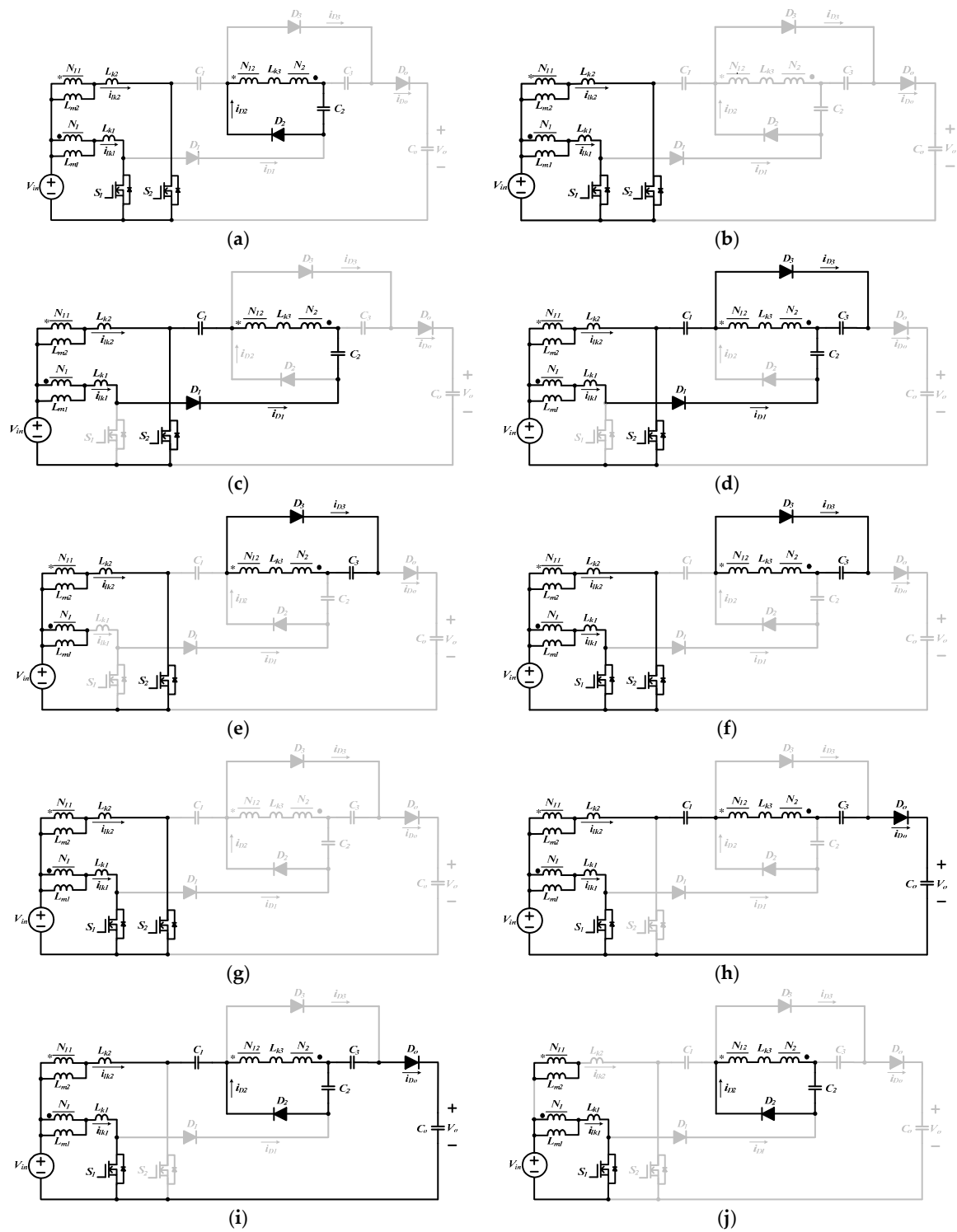
**Mode 6 ( $t_5-t_6$ ) (Figure 2f):** During this mode,  $S_1$  and  $S_2$  are both in on state. Diodes  $D_1$ ,  $D_2$  and  $D_o$  are off, but  $D_3$  is on.  $L_{m1}$  starts to draw energy from  $V_{in}$ . The stored energy in  $L_{k3}$  will release to  $C_3$  through  $D_3$ . This mode sustains until  $i_{D3}$  decreases to zero.

**Mode 7 ( $t_6-t_7$ ) (Figure 2g):** During this time interval,  $S_1$  and  $S_2$  are both in on state, but  $D_1$ ,  $D_2$ ,  $D_3$  and  $D_o$  are all reversely-biased. Since the primaries of the two coupled inductors are in parallel,  $V_{in}$  will supply energy to  $L_{m1}$ ,  $L_{m2}$ ,  $L_{k1}$  and  $L_{k2}$ . Therefore,  $i_{Lm1}$  and  $i_{Lm2}$  will increase linearly, which are identical to  $i_{S1}$  and  $i_{S2}$ , respectively. This mode is ended when  $S_2$  is turned off.

**Mode 8 ( $t_7-t_8$ ) (Figure 2h):** During this time interval,  $S_1$  remains in on state, but  $S_2$  is in off state.  $D_1$ ,  $D_2$  and  $D_3$  are off, but  $D_o$  is on. The  $L_{m2}$  starts to release its stored energy so that the current flowing through  $L_{m2}$  decays. Meanwhile, the current  $i_{lk3}$  increases. The input  $V_{in}$  and the voltages across  $L_{m2}$ ,  $L_{k2}$ ,  $C_1$ , and  $C_3$  will be stacked up to supply  $C_o$ . This mode terminates when  $L_{k3}$  starts to charge  $C_2$ .

**Mode 9 ( $t_8-t_9$ ) (Figure 2i):** In this mode,  $S_1$  is still closed and  $S_2$  is open. The  $V_{in}$  will charge  $C_2$  via coupled inductor  $T_1$ ; meanwhile, the energy stored in  $L_{m2}$  will also be transferred to the secondary of  $T_2$  for powering  $C_2$ . Therefore,  $i_{Lm2}$  drops and  $C_o$  keeps on charging. In Mode 9, the energy in  $L_{k2}$  is recycled to the output. This mode ends as  $i_{lk2}$  falls to zero.

**Mode 10 ( $t_9-t_{10}$ ) (Figure 2j):** The diode  $D_o$  will become reversely biased when  $i_{lk2}$  drops to zero. In Mode 10,  $S_1$  proceeds with on-state conducting and  $S_2$  remains in off state. With respect to diode status, the diodes  $D_1$ ,  $D_3$  and  $D_o$  are in reverse-bias and  $D_2$  is still in on state. The  $V_{in}$  and  $L_{m2}$  will forward energy to  $C_2$  through the coupled inductors  $T_1$  and  $T_2$ , respectively. This mode ends when  $S_2$  is turned on again, and then the operation returns to Mode 1.



**Figure 2.** Mode equivalents of the proposed NIC over one switching period. (a) Mode 1 ( $t_0-t_1$ ); (b) Mode 2 ( $t_1-t_2$ ); (c) Mode 3 ( $t_2-t_3$ ); (d) Mode 4 ( $t_3-t_4$ ); (e) Mode 5 ( $t_4-t_5$ ); (f) Mode 6 ( $t_5-t_6$ ); (g) Mode 7 ( $t_6-t_7$ ); (h) Mode 8 ( $t_7-t_8$ ); (i) Mode 9 ( $t_8-t_9$ ); and (j) Mode 10 ( $t_9-t_{10}$ ).

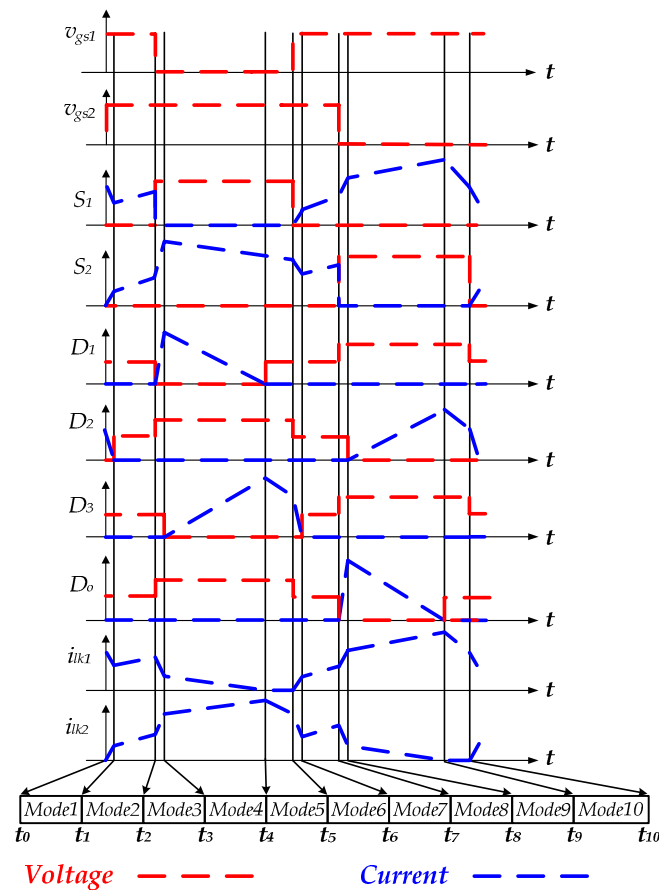


Figure 3. Conceptual key waveforms of the proposed NIC.

### 3. Voltage Gain Derivation

Voltage gain is the most important characteristic of a high step-up converter. As the analysis in Section 2 shows, the switched capacitors  $C_1$  and  $C_3$  have the benefit of voltage stacking for achieving extra-high voltage gain. This section focuses on the voltage gain derivation of the proposed NIC. For high power applications, the converter is designed in CCM. Assumptions made in Section 2 are also adopted for simplifying the derivation. Furthermore, the coupling coefficients of the coupled inductors are both supposed at unity; that is, there is no leakage inductance.

According to the description for Mode 4 in Section 2,  $C_1$  is charged by  $V_{in}$ ,  $C_2$ ,  $T_1$ , and  $T_2$ , whereas  $C_3$  is charged by the two coupled inductors. Referring to Mode 9 in Section 2, if the leakage inductances are ignored, the output port is supplied by  $V_{in}$ ,  $T_1$ ,  $T_2$ ,  $C_1$ , and  $C_3$ . Hence, to determine the voltage gain,  $V_o/V_{in}$ , the relationships of  $V_{C1}$ ,  $V_{C2}$  and  $V_{C3}$  in terms of  $V_{in}$  have to be found in advance.

#### 3.1. The Ratio of $V_{C3}$ to $V_{in}$

As  $S_1$  is closed,  $V_{in}$  will supply energy to  $L_{m1}$ . After an on-time interval  $DT_s$ , the change in  $i_{Lm1}$  can be estimated as:

$$(\Delta i_{Lm1})_{on} = \frac{V_{in}DT_s}{L_{m1}} \quad (1)$$

In the opposite switch statuses, that is,  $S_1$  off and  $S_2$  on, the energy stored in  $L_{m1}$  will be transferred to the secondary of the coupled inductor  $T_1$  and then be forwarded to  $C_3$  by the loop of  $N_2$ - $N_{12}$ - $D_3$ - $C_2$ . In addition, the source voltage  $V_{in}$  also supplies energy to  $C_3$  via  $T_2$ . By Kirchhoff's voltage law (KVL) and from the closed loop  $N_2$ - $N_{12}$ - $D_3$ - $C_2$ , it can be found that:

$$n_2V_{Lm2} - n_1V_{Lm1} - V_{C3} = 0 \quad (2)$$

Since voltage across  $L_{m2}$  is  $V_{in}$ , rewriting Equation (2) becomes:

$$V_{Lm1} = \frac{nV_{in} - V_{C3}}{n} = L_{m1} \frac{di_{Lm1}}{dt} \quad (3)$$

From Equation (3), the current change in  $L_{m1}$  after a switch-off interval  $(1 - D)T_s$ , is found by:

$$(\Delta i_{Lm1})_{off} = \frac{(nV_{in} - V_{C3})(1 - D)T_s}{nL_{m1}} \quad (4)$$

In steady state, over one switching cycle the net change of inductor current  $i_{Lm1}$  is zero. That is:

$$nV_{in}DT_s + (nV_{in} - V_{C3})(1 - D)T_s = 0 \quad (5)$$

Rearranging the above equation can obtain the voltage of  $V_{C3}$  in terms of  $V_{in}$  as follows:

$$V_{C3} = \frac{nV_{in}}{(1 - D)} \quad (6)$$

### 3.2. The Ratio of $V_{C2}$ to $V_{in}$

With respect to the ratio of  $V_{C2}$  to  $V_{in}$ , the current change in  $L_{m2}$  has to be dealt with first. The current flowing through  $L_{m2}$  increases when  $S_2$  is closed. After  $DT_s$ , the change  $(\Delta i_{Lm2})_{on}$  can be expressed as:

$$(\Delta i_{Lm2})_{on} = \frac{V_{in}DT_s}{L_{m2}} \quad (7)$$

when switch  $S_2$  is open for  $(1 - D)T_s$  and  $S_1$  is in on state. The energy stored in  $L_{m2}$  will be released to  $C_2$  by coupled inductor  $T_2$  as well as the loop of  $N_{12}$ - $N_2$ - $C_3$ - $D_2$ . Therefore:

$$nV_{Lm1} - nV_{Lm2} - V_{C2} = 0 \quad (8)$$

In Equation (8), the voltage across  $L_{m1}$  equals  $V_{in}$ , thus:

$$V_{Lm2} = \frac{nV_{in} - V_{C2}}{n} = L_{m2} \frac{di_{Lm2}}{dt} \quad (9)$$

The total current drop in  $L_{m2}$  can be found by:

$$(\Delta i_{Lm2})_{off} = \frac{(nV_{in} - V_{C2})(1 - D)T_s}{nL_{m2}} \quad (10)$$

In steady state, over one switching cycle the net change of the inductor current  $i_{Lm2}$  is zero. That is:

$$nV_{in}DT_s + (nV_{in} - V_{C2})(1 - D)T_s = 0 \quad (11)$$

Thus, the voltage of  $V_{C2}$  in terms of  $V_{in}$  is as follows:

$$V_{C2} = \frac{nV_{in}}{(1 - D)} \quad (12)$$

### 3.3. The Ratio of $V_{C1}$ to $V_{in}$

While  $S_1$  is open and  $S_2$  is closed, from the current flow path of  $V_{in}$ - $L_{m1}$ - $D_1$ - $C_2$ - $N_2$ - $N_{12}$ - $C_1$ - $S_2$ , the following relationship can be found:

$$V_{Lm1} = \frac{V_{in} + V_{C2} + nV_{Lm2} - V_{C1}}{(1 + n)} = L_{m1} \frac{di_{Lm1}}{dt} \quad (13)$$

Since the voltage across  $L_{m2}$  in Equation (13) is  $V_{in}$ , the current decrease on  $L_{m1}$  is derived as:

$$(\Delta i_{Lm1})_{off} = \frac{(V_{in} + V_{C2} + nV_{in} - V_{C1})(1 - D)T_s}{(1 + n)L_{m1}} \quad (14)$$

In addition, the total amount of current increase on  $L_{m1}$  over the  $S_1$ -closed interval has been depicted as Equation (1). This increment is equal to the decrease amount in  $i_{Lm1}$  over one switching cycle, which yields:

$$\frac{V_{in}DT_s}{L_{m1}} + \frac{(V_{in} + V_{C2} + nV_{in} - V_{C1})(1 - D)T_s}{(1 + n)L_{m1}} = 0 \quad (15)$$

Rearranging Equation (15) results in:

$$V_{C1} = \frac{(1 + 2n)}{(1 - D)} V_{in} \quad (16)$$

### 3.4. The Ratio of $V_o$ to $V_{in}$

Under the condition that  $S_1$  is closed and  $S_2$  is in off state, the voltage  $V_{Lm2}$  can be determined by applying KVL to the loop enclosed by  $V_{in}$ ,  $L_{m2}$ ,  $C_1$ ,  $N_{12}$ ,  $N_2$ ,  $C_3$ ,  $D_o$ , and  $C_o$ . Therefore:

$$V_{Lm2} = \frac{V_{in} + V_{C1} + nV_{in} + V_{C3} - V_o}{(1 + n)} = L_{m2} \frac{di_{Lm2}}{dt} \quad (17)$$

Thus, the decreased quantity of  $i_{Lm2}$  is expressed as:

$$(\Delta i_{Lm2})_{off} = \frac{(V_{in} + V_{C1} + nV_{in} + V_{C3} - V_o)(1 - D)T_s}{(1 + n)L_{m2}} \quad (18)$$

From the increment  $(\Delta i_{Lm2})_{on}$  in Equation (7) and the condition  $(\Delta i_{Lm2})_{off} = (\Delta i_{Lm2})_{on}$ , the following relationship holds:

$$\frac{V_{in}DT_s}{L_{m2}} + \frac{(V_{in} + V_{C1} + nV_{in} + V_{C3} - V_o)(1 - D)T_s}{(1 + n)L_{m2}} = 0 \quad (19)$$

After simplifying, the following equation can be obtained:

$$V_{in} \frac{(1 + n)D}{(1 - D)} + V_{in} + V_{C1} + nV_{in} + V_{C3} - V_o = 0 \quad (20)$$

Substituting Equations (6) and (16) into Equation (20) can obtain the voltage gain of the proposed converter,  $V_o/V_{in}$ , and yields:

$$\frac{V_o}{V_{in}} = \frac{2(2n + 1)}{(1 - D)} \quad (21)$$

## 4. Voltage Stress of Power Component

This section begins with the determination of voltage stresses across  $S_1$  and  $S_2$ . Supposing that all leakage inductances are neglected, Modes 4 and 9 in Section 2 will therefore dominate the estimation of voltage stress. When  $S_1$  is open, from Figure 2d it can be found that the blocking voltage of  $S_1$ ,  $V_{DS1, stress}$ , can be expressed as

$$V_{DS1, stress} = V_{C1} - V_{C2} - V_{C3} = \frac{1}{1 - D} V_{in} \quad (22)$$

With respect to active switch  $S_2$ , its blocking voltage,  $V_{DS2, stress}$ , can be determined from Figure 2i and the following relationship can be found:

$$V_{DS2, stress} = V_o - V_{C3} - V_{C2} - V_{C1} = \frac{1}{1 - D} V_{in} \quad (23)$$

Equations (22) and (23) reveal that the voltage stresses of  $S_1$  and  $S_2$  are identical and irrelative to turns ratio of coupled inductor. Voltage stresses across active switches only depend on duty ratio and input voltage. Rewriting Equations (22) and (23) in terms of  $V_o$  results in:

$$V_{DS1, \text{stress}} = V_{DS2, \text{stress}} = \frac{V_o}{2(1+n)} \quad (24)$$

Equation (24) implies that the voltage stresses of  $S_1$  and  $S_2$  are much lower than output voltage. Considering the statues of  $S_1$  on and  $S_2$  off, the voltage across  $D_1$  and  $D_3$  can be determined as follows:

$$V_{D1, \text{stress}} = V_o - V_{C3} - V_{C2} = \frac{2(1+n)}{1-D} V_{in} \quad (25)$$

and:

$$V_{D3, \text{stress}} = V_{C3} + V_{C2} = \frac{2n}{1-D} V_{in} \quad (26)$$

With respect to  $D_2$  and  $D_o$ , their voltage stresses are calculated during the time interval of  $S_1$  off and  $S_2$  on. The corresponding voltage stress calculations can be:

$$V_{D2, \text{stress}} = V_{C2} + V_{C3} = \frac{2n}{1-D} V_{in} \quad (27)$$

and:

$$V_{D_o, \text{stress}} = V_o - V_{C1} = \frac{1+2n}{1-D} V_{in} \quad (28)$$

According to Equations (25)–(28), it can be observed that  $D_1$  endures the highest voltage stress among the four diodes. Table 1 summaries the comparison between NIC and other high step-up converters proposed in [13–16]. If the duty cycle  $D$  is 0.6, and the transformer turns ratio  $n$  is 1, the proposed converter can boost 15-times input voltage. However, the voltage gains of the converters in [13–16] are 5, 5.6, 10, and 10, respectively. It is obvious that the proposed NIC can exceed these high step-up converters in voltage gain. With respect to voltage stress across semiconductor device, if under the same condition that  $D = 0.6$ ,  $n = 1$ , and  $V_o = 380$  V, the maximum voltage stress of the active switches in [15,16] and the proposed NIC are all 95 V, but the converters in [13,14] are up to 190 V and 170 V, respectively. That is, the proposed converter features an advantage over other high step-up converters.

**Table 1.** Comparison among the proposed and other high step-up converters.

Items	Converter Introduced in [13]	Converter Introduced in [14]	Converter Introduced in [15]	Converter Introduced in [16]	Proposed Converter
Voltage gain	$\frac{1+n}{1-D}$	$\frac{2+nD-nD^2}{1-D}$	$\frac{2(1+n)}{1-D}$	$\frac{2(1+n)}{1-D}$	$\frac{2(1+2n)}{1-D}$
Number of active switches	4	2	2	2	2
Number of diodes	4	4	6	4	4
Number of capacitors	3	3	5	4	4
Number of transformers	1	1	2	2	2
Number of inductors	2	2	0	0	0
Maximum voltage stress of active switch	$\frac{V_o}{1+n}$	$\frac{V_o}{2+nD-nD^2}$	$\frac{V_o}{2(1+n)}$	$\frac{V_o}{2(1+n)}$	$\frac{V_o}{2(1+n)}$
Maximum voltage stress of diode	$V_o$	$\frac{2V_o}{2+nD-nD^2}$	$\frac{(1+2n)V_o}{2(1+n)}$	$\frac{nV_o}{1+n}$	$\frac{(1+n)V_o}{1+2n}$

## 5. Experimental Results

To validate the proposed NIC, a prototype based on the specifications summarized in Table 2 is designed, built, and tested. The types of semiconductor devices used in the prototype are given in Table 3. The power MOSFET, IRFSL4615PbF (International Rectifier, El Segundo, CA, USA), is selected to serve as active switches for controlling the current flow, of which maximum on-state resistance



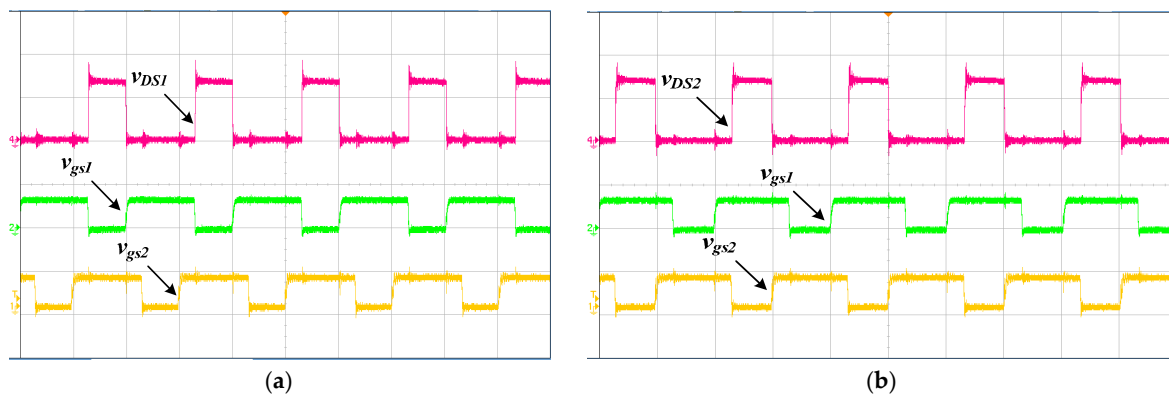
$R_{DS(on)}$  is 42 m $\Omega$ . The FEP16GT (Fairchild, Sunnyvale, CA, USA) is employed as diodes  $D_1$  and  $D_o$ , of which forward voltage is 1.3 V and reverse recovery time is 50 ns. With regard to diodes  $D_2$  and  $D_3$ , the hyper-fast rectifier VS-8ETH03-1PbF (Nichicon, Kyoto, Japan) is considered, which has 1.25 V forward voltage and 35 ns reverse recovery time. The voltage waveforms of active power switches and control signals are shown in Figure 4a,b, which indicate that the voltage across  $S_1$  and  $S_2$  are both near 65 V. This value also demonstrates a relatively low voltage stress across the active power semiconductor, as compared with other high step-up converters.

**Table 2.** Specifications of the proposed converter.

Symbols	Items	Values
$V_{in}$	Input voltage	24 V
$V_o$	Output voltage	380 V
$P_o$	Output power	200 W
$D$	Duty cycle	0.62
$f_s$	Switching frequency	50 kHz
$n$	Transformer turns ratio	1
$L_m$	Magnetizing inductance	93 $\mu$ H
$L_{lk}$	Leakage inductance	1.9 $\mu$ H
$C_1, C_2$ , and $C_3$	Capacitances	68 $\mu$ F
$C_o$	Output capacitance	330 $\mu$ F

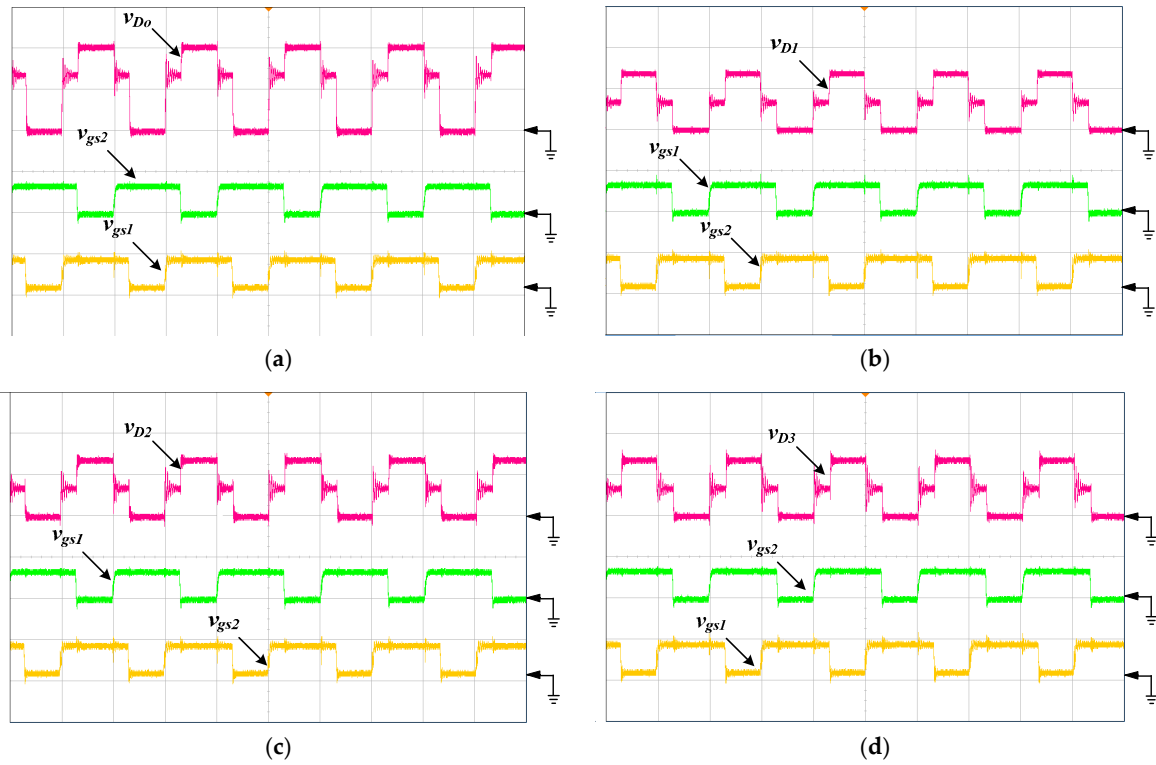
**Table 3.** Semiconductor devices used in the prototype.

Components	Types	Absolute Maximum Ratings
$D_1$ and $D_o$	FEP16GT	400 V/16 A
$D_2$ and $D_3$	VS-8ETH03-1PbF	300 V/8 A
$S_1$ and $S_2$	IRFSL4615PbF	150 V/33 A



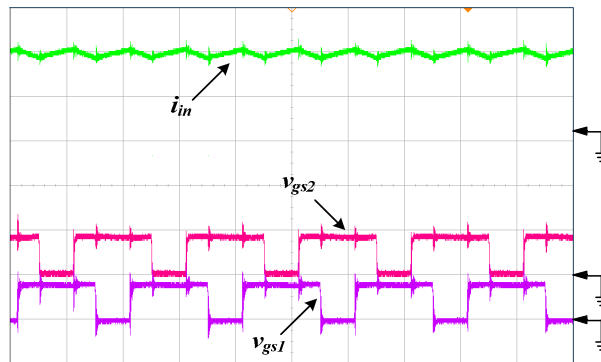
**Figure 4.** Experimental waveforms of active power switches in CCM operation and at  $D = 0.62$ . (a)  $v_{DS1}$  and the corresponding control signals ( $v_{DS1}$ : 50 V/div,  $v_{gs1}$  and  $v_{gs2}$ : 10 V/div, time: 10  $\mu$ s/div). (b)  $v_{DS2}$  and the corresponding control signals ( $v_{DS2}$ : 50 V/div,  $v_{gs1}$  and  $v_{gs2}$ : 10 V/div, time: 10  $\mu$ s/div).

Figure 5a,d is the practical measurements of voltage waveforms of diodes  $D_o$ ,  $D_1$ ,  $D_2$  and  $D_3$ , in turn, at the condition  $D = 0.62$  and in CCM operation. Figure 5a illustrates that the maximum blocking voltage of  $D_o$  is nearly 200 V. With respect to  $D_1$ , its voltage stress approaches to 280 V, as shown in Figure 5b. Diodes  $D_2$  and  $D_3$  endure the same voltage of 130 V. In Figure 5, all the diode voltage stresses are in compliance with Equations (25)–(28).



**Figure 5.** Experimental waveforms of diodes: (a)  $v_{D0}$  ( $v_{D0}$ : 100 V/div,  $v_{gs1}$  and  $v_{gs2}$ : 20 V/div, time: 5  $\mu$ s/div); (b)  $v_{D1}$  ( $v_{D1}$ : 200 V/div,  $v_{gs1}$  and  $v_{gs2}$ : 20 V/div, time: 5  $\mu$ s/div); (c)  $v_{D2}$  ( $v_{D2}$ : 100 V/div,  $v_{gs1}$  and  $v_{gs2}$ : 20 V/div, time: 5  $\mu$ s/div); (d)  $v_{D3}$  ( $v_{D3}$ : 100 V/div,  $v_{gs1}$  and  $v_{gs2}$ : 20 V/div, time: 5  $\mu$ s/div).

Figure 6 shows the waveforms of input current and the corresponding control signals. It indicates that the magnitude of input ripple current is limited to less than 2 A. Figure 7 depicts the measured and simulated efficiencies from light load to full load. In the simulations, the considered conditions include forward voltage of diode,  $R_{DS(on)}$  of MOSFET, copper loss of the coupled inductor, switching loss of MOSFET, and the equivalent resistance of diode. The maximum value of the measured efficiency is 93.7% at  $P_o = 140$  W. Figure 8 is the photo of test bench, in which PV simulator Chroma 62050H-600S (Taoyuan, Taiwan) serves as input source, electronic load Chroma 6320 draws power from the converter, and all waveforms are measured by oscilloscope KEYSIGHT DSOX4024A (Santa Rosa, CA, USA).



**Figure 6.** Experimental waveforms of input current and corresponding control signals ( $i_{in}$ : 5 A/div,  $v_{gs1}$  and  $v_{gs2}$ : 20 V/div, time: 10  $\mu$ s/div).

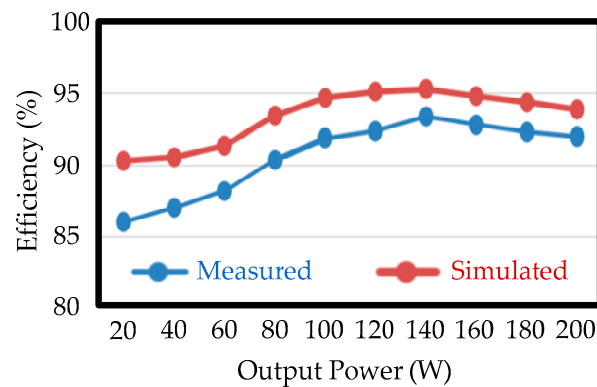


Figure 7. The measured and simulated efficiencies of the proposed NIC.

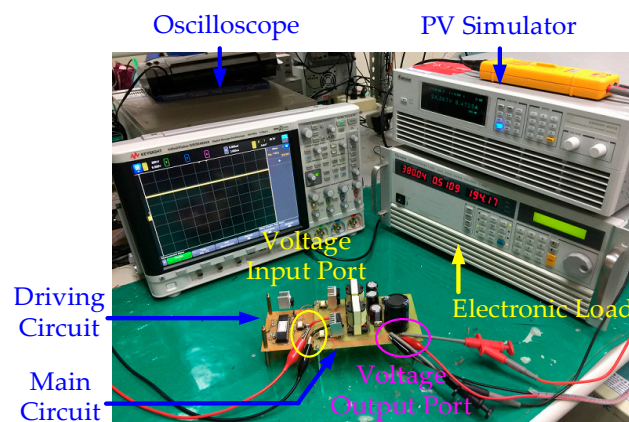


Figure 8. Photo of the experimental setup.

## 6. Conclusions

This paper proposes a NIC, which is applicable to PV systems or fuel cells for grid-connected high-power applications. The proposed converter utilizes the interleaved technique for current sharing to decrease input current ripples. Furthermore, the proposed converter can achieve a much higher voltage gain than a conventional interleaved converter. The operation principle and steady-state analysis of the proposed converter are described in detail. A 24 V/380 V 200 W prototype has been examined to demonstrate the feasibility of the proposed NIC. The maximum measured efficiency of the proposed converter is 93.7%. This value is a little lower than some of other high step-up converters. However, if the soft-switching technique is employed to make the switches operate at zero-voltage-switching or zero-current-switching condition, the efficiency of the proposed NIC can be improved significantly.

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**Conflicts of Interest:** The authors declare that there is no conflict of interests regarding the publication of this paper.

## References

1. Lin, B.R.; Dong, J.Y. New zero-voltage switching DC–DC converter for renewable energy conversion system. *IET Power Electron.* **2012**, *5*, 393–400. [[CrossRef](#)]

2. Kwon, J.-M.; Kwon, B.-H.; Nam, K.-H. High-efficiency module-integrated photovoltaic power conditioning system. *IET Power Electron.* **2009**, *2*, 410–420. [[CrossRef](#)]
3. Li, W.; Xu, C.; Yu, H.; Gu, Y.; He, X. Analysis, design and implementation of isolated bidirectional converter with winding-cross-coupled inductors for high step-up and high step-down conversion system. *IET Power Electron.* **2014**, *7*, 67–77. [[CrossRef](#)]
4. Lee, K.-H.; Joo, M.-C.; Baek, N.-C. Experimental evaluation of simple thermal storage control strategies in low-energy solar houses to reduce electricity consumption during grid on-peak periods. *Energies* **2015**, *8*, 9344–9364. [[CrossRef](#)]
5. Li, W.; Li, W.; He, X. Zero-voltage transition interleaved high step-up converter with built-in transformer. *IET Power Electron.* **2011**, *4*, 523–531. [[CrossRef](#)]
6. Tseng, S.-Y.; Wang, H.-Y. A photovoltaic power system using a high step-up converter for DC load applications. *Energies* **2013**, *6*, 1068–1100. [[CrossRef](#)]
7. Shen, C.-L.; Chen, H.-Y.; Chiu, P.-C. Integrated three-voltage-booster DC–DC converter to achieve high voltage gain with leakage-energy recycling for PV or fuel-cell power systems. *Energies* **2015**, *8*, 9843–9859. [[CrossRef](#)]
8. Sabzali, A.J.; Ismail, E.H.; Behbehani, H.M. High voltage step-up integrated double Boost-Sepic DC–DC converter for fuel-cell and photovoltaic applications. *Renew. Energy* **2015**, *82*, 44–53. [[CrossRef](#)]
9. Tsai, C.-T.; Shen, C.-L. A high step-down interleaved buck converter with active-clamp circuits for wind turbines. *Energies* **2012**, *5*, 5150–5170. [[CrossRef](#)]
10. Hu, Y.; Xiao, W.; Li, W.; He, X. Three-phase interleaved high-step-up converter with coupled-inductor-based voltage quadrupler. *IET Power Electron.* **2014**, *7*, 1841–1849. [[CrossRef](#)]
11. Lai, C.-M.; Lin, Y.-C.; Lee, D. Study and implementation of a two-phase interleaved bidirectional dc/dc converter for vehicle and DC-microgrid systems. *Energies* **2015**, *8*, 9969–9991. [[CrossRef](#)]
12. Jang, Y.; Jovanovic, M.M. Interleaved boost converter with intrinsic voltage-doubler characteristic for universal-line PFC front end. *IEEE Trans. Power Electron.* **2007**, *22*, 1394–1401. [[CrossRef](#)]
13. Li, W.; Li, W.; He, X.; Xu, D.; Wu, B. General derivation law of nonisolated high-step-up interleaved converters with built-in transformer. *IEEE Trans. Ind. Electron.* **2012**, *59*, 1650–1661. [[CrossRef](#)]
14. Lai, C.-M.; Pan, C.-T.; Cheng, M.-C. High-efficiency modular high step-up interleaved boost converter for DC-microgrid applications. *IEEE Trans. Ind. Appl.* **2012**, *48*, 161–171. [[CrossRef](#)]
15. Li, W.; Zhao, Y.; Wu, J.; He, X. Interleaved high step-up converter with winding-cross-coupled inductors and voltage multiplier cells. *IEEE Trans. Power Electron.* **2012**, *27*, 133–143. [[CrossRef](#)]
16. Tseng, K.-C.; Huang, C.-C.; Shih, W.-Y. A high step-up converter with a voltage multiplier module for a photovoltaic system. *IEEE Trans. Power Electron.* **2013**, *28*, 3047–3057. [[CrossRef](#)]

