



Article An Improved Modulation Method for Suppressing High Frequency Common-Mode Voltage in SiC Motor Drive System

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Abstract: High-frequency common-mode voltage generated by inverters causes severe negative effects, particularly in silicon carbide (SiC) Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs)-driven motors. Additionally, common suppression strategies would increase hardware expenses or sacrifice the switching speed of SiC devices. This article proposes an improved no-zero vector modulation strategy to suppress high-frequency common-mode voltage without increasing the cost of hardware. In this method, only nonzero vectors are utilized to reduce common-mode voltage. Firstly, the influence of different switching states on the characteristics of SiC MOSFETs has been studied by double-pulse tests, which explains why zero vectors will cause more serious voltage oscillations. Secondly, common-mode voltage suppression failure caused by the high-frequency dead zone effect has been analyzed in detail. Based on traditional Active Zero State Pulse Width Modulation (AZSPWM), complementary device conduction logic and dead-zone compensation methods are proposed. In switching moments, different turn-on logic is selected to ensure that only one switch acts, and different dead zone compensation methods are selected to deal with the common-mode suppression failure, which effectively avoids high-frequency common-mode voltage spikes. Finally, simulation and experimental results verify that the improved modulation algorithm can effectively suppress high-frequency common-mode voltage.

Keywords: permanent magnet motor; silicon carbide inverter; common-mode voltage; modulation; electric drive

1. Introduction

Silicon carbide devices have unparalleled advantages in high-frequency and highpower-density applications due to their fast switching speed, high voltage level withstood, and high working temperature, which are designed to improve the efficiency and power density of motor drive systems [1,2]. However, due to the faster switching speed of SiC MOSFETs, the switching transient oscillation is much more serious than that of Si devices, causing electromagnetic compatibility problems to be more serious than those of traditional motor drive systems. Studies have shown that high-frequency common-mode voltage generated by PWM inverters is the main reason for the problems related to EMI in the motor drive system [3]. Therefore, to solve the problems such as EMI in SiC motor drive system, it is necessary to effectively suppress high-frequency common-mode voltage.

Common-mode voltage suppression methods are generally divided into passive suppression [4–6] and active suppression [7–16]. Passive suppression methods reduce common-mode output by adding passive components in the circuit such as common-mode inductors [4] or passive filters [5,6]. Although passive suppression methods can suppress common-mode voltage and its negative effects to a certain extent, they increase the hardware cost and volume. Active suppression methods include inserting an active filter in the circuit [7], adopting a three-phase four-leg converter [8], or changing the inverter control algorithm [9–16]. To overcome the overvoltage problem of AZSPWM and the limited operating range of NSPWM, a modified AZSPWM and a hybrid algorithm have



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Copyright: © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). been proposed in [9]. Reference [9] verified that common-mode voltage can be effectively suppressed under AZSPWM and Near State Pulse Width Modulation (NSPWM), but the influence of dead zone effect on the common-mode voltage is neglected. In addition, the adverse effects of these modulation techniques, e.g., more severe current ripple for AZSPWM [9], have not been discussed for a SiC-based inverter. In reference [10], the influence of dead zone on the common-mode voltage of AZSPWM is analyzed, but only dead zone compensation is carried out for the failure of one of the two effective switching vectors. In reference [11], common-mode chokes and AZSPWM are used to suppress high-frequency common-mode voltage, but the parameter design of common-mode chokes depends on system parasitic parameters, and the value is difficult to determine. These PWM techniques reduce the amplitude of common-mode voltage by cutting back the use of zero vectors. Among the effective modulation techniques for common-mode voltage reduction, AZSPWM in [9] and tri-state pulse width modulation (TSPWM) in [14] are relatively easy to implement. Without utilizing the zero voltage vectors, active zero-state PWM (AZSPWM1, AZSPWM2, and AZSPWM3), remote-state PWM (RSPWM1, RSPWM2, and RSPWM3), and near-state PWM (NSPWM) have been investigated [15], [16]. However, the output waveforms quality is poor when using these methods, especially at a low modulation index. It can be seen that there is a lack of comprehensive systematic research

on high-frequency common-mode voltage in SiC motor drive systems. This paper analyzes common-mode voltage and evaluates and modifies the corresponding suppression method in SiC-based inverters for electric vehicle (EV) applications. In Section 2, double pulse tests of a three-phase full-bridge SiC inverter connected with motor load are carried out to study the influence of different switching states on the characteristics of SiC devices. Double pulse tests results reveal the law of high-frequency voltage oscillation, and based on the test results, no-zero vector modulation is selected to suppress high-frequency common-mode voltage. In Section 3, the conduction logic and dead zone effect of traditional AZSPWM at high switching frequency are analyzed in detail. On the basis of traditional AZSPWM, a set of complementary device conduction logic and dead zone compensation methods are added. In sector switching moments, different turn-on logic is selected to ensure that only one switch acts to avoid the common-mode voltage spike, and different dead zone compensation methods are selected to deal with the common-mode suppression failure caused by different switches. The commutation logic and action time of improved AZSPWM are given in the form of a table. Section 4 presents the simulation and experimental verification, and conclusions are drawn in Section 5.

2. Influence of Voltage Vectors on the Switching Performance of SiC devices

2.1. Definition of Common-Mode Voltage

The typical structure of a two-level three-phase voltage source inverter is shown in Figure 1. According to the definition, common-mode voltage U_{ng} is the voltage between load neutral point n and grounding point g, $U_{ng} = U_{no} + U_{og}$, considering that U_{og} is relatively small and changes slowly, U_{og} can be ignored, and U_{no} is used to approximate the common-mode voltage of the system:

$$U_{no} \approx \frac{U_{ao} + U_{bo} + U_{co}}{3} \tag{1}$$

 U_{ao} , U_{bo} , U_{co} is the voltage between *a*, *b*, *c* and the neutral point o of the capacitor, respectively.



Figure 1. Structure diagram of three-phase voltage source inverter.

The corresponding common-mode voltage value when each switch vector acts is shown in Table 1. Under conventional PWM modulation, common-mode voltage generated by the three-phase two-level inverter is a four-step wave jumping between $\pm V_{dc}/2$ and $\pm V_{dc}/6$.

Vectors	Vao	V_{bo}	V_{co}	Vno
000	$-V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/2$
100	$V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/6$
110	$V_{dc}/2$	$V_{dc}/2$	$-V_{dc}/2$	$V_{dc}/6$
010	$-V_{dc}/2$	$V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/6$
011	$-V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/6$
001	$-V_{dc}/2$	$-V_{dc}/2$	$V_{dc}/2$	$-V_{dc}/6$
101	$V_{dc}/2$	$-V_{dc}/2$	$V_{dc}/2$	$V_{dc}/6$
111	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$

 Table 1. Relationship between switching vectors and common-mode voltage.

2.2. Double Pulse Test of SiC Three-Phase Full Bridge

Double pulse test (DPT) is a widely accepted method for evaluating the characteristics of semiconductor switches. However, in three-phase inverter of a PWM motor drive, the switching performance of SiC devices is always worse than the double pulse test results, which is manifested as slower switching speed, larger switching loss, and more serious ringing. Therefore, a simple double pulse test with load inductance is not enough to represent the actual situation of the inverter in the motor drive system. In order to fully utilize the potential advantages of SiC devices in motor drive systems, this paper systematically evaluates the switching characteristics of three-phase SiC inverter devices with motor loads. First, the eight switching vectors are classified according to the common-mode voltage amplitude in Table 1: I (100, 010, 001), II (110, 101, 011), and III (000, 111). Then, the switching characteristics of the SiC devices are tested under motor load, switching state I, switching state II, and switching state III, respectively, as shown in Figure 2.



Figure 2. Double Pulse Test of SiC Three-phase Full Bridge.

The test results in Figure 3a show that at the turn-on moment, the drain-source voltage V_{ds} of the tested SiC device does not have a voltage spike when a motor load is connected to the half bridge. However, in a three-phase full bridge circuit, as Figure 3b–d indicates, with the changes of phase B and phase C switching states, the higher the amplitude of the common-mode voltage is, the more severe the high-frequency voltage oscillates (d > c > b). In zero vector states, the common-mode voltage is the higher the voltage oscillation is the most serious. The approximate formula $U_{no} \approx (U_{ao} + U_{bo} + U_{co})/3$ demonstrates that high-frequency drain-source voltage oscillation generated by SiC devices during the switching process will lead to high-frequency common-mode voltage oscillation and eventually aggravate a series of negative effects such as electromagnetic interference.



Figure 3. Double-pulse test results.

3. High-Frequency Common-Mode Voltage Suppression Strategy

3.1. Reduced Common-Mode Voltage PWM

In a two-level PWM inverter, the amplitude of common-mode voltage generated by the zero vector is $\pm V_{dc}/2$, and the amplitude of the common-mode voltage is $\pm V_{dc}/6$ when the non-zero vector is applied. Through the double pulse tests in the previous section, it is found that under the action of zero vectors, the leakage-source voltage oscillation of SiC devices will be more serious in the switching process, thus aggravating the high-frequency oscillation of common-mode voltage. Therefore, one idea to suppress high-frequency common-mode voltage is to avoid using zero vectors.

The peak value of common-mode voltage can be reduced by 66.7% by using only six other effective vectors instead of zero vectors. According to the effective vector used, the suppression common-mode voltage PWM can be divided into three categories: active zero state PWM (AZSPWM), remote state PWM (RSPWM), and near state PWM (NSPWM). Taking the reference voltage in the first sector as an example, the combination modes of



the reference voltage vector under three kinds of no-zero vectors modulation are shown in Figure 4.

Figure 4. Reduced Common-Mode Voltage PWM.

Since the use of zero vectors is avoided, all three modulation methods can reduce the common-mode voltage amplitude from $\pm V_{dc}/2$ to $\pm V_{dc}/6$. However, AZSPWM will cause the problem of simultaneous operation of two-phase switches, which will further cause the line voltage polarity to jump rapidly. RSPWM and NSPWM will be limited by the modulation range, and the output line voltage will be distorted, which will cause phase current distortion. In practical applications, all three modulation methods exist: commonmode voltage spikes caused by the dead-time effect and sector jump, and motor-side overvoltage caused by rapid line voltage polarity jumps. In order to avoid being restricted by the linear modulation range, this article focuses on the analysis and improvement of the traditional AZSPWM.

3.2. Dead-Zone Effect under High Switching Frequency

AZSPWM chooses two voltage vectors with 180° difference to replace zero vectors, so that the amplitude of common-mode voltage can be suppressed. Taking the reference voltage in sector I as an example, the order of reference voltage vector synthesis is $U_6 \rightarrow U_1 \rightarrow U_2 \rightarrow U_3 \rightarrow U_2 \rightarrow U_1 \rightarrow U_6$, and the conduction logic sequence of the inverter is shown in Figure 5. According to the principle of volt-second balance, the relationship is as follows:

$$U_1T_1 + U_2T_2 + U_3T_3 + U_6T_6 = U_{ref}T_s$$
⁽²⁾

$$T_1 + T_2 + T_3 + T_6 = T_s \tag{3}$$

When the reference voltage vector position angle θ_r is between 0 and $\pi/6$, if $t_2 < 2t_d$ and $t_1 > 2t_d$, there will be a dead zone overlap area between the inverter output voltage u_{ao} and u_{bo} . In this area, if i_a and i_b are greater than zero at the same time, u_{ao} and u_{bo} will be clamped on the negative pole of the DC bus. At this time, u_{co} is also on the negative pole of the DC bus, so a voltage spike of $-V_{dc}/2$ will appear in common-mode voltage output, and the suppression algorithm becomes invalid.

When the reference voltage vector position angle θ_r is between $\pi/6$ and $\pi/3$, if $t_1 < 2t_d$ and $t_2 > 2t_d$, there will be a dead zone overlap area between the inverter output voltage u_{bo} and u_{co} . In this area, if i_b and i_c are smaller than zero at the same time, u_{bo} and u_{co} will be clamped on the positive pole of the DC bus. At this time, u_{ao} is also on the positive pole of the DC bus, so a voltage spike of $V_{dc}/2$ will appear in common-mode voltage output, and the suppression algorithm becomes invalid.

In summary, under high switching frequency, there is a working interval where the modulation algorithm fails at the moment of sector switching. In order to ensure that the common-mode voltage suppression algorithm is always effective, the modulation algorithm needs to be modified.



Figure 5. Conduction logic sequence of AZSPWM.

3.3. Modified Active Zero State PWM

It can be seen from the analysis in Section 3.2 that under high switching frequency, taking the reference voltage vector located in the first sector as an example, when the action time of an effective voltage vector V_1 , V_2 is less than the dead time or the reference voltage vector switches from sector I to sector II (switching state changing from {101} to {011}), failure of common-mode voltage suppression may occur, and common-mode voltage spikes may emerge. In order to avoid common-mode voltage spikes under high switching frequencies, this article proposes the following improvement measures on the basis of AZSPWM:

To eliminate the common-mode voltage spikes appearing in the sector conversion process, a complementary switching logic is proposed. Without changing the duty cycle time, switching logic Type I inverts the gate signals generated by T_{max} and T_{min} , respectively, and keeps the gate signal generated by T_{mid} ; switching logic Type II inverts the gate signal generated by T_{mid} , and keep the gate signal generated by T_{max} and T_{min} . Type I and II constitute complementary conduction logic and the timing diagram is shown in Figure 6a.



Figure 6. Modified-AZSPWM.

To avoid the suppression failure caused by the dead zone effect, a compensation strategy is proposed. Taking the reference voltage vector in sector I as an example, on the basis of keeping volt-second balance, if V_1 action time is less than the dead zone, the compensation I will be performed according to the vector synthesis method in Figure 6b; if V_2 action time is less than the dead zone, the compensation II will be performed according to the vector synthesis method in Figure 6c. Additionally, other sectors can be deduced by analogy.

The optimized switching logic and action time are shown in Table 2, where $X = \frac{\sqrt{3}T_s u_{\beta}}{U_{dc}} Y = \frac{\sqrt{3}T_s}{U_{dc}} \left(\frac{\sqrt{3}}{2}u_{\alpha} + \frac{1}{2}u_{\beta}\right) Z = \frac{\sqrt{3}T_s}{U_{dc}} \left(-\frac{\sqrt{3}}{2}u_{\alpha} + \frac{1}{2}u_{\beta}\right)$ and μ_{β} are the components of the reference voltage vector on the axis α - β

Sector	Logic	Condition	Compensation	T _{cmpa}	T _{cmpb}	T _{cmpc}
Ι	Type I Type I	$\begin{array}{l} t_1 < 2t_d \\ t_2 < 2t_d \end{array}$	I II	$(T_s + X - Z)/4 - t_d/2$ $(T_s + X - Z)/4 + t_d/2$	$(T_s - X - Z)/4 + t_d/2$ $(T_s - X - Z)/4 - t_d/2$	$(T_s - X + Z)/4 - t_d/2$ $(T_s - X + Z)/4 + t_d/2$
II	Type II Type II	$\begin{array}{l} t_2 < 2t_d \\ t_3 < 2t_d \end{array}$	I II	$(T_s - Y + Z)/4 + t_d/2$ $(T_s - Y + Z)/4 - t_d/2$	$(T_s - Y - Z)/4 - t_d/2$ $(T_s - Y - Z)/4 + t_d/2$	$(T_s + Y + Z)/4 - t_d/2$ $(T_s + Y + Z)/4 + t_d/2$
III	Type I Type I	$\begin{array}{l} t_3 < 2t_d \\ t_4 < 2t_d \end{array}$	I II	$(T_s + Y - X)/4 - t_d/2$ $(T_s + Y - X)/4 + t_d/2$	$(T_s - Y + X)/4 - t_d/2$ $(T_s - Y + X)/4 + t_d/2$	$(T_s + Y + X)/4 + t_d/2$ $(T_s + Y + X)/4 - t_d/2$
IV	Type II Type II	$\begin{array}{l}t_4 < 2t_d \\t_5 < 2t_d\end{array}$	I II	$(T_s + Z - X)/4 - t_d/2$ $(T_s + Z - X)/4 + t_d/2$	$(T_s - Z - X)/4 + t_d/2$ $(T_s - Z - X)/4 - t_d/2$	$(T_s - Z + X)/4 - t_d/2$ $(T_s - Z + X)/4 + t_d/2$
V	Type I Type I	$\begin{array}{l}t_5 < 2t_d \\t_6 < 2t_d\end{array}$	I II	$(T_s - Y + Z)/4 + t_d/2$ $(T_s - Y + Z)/4 - t_d/2$	$(T_s + Y + Z)/4 - t_d/2$ $(T_s + Y + Z)/4 + t_d/2$	$(T_s - Y - Z)/4 - t_d/2$ $(T_s - Y - Z)/4 + t_d/2$
VI	Type II Type II	$\begin{array}{l} t_6 < 2t_d \\ t_1 < 2t_d \end{array}$	I II	$(T_s - Y + X)/4 - t_d/2$ $(T_s - Y + X)/4 + t_d/2$	$(T_s + Y - X)/4 - t_d/2$ $(T_s + Y - X)/4 + t_d/2$	$(T_s + Y + X)/4 + t_d/2$ $(T_s + Y + X)/4 - t_d/2$

Table 2. Voltage Vector Synthesis Logic and Time under Modified AZSPWM.

4. Simulation and Experimental Verification

With a switching frequency of 20 kHz, a DC bus voltage of 300 V, and a dead time of 2 us, the simulation results of the motor common-mode voltage generated by SVPWM, AZSPWM and Modified AZSPWM are shown in Figure 7. Under SVPWM, the common-mode voltage generated by the three-phase two-level inverter is a four-step wave that jumps between $\pm V_{dc}/2$ and $\pm V_{dc}/6$, and its frequency hopping rate is 6 times that of the switching frequency. Under AZSPWM, the common-mode voltage waveform is mostly limited to $\pm V_{dc}/6$, but there are moments when common-mode suppression fails, resulting in common-mode voltage spikes with an amplitude of $\pm V_{dc}/2$. Under Modified AZSPWM, the common-mode voltage spikes with an amplitude of $\pm V_{dc}/2$. Under Modified AZSPWM, the common-mode voltage spikes with an amplitude of $\pm V_{dc}/6$, and there exists no common-mode suppression failure moment, which can effectively suppress common-mode voltage spikes.

Figure 7. Common-mode voltage waveform at 20 kHz switching frequency.

The experiment platform was a 7.5 KW permanent magnet synchronous motor drag platform, which is driven by Cree CCS050M12CM2 Silicon Carbide full-bridge module. Drive circuit adopted CGD15FB45P1, and the controller was TMS320F28335 control chip produced by TI company. Current sampling adopted Hall Current Sensor HNC-50LT for measurement. The measuring instruments were CYBERTEK DP6150B and Tektronix MDO34 digital oscilloscope, as shown in Figure 8. In order to facilitate the measurement, the common-mode voltage was indirectly measured by measuring the three-phase terminal voltage of the motor. Under SVPWM, AZSPWM, and Modified AZSPWM modulation, the three-phase terminal voltage waveforms of the motor are shown in Figures 9–11.

Figure 8. Experimental platform.

Under SVPWM, there are serious voltage oscillations and over-voltage phenomena at the moment of switching action, which is the most serious at the moment of zero-vector switching. Additionally, traditional AZSPWM can alleviate the high-frequency voltage oscillation in the SiC switching process, but there will be phenomena such as multiple switches operating at the same time, incomplete attenuation of voltage oscillation during the conduction time, and overvoltage. Modified AZSPWM ensures only one switching action at the time of sector conversion, avoiding rapid jumps in line voltage polarity. By selecting different dead-zone compensation strategies, it can effectively suppress highfrequency voltage oscillation and overvoltage phenomena, thereby reducing the commonmode voltage. The amplitude of common-mode voltage is limited to $\pm V_{dc}/6$, so that high-frequency common-mode voltage can be effectively suppressed.

Figure 9. Three-phase voltage waveform of SVPWM different switching states.

Figure 10. Three-phase voltage waveform of AZSPWM different switching states.

Figure 11. Three-phase voltage waveform of Modified-AZSPWM different switching states.

5. Conclusions

In this paper, high-frequency common-mode voltage in the SiC motor drive system is analyzed and researched in detail. By analyzing the switching characteristics of SiC devices under different switching states, a no-zero-vector modulation method is selected to suppress the common-mode voltage. The influence of the dead zone effect of traditional no-zero vector modulation under high switching frequency is analyzed, and an improved zero-free vector modulation method is proposed to suppress the high-frequency commonmode voltage of the system.

- The root of high-frequency common-mode voltage oscillation in SiC motor drive system is from the voltage V_{ds} oscillation during the conduction process of the SiC device. At the time of switching, the higher the amplitude of the common-mode voltage, the stronger the high-frequency voltage oscillation of the SiC device. In the zero vector (000, 111) state, the common-mode voltage amplitude is the highest, and the high-frequency voltage oscillation generated by the device is the most serious.
- Traditional AZSPWM method for suppressing common-mode voltage causes the problem of simultaneous operation of two-phase switches. At high switching frequencies, the dead zone effect causes common-mode suppression to fail, resulting in commonmode voltage spikes with an amplitude of $\pm V_{dc}/2$. The improved AZSPWM adds a set of complementary device turn-on logic to ensure that only one switch acts at the same time, avoiding common-mode voltage spikes caused by sector switching. In view of the influence of the dead zone effect of different switches, different dead zone compensation methods are selected to limit the common-mode voltage amplitude to $\pm V_{dc}/6$.
- Without increasing hardware cost and sacrificing SiC switching speed, the improved AZSPWM proposed in this paper can solve common-mode voltage suppression failure caused by the dead-zone effect at a high switching frequency and suppress high-

frequency voltage oscillation and the overvoltage phenomenon. This can effectively suppress high-frequency common-mode voltage, thereby alleviating the negative effects of high-frequency common-mode voltage in SiC motor drive systems.

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