



Article Multi-Port High Voltage Gain Modular Power Converter for Offshore Wind Farms

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Abstract: In high voltage direct current (HVDC) power transmission of offshore wind power systems, DC/DC converters are applied to transfer power from wind generators to HVDC terminals, and they play a crucial role in providing a high voltage gain, high efficiency, and high fault tolerance. This paper introduces an innovative multi-port DC/DC converter with multiple modules connected in a scalable matrix configuration, presenting an ultra-high voltage step-up ratio and low voltage/current rating of components simultaneously. Additionally, thanks to the adoption of active clamping current-fed push–pull (CFPP) converters as sub-modules (SMs), soft-switching is obtained for all power switches, and the currents of series-connected CFPP converters are auto-balanced, which significantly reduce switching losses and control complexity. Furthermore, owing to the expandable matrix structure, the output voltage and power of a modular converter can be controlled by those of a single SM, or by adjusting the column and row numbers of the matrix. High control flexibility improves fault tolerance. Moreover, due to the flexible control, the proposed converter can transfer power directly from multiple ports to HVDC terminals without bus cable. In this paper, the design of the proposed converter is introduced, and its functions are illustrated by simulation results.

Keywords: high voltage direct current (HVDC); power transmission; DC/DC converter; high voltage gain; modular; multi-port

1. Introduction

The global number of offshore wind farms has increased in recent years [1,2]. In Europe, 560 new offshore wind turbines were built in 17 wind farms in 2017 with a total generation capacity of 3148 MW, which is about 20% of the total offshore generation capacity [3]. The power generated offshore is typically transmitted over an average distance of 41 km (in 2017) through submarine cables before reaching a connection point with the existing onshore grid [3]. For example, Hornsea wind farm is located around 40 km from the onshore station. Compared with high voltage alternating current (HVAC) transmission, high voltage direct current (HVDC) transmission is the preferred method to transfer power over a long distance (>40 km) in terms of the factors of economy and power efficiency [4,5]. When delivering the same amount of power, the purchase price for the bipolar HVDC cable is lower than that of two parallel 3-core HVAC ones [6]. Additionally, HVDC has a higher transmission efficiency than HVAC since no inductance-reactive power exists within DC transmission cables.

Figure 1 presents three HVDC configurations. The hybrid HVDC system illustrated in Figure 1a uses a medium voltage (MV)—high voltage (HV) AC/DC converter to obtain high voltage DC power. However, line-frequency (50/60 Hz) AC/AC transformers for low-voltage (LV)—MV conversion still occupy a significant portion of the substation space. In this topology, the transformer is replaced by a converter as shown in Figure 1b, which significantly reduces the system size and weight [7]. These two configurations use two-stage conversion to meet the voltage level of HVDC transmission. However, Reference [8] points out that the configuration of two DC/DC conversion stages has the highest power loss, which is around four times that of a one conversion stage configuration presented in Figure 1c taking into consideration the winding and core losses of transformers and the given datasheets of the semiconductors. The converter applied in Figure 1c not only provides a high voltage gain but also transfers power directly from multiple generators to HVDC terminals without bus cable. The converter design is a technical challenge for boosting LV directly to HV due to the conflict between the required high voltage level, e.g., ± 800 kV [9] and the restricted voltage ratings of semiconductor components, e.g., 22 kV for SiC thyristors, and 15 kV for SiC transistors [10]. Fortunately, with the development of semiconductors and converter topologies, possible solutions are provided [11–13].



Figure 1. High voltage direct current (HVDC) configurations for wind power transmission: (a) DC-based connection with two-stage hybrid conversion; (b) DC-based connection with two-stage DC/DC conversion; (c) DC-based connection with the proposed modular converter.

To address the challenges, DC converters with high voltage gains [14–17], modular multilevel converters (MMCs) [18–22] and multi-module converters [23–25] are studied extensively. Although dual-active bridge (DAB) converters [14,15] and resonant converters [16,17] can obtain high voltage step-up ratios, the voltage stress on their semiconductor components is high, which can be reduced by applying MMCs. By adding sub-modules (SMs), a high output voltage is achieved without increasing the voltage stress. However, the MMC topologies based on half-bridge (HB) or full-bridge (FB) [18,19] and resonant MMC [20] cannot provide electrical isolation. The isolated MMCs in References [21,22] are presented with DC/AC/DC configuration, where medium-frequency high turns-ratio transformers are employed, resulting in a vast volume. Although resonant MMCs [26]

achieve galvanic isolation and a small volume of transformers at the same time, its conversion ratio only satisfies MV applications. Alternatively, transformers can be decentralized into multi-module converters, enabling the installation of high-frequency transformers, which reduces the sizes of transformers and reactive components. However, by adopting active-clamping flyback–forward converters as SMs, the currents of different SMs are unbalanced because of the non-ideal factors such as unequable leakage inductances of transformers, and only half of the power switches can achieve zero voltage switching (ZVS), resulting in high switching losses [23].

In this paper, based on the multi-modular converter in Reference [23], active-clamping current-fed push–pull (CFPP) converters are adopted to replace the flyback–forward SMs. The currents of modules in series-connection are auto-balanced, and all power switches can achieve soft-switching. Therefore, control complexity and switching loss are reduced. Furthermore, the matrix configuration brings about high control flexibility, which improves the fault tolerance capability. Additionally, thanks to the independent operation of each port, the converter can collect power from multiple sources without bus cable.

The paper is organized as follows: The basic cell and two interleaved working modes are analyzed in Section 1; the scalable topology design is discussed in Section 3; Section 4 depicts the fault tolerance strategies of the topology; simulation results are presented in Section 5 to demonstrate the effectiveness and efficiency of the converter, and finally, conclusions are drawn in Section 4.

2. Analysis of the Basic Cell and Working Strategies of Matrix Configuration

2.1. Operation of the Basic Cell

The basic cell topology based on CFPP converter shown in Figure 2 has similar operation principles and characteristics as the converter presented in Reference [27]. S_1 – S_2 are the two main switches. S_{c1} – S_{c2} are the two active clamping switches. C_c is the clamp capacitor. L_1 is the input transistor. The tri-winding transformer has a turns ratio of N_{p1} : N_{p2} : $N_s = 1:1:n$ and leakage inductance L_k at the secondary side. Furthermore, the secondary circuit consists of four rectifier diodes D_1 – D_4 , one output capacitor C_{out} and a load resistor R.



Figure 2. Topology of the basic cell based on active-clamping fed push-pull (CFPP) converter.

The key operating waveforms of CFPP cell are depicted in Figure 3. $V_{gs1}-V_{gs2}$ are the control signals for the two main switches S_1-S_2 , which have the phase shift angle of 180° . $V_{gsc1}-V_{gsc2}$ are the control signals for the two clamp switches $S_{c1}-S_{c2}$. The control signals of the main switches and clamping switches are complementary. $v_{ds1}-v_{ds2}$ and $v_{dsc1}-v_{dsc2}$ are the drain-to-source voltages of the main switches and clamping switches respectively. i_{L1} is the current of input inductor L_1 . v_s and i_s are the secondary voltage and current of the transformer respectively. The following assumptions are made to simplify the analysis.



Figure 3. Operating waveforms of the basic cell.

- All switches and diodes are identical.
- The capacitance of clamp capacitor is large enough so that its voltage ripple can be ignored. Due to the symmetrical operation, a brief introduction of the operation during t₀−t₅ when D ≤ 0.5 is presented in this part.

Mode 1 (t_0 - t_1): In this mode, the main switch S_1 and the clamping switch S_{c2} are on. The power is transferred to the output. The diodes D_2 and D_3 are forward biased, and the secondary current i_s decreases.

Mode 2 (t_1 – t_2): At t_1 , the main switch S_1 is turned off. The leakage inductances L_k resonate with the parasitic capacitances of S_1 and S_{c1} . Then, the voltage of S_{C1} drops to zero at t_2 to achieve ZVS turn-on. At the same time, capacitance C_{S1} is charged.

Mode 3 (t_2-t_3) : At t_2 , the clamping switch S_{C1} is turned on with zero voltage. Because both the clamping switches S_{C1} and S_{C2} are on, the primary sides of the transformer are short-circuited. Then the power is transferred to the input inductor L_1 , and the secondary current i_s rises rapidly.

Mode 4 (t_3 – t_4): At t_{3} , the secondary current reaches zero. All four diodes are reverse biased. Additionally, the secondary voltage recovers to zero within a short time.

Mode 5 (t_4 – t_5): At t_4 , the clamping switch S_{C2} is turned off. The leakage inductances L_k resonate with parasitic capacitances of S_2 and S_{C2} . The voltage across S_2 drops to zero at t_5 so that ZVS turn-on of S_2 is obtained.

The operation in intervals (t_0-t_5) and (t_5-t_{10}) is symmetrical. The power is transferred to the output load *R* when one main switch and one clamping switch are on, and then the power flows from the input to inductor L_1 when both clamping switches are on. All switches can obtain ZVS turn-on and the energy stored in L_k is recycled by the parasitic capacitances of clamping switches, which contributes to a higher conversion efficiency.

The voltage of clamp capacitor V_{Cc} can be obtained according to the flux balance of L_1 :

$$V_{Cc} = \frac{V_{in}}{1 - D} \tag{1}$$

Additionally, with the turns ratio as 1:1:*n*, the output voltage of basic cell $V_{o,BC}$ can be determined:

$$V_{o,BC} = \frac{n}{2} V_{Cc} = \frac{n}{2} \frac{V_{in}}{(1-D)}$$
(2)

The voltage stress of all four power switches V_{ds} can be obtained by:

$$V_{ds} = V_{Cc} = \frac{V_{in}}{1 - D} \tag{3}$$

2.2. Working Strategies of Matrix Configuration

A fundamental 2×2 modular topology is presented in Figure 4. The primary circuits of power cells are parallel connected so that they have an equal secondary voltage value with the same duty cycle of main switches. The secondary side of each cell is connected with four rectifier diodes for power regulation.



Figure 4. 2×2 topology of the isolated high voltage gain DC/DC converter with basic cells.

As illustrated in Figure 5a,b, adjacent cells have opposite polarities in column interleaved modes. For example, the polarity of cell 11 is opposite to those of cell 21 and 12. In this case, cells in the same column are connected in series, and the adjacent columns are in parallel connection. The voltage ratings of diodes in the first and last rows, $D_{00}-D_{02}$ and $D_{20}-D_{22}$, are equal to the voltage of power cells v_s . While the voltage ratings of other diodes $D_{10}-D_{12}$ have twice the value of v_s since they are connected with two cells. The current stresses of diodes in the first and last columns, $D_{00}-D_{20}$ and $D_{02}-D_{22}$ have the same value as the secondary current of one column. Diodes $D_{01}-D_{21}$ connect with two columns so that they have double the current stress of the others. Additionally, the sum of the average diode currents in all columns is equal to the output current. Therefore, in column interleaved modes, the voltage and current ratings of diodes in an expanded topology as shown in Figure 6 composed of *s* rows and *p* columns can be obtained:

$$V(D_{ij}) = \begin{cases} \frac{1}{s} V_{o,s \times p} = V_{o,BC} = \frac{n}{2(1-D)} V_{in} & i = 0, s \\ \frac{2}{s} V_{o,s \times p} = 2 \times V_{o,BC} = \frac{n}{(1-D)} V_{in} & i = 1, 2, \cdots, (s-1) \end{cases}$$
(4)

$$I(D_{ij}) = \begin{cases} \frac{1}{2}I_{o,BC} = \frac{1}{2p}I_{o,s \times p} & j = 0, p\\ I_{o,BC} = \frac{1}{p}I_{o,s \times p} & j = 1, 2, \cdots, (p-1) \end{cases}$$
(5)

$$\sum_{i=0}^{p} I(D_{ij}) = I_{o,sp} \tag{6}$$

where $I_{o,BC}$ is the average output current of a single basic cell; $V_{o,s\times p}$ and $I_{o,s\times p}$ are the output voltage and current of $s \times p$ topology. In this case, all semiconductor components have low voltage and current ratings.



Figure 5. 2×2 topology with different interleaved strategies: (a) Column interleaved mode 1; (b) Column interleaved mode 2; (c) Series interleaved mode 1; (d) Series interleaved mode 2.





Figure 6. Topology of the proposed converter with three input-ports: (**a**) primary circuits with three power sources; (**b**) secondary circuits collecting power and delivering it to load.

From Figure 5c,d, in series interleaved modes, all cells are series-connected. The cells in adjacent rows have the opposite polarities while the cells in the same row have the same polarity. Similar to Equation (4), diodes D_{10} and D_{12} have twice the voltage rating higher than that of diodes in the first and last rows because they connect with two rows. The currents of all operating diodes have the same value since they are in series-connection. Hence, the voltage and current ratings of diodes in series interleaved modes can be calculated as:

$$V(D_{ij}) = \begin{cases} \frac{1}{s} V_{o,s \times p} = p \times V_{o,BC} = \frac{p \times n}{2(1-D)} V_{in} & i = 0, s \\ \frac{2}{s} V_{o,s \times p} = 2p \times V_{o,BC} = \frac{p \times n}{(1-D)} V_{in} & i = 1, 2, \cdots, (s-1) \end{cases}$$
(7)

$$I(D_{ij}) = \frac{1}{2}I_{o,BC} = \frac{1}{2}I_{o,s \times p} \qquad j = 0, p$$
(8)

According to Equation (8), for series interleaved modes, the current rating of diodes is increased with the increase of output power. Besides which, the diodes D_{01} – D_{21} are blocked, which benefits the fault tolerance operation to be described in Section 4.

3. Analysis of the Proposed Converter with Multi-Input Ports

3.1. Scalable Topology

Thanks to modularity, multi-module converters can be easily expanded by increasing its row number and column number to attain a high voltage gain and the desired high power level. In the normal scenario, the proposed converter operates with column interleaved modes to keep a low voltage/current rating of components. Three wind-turbine-generators, WTGs 1–3, are connected to the proposed converter as illustrated in Figure 6a. Figure 6b shows the secondary circuits that are divided into three independent, Groups 1–3, by diodes $D_{1-0p}-D_{1-sp}$, $D_{2-0p}-D_{2-sp}$, $D_{3-00}-D_{3-s0}$ on the basis of input ports. The output power of each group consisting of the $s \times p$ expanded topology can be controlled individually, and the bus cable is eliminated. With the same input voltage and power of each port, the voltages and currents of all basic cells are identical.

The cells in the same column are in series-connection. Hence, every column has the same terminal voltage which is the sum of the voltages of cells in the same column. For a converter with multi-ports, output voltage V_{out} equals to the identical terminal voltage of columns and the output current I_{out} is the sum of secondary currents of all columns. Therefore, the row number *s* determines the output voltage, and the group number *x* with column number *p* determines the output power.

$$\begin{cases} V_{out} = V_{o,s \times p} = s \times V_{o,BC} = \frac{s \times n}{2(1-D)} V_{in} \\ I_{out} = x \times I_{o,s \times p} = x \times p \times I_{o,BC} \end{cases}$$
(9)

3.2. Current Balance with Column Interleaved Mode

The control complexity is reduced by the auto-balanced currents of cells in the same column. According to the currents through diodes D_{10} – D_{13} and D_{20} – D_{23} , as shown in Figure 7, the relationships among all cells can be obtained as:

$$\begin{cases} I_{o,BC11+} + I_{o,BC12+} = I_{o,BC21+} + I_{o,BC22+} \\ I_{o,BC31+} = I_{o,BC21+} \\ I_{o,BC23+} = I_{o,BC13+} \\ I_{o,BC32+} + I_{o,BC33+} = I_{o,BC22+} + I_{o,BC23+} \end{cases}$$
(10)

$$\begin{cases} I_{o,BC11-} = I_{o,BC21-} \\ I_{o,BC31-} + I_{o,BC32-} = I_{o,BC21-} + I_{o,BC22-} \\ I_{o,BC12-} + I_{o,BC13-} = I_{o,BC22-} + I_{o,BC23-} \\ I_{o,BC33-} = I_{o,BC23-} \end{cases}$$
(11)

where $I_{o,BC+}$ is the average current of secondary circuit in the interval (t_0-t_5) and $I_{o,BC-}$ is that in the interval (t_5-t_{10}) . According to the symmetrical operation of the basic cell between the two intervals, it can be derived that $I_{o,BC+} = I_{o,BC-}$. Therefore, Equation (12) is obtained with $I_{o,BC} = I_{o,BC+} + I_{o,BC-}$.

$$\begin{cases} I_{o,BC11} = I_{o,BC21} = I_{o,BC31} \\ I_{o,BC12} = I_{o,BC22} = I_{o,BC32} \\ I_{o,BC13} = I_{o,BC23} = I_{o,BC33} \end{cases}$$
(12)

According to Equation (12), the average currents for cells in the same column are auto-balanced. Therefore, as shown in Figure 8, only the control of output voltage and current sharing in different columns is employed to achieve the required output voltage and power in the $s \times p$ topology, where $v_{o,ref}$ is the desired output voltage and $i_{L,i1}-i_{L,ip}$ are the currents collected from columns 1–*p*.



Figure 7. Auto-balanced currents of cells in the same column with column interleaved working strategy: (a) Column interleaved working mode 1; (b) Column interleaved working mode 2.



Figure 8. Control scheme of the $s \times p$ topology.

4. Fault Tolerance

4.1. Fault Tolerance for WTGs with Different Output Power

When disturbances occur, proper control strategies of WTGs and converters should be applied to ensure system protection and high power efficiency [28,29]. For the proposed converter, the output power of one group is determined not only by the column number of the secondary circuits but also,

by the duty-cycles of main switches. According to Equation (8), the output power of one group is obtained as:

$$P_{group} = (p - m) \times V_{out} \times I_{o,BC}$$
(13)

where *m* is the number of idle column in the corresponding group.

The variation of a duty-cycle will cause the change of currents through the cells in one column as:

$$I_{sub} = I_{o,BC} = \frac{2}{T_s} \cdot \int_0^{t_{on}} i_{out} \approx i_{\max} \cdot D$$
(14)

Hence the output power is:

$$P_{group} = p \cdot V_{out} \cdot I_{sub} = p \cdot D \cdot V_{out} \cdot i_{max}$$
(15)

where i_{max} is the maximum output current of power cells.

4.2. Fault Tolerance for Semiconductor Components

Semiconductor components are vulnerable components in a converter [30]. For offshore HVDC stations, faulty components take a long time for maintenance, resulting in high cost and loss [31].

Figure 9 shows the fault tolerance operation derived by installing redundant power cells. To maintain normal operation, the column in a red dotted box containing the damaged Cell 11 is replaced by one redundant column that is in the other red dotted box. For the faulty diodes $D_{00}-D_{s0}$, they require only one redundant column since they connect with one column. However, for other diodes, two redundant columns are demanded. For example, when diode D_{11} fails, the columns 1–2 in the blue dotted box are idle, and the redundant columns p1-p2 are applied.

$$V_{o,FBC} = \frac{V_{o,s \times p}}{2 \times s} = \frac{1}{2} V_{o,BC}$$

$$\tag{16}$$



Figure 9. Fault tolerance with redundancy.

The proposed topology can also obtain fault tolerant operation of diodes and power switches without redundancy. In Figure 10a,b, when diode D_{11} is short-circuited, the cells in rows 1–2 are inactive to block the faulty components, while the fault tolerance group still operates with the column interleaved strategy. Additionally, to maintain normal operation, the output voltages of the faulty group are controlled according to Equations (2) and (9) to ensure the output voltage is the same as that in the normal case. When diode D_{11} is open-circuited as illustrated in Figure 10c,d, the fault tolerant operation group consisting of two columns works under the series interleaved modes to block D_{11} . Compared with the normal operation group, the number of cells in series connection in the faulty

group is doubled. The voltages of cells in the fault group are adjusted as illustrated in Equation (15) to ensure they have the same terminal voltage.

Moreover, the fault tolerant operation of damaged cells without redundancy is similar to that when diodes are short-circuited. For instance, when cell 11 fails, cells 11-1p and 21-2p are idle so that the faulty one is blocked.



Figure 10. Fault tolerance without redundancy: (a) Working mode 1 under diode short-circuit;(b) Working mode 2 under diode short-circuit; (c) Working mode 1 under diode open-circuit;(d) Working mode 2 under diode open-circuit.

5. Simulation Results and Discussion

To illustrate the functionality of the proposed power converter, a simulation model consisting of 3 groups \times 4 rows \times 5 columns with 2 redundant columns is built by software *PSIM*, which is similar to the model shown in Figure 6. The cells in columns 1–3 are active, while those in columns 4–5 are inactive.

Table 1 presents the initial values for the simulation. It is noted that to verify the auto-balanced current characteristic, the leakage inductances of cells in column 1 are set as 70, 75, 80, 85 μ H.

Table 1. Initial values of simulation.

Values	Components	Values
650 V	Turns ratio 1:1: <i>n</i>	1:1:2
6400 V	Leakage inductance	80 µH
5 kHz	Input inductance	5 mH
40 kW	Clamp capacitor	20 µF
	Values 650 V 6400 V 5 kHz 40 kW	ValuesComponents650 VTurns ratio 1:1:n6400 VLeakage inductance5 kHzInput inductance40 kWClamp capacitor

The steady-state waveforms of the converter with the same input power from WTGs are shown in Figure 11. All groups work under the column interleaved strategy, and the voltages of the adjacent

cells in the same column have opposite polarities. Meanwhile, the currents of cells with diverse leakage inductances in column 1 are almost equal. The voltage stress of power switches is 1/4 of the output voltage, and all diodes have the voltage and current stresses as low as 1/4 or 1/2 of the output voltage and current, respectively.

For Figure 12, every group has different numbers of rows. Only one row operates in Group 1; in Group 2, there are two rows; Group 3 has four rows. The duty-cycle *D* of cells in each group is regulated to obtain the same terminal voltage, and the voltages of cells are shown in Figure 12 as: $V_{s_cell \ 1-11} = 2 \times V_{s_cell \ 2-11} = 4 \times V_{s_cell \ 3-11} = V_{out}$.

The peak current values of different columns are almost equal so that the duty-cycle power transmission control presented in Equation (15) is verified.

Figure 13 shows the voltages of diodes in Group 1–2. The voltage of diodes in Group 3 has the same waveforms as those presented in Figure 10. It can be found that the voltage value is increased as the number of idle rows increases.



Figure 11. Steady-state waveforms for cells and diode: (a) voltage/current of basic cells; (b) voltage/current of diodes.



Figure 12. Waveforms of cells when Groups 1–3 have different output power.



Figure 13. Voltages of diodes in each Group when Groups 1–3 have different output power: (**a**) Voltages of diodes in Group 1; (**b**) Voltages of diodes in Group 2.

As illustrated in Figure 14, before turning on switches S_1 or S_{C1} , the drain-to-source current flows through the parasitic diode of the switch to achieve ZVS operation. Similarly, the switches S_2 and S_{C2} can also obtain soft-switching. Therefore, the switching loss is significantly reduced.



Figure 14. Zero voltage switching (ZVS) of main switches and clamping switches.

Figure 15a shows the fault tolerance operation with redundancy. At 0.07 s, fault cells 1–2 are idle, and the redundant columns 4–5 start to work to guarantee normal operation. Figure 15b,c presents the fault tolerance without redundancy, where only columns 1–3 are active. In Figure 15b, when the diode D_{11} is short-circuited, the cells in rows 1–2 are blocked. The voltages of cells in row 3–4 are doubled to achieve the same terminal voltage. The diode D_{11} is open in Figure 15c. The faulty group consisting of columns 1–2 works in the series interleaved mode by changing the polarities of cells. Moreover, the voltages of cells in the faulty group are reduced to half of that in the normal operation group to obtain the same output voltage.



Figure 15. Fault tolerance operation: (a) With redundancy; (b) Without redundancy for D_{11} short-circuit; (c) Without redundancy for D_{11} open-circuit.

Where *N* is the number of SMs or power cells; n is the turns ratio of transformers. Table 2 shows a performance comparison among several literatures. Due to hard switching, References [21,23] have higher switching losses. Multi-module converters can achieve a higher voltage step-up ratio by increasing the power cells number and the voltage gain of power cells. For MMCs, fault tolerance is achieved by redundancy. However, the proposed converter has an improved fault tolerance capability which can maintain normal operation without redundancy. Therefore, to achieve the same performance, a multi-module converter with CFPP cells requires fewer components.

Table 2. Performance comp	arison.
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	MMCs		Multi-Module Converters	
	HB/FB [21,32]	Resonant MMC [20]	Flyback–Forward [23]	CFPP Converter
Soft-switching	×	\checkmark	×	\checkmark
Conversion ratio	$\propto N, n$	$\propto N$	$\propto N, \frac{1}{1-D}, n$	$\propto N, \frac{1}{1-D}, n$
Transformer	Large	×	Small	Small
Fault tolerance	Low	Low	Medium	High

6. Conclusions

A multi-port high voltage gain modular DC/DC power converter applied in offshore wind farms is proposed in this paper. Thanks to the modularity, the high output voltage and power is achieved

by adding power cells. With the independent operation of each port and high control flexibility, the converter can collect power from multi-sources without bus cable. Additionally, the CFPP cells reduce the switching losses and control complexity.

The performances of MMC with galvanic isolation, resonant MMC, multi-module converter with flyback–forwarding cells and CFPP cells are compared. The proposed model appears to be more efficient and reliable, including fewer switching losses, higher conversion ratio, fewer components, smaller volume, and higher reliability.

The simulation results verify the advantages of the proposed converter are the soft-switching of all power switches, flexible control, and improved fault tolerance operation.

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