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# In-Built N<sup>+</sup> Pocket Electrically Doped Tunnel FET With Improved DC and Analog/RF Performance

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Received: 3 October 2020; Accepted: 25 October 2020; Published: 27 October 2020



**Abstract:** In this paper, we present an in-built N<sup>+</sup> pocket electrically doped tunnel FET (ED-TFET) based on the polarity bias concept that enhances the DC and analog/RF performance. The proposed device begins with a MOSFET like structure (n-p-n) with a control gate (CG) and a polarity gate (PG). The PG is biased at  $-0.7$  V to induce a P<sup>+</sup> region at the source side, leaving an N<sup>+</sup> pocket between the source and the channel. This technique yields an N<sup>+</sup> pocket that is realized in the in-built architecture and removes the need for additional chemical doping. Calibrated 2-D simulations have demonstrated that the introduction of the N<sup>+</sup> pocket yields a higher  $I_{ON}$  and a steeper average subthreshold swing when compared to conventional ED-TFET. Further, a local minimum on the conduction band edge ( $E_C$ ) curve at the tunneling junction is observed, leading to a dramatic reduction in the tunneling width. As a result, the in-built N<sup>+</sup> pocket ED-TFET significantly improves the DC and analog/RF figure-of-merits and, hence, can serve as a better candidate for low-power applications.

**Keywords:** band-to-band tunneling (BTBT); polarity gate (PG); ON-state current; electrically doping; tunnel FETs (TFETs)

## 1. Introduction

A tunnel field-effect transistor (TFET) is considered to be one of the most promising candidates for low-power applications [1–5]. TFET devices transport carriers by band-to-band tunneling (BTBT), which differs from the drift-diffusion working principle of conventional metal-oxide-semiconductor field-effect transistor (MOSFET). Theoretically, TFET can break through the limit of thermoelectric potential, obtain an ultra-steep subthreshold swing (SS) below 60 mV/dec at room temperature, and achieve extremely high on/off current ratio at very low voltage. However, the low ON-state current of TFET, originating from the large tunneling resistance at the tunneling junction, limits its application in high-speed integrated circuits [6]. Source-pocket (PNPN) TFETs have been investigated to overcome these shortcomings [7,8]. The PNP TFET has the same structure as the conventional p-i-n TFET, except that a narrow N<sup>+</sup> doped pocket is introduced between the source and the channel. Compared with the conventional TFET, the PNP TFET exhibits an increased ON-state current, enhanced SS, and improved device reliability [9,10]. Although the introduction of the N<sup>+</sup> pocket can improve electrical characteristics, it is still a technical challenge to realize such a narrow and highly doped pocket [11–14].

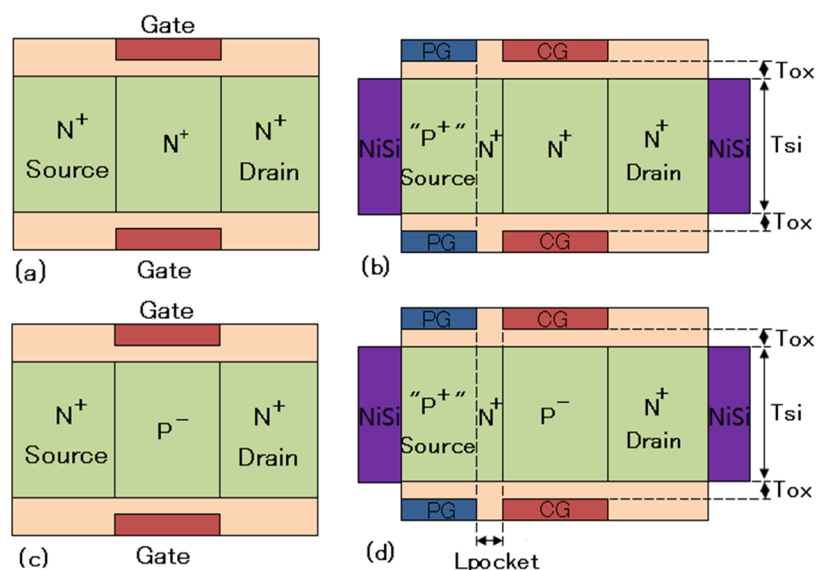
To address the aforementioned issues, we propose an in-built N<sup>+</sup> pocket electrically doped TFET (ED-TFET) using the polarity bias concept [15–17], where the narrow N<sup>+</sup> pocket is realized in the in-built architecture and does not require additional chemical doping. Recently, an ED-TFET with bandgap engineering for analog/RF applications has been reported, which uses the polarity bias

concept on a junctionless (JL)  $N^+$  starting structure and shows simplicity in fabrication steps [18]. However, using calibrated two-dimensional simulations, we demonstrate that the proposed in-built  $N^+$  pocket ED-TFET exhibits improved DC and analog/RF characteristics compared to the conventional Silicon-based ED-TFET.

In this work, we investigate device design and DC and analog/RF performances of the proposed transistors with regard to several key parameters. First, the device concept, as well as the principle of operation, is discussed in Section 2. Second, simulation results and considerations for optimal design are described in Section 3. Finally, Section 4 draws conclusions by summarizing the attractive properties of the proposed in-built  $N^+$  pocket ED-TFETs.

## 2. Device Structure and Operating Principle

To investigate the DC and analog/RF performance of an ED-TFET with an insertion of an  $N^+$  pocket, the proposed device has been simulated in comparison with a conventional ED-TFET without an  $N^+$  pocket. Figure 1a,b show the cross-sectional views of the starting JL field-effect transistor (FET) structure and the final structure of conventional ED-TFET, respectively. Figure 1c,d show the cross-sectional views of the starting MOSFET structure and the final structure of the proposed in-built  $N^+$  pocket ED-TFET. Both types of devices are composed of two sets of gate electrodes: a control gate (CG) and a polarity gate (PG). The effective tunneling barrier of the devices can be modulated by adjusting the work function of the CG. In addition, the PG embedded on the source side is used to convert part of the  $N^+$  doped source into a “ $P^+$ ” region, as depicted in Figure 1b,d. To create a  $P^+$  source region, the PG terminal is biased by an adequate negative voltage to increase the carrier concentration to  $\sim 10^{19} \text{ cm}^{-3}$ . Source and drain contacts are composed of nickel silicide (NiSi) with a Schottky barrier height of 0.45 eV.



**Figure 1.** Cross-sectional views of (a) Beginning JL FET structure to realize conventional electrically doped TFET (ED-TFET), (b) Conventional ED-TFET [19], (c) Beginning MOSFET structure to realize the in-built  $N^+$  pocket ED-TFET, (d) In-built  $N^+$  pocket ED-TFET. JL FET, junctionless field-effect transistor; ED-TFET, electrically doped tunnel field-effect transistor; MOSFET, metal-oxide-semiconductor field-effect transistor.

The main fabrication processes of the proposed in-built  $N^+$  pocket ED-TFET are listed as in the following steps. In the first step, the devices can be fabricated using nonplanar technologies, exploiting deep reactive ion etching (DRIE) or Bosch processes to form device channels [18]. The gate oxide is then deposited on the whole channel following by the deposition of the control gate. After that, the polarity gate is patterned all around the channel using e-beam lithography. After both sets of gates

are formed, the spacers are patterned, and a nickel layer is deposited to generate NiSi at the source and drain contacts [16].

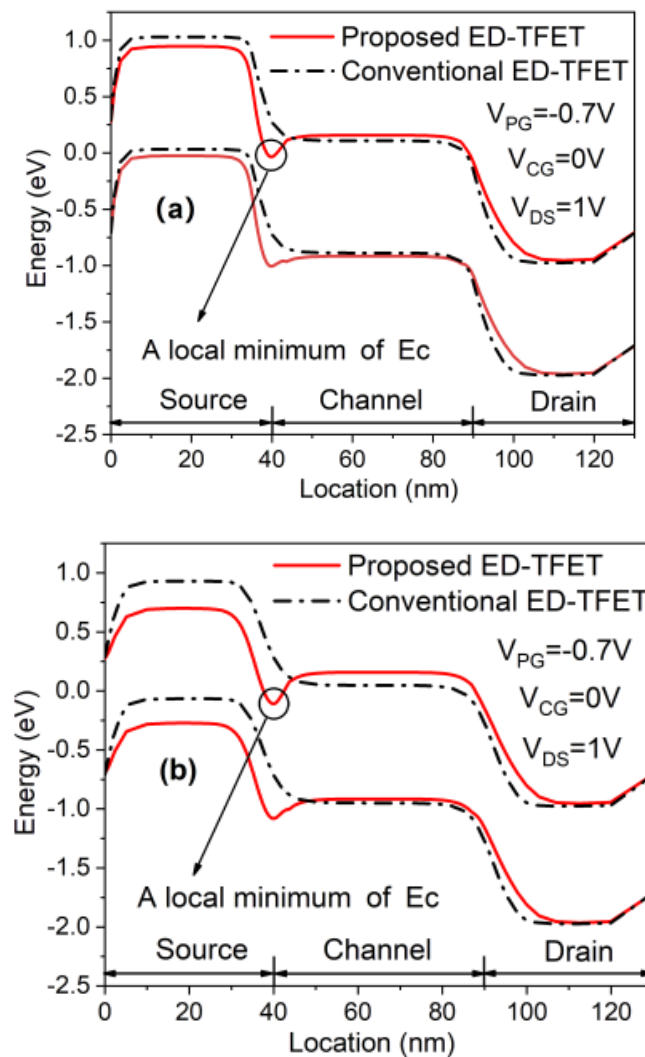
The major difference between conventional ED-TFET and the proposed in-built  $N^+$  pocket ED-TFET lies in the doping concentration in their starting structures. In a conventional ED-TFET, the film is uniformly doped with no p-n junctions. Using the concept of polarity bias, the  $N^+$ - $N^+$ - $N^+$  film (source, channel, and drain) is converted into  $P^+$ -I- $N^+$  gated structure, similar to a conventional TFET. The spacer thickness between the CG and PG is chosen to be 5 nm to obtain the optimum simulation results in ED-TFET [19]. In order to realize the in-built  $N^+$  pocket ED-TFET, it is necessary to construct a MOSFET as a beginning structure in which the source, channel, and drain are  $N^+$ ,  $P^-$ ,  $N^+$  doped, respectively, as shown in Figure 1c. The role of the polarity gate is to form a  $P^+$  region at the source. This creates the  $N^+$  doped pocket between the source and the channel, thereby achieving the same doping sequence as in the PNP TFET, as illustrated in Figure 1d. This method realizes the formation of a narrow  $N^+$  pocket in the ED-TFET without the additional chemical doping process. The device design parameters that we have used in simulations are listed in Table 1. In order to have an  $N^+$  pocket in the proposed ED-TFET, the channel doping switches from an n-type with a concentration of  $1 \times 10^{19} \text{ cm}^{-3}$  to a p-type with a concentration of  $1 \times 10^{17} \text{ cm}^{-3}$ . Furthermore, to reduce the ambipolar current, a drain doping of  $N_D = 5 \times 10^{18} \text{ cm}^{-3}$  is used. The  $N^+$  pocket length ( $L_{\text{pocket}}$ ) varies from 1 nm to 9 nm to maintain the expected tunneling performance. Making the layer underneath the polarity gate intrinsic, the work functions of the PG in conventional and proposed ED-TFET are chosen to be 4.33 eV and 4.74 eV, respectively. The simulation technique requires the source terminals to be grounded ( $V_S = 0$ ). Hence, we have considered  $V_{CG} = V_{CGS}$  and  $V_{PG} = V_{PGS}$  in all the devices.

**Table 1.** Parameters used for device simulation.

Parameter	Conventional ED-TFET <sup>1</sup>	In-Built $N^+$ pocket ED-TFET
Effective Gate Oxide Thickness ( $EOT$ <sup>2</sup> )	0.8 nm	0.8 nm
Silicon Film Thickness ( $T_{Si}$ )	10 nm	10 nm
Control Gate Length	50 nm	50 nm
Spacer Thickness between CG <sup>3</sup> and PG <sup>4</sup>	5 nm	1~9 nm
Channel Doping	$1 \times 10^{19} \text{ cm}^{-3}$ ( $N^+$ )	$1 \times 10^{17} \text{ cm}^{-3}$ ( $P^-$ )
Source Doping	$1 \times 10^{19} \text{ cm}^{-3}$ ( $N^+$ )	$4 \times 10^{19} \text{ cm}^{-3}$ ( $N^+$ )
Drain Doping	$1 \times 10^{19} \text{ cm}^{-3}$ ( $N^+$ )	$5 \times 10^{18} \text{ cm}^{-3}$ ( $N^+$ )
Control Gate Work-Function	4.74 eV	4.74 eV
Polarity Gate Work-Function	4.74 eV	4.33 eV

<sup>1</sup> ED-TFET: electrically doped tunnel FET; <sup>2</sup>  $EOT$ : equivalent oxide thickness; <sup>3</sup> CG: control gate; <sup>4</sup> PG: polarity gate.

The working mechanism of the proposed ED-TFET is consistent with that of a conventional PNP TFET. Figure 2 shows the energy band diagrams for the proposed and conventional ED-TFET at 1 nm and 5 nm below the Si-oxide interface. A local minimum point appears on the conduction energy band edge ( $E_C$ ) at  $V_{CG} = 0$  V. This happens because the introduction of the  $N^+$  pocket leads to a lowering of the  $E_C$  curve and a rapid reduction in the tunneling barrier width due to the alignment of this local minimum with the valence energy band edge ( $E_V$ ) at the source [20–22]. Conventional ED-TFET does not have this local minimum on the  $E_C$  curve, as illustrated in Figure 2. Overall, tunneling efficiency is expected to be improved due to the reduced tunneling barrier width as compared to conventional ED-TFETs.



**Figure 2.** Energy band diagrams at (a) 1 nm and (b) 5 nm below the Si-oxide interface of the conventional and proposed ED-TFET at OFF-state.

### 3. Simulation Results and Discussions

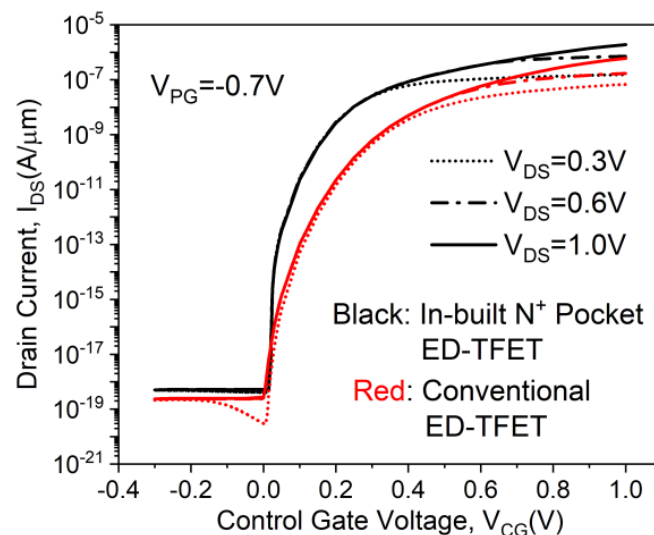
This section describes the simulated DC and analog/RF performance of the proposed device in ultra-low power applications. First, the DC transfer characteristics of the proposed and conventional ED-TFETs are simulated. Then, the influence of the critical structural parameters on the performance of the proposed device is discussed. Finally, using AC signal analysis, the enhancement in the analog/RF performance of the proposed ED-TFET is evaluated through the comparison to its conventional counterpart.

#### 3.1. DC Characteristics

All ED-TFET structures are simulated using the Silvaco Atlas device simulation tool [23]. In reality, band-to-band tunneling (BTBT) is a nonlocal process, and the spatial variation of the energy bands should be accounted for. Therefore, a non-local BTBT model is chosen prior to a local BTBT to consider the tunneling along the lateral direction for both devices. Besides, the Lombardi mobility model is included to take into account mobility degradation owing to the electric field. In addition, the concentration-dependent Shockley–Read–Hall (SRH) recombination model is applied and combined with the Auger recombination model. Bandgap narrowing (BGN) model is enabled to account for the highly doped regions of both devices. Besides, Fermi–Dirac statistics is incorporated in the

simulation [24]. An  $\text{HfO}_2$  gate dielectric with a physical thickness of approximately 4.5 nm and an equivalent oxide thickness (EOT) of 0.8 nm is used in the simulations. The quantum confinement (QC) model is not included. The direct tunneling model is not utilized because of the assumption of high- $\kappa$ /metal gate-stack technology [25]. Simulation models are verified by reproducing the results reported in [26].

The transfer characteristics of the conventional ED-TFET and the proposed in-built  $\text{N}^+$  pocket ED-TFET under different  $V_{\text{DS}}$  biases from 0.3 to 1 V are compared in Figure 3. The length of the  $\text{N}^+$  pocket ( $L_{\text{pocket}}$ ) is fixed at 5 nm. For fair comparisons, all simulations use a control gate work-function that achieves  $V_{\text{onset}} = 0$  V for both devices. The value of the control gate work-function is  $\sim 4.37$  eV in the proposed device, which can be achieved by using metal gates. We observe from Figure 3 that the ON-state current ( $I_{\text{ON}}$ ) and the subthreshold slope (SS) are significantly improved in the proposed device. This happens due to the formation of the local minimum point in the conduction energy band edge discussed above. Noted that the displayed SS is underestimated in the absence of the QC model. It can be inferred that the ON-state current of the proposed ED-TFET has improved by a factor of 3 over the conventional ED-TFET without the  $\text{N}^+$  pocket. The  $I_{\text{ON}}$  is regarded as a drain current ( $I_{\text{DS}}$ ) at  $V_{\text{CG}} = V_{\text{DS}} = 1$  V. For the proposed device and the conventional ED-TFET, the average SS extracted according to the literature [27] is 28 mV/decade and 57 mV/decade, respectively. Moreover, the ON-state current of the proposed ED-TFET can be further enhanced by using low bandgap materials, heterostructures, and strain technology.

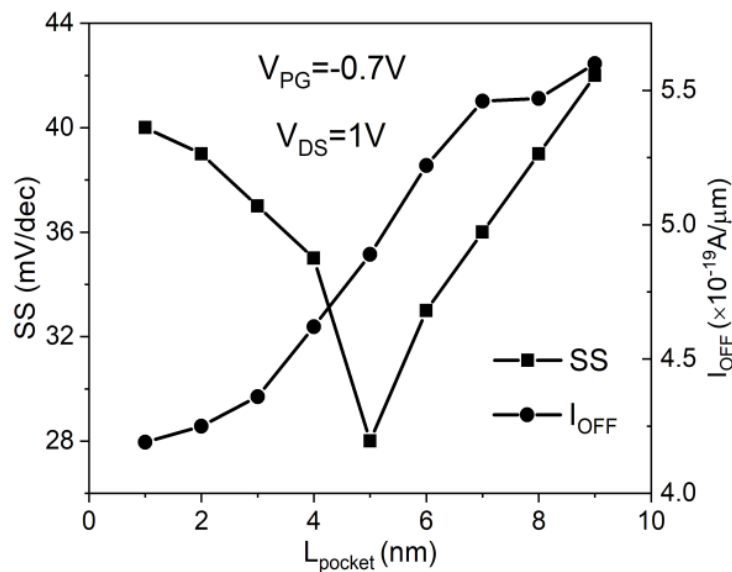


**Figure 3.** Transfer characteristics of conventional and in-built  $\text{N}^+$  pocket ED-TFET for different  $V_{\text{DS}}$ .

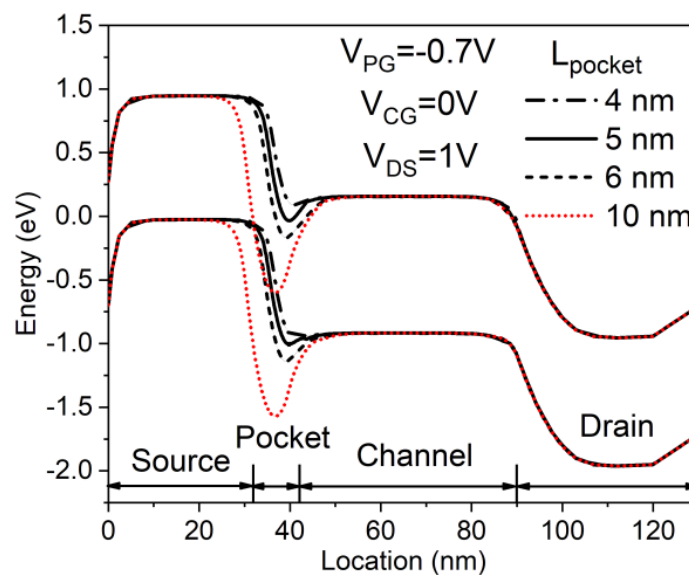
### 3.2. Device Optimizations

Optimizing the design of the in-built  $\text{N}^+$  pocket ED-TFETs is achieved by optimizing  $L_{\text{pocket}}$ . Figure 4 depicts SS and  $I_{\text{OFF}}$  as a function of  $L_{\text{pocket}}$ . To find the optimum length of  $\text{N}^+$  pocket,  $L_{\text{pocket}}$  is adjusted in the range of 1 to 10 nm. The  $I_{\text{OFF}}$  is defined as a drain current ( $I_{\text{DS}}$ ) at  $V_{\text{CG}} = 0$  V and  $V_{\text{DS}} = 1$  V. Figure 5 illustrates the energy band diagram of the in-built  $\text{N}^+$  pocket ED-TFETs with varying  $L_{\text{pocket}}$  values at OFF-states ( $V_{\text{CG}} = 0$  V). In the case of  $L_{\text{pocket}} = 4$  nm, the depth of the conduction band well where the local minimum of  $E_C$  is located is significantly reduced, making it difficult to induce band-to-band tunneling. This degrades the SS as  $L_{\text{pocket}}$  drops below 4 nm. However, when  $L_{\text{pocket}}$  exceeds 6 nm, the width of the conduction band well increases, resulting in fewer abrupt transitions between ON- and OFF-states. As a result, the subthreshold characteristics significantly deteriorate. In addition, as  $L_{\text{pocket}}$  is increased to 10 nm, an energy barrier forms between the  $\text{N}^+$  pocket and the channel, similar to an n-channel MOSFET. Under this condition, the carrier injection mechanism

switches from band-to-band tunneling to diffusion over the barrier. Taking all these effects into account, the optimal length of the  $N^+$  pocket is found to be 5 nm.



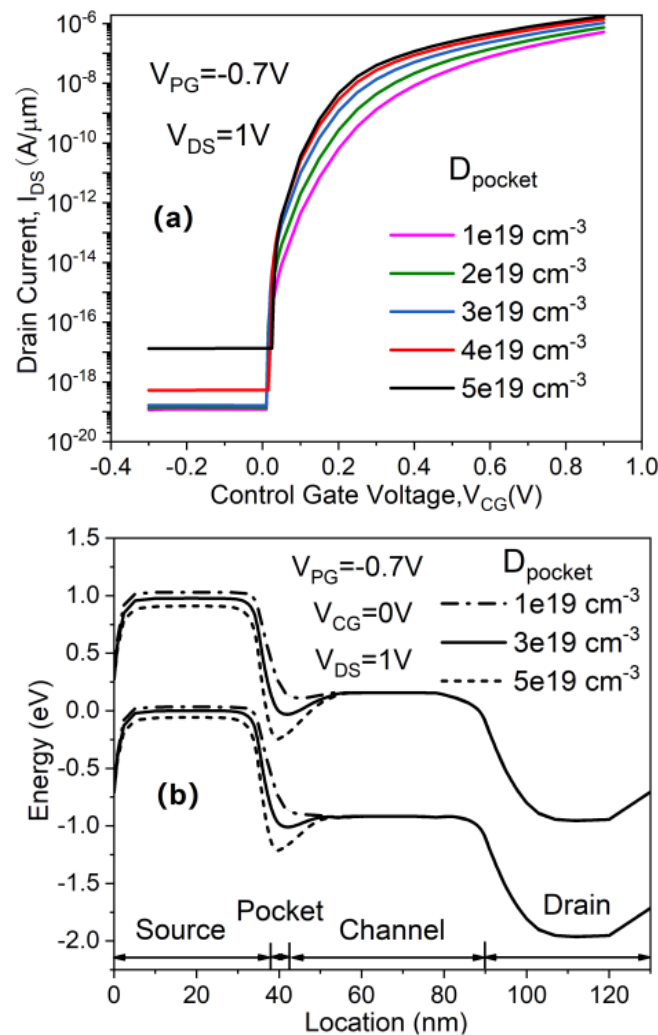
**Figure 4.** Average subthreshold swing (SS) and OFF-state current ( $I_{OFF}$ ) of the in-built  $N^+$  pocket ED-TFET as a function of the length of the pocket ( $L_{pocket}$ ).



**Figure 5.** OFF-state energy band diagram for the in-built  $N^+$  pocket ED-TFET for different pocket lengths ( $L_{pocket}$ ).

A laterally modulated energy band is obtained with an  $N^+$  pocket inserted in the proposed device. The doping concentration of the  $N^+$  pocket ( $D_{pocket}$ ), therefore, has an important influence in determining the improvement of electrical characteristics. Figure 6a,b illustrate the impact of  $D_{pocket}$  on the transfer characteristics and the OFF-state band diagrams of the in-built  $N^+$  pocket ED-TFET. For the optimized device with  $L_{pocket} = 5$  nm, both ON-state current and SS are enhanced with an increase in  $D_{pocket}$ , as depicted in Figure 6a. The reason can be inferred from Figure 6b that as  $D_{pocket}$  decreases to  $1 \times 10^{19} \text{ cm}^{-3}$ , the depth of the conduction band well in which the local minimum of  $E_C$  is located significantly reduces, thus leading to a reduced  $I_{ON}$  and a degraded SS. As  $D_{pocket}$  is increased from  $1 \times 10^{19} \text{ cm}^{-3}$  to  $5 \times 10^{19} \text{ cm}^{-3}$ ,  $I_{OFF}$  dramatically increases, although  $I_{ON}$  only increases slightly,

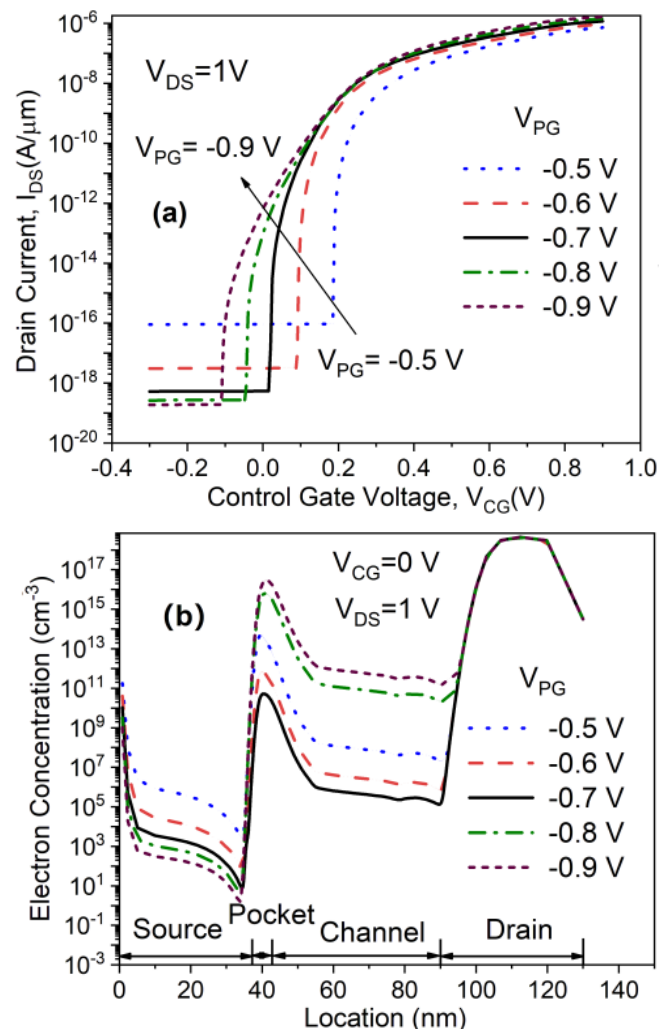
as shown in Figure 6a. The  $N^+$  pocket becomes partially depleted at higher  $D_{\text{pocket}}$  values, resulting in an increased  $I_{\text{OFF}}$ . From this point of view,  $4 \times 10^{19} \text{ cm}^{-3}$  is chosen as the optimal value of  $D_{\text{pocket}}$ .



**Figure 6.** Impact of  $D_{\text{pocket}}$  on (a) transfer characteristics and (b) OFF-state energy band diagram of the in-built  $N^+$  pocket ED-TFET.

In the proposed device, an adequate negative bias is applied at the PG terminal to generate a  $P^+$  source region with a hole concentration similar to its conventional counterpart, as mentioned above. Therefore, the PG terminal bias ( $V_{PG}$ ) needs to be optimized as well. Figure 7a,b show the transfer characteristics and electron concentration of the in-built  $N^+$  pocket ED-TFET as a function of  $V_{PG}$ . One can observe from Figure 7a that the scaling of  $|V_{PG}|$  causes an increase in the OFF-state current, which is consistent with the previously reported results [17]. Furthermore, the OFF-state leakage current is drastically increased when  $V_{PG} = -0.5\text{V}$ . However, the ON-state current is slightly reduced as  $|V_{PG}|$  is scaled. The decrease in  $|V_{PG}|$  results in a lower vertical electric field, which, in turn, leads to a decrease in the number of holes. Thus, an increase in  $|V_{PG}|$  causes a reduction in electron concentration in the source region of the in-built  $N^+$  pocket ED-TFET, as shown in Figure 7b. In addition, it can be seen from Figure 7a that the optimal PG bias in terms of average SS is  $-0.7\text{V}$ . This can be understood from the electron concentration distribution with different PG bias at OFF-state. In the case of the proposed device with  $V_{PG} = -0.7\text{V}$ , the electron concentration in the pocket region shows the lowest value, as illustrated in Figure 7b. When  $V_{PG}$  increases above or decreases below this value, the  $N^+$  pocket begins to be partially depleted at OFF-state, and the electron concentration in the pocket

region increases. This increased electron concentration in the partially depleted  $N^+$  pocket affects the conduction band profile at OFF-state. As a result, the conduction band well becomes wider, resulting in SS optimum value for the PG bias of the in-built  $N^+$  pocket ED-TFET with the lowest SS and a considerably high  $I_{ON}/I_{OFF}$  ratio ( $\sim 10^{12}$ ).

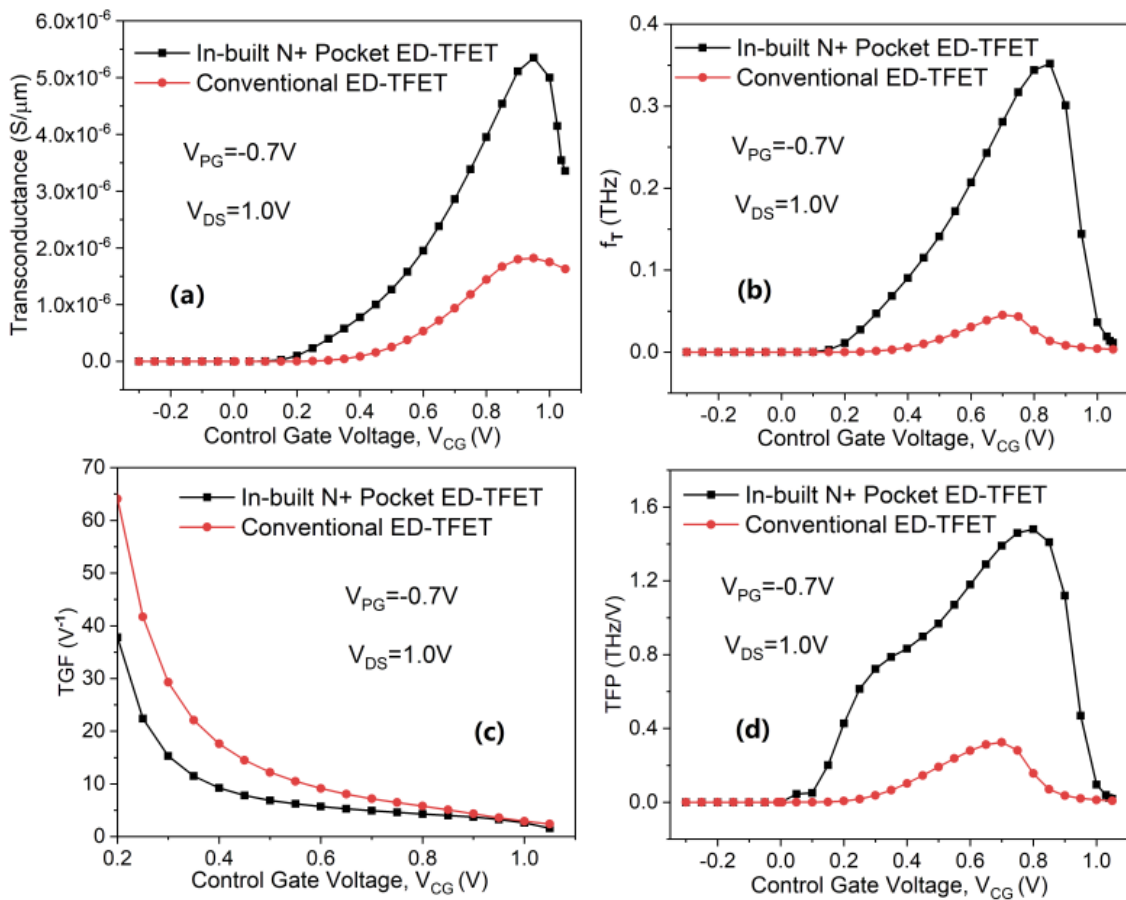


**Figure 7.** Impact of polarity gate (PG) bias on (a) transfer characteristics and (b) electron concentration of the in-built  $N^+$  pocket ED-TFET.

### 3.3. Analog/RF Performance

The analog/RF performance of the in-built  $N^+$  pocket ED-TFET is simulated and compared with a conventional ED-TFET having identical physical dimensions. Therefore, the analog/RF figure-of-merits (FOMs) are investigated, including transconductance ( $g_m$ ), transconductance-to-drain current ratio, also known as transconductance generation factor (TGF), cutoff frequency ( $f_T$ ), and transconductance frequency product (TFP). Transconductance is considered a critical parameter for obtaining high gain and  $f_T$  in analog circuit applications [28,29]. The  $g_m$  of the device is calculated by the slope of the  $\log(I_{DS})-V_{CG}$  curve when  $V_{DS}$  remains constant, which can be expressed as  $g_m = dI_{DS}/dV_{CG}$ . Figure 8a compares the  $g_m$  characteristics of a conventional and the proposed ED-TFETs as a function of  $V_{CG}$ . It can be seen that the  $g_m$  of the proposed in-built  $N^+$  pocket ED-TFET is larger than that of the conventional ED-TFET. For the proposed structure,  $I_{DS}$  changes greatly with  $V_{CG}$ , while  $I_{ON}$  maintains a high value, resulting in a higher  $g_m$ . In addition, it can be inferred that  $g_m$  increases with the increase

of  $V_{CG}$  until it enters the saturation region. The increase of the BTBT generation rate directly leads to an increase in  $g_m$ . However, it decreases at higher  $V_{CG}$  due to reduced mobility.



**Figure 8.** Variation of (a) transconductance, (b) cutoff frequency, (c) TGF, and (d) TFP along  $V_{CG}$  of the conventional and in-built  $N^+$  pocket ED-TFET.

For RF applications, the cutoff frequency ( $f_T$ ) is another important parameter. This is defined as the frequency at which the short circuit current gain reaches unity and can be expressed as  $f_T = g_m / 2\pi(C_{gs} + C_{gd})$ . Generally,  $f_T$  should be as high as possible to enable the device to be used broadly in high-frequency circuit applications. Figure 8b shows the dependence of  $f_T$  on  $V_{CG}$ . It can be inferred that the significant improvement in  $f_T$  of the in-built  $N^+$  pocket ED-TFET is due to its larger  $g_m$  compared to the conventional counterpart. It can be clearly seen from the figure that this rapid increase in  $g_m$  results in an increase in  $f_T$  until  $V_{CG}$  reaches 0.8 V. After that, a sharp drop in  $g_m$  and an increase in gate capacitance results in a decrease in the  $f_T$ . The proposed and conventional ED-TFETs achieve a maximum  $f_T$  of 0.352 and 0.045 THz, respectively.

TGF is another critical parameter that quantifies the device efficiency [30] and can be expressed as  $TGF = g_m/I_{DS}$ . The variation in TGF with  $V_{CG}$  for both ED-TFETs is shown in Figure 8c. The proposed device has a lower TGF compared to its conventional counterpart. This is happening because, in the case of TGF, the drain current is dominant as compared to  $g_m$ . When the control gate voltage is high, the drain current increases rapidly, resulting in a corresponding decrease in the TGF. The TFP is another key FOM for high-frequency circuits and is essentially the product of the TGF and  $f_T$ , which is expressed as  $TFP = (g_m/I_{DS}) \times f_T$  [31]. From Figure 8d, it can be observed that the proposed ED-TFET has a higher value of TFP compared with the conventional ED-TFET. The improvement in TFP is due to the higher  $f_T$ . This simulation analysis shows that overall the in-built  $N^+$  pocket ED-TFET appears to be more suitable for RF applications than conventional ED-TFETs.

#### 4. Conclusions

In this paper, we have presented a method to insert an  $N^+$  pocket in an ED-TFET by using the polarity bias concept. This  $N^+$  pocket is realized without the need for additional chemical doping. In addition, device design has been optimized by modulating  $L_{\text{pocket}}$ ,  $D_{\text{pocket}}$ , and  $V_{\text{PG}}$ . The DC and analog/RF performance is evaluated using 2-D simulations. At the optimized dimensions, the in-built  $N^+$  pocket ED-TFET has a better simulated performance to the conventional ED-TFET in terms of SS,  $I_{\text{ON}}$ ,  $g_m$ ,  $f_T$ , TGF, and TFP. The enhancement in SS and  $I_{\text{ON}}$  is attributed to a local minimum of  $E_C$ , which is formed by the introduction of the  $N^+$  pocket, resulting in a higher  $g_m$  and thereby an increase in  $f_T$  and TFP. The in-built  $N^+$  pocket ED-TFET appears to be an attractive candidate for future low power applications.

**Author Contributions:** Conceptualization: C.S.; Investigation: J.L.; Software: Y.L.; Investigation: S.-f.W. All authors have read and agreed to the published version of the manuscript.

**Funding:** This work was supported in part by the Jimei University Doctoral Research Startup Fund (C618024) and in part by the Fujian Province Young and Middle-aged Teacher Education Research Project (JAT190302) and in part by the Jimei University Scientific Research Project (C619030).

**Conflicts of Interest:** The authors declare no conflict of interest.

#### References

1. Tamersit, K. Computational study of p-n carbon nanotube tunnel field-effect transistor. *IEEE Trans. Electron Devices* **2020**, *67*, 704–710. [[CrossRef](#)]
2. Saurabh, S.; Kumar, M.J. Novel attributes of a dual material gate nanoscale tunnel field-effect transistor. *IEEE Trans. Electron Devices* **2010**, *58*, 404–410. [[CrossRef](#)]
3. Bhattacharyya, A.; De Chanda, M.D. Performance assessment of new dual-pocket vertical heterostructure tunnel FET-based biosensor considering steric hindrance issue. *IEEE Trans. Electron Devices* **2019**, *66*, 3988–3993. [[CrossRef](#)]
4. Ghosh, B.; Akram, M.W. Junctionless tunnel field effect transistor. *IEEE Electron Device Lett.* **2013**, *34*, 584–586. [[CrossRef](#)]
5. Shaikh, M.R.U.; Loan, S.A. Drain-engineered TFET with fully suppressed ambipolarity for high-frequency application. *IEEE Trans. Electron Devices* **2019**, *66*, 1628–1634. [[CrossRef](#)]
6. Tura, A.; Woo, J.C.S. Performance comparison of silicon steep subthreshold FETs. *IEEE Trans. Electron Devices* **2010**, *57*, 1362–1368. [[CrossRef](#)]
7. Nagavarapu, V.; Jhaveri, R.; Woo, J.C.S. The tunnel source (PNPN) n-MOSFET: A novel high performance transistor. *IEEE Trans. Electron Devices* **2008**, *55*, 1013–1019. [[CrossRef](#)]
8. Cho, S.; Kang, I.M. Design optimization of tunneling field-effect transistor based on silicon nanowire PNPN structure and its radio frequency characteristics. *Curr. Appl. Phys.* **2012**, *12*, 673–677. [[CrossRef](#)]
9. Cao, W.; Yao, C.J.; Jiao, G.F.; Huang, D.; Yu, H.Y.; Li, M.F. Improvement in reliability of tunneling field-effect transistor with pnin structure. *IEEE Trans. Electron Devices* **2011**, *58*. [[CrossRef](#)]
10. Verreck, D.; Verhulst, A.S.; Kao, K.H.; Vandenberghe, W.G.; De Meyer, K.; Groeseneken, G. Quantum mechanical performance predictions of pnin versus pocketed line tunnel field-effect transistors. *IEEE Trans. Electron Device* **2013**, *60*, 2128–2134. [[CrossRef](#)]
11. Jhaveri, R.; Nagavarapu, V.; Woo, J.C.S. Effect of pocket doping and annealing schemes on the source-pocket tunnel field-effect transistor. *IEEE Trans. Electron Devices* **2010**, *58*, 80–86. [[CrossRef](#)]
12. Tura, A.; Zhang, Z.; Liu, P.; Xie, Y.H.; Woo, J.C. Vertical silicon pnin tunnel nMOSFET with MBE-grown tunneling junction. *IEEE Trans. Electron Devices* **2011**, *58*, 1907–1913. [[CrossRef](#)]
13. Chang, H.Y.; Adams, B.; Chien, P.Y.; Li, J.; Woo, J.C. Improved subthreshold and output characteristics of source-pocket Si tunnel FET by the application of laser annealing. *IEEE Trans. Electron Devices* **2012**, *60*, 92–96. [[CrossRef](#)]
14. Zhang, Y.; Chu, H. Tunneling Field Effect Transistor (TFET) with Ultra-Shallow Pockets Formed by Asymmetric Ion Implantation and Method of Making Same. US Patent 20140158990, 12 June 2014.

15. De Marchi, M.; Zhang, J.; Frache, S.; Sacchetto, D.; Gaillardon, P.E.; Leblebici, Y.; De Micheli, G. Configurable logic gates using polarity-controlled silicon nanowire gate-all-around FETs. *IEEE Electron Device Lett.* **2014**, *35*, 880–882. [[CrossRef](#)]
16. De Marchi, M.; Sacchetto, D.; Frache, S.; Zhang, J.; Gaillardon, P.E.; Leblebici, Y.; De Micheli, G. Polarity control in double-gate, gate-all-around vertically stacked silicon nanowire FETs. In Proceedings of the 2012 International Electron Devices Meeting, San Francisco, CA, USA, 10–13 December 2012. [[CrossRef](#)]
17. Lahgere, A.; Sahu, C.; Singh, J. PVT-aware design of dopingless dynamically configurable tunnel FET. *IEEE Trans. Electron Devices* **2015**, *62*, 2404–2409. [[CrossRef](#)]
18. Zervas, M.; Sacchetto, D.; De Micheli, G.; Leblebici, Y. Top-down fabrication of very-high density vertically stacked silicon nanowire arrays with low temperature budget. *Microelectron. Eng.* **2011**, *88*, 3127–3132. [[CrossRef](#)]
19. Kondekar, P.N.; Nigam, K.; Pandey, S.; Sharma, D. Design and analysis of polarity controlled electrically doped tunnel FET with bandgap engineering for analog/RF applications. *IEEE Trans. Electron Devices* **2016**, *64*, 412–418. [[CrossRef](#)]
20. Choi, W.Y.; Lee, W. Hetero-gate-dielectric tunneling field-effect transistors. *IEEE Trans. Electron Devices* **2010**, *57*, 2317–2319. [[CrossRef](#)]
21. Abdi, D.B.; Kumar, M.J. In-built N+ pocket pnpn tunnel field-effect transistor. *IEEE Electron Device Lett.* **2014**, *35*, 1170–1172. [[CrossRef](#)]
22. Ram, M.S.; Abdi, D.B. Dopingless PNP tunnel FET with improved performance: Design and analysis. *Superlattices Microstruct.* **2015**, *82*, 430–437. [[CrossRef](#)]
23. *ATLAS Device Simulation Software*; Silvaco: Santa Clara, CA, USA, 2018.
24. Padilla, J.L.; Gamiz, F.; Godoy, A. Impact of quantum confinement on gate threshold voltage and subthreshold swings in double-gate tunnel FETs. *IEEE Trans. Electron Devices* **2012**, *59*, 3205–3211. [[CrossRef](#)]
25. Fahad, H.M.; Hussain, M.M. High-performance silicon nanotube tunneling FET for ultralow-power logic applications. *IEEE Trans. Electron Devices* **2013**, *60*, 1034–1039. [[CrossRef](#)]
26. Boucart, K.; Ionescu, A.M. Double-gate tunnel FET with high- $\kappa$  gate dielectric. *IEEE Trans. Electron Devices* **2007**, *54*, 1725–1733. [[CrossRef](#)]
27. Kumar, M.J.; Janardhanan, S. Doping-less tunnel field effect transistor: Design and investigation. *IEEE Trans. Electron Devices* **2013**, *60*, 3285–3290. [[CrossRef](#)]
28. Imenabadi, R.M.; Saremi, M.; Vandenberghe, W.G. A novel PNP-like Z-shaped tunnel field-effect transistor with improved ambipolar behavior and RF performance. *IEEE Trans. Electron Devices* **2017**, *64*, 4752–4758. [[CrossRef](#)]
29. Raad, B.R.; Nigam, K.; Sharma, D.; Kondekar, P.N. Performance investigation of bandgap, gate material work function and gate dielectric engineered TFET with device reliability improvement. *Superlattices Microstruct.* **2016**, *94*, 138–146. [[CrossRef](#)]
30. Tirkey, S.; Sharma, D.; Yadav, D.S.; Yadav, S. Analysis of a novel metal implant junctionless tunnel FET for better DC and analog/RF electrostatic parameters. *IEEE Trans. Electron Devices* **2017**, *64*, 3943–3950. [[CrossRef](#)]
31. Madan, J.; Chaujar, R. Interfacial charge analysis of heterogeneous gate dielectric-gate all around-tunnel FET for improved device reliability. *IEEE Trans. Device Mater. Reliab.* **2016**, *16*, 227–234. [[CrossRef](#)]

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